

Description

The AP120N03NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

Battery protection or in other Switching application.

General Features

 $V_{DS} = 30V I_{D} = 120A$

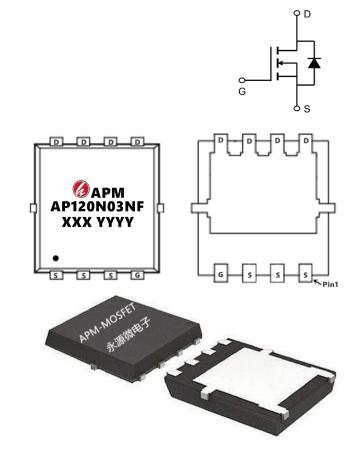
 $R_{DS(ON)}$ < 2.4m Ω @ V_{GS} =10V

Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



Package Marking and Ordering Information

| i ackage markii | tekage marking and ordering information | | | | |
|-----------------|---|---------------------|----------|--|--|
| Product ID | Pack | Marking | Qty(PCS) | | |
| AP120N03NF | PDFN5*6-8L | AP120N03NF XXX YYYY | 5000 | | |

Absolute Maximum Ratings (T_C=25°Cunless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---------------------------------------|--|------------|-------|
| VDS | Drain-Source Voltage | 30 | V |
| VGS Gate-Source Voltage | | ±20 | V |
| I _D @T _C =25°C | Continuous Drain Current, V _{GS} @ 10V ^{1,6} | 120 | A |
| I _D @T _C =100°C | Continuous Drain Current, V _{GS} @ 10V ^{1,6} | 66 | A |
| IDM | Pulsed Drain Current ² | 320 | A |
| EAS | Single Pulse Avalanche Energy ³ | 180 | mJ |
| IAS | Avalanche Current | 60 | А |
| P _D @T _C =25°C | Total Power Dissipation⁴ | 187 | W |
| TSTG | Storage Temperature Range | -55 to 150 | ℃ |
| TJ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| R₀JA | Thermal Resistance Junction-Ambient ¹ | 62 | °C/W |
| R₀JC | Thermal Resistance Junction-Case ¹ | 1.1 | °C/W |



Electrical Characteristics (T_J=25℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit |
|------------------------|--|---|------|-------|------|------|
| BVDSS | Drain-Source Breakdown Voltage | V _{GS} =0V , I _D =250uA | 30 | 32 | | V |
| ∆BVDSS/∆TJ | BV _{DSS} Temperature Coefficient | Reference to 25℃ , I _D =1mA | | 0.014 | | V/°C |
| DDC(ON) | Static Drain-Source On-Resistance ² | V _{GS} =10V , I _D =30A | | 2.0 | 2.4 | mΩ |
| RDS(ON) | | V _{GS} =4.5V , I _D =15A | | 3.5 | 4.5 | |
| VGS(th) | Gate Threshold Voltage | $V_{GS}=V_{DS}$, I_{D} =250uA | 1.2 | 1.5 | 2.5 | V |
| $\triangle V_{GS(th)}$ | V _{GS(th)} Temperature Coefficient | VGS-VDS , ID -230UA | | -4 | | mV/℃ |
| IDSS | Drain-Source Leakage Current | V_{DS} =24V , V_{GS} =0V , T_{J} =25 $^{\circ}$ C | | | 1 | uA |
| פסטו | | V_{DS} =24V , V_{GS} =0V , T_{J} =55 $^{\circ}$ C | | | 5 | |
| IGSS | Gate-Source Leakage Current | V _{GS} =±20V , V _{DS} =0V | | | ±100 | nA |
| gfs | Forward Transconductance | V _{DS} =5V , I _D =30A | | 50 | | S |
| Rg | Gate Resistance | V _{DS} =0V , V _{GS} =0V , f=1MHz | | 1.7 | | Ω |
| Qg | Total Gate Charge (4.5V) | V _{DS} =15V , V _{GS} =10V , I _D =15A | | 56.9 | | |
| Qgs | Gate-Source Charge | | | 13.8 | | nC |
| Qgd | Gate-Drain Charge | | | 23.5 | | |
| Td(on) | Turn-On Delay Time | | | 20.1 | | |
| Tr | Rise Time | V_{DD} =15V , V_{GS} =10V , R_{G} =3.3 Ω , | | 6.3 | | 20 |
| Td(off) | Turn-Off Delay Time | I _D =1A | | 124.6 | | ns |
| T _f | Fall Time | | | 15.8 | | |
| Ciss | Input Capacitance | | | 4345 | | |
| Coss | Output Capacitance | V_{DS} =15V , V_{GS} =0V , f=1MHz | | 340 | | pF |
| Crss | Reverse Transfer Capacitance | | | 225 | | |
| IS | Continuous Source Current ^{1,6} | V _G =V _D =0V , Force Current | | | 85 | Α |
| VSD | Diode Forward Voltage ² | V _{GS} =0V , I _S =1A , T _J =25℃ | | | 1.2 | V |

Note:

- 1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2. The data tested by pulsed , pulse width ≤ 300 us , duty cycle $\leq 2\%$
- 3 The EAS data shows Max. rating . The test condition is V DD =25V,V GS =10V,L=0.1mH,I AS =60A
- 4. The power dissipation is limited by 150 $\!\!\!\!^{\,\circ}\!\!\!\!^{\,\circ}$ junction temperature
- 5. The data is theoretically the same as I D and I DM, in real applications, should be limited by total power dissipation.



Typical Characteristics

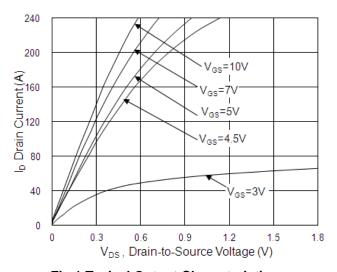


Fig.1 Typical Output Characteristics

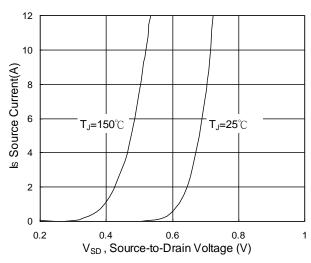


Fig.3 Forward Characteristics of Reverse

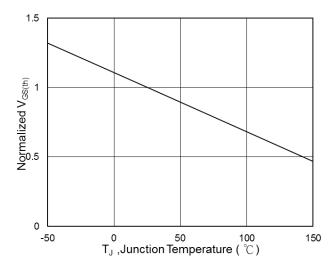


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

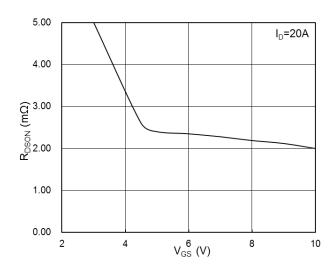


Fig.2 On-Resistance v.s Gate-Source

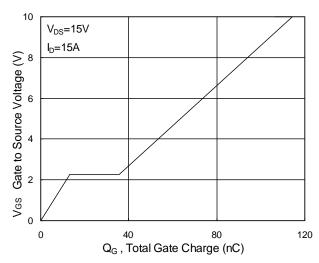


Fig.4 Gate-Charge Characteristics

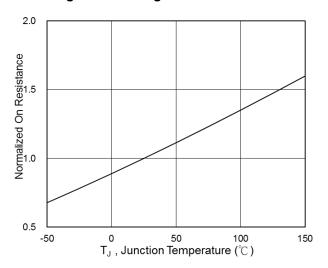
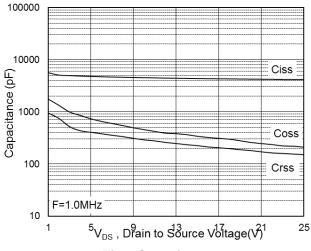


Fig.6 Normalized R_{DSON} v.s T_J



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30V N-Channel Enhancement Mode MOSFET



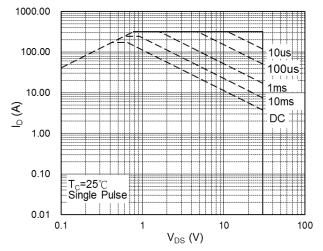


Fig.7 Capacitance

Fig.8 Safe Operating Area

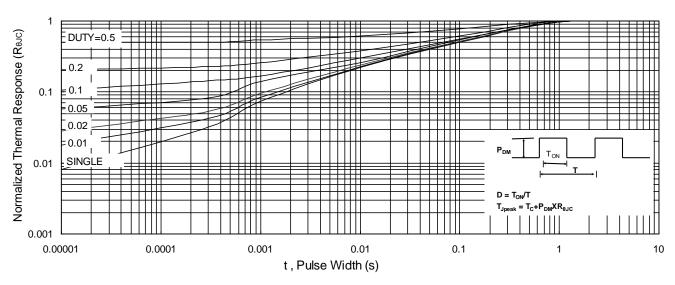


Fig.9 Normalized Maximum Transient Thermal Impedance

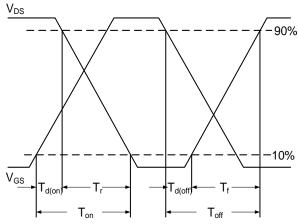


Fig.10 Switching Time Waveform

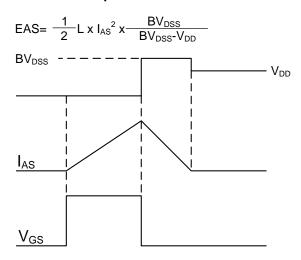


Fig.11 Unclamped Inductive Switching Waveform





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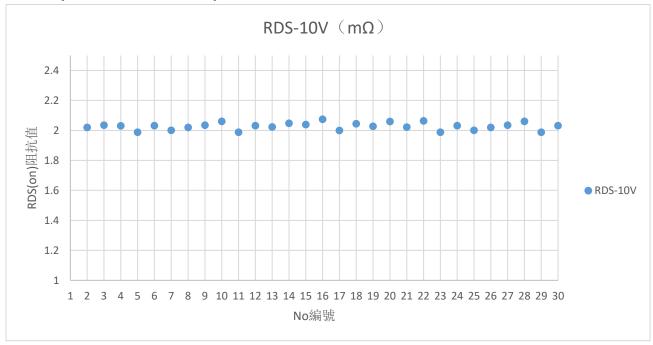
30V N-Channel Enhancement Mode MOSFET

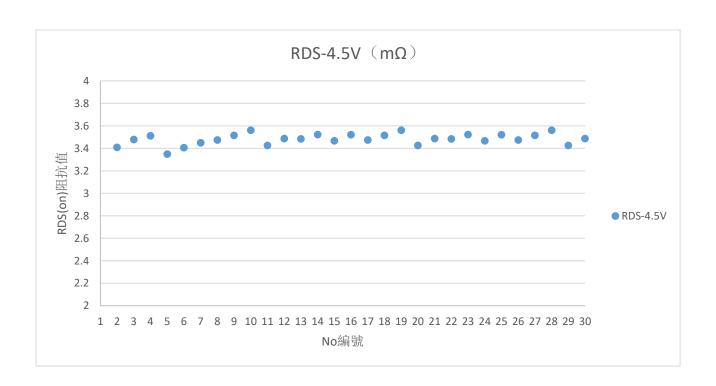
| Edition | Date | Change |
|---------|-----------|-----------------|
| Rve1.0 | 2019/4/10 | Initial release |
| Rve2.0 | 2020/7/8 | |

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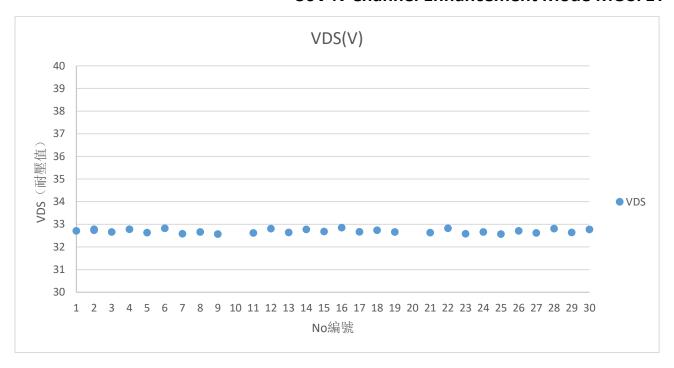


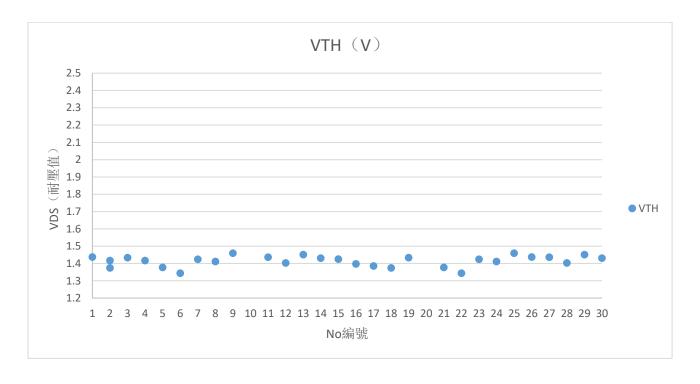
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