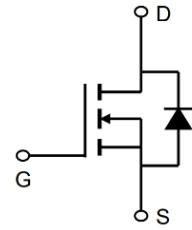


20V N-Channel Enhancement Mode MOSFET

Description

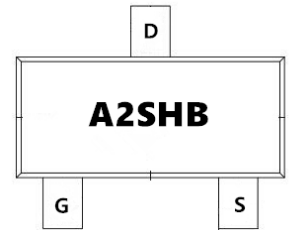
The AP2302AI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 20V$ $I_D = 3.2A$

$R_{DS(ON)} < 32m\Omega$ @ $V_{GS}=4.5V$



Application

Battery protection
 Load switch
 Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2302AI	SOT-23	A2SHB	3000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	3.2	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	2.8	A
I_{DM}	Pulsed Drain Current ²	14.4	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ³	1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	125	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	80	$^\circ C/W$

20V N-Channel Enhancement Mode MOSFET

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=3A$	---	23	32	m Ω
		$V_{GS}=2.5V, I_D=2A$	---	29	35	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.4	0.7	1.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=16V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=3A$	---	10.5	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=3A$	---	4.6	---	nC
Q_{gs}	Gate-Source Charge		---	0.7	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega, I_D=3A$	---	1.6	---	ns
T_r	Rise Time		---	42	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	7	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	310	---	pF
C_{oss}	Output Capacitance		---	49	---	
C_{rss}	Reverse Transfer Capacitance		---	35	---	
I_s	Continuous Source Current ^{1,4}	$V_G=V_D=0V, \text{Force Current}$	---	---	3.6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_s=1A, T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

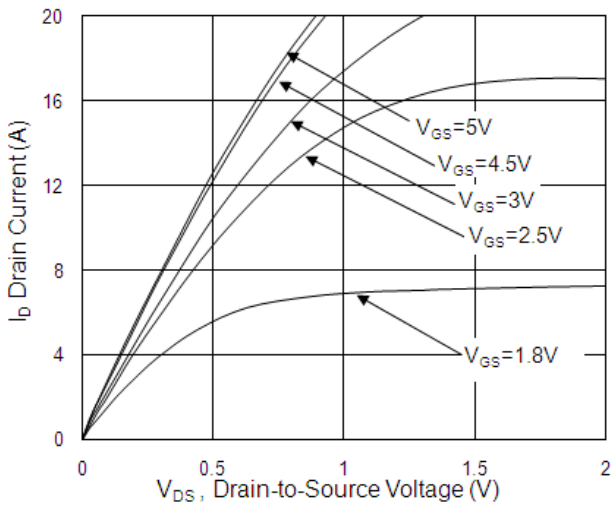


Fig.1 Typical Output Characteristics

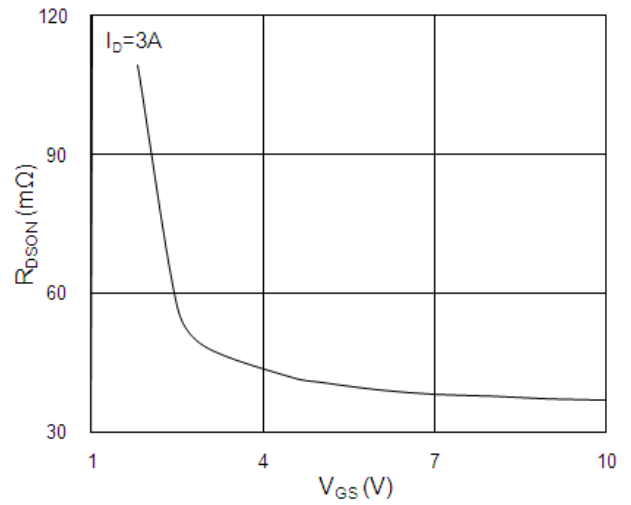


Fig.2 On-Resistance vs. G-S Voltage

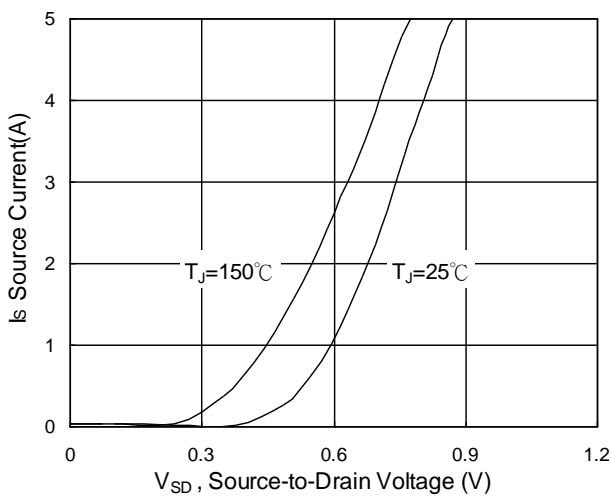


Fig.3 Source Drain Forward Characteristics

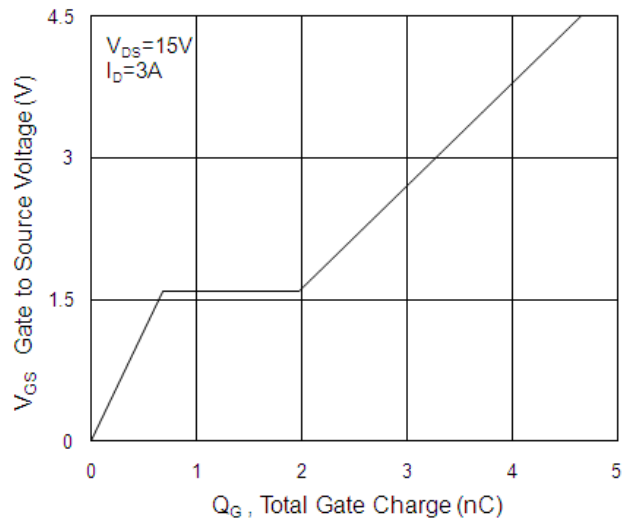


Fig.4 Gate-Charge Characteristics

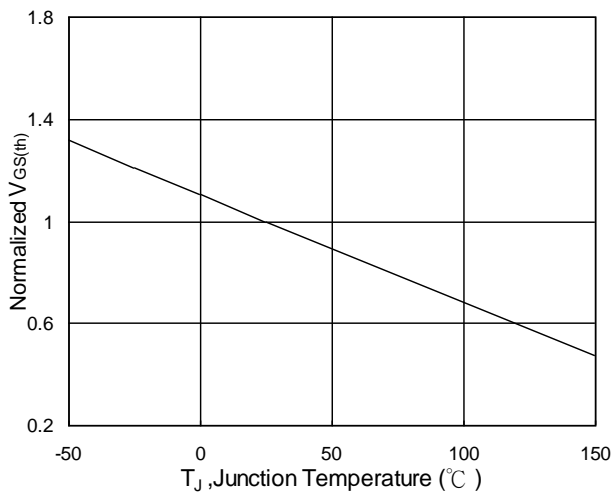


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

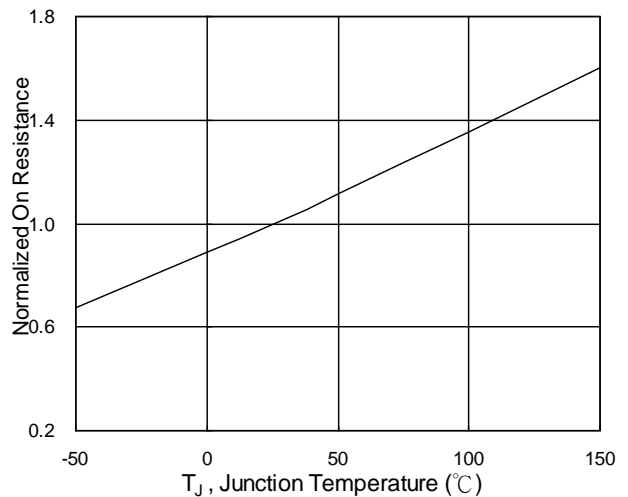


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



20V N-Channel Enhancement Mode MOSFET

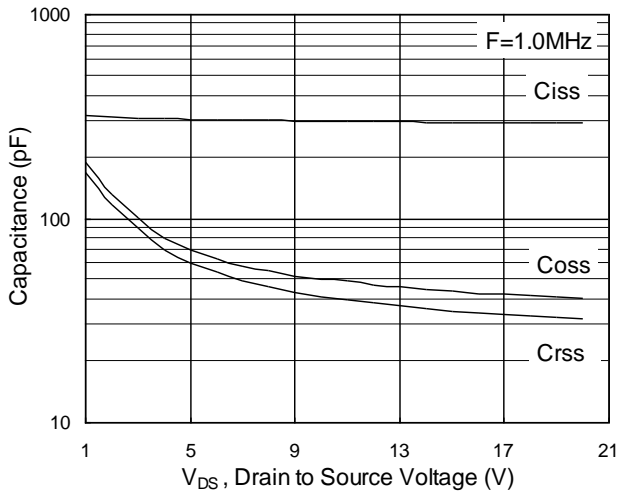


Fig.7 Capacitance

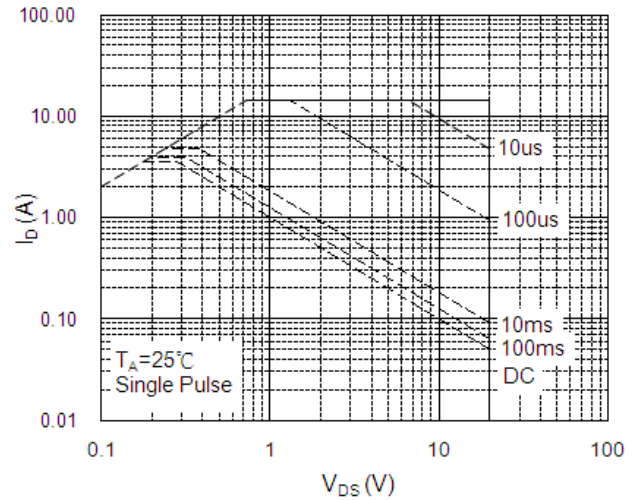


Fig.8 Safe Operating Area

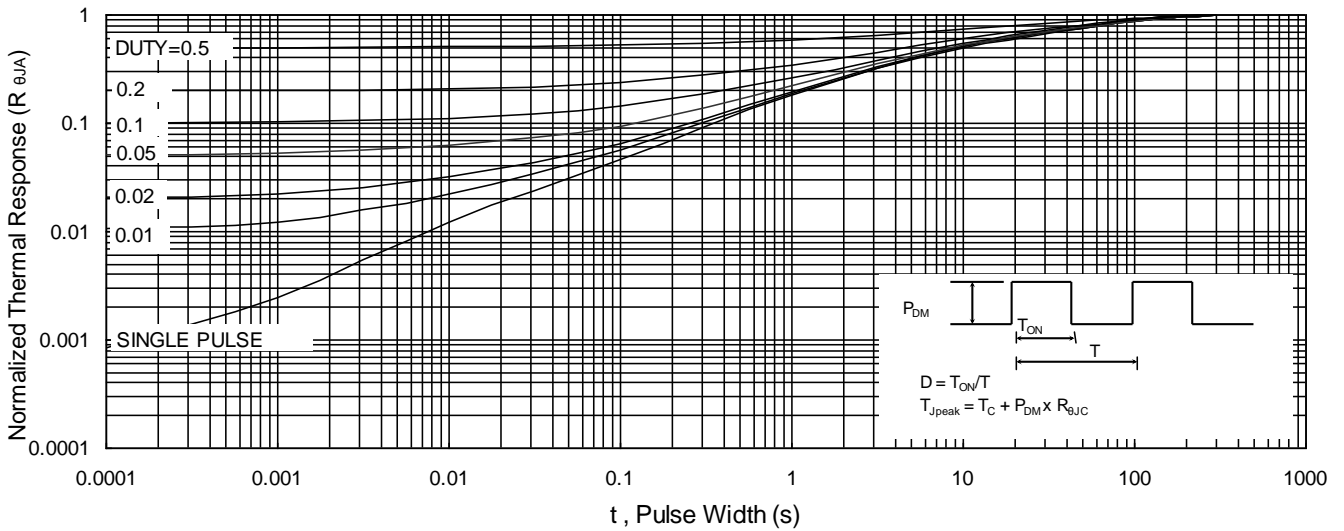


Fig.9 Normalized Maximum Transient Thermal Impedance

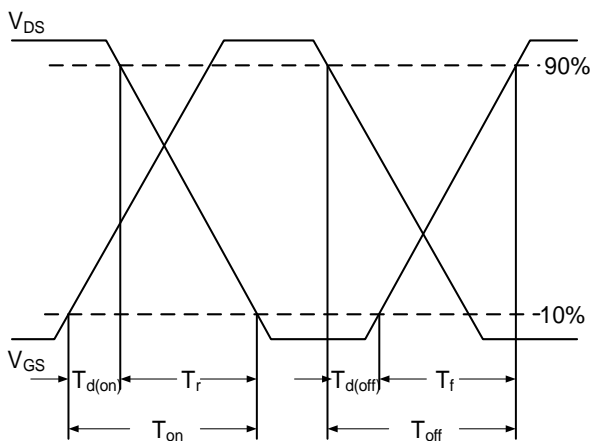


Fig.10 Switching Time Waveform

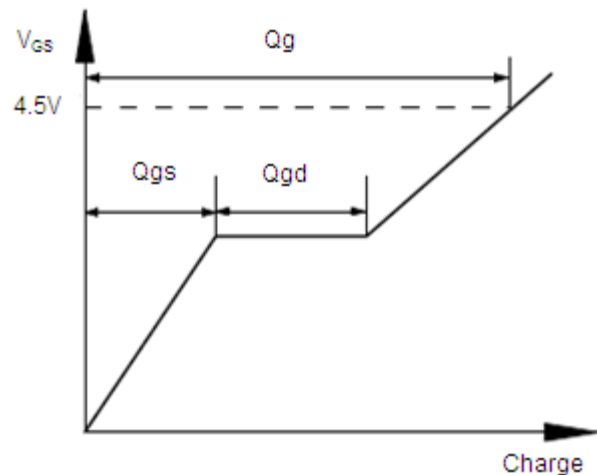
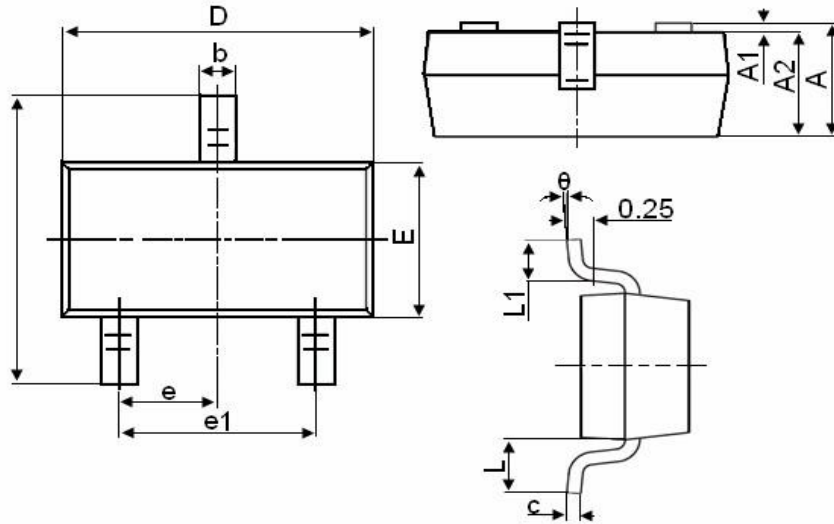


Fig.11 Gate Charge Waveform

20V N-Channel Enhancement Mode MOSFET

Package Mechanical Data-SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

20V N-Channel Enhancement Mode MOSFET**Attention**

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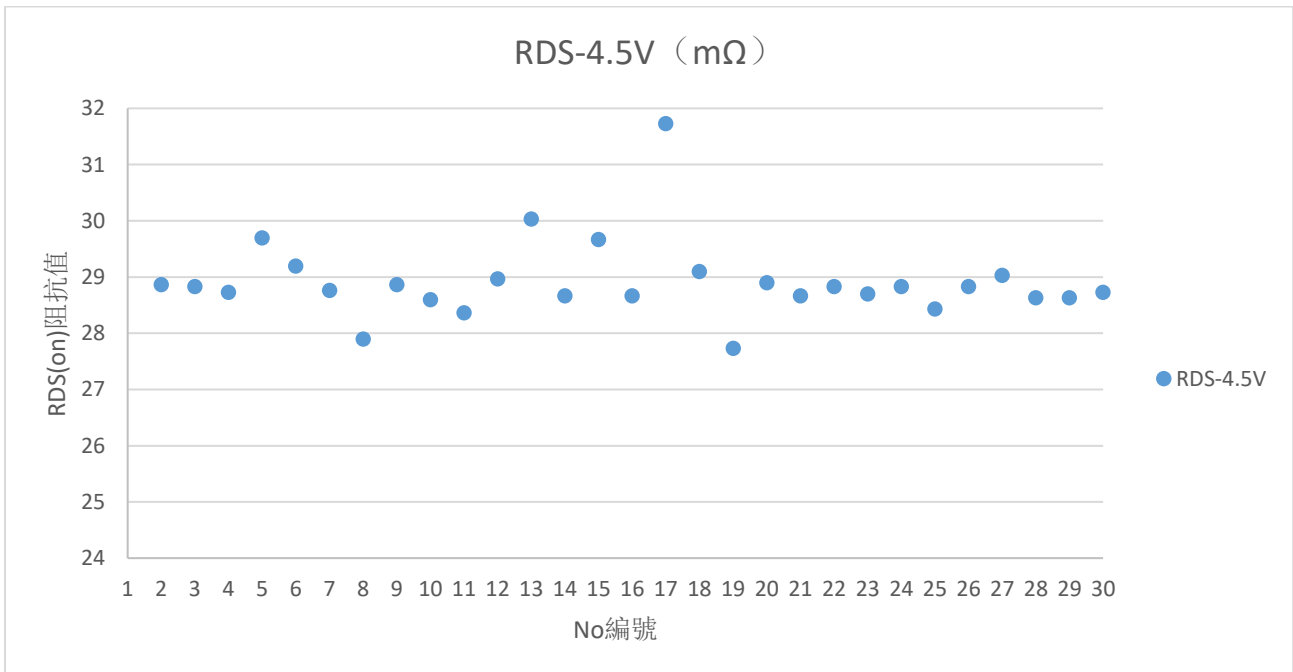
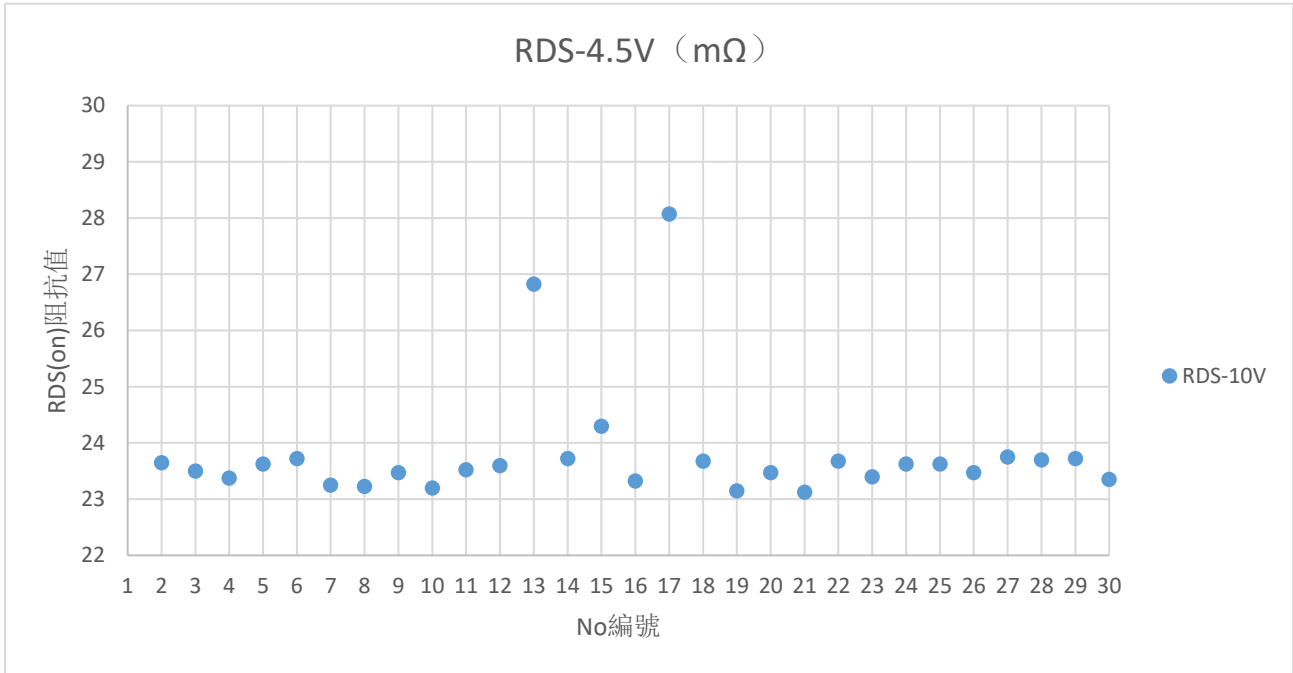
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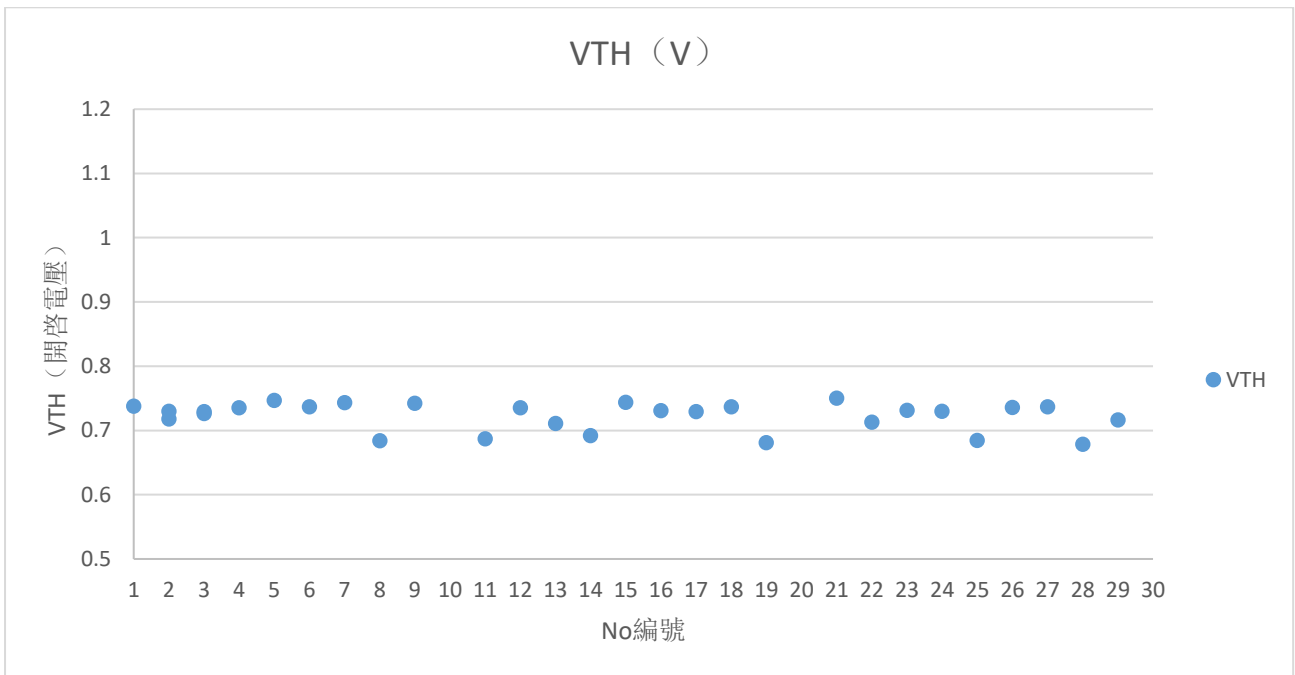
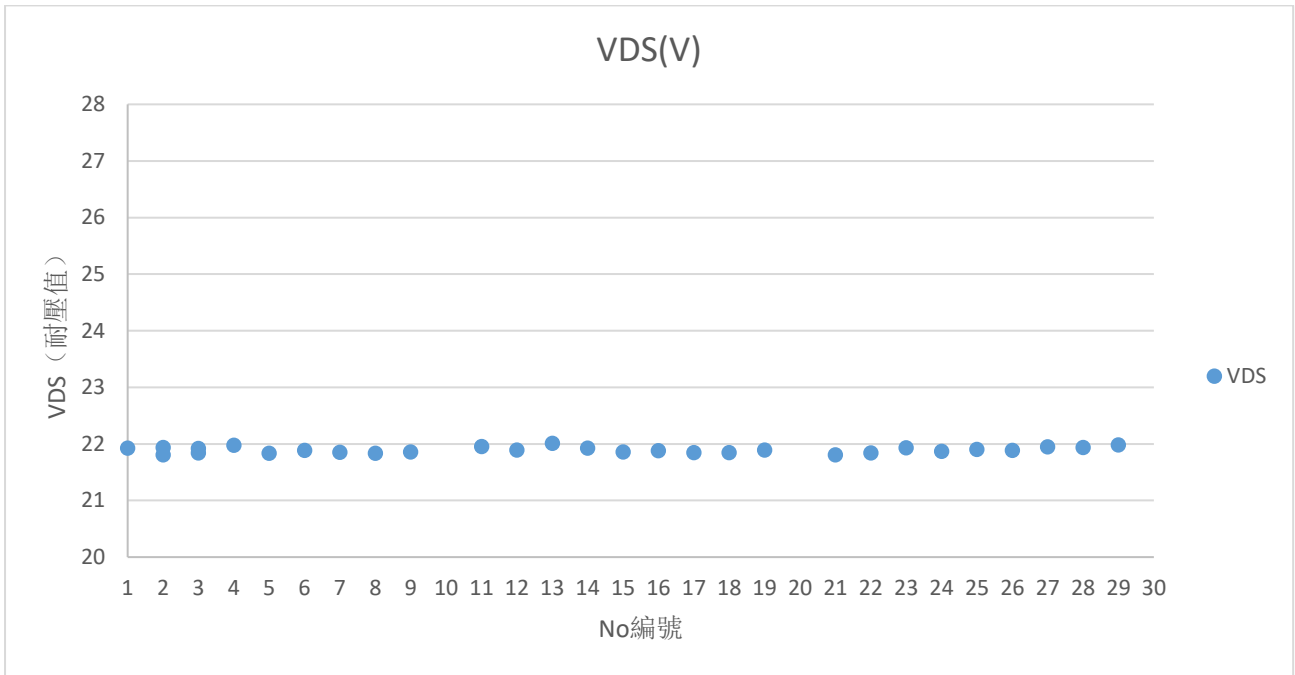
Edition	Date	Change
Rve3.0	2017/6/1	Initial release
Rve3.1	2020/6/09	Reduce RDS(on)

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