

## -12V P-Channel Enhancement Mode MOSFET

### Description

The AP2311MI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

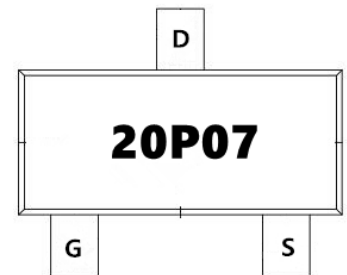
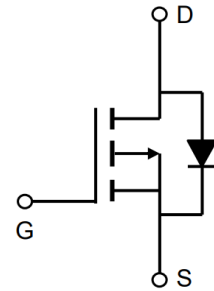
$V_{DS} = -12V$   $I_D = -7.0A$

$R_{DS(ON)} < 24m\Omega$  @  $V_{GS}=4.5V$  (Type: 19m $\Omega$ )

### Application

electronic cigarette

Load switch



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2311MI	SOT23-3L	20P07	3000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-Source Voltage	-12	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	-7.0	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	-3.6	A
IDM	Pulsed Drain Current <sup>note1</sup>	-22	A
$P_D@T_C=25^\circ\text{C}$	Power Dissipation	1.6	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125	$^\circ\text{C/W}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$



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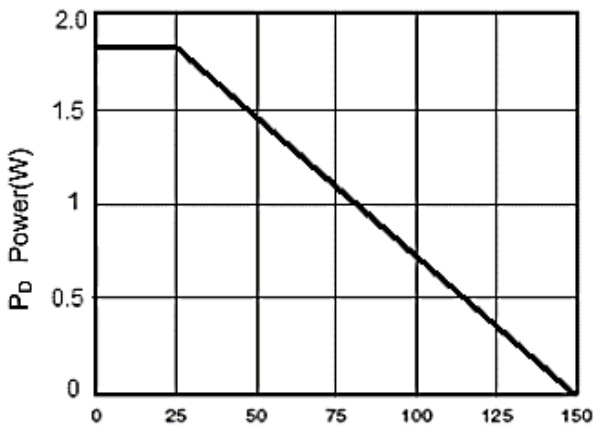
### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-12	-18	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.5	-0.65	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5.2A	-	19	24	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4.2A	-	28	35	mΩ
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-6V, V <sub>GS</sub> =0V f=1.0MHz	-	1100	-	pF
C <sub>oss</sub>	Output Capacitance		-	390	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	300	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-4V, I <sub>D</sub> =-4.1A, V <sub>GS</sub> = -4.5V	-	11.5	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.5	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	3.2	-	nC
td(on)	Turn-on Delay Time	V <sub>DD</sub> =-4V, I <sub>D</sub> =-3.3A, R <sub>G</sub> =1.0Ω, V <sub>GEN</sub> =-4.5V, R <sub>L</sub> =1.2Ω	-	25	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	45	-	ns
td(off)	Turn-off Delay Time		-	72	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	60	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-6.0	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =-4.1A	-	-	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =-4.1A, di/dt=100A/μs	-	20	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	9	-	nC

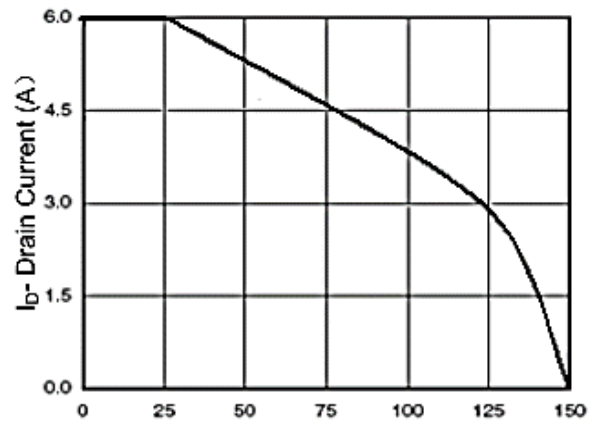
**Note :**

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

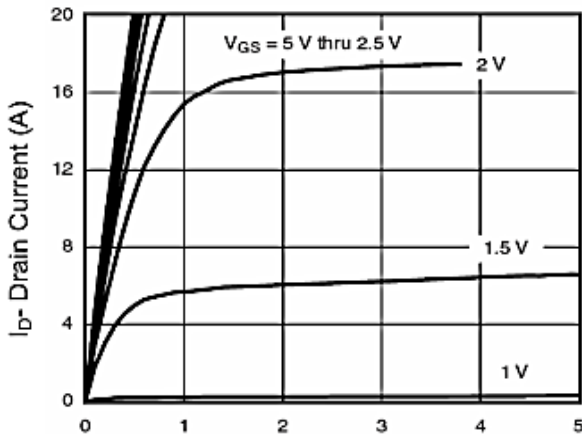
### Typical Characteristics



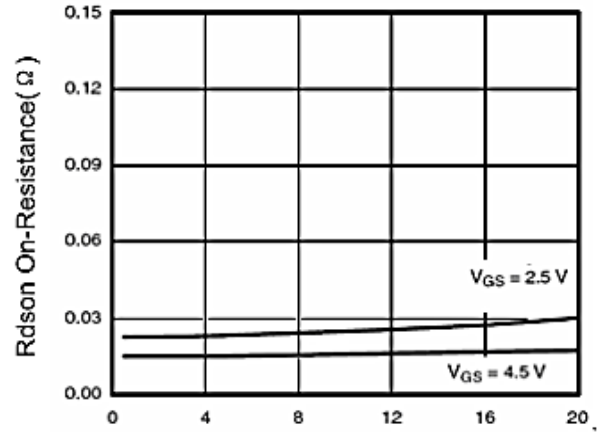
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 1 Power Dissipation**



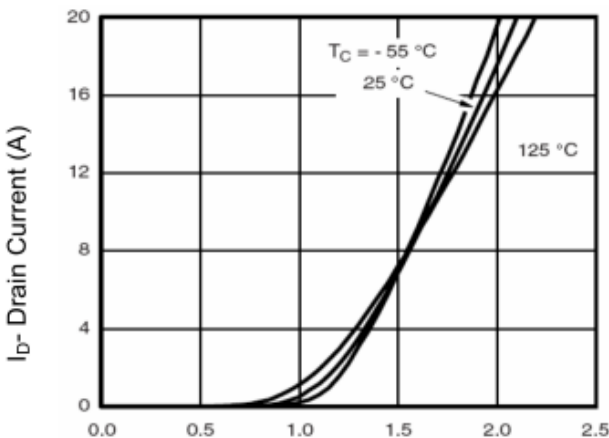
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 2 Drain Current**



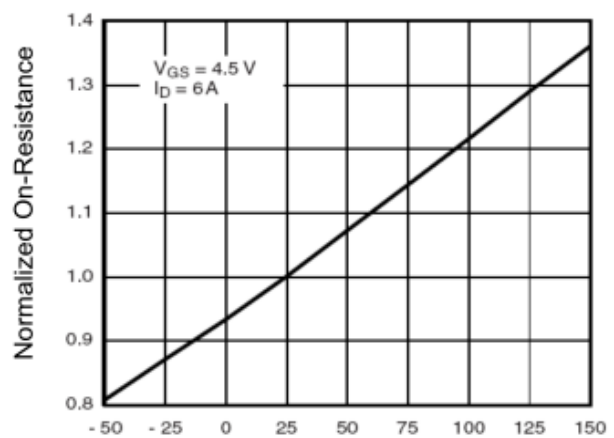
V<sub>ds</sub> Drain-Source Voltage (V)  
**Figure 3 Output Characteristics**



I<sub>D</sub>- Drain Current (A)  
**Figure 4 Drain-Source On-Resistance**

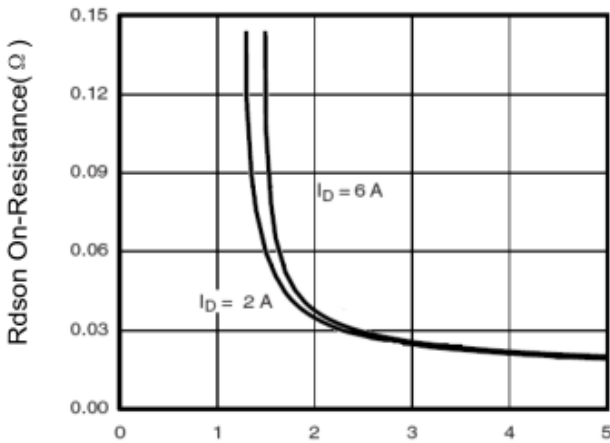


V<sub>gs</sub> Gate-Source Voltage (V)  
**Figure 5 Transfer Characteristics**

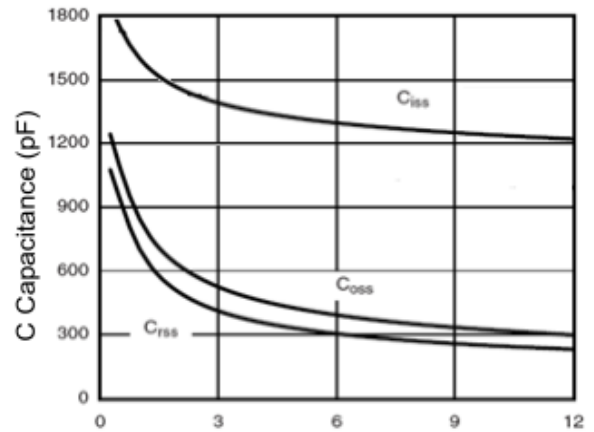


T<sub>J</sub>-Junction Temperature(°C)  
**Figure 6 Drain-Source On-Resistance**

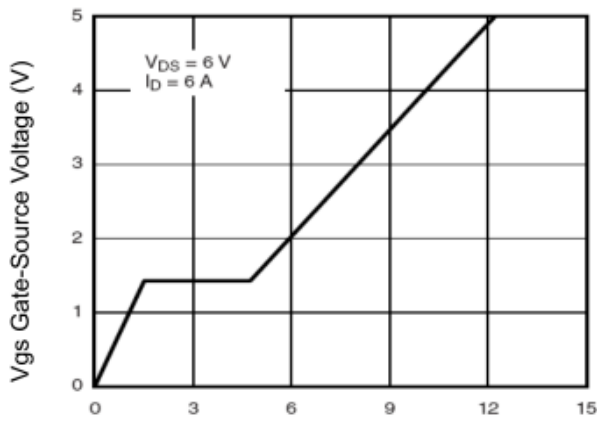
**-12V P-Channel Enhancement Mode MOSFET**



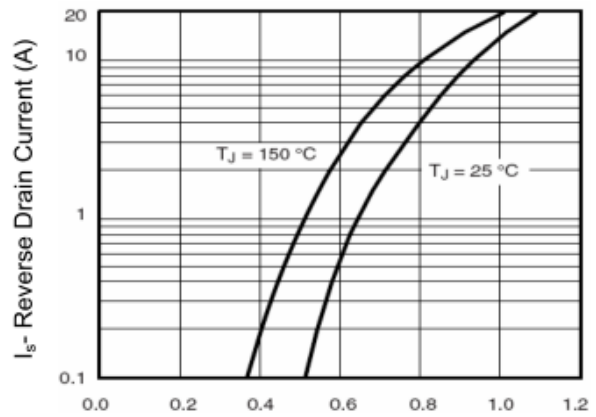
Vgs Gate-Source Voltage (V)  
**Figure 7 Rdson vs Vgs**



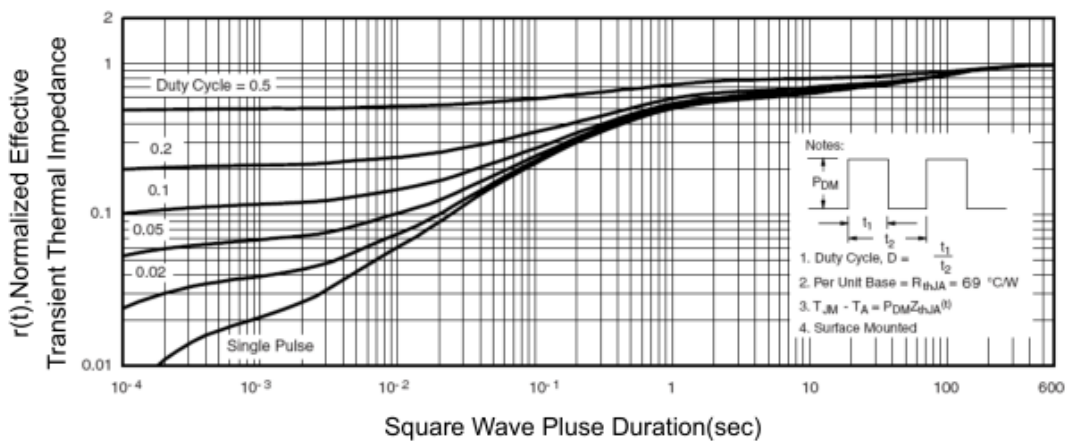
Vds Drain-Source Voltage (V)  
**Figure 8 Capacitance vs Vds**



Qg Gate Charge (nC)  
**Figure 9 Gate Charge**

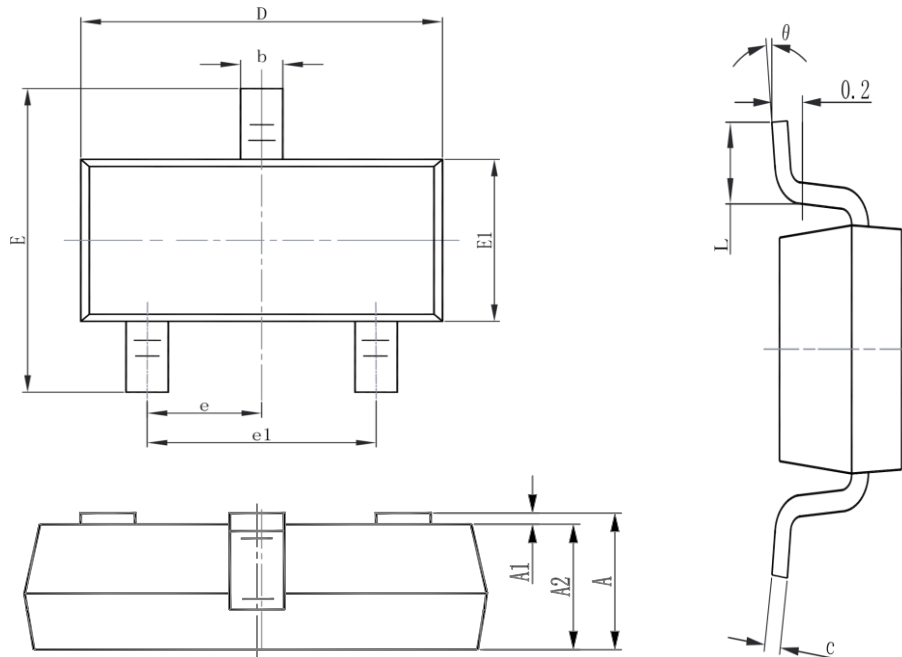


Vsd Source-Drain Voltage (V)  
**Figure 10 Source-Drain Diode Forward**



**Figure 12 Normalized Maximum Transient Thermal Impedance**

### Package Mechanical Data-SOT23-3



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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Edition	Date	Change
Rve1.0	2020/9/8	Initial release

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