

### **100V N-Channel Enhancement Mode MOSFET**

### Description

The AP50N10P uses advanced trench technology

to provide excellent  $R_{\text{DS}(\text{ON})},$  low gate charge and

operation with gate voltages as low as 4.5V. This

device is suitable for use as a

Battery protection or in other Switching application.

#### **General Features**

V<sub>DS</sub> = 100V I<sub>D</sub> =50 A

 $R_{DS(ON)}$  < 22m $\Omega$  @ V<sub>GS</sub>=10V

### Application

Battery protection

Load switch Uninterruptible power supply



#### Package Marking and Ordering Information

<u> </u>	0		
Product ID	Pack	Marking	Qty(PCS)
AP50N10P	TO-220-3L	AP50N10P XXX YYYY	1000

#### Absolute Maximum Ratings (T<sub>c</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
Vds	Drain-Source Voltage	100	V
Vgs	Gate-Source Voltage	±20	V
I₀@Tc=25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	50	A
I⊳@Tc=100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	37	A
Ідм	Pulsed Drain Current <sup>2</sup>	130	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	84	mJ
las	Avalanche Current	41	А
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	149	W
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
R <sub>0JA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	62	°C/W
R <sub>θ</sub> JC	Thermal Resistance Junction-Case <sup>1</sup>	0.84	°C/W

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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =30A			22	mΩ
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	2.5		4.5	V
_	Drain-Source Leakage Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA
DSS		V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	
lgss	Gate-Source Leakage Current	$V_{GS}=\pm20V$ , $V_{DS}=0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =30A		31		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		1.9	3.8	Ω
Qg	Total Gate Charge (10V)	V <sub>DS</sub> =80V , V <sub>GS</sub> =10V , I <sub>D</sub> =30A		27.6		nC
Qgs	Gate-Source Charge			11.4		
Qgd	Gate-Drain Charge			7.9		
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =50V , V <sub>GS</sub> =10V , R <sub>G</sub> =3.3 , I <sub>D</sub> =30A		16.5		
Tr	Rise Time			35		ns
Td(off)	Turn-Off Delay Time			17.5		
T <sub>f</sub>	Fall Time			12		
Ciss	Input Capacitance			1890		
Coss	Output Capacitance	$V_{DS}$ =15V , $V_{GS}$ =0V , f=1MHz $V_{G}$ =V <sub>D</sub> =0V , Force Current		268		pF
Crss	Reverse Transfer Capacitance			67		
ls	Continuous Source Current <sup>1,5</sup>				58	А
lsм	Pulsed Source Current <sup>2,5</sup>				130	А
Vsd	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V
trr	Reverse Recovery Time	IF=30A , dI/dt=100A/μs , T」=25°C		22		nS
Qrr	Reverse Recovery Charge			20		nC

Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width  $\,\leq\,$  300us , duty cycle  $\,\leq\,$  2%

3. The EAS data shows Max. rating . The test condition is  $V_{DS}$ =25V,  $V_{GS}$ =10V, L=0.1mH,  $I_{AS}$ =41A

4.The power dissipation is limited by 150°C junction temperature

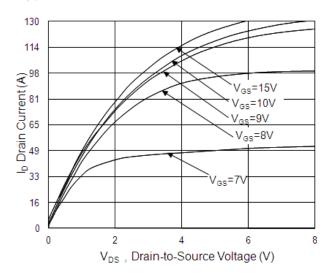
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

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#### **Typical Characteristics**

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**Fig.1 Typical Output Characteristics** 

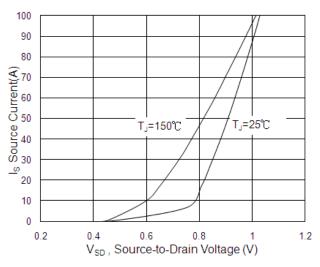


Fig.3 Forward Characteristics of Reverse

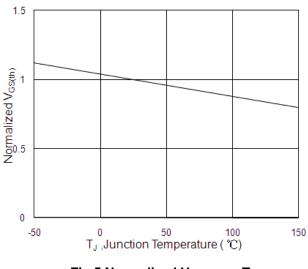


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

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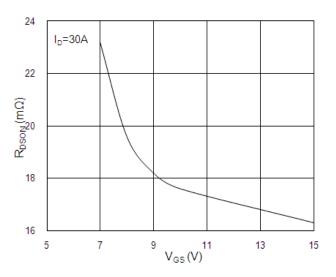


Fig.2 On-Resistance v.s Gate-Source

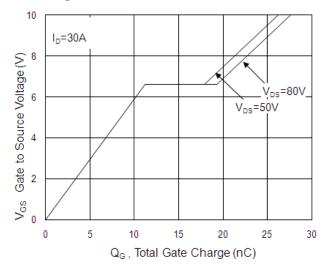
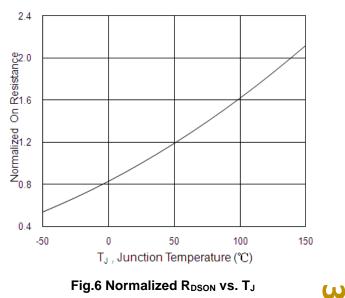


Fig.4 Gate-Charge Characteristics



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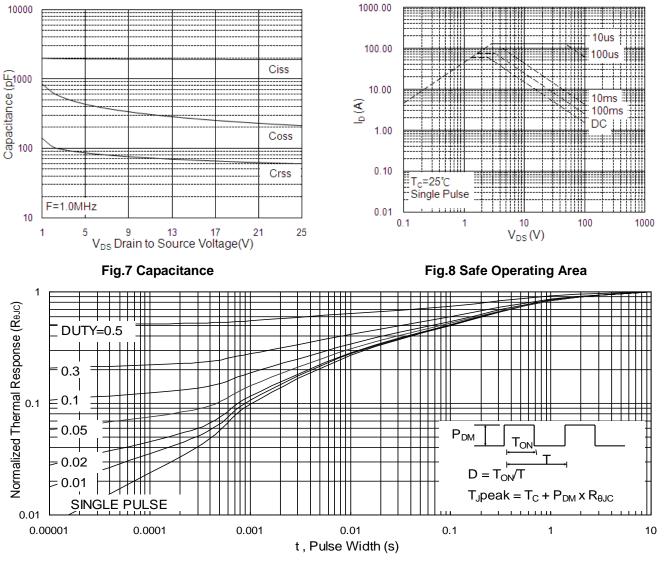
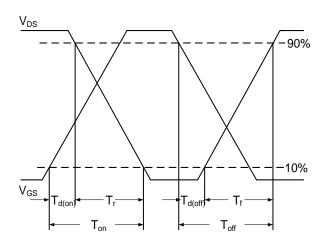


Fig.9 Normalized Maximum Transient Thermal Impedance





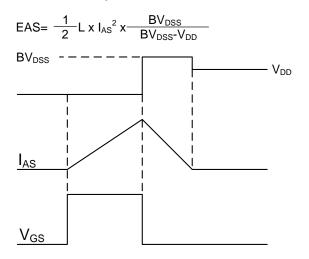
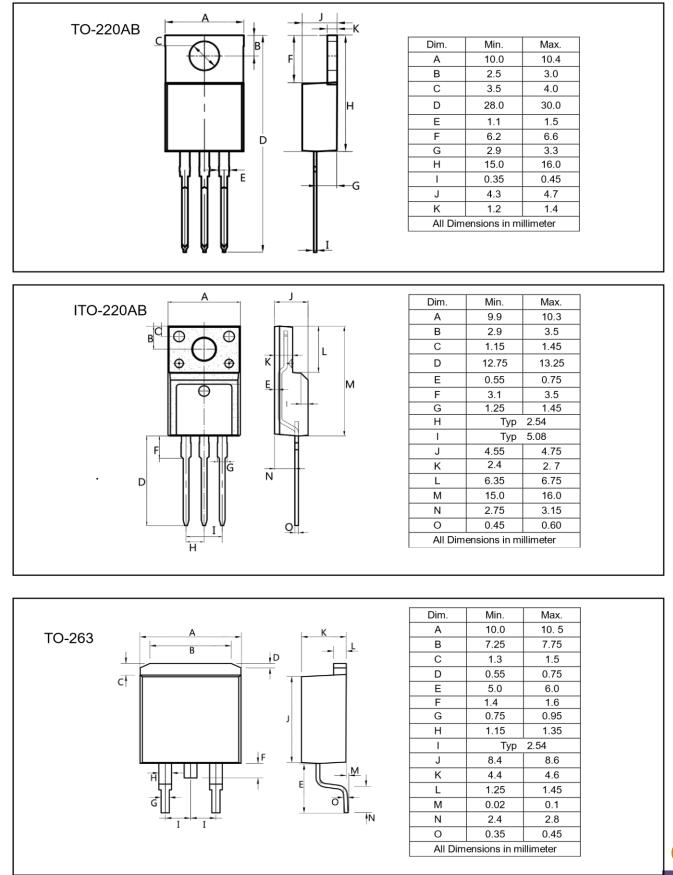


Fig.11 Unclamped Inductive Switching Waveform



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