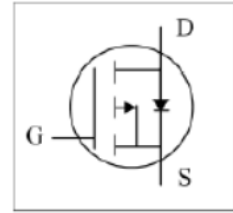


## - 100V P-Channel Enhancement Mode MOSFET

### Description

The AP50P10D uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

It is ESD protected.



### General Features

$V_{DS} = -100V, I_D = -50A$

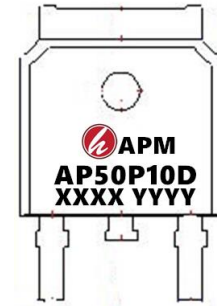
$R_{DS(ON)} < 50m \text{ @ } V_{GS} = -10V$  (Typ:42m)

Super high dense cell design

Advanced trench process technology

Reliable and rugged

High density cell design for ultra low on-resistance



### Application

Power switch

DC/DC converters



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P10D	TO-252-3L	AP50P10D XXX YYYY	2500

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-50	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-23	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-100	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	345	mJ
$I_{AS}$	Avalanche Current	28	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>4</sup>	104	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.2	$^\circ C/W$

## - 100V P-Channel Enhancement Mode MOSFET

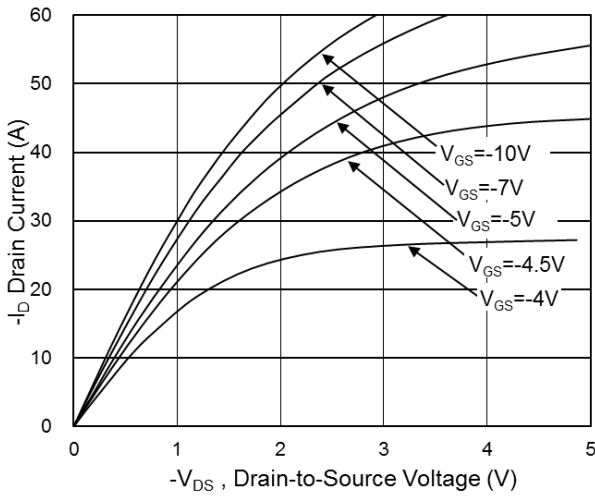
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-100	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-10A	---	42	50	mΩ
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-8A	---	46	55	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	-1.8	-2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-100V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	-50	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =± 20V , V <sub>DS</sub> =0V	---	---	± 100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-10V , I <sub>D</sub> =-10A	---	32	---	S
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-80V , V <sub>GS</sub> =-10V , I <sub>D</sub> =-14A	---	92	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	17.5	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	14	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-50V , V <sub>GS</sub> =-10V , R <sub>G</sub> =3.3 , I <sub>D</sub> =-14A	---	20.5	---	ns
T <sub>r</sub>	Rise Time		---	32.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	123	---	
T <sub>f</sub>	Fall Time		---	63.7	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-25V , V <sub>GS</sub> =0V , f=1MHz	---	6516	---	pF
C <sub>oss</sub>	Output Capacitance		---	223	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	125	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	-35	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C	---	---	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =-14A , di/dt=-100A/μs , T <sub>J</sub> =25°C	---	31.2	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	31.97	---	nC

Note :

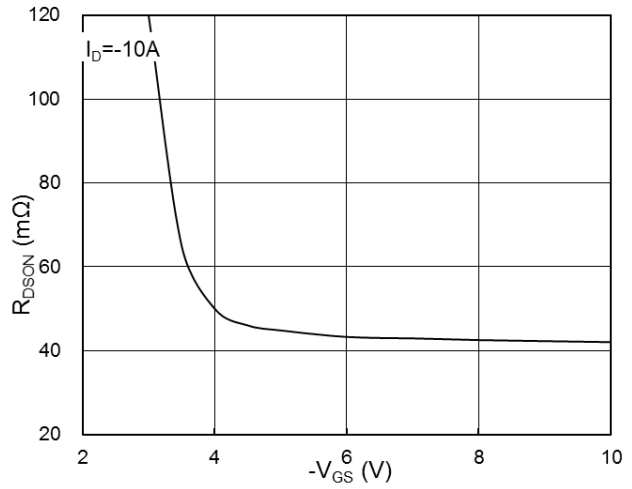
- 1.The data tested by surface mounted on a 1 inch FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is V<sup>DD</sup>=-25V,V<sup>GS</sup>=-10V,L=0.88mH,I<sup>AS</sup>=-28A
- 4.The power dissipation is limited by 150°C junction temperature
- 5 .The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

## -100V P-Channel Enhancement Mode MOSFET

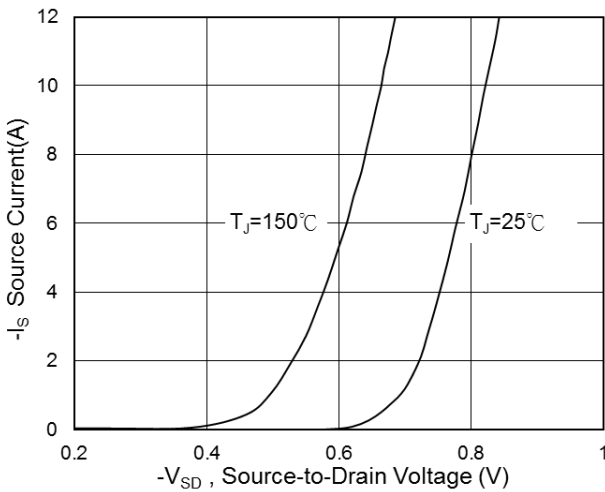
### Typical Characteristics



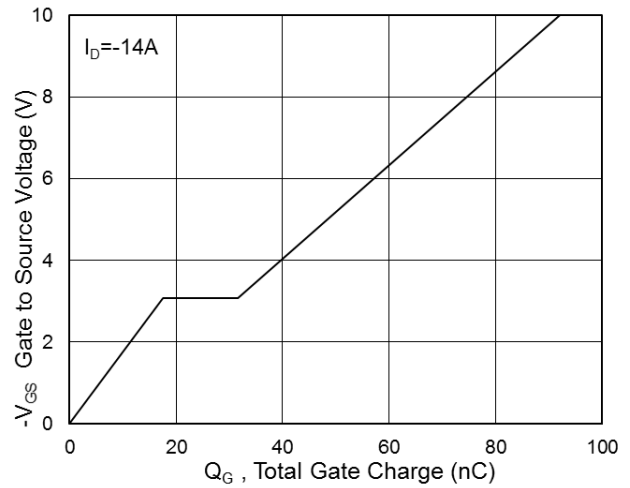
**Fig.1 Typical Output Characteristics**



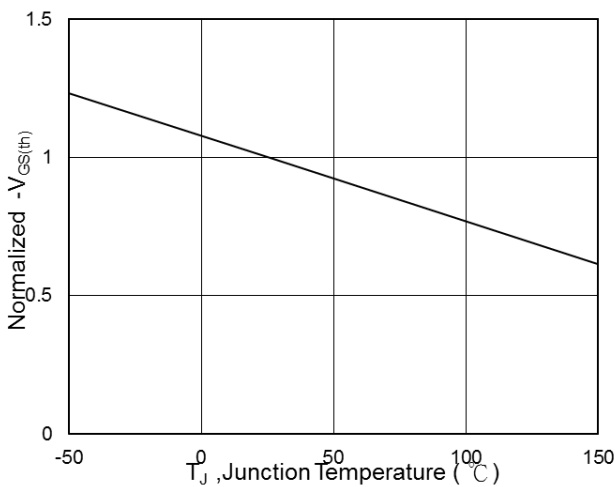
**Fig.2 On-Resistance vs. G-S Voltage**



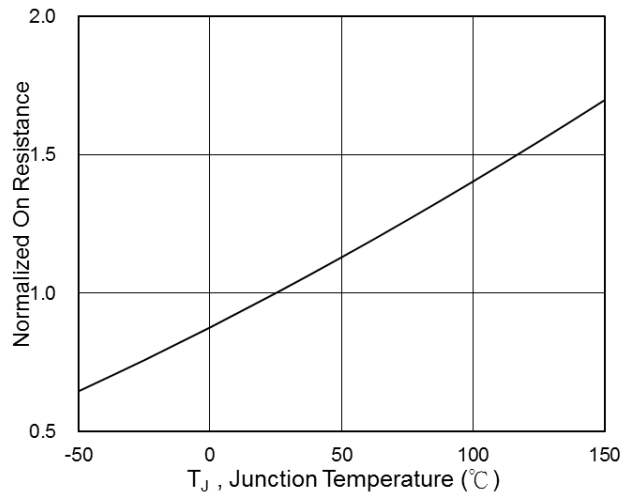
**Fig.3 Typical S-D Diode Forward Voltage**



**Fig.4 Gate-Charge Characteristics**

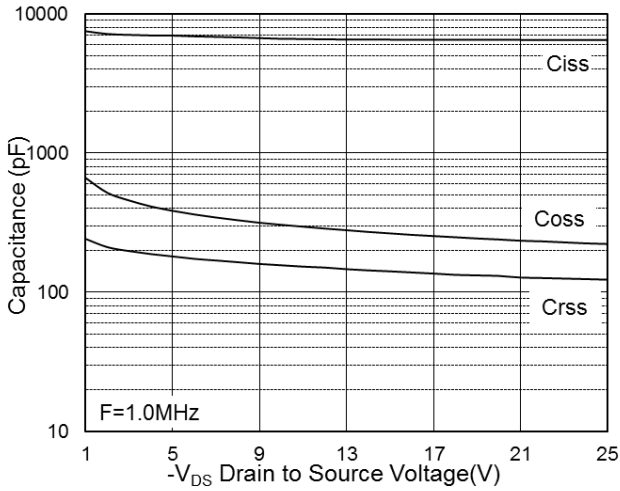


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

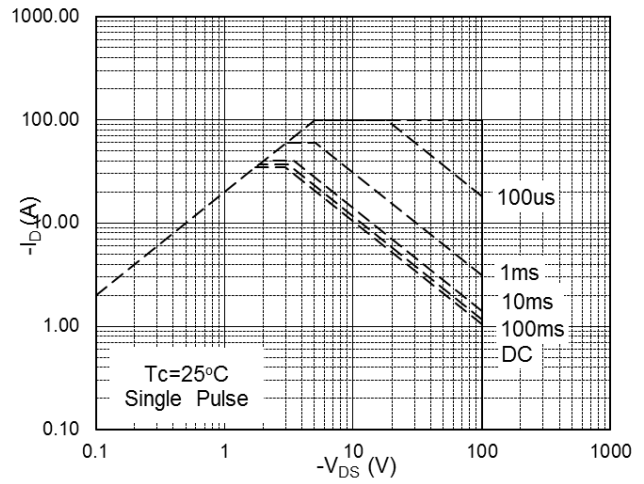


**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

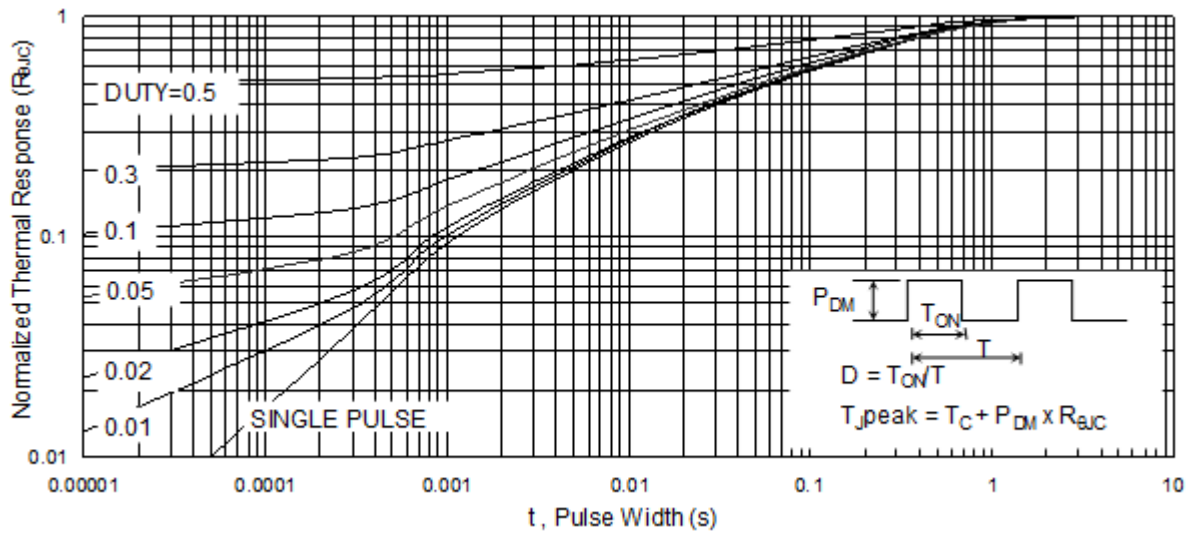
## -100V P-Channel Enhancement Mode MOSFET



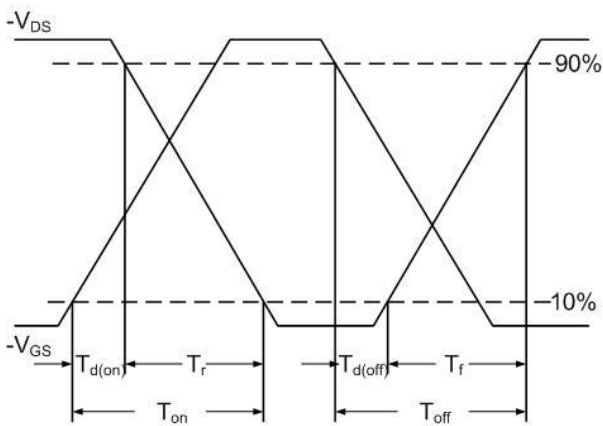
**Fig.7 Capacitance**



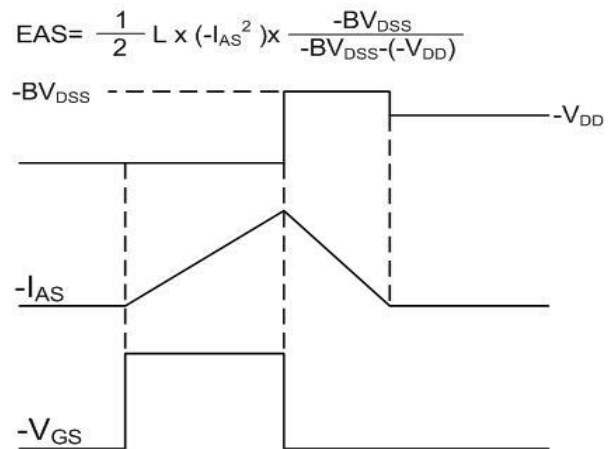
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



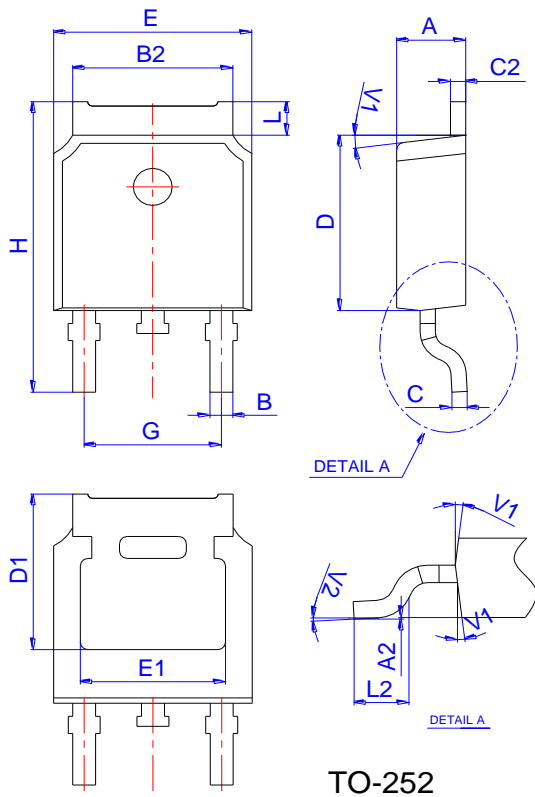
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

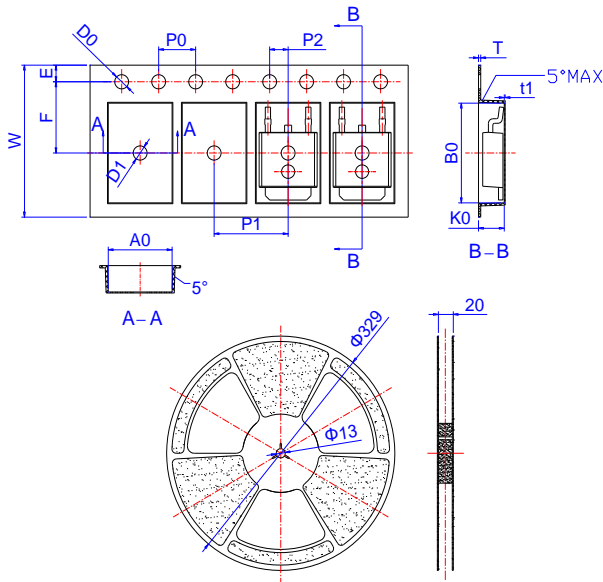
## -100V P-Channel Enhancement Mode MOSFET

### Package Mechanical Data



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

### Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

**- 100V P-Channel Enhancement Mode MOSFET**  
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