### **30V N-Channel Enhancement Mode MOSFET**

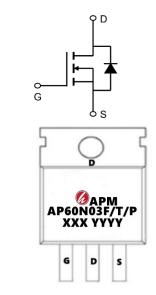
### Description

The AP60N03F/T/P uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = 30V I_{D} = 60A$ 

 $R_{DS(ON)} < 8.5 \text{m}\Omega$  @  $V_{GS}=10V$  (Type:  $6.0 \text{m}\Omega$ )



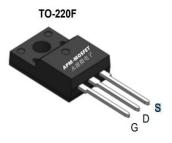
#### **Application**

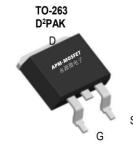
**BLDC** 

Wireless impact

Mobile phone fast charging







**Package Marking and Ordering Information** 

Product ID	Pack	Marking	Qty(PCS)
AP60N03F	TO-220-3L	AP60N03F XXX YYYY	1000
AP60N03T	TO-263-3L	AP60N03T XXX YYYY	800
AP60N03P	TO-220-3L	AP60N03P XXX YYYY	1000

### Absolute Maximum Ratings (T<sub>C</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	30	V
VGS	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	60	А
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	40	А
IDM	Pulsed Drain Current <sup>2</sup>	92	Α
EAS	Single Pulse Avalanche Energy <sup>3</sup>	57.8	mJ
IAS	Avalanche Current	34	Α
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	29	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	℃
R <sub>θ</sub> JA	Thermal Resistance Junction-ambient <sup>1</sup>	62	°C/W
R₀JC	Thermal Resistance Junction-Case <sup>1</sup>	4.32	°C/W



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## Electrical Characteristics (Tc=25°Cunless otherwise noted)

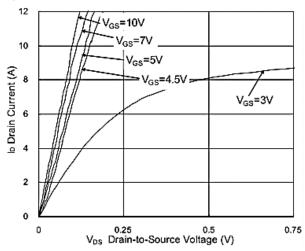
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	30	33		V
RDS(ON) S	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =12A		6.0	8.5	mΩ
KD3(ON)	Static Drain-Source On-Nesistance	auc Drain-Source On-Resistance V <sub>GS</sub> =4.5V , I <sub>D</sub> =10A		8.0	13	11177
VGS(th)	Gate Threshold Voltage	\/=\/	1.0	1.6	2.5	V
△VGS(th)	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=250$ uA		-5.8		mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	-		1	uA
1000	Diam-Source Leakage Current	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =15A		9.8		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		1.7		Ω
Qg	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =12A		12.8		
Qgs	Gate-Source Charge			3.3		nC
Qgd	Gate-Drain Charge			6.5		
Td(on)	Turn-On Delay Time			4.5		
Tr	Rise Time	V <sub>DD</sub> =12V , V <sub>GS</sub> =10V ,		10.8		
Td(off)	Turn-Off Delay Time	$R_G$ =3.3Ω $I_D$ =5Α		25.5		ns
T <sub>f</sub>	Fall Time			9.6		
Ciss	Input Capacitance			1317		
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		163		pF
Crss	Reverse Transfer Capacitance			131		
IS	Continuous Source Current <sup>1,6</sup>	\/ -\/ -0\/ Fares C:			46	Α
ISM	Pulsed Source Current <sup>2,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	-		92	Α
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1	V

#### Note:

- 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- $2 \, {}_{\searrow}$  The data tested by pulsed , pulse width  $\leqq 300 us$  , duty cycle  $\leqq 2\%$
- $3 \times$  The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=34A
- $4 \, {\rm ^{\! \circ}}$  The power dissipation is limited by 150°C junction temperature
- 5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

### **30V N-Channel Enhancement Mode MOSFET**

## **Typical Characteristics**



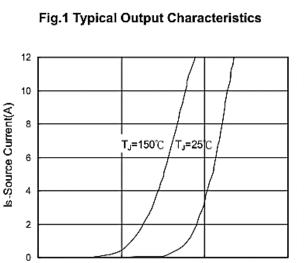


Fig.3 Forward Characteristics of Reverse

V<sub>SD</sub>, Source-to-Drain Voltage (V)

0.9

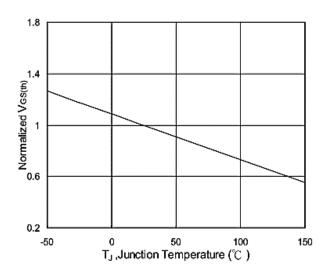


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

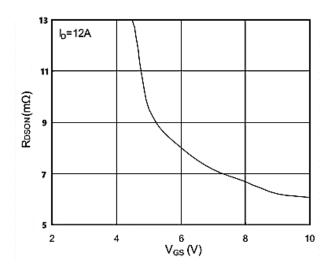


Fig.2 On-Resistance vs. G-S Voltage

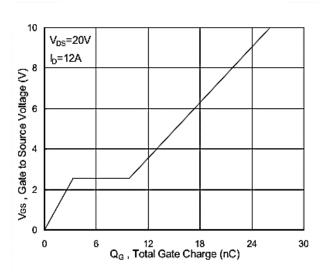


Fig.4 Gate-Charge Characteristics

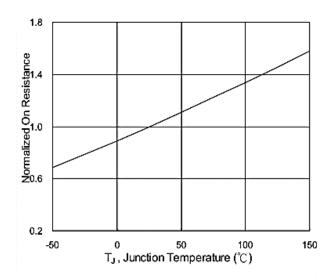
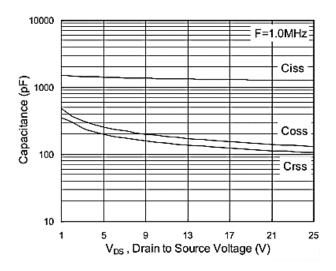


Fig.6 Normalized RDSON vs. TJ



### 30V N-Channel Enhancement Mode MOSFET



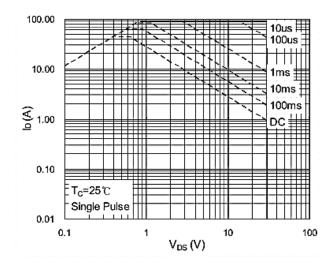


Fig.7 Capacitance

Fig.8 Safe Operating Area

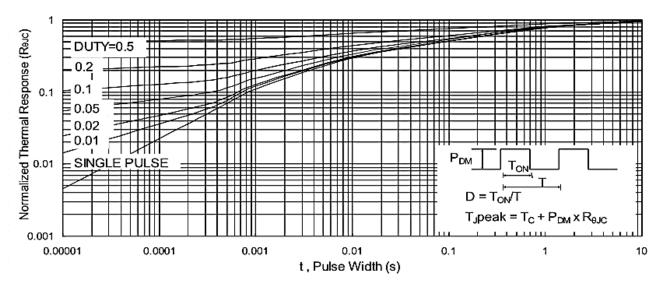


Fig.9 Normalized Maximum Transient Thermal Impedance

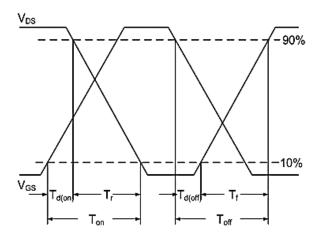


Fig.10 Switching Time Waveform

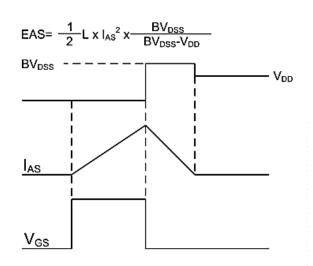
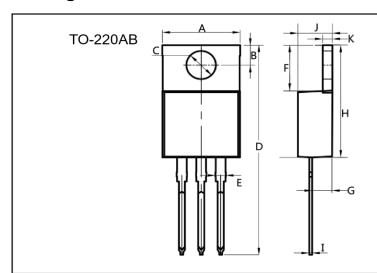


Fig.11 Unclamped Inductive Switching Waveform

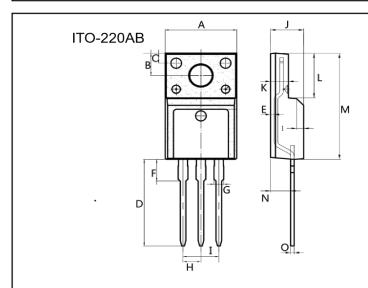


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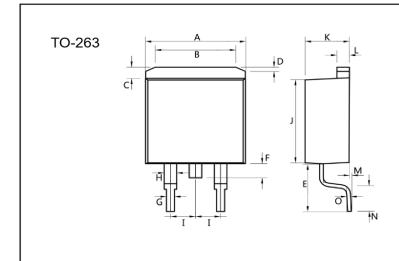
# Package Mechanical Data-PDFN5\*6-8L-JQ Single



Min.	Max.	
10.0	10.4	
2.5	3.0	
3.5	4.0	
28.0	30.0	
1.1	1.5	
6.2	6.6	
2.9	3.3	
15.0	16.0	
0.35	0.45	
4.3	4.7	
1.2	1.4	
All Dimensions in millimeter		
	10.0 2.5 3.5 28.0 1.1 6.2 2.9 15.0 0.35 4.3	



Dim.	Min.	Max.
Α	9.9	10.3
В	2.9	3.5
С	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
Н	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2. 7
L	6.35	6.75
М	15.0	16.0
N	2.75	3.15
0	0.45	0.60
All Dimensions in millimeter		



Dim.	Min.	Max.
Α	10.0	10. 5
В	7.25	7.75
С	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
Н	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
М	0.02	0.1
N	2.4	2.8
0	0.35	0.45
All Dimensions in millimeter		



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## **30V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2019/4/10	Initial release
Rve1.1	2022/1/10	Reduce internal RDS

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TK16J60W,S1VQ(O 2SK2614(TE16L1,Q) DMN1017UCP3-7 DMN1053UCP4-7 SQJ469EP-T1-GE3 NTE2384 DMC2700UDMQ-7
DMN2080UCB4-7 DMN61D9UWQ-13 US6M2GTR DMN31D5UDJ-7 DMP22D4UFO-7B DMN1006UCA6-7 DMN16M9UCA6-7
STF5N65M6 IRF40H233XTMA1 STU5N65M6 DMN6022SSD-13 DMN13M9UCA6-7 DMTH10H4M6SPS-13 DMN2990UFB-7B
IPB80P04P405ATMA2 2N7002W-G MCAC30N06Y-TP MCQ7328-TP BXP7N65D BXP4N65F AOL1454G WMJ80N60C4 BXP2N20L
BXP2N65D BXT1150N10J BXT1700P06M TSM60NB380CP ROG RQ7L055BGTCR DMNH15H110SK3-13 SLF10N65ABV2
BSO203SP BSO211P IPA60R230P6 IPA60R460CE