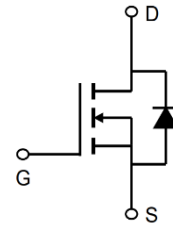


## 500V N-Channel Enhancement Mode MOSFET

### Description

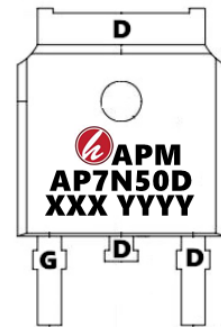
The AP7N50D is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



### General Features

$V_{DS} = 500V$   $I_D = 7A$

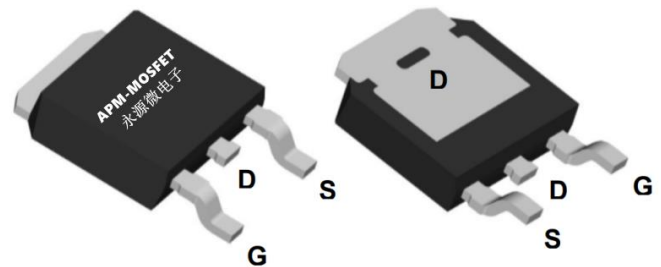
$R_{DS(ON)} < 1.5\Omega @ V_{GS}=10V$  (Type:  $1.2\Omega$ )



### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP7N50D	TO-252-3L	AP7N50D XXX YYYY	2500

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage ( $V_{GS} = 0V$ )	500	V
$I_D$	Continuous Drain Current	7	A
$I_{DM}$	Pulsed Drain Current (note1)	28	A
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy (note2)	247	mJ
$I_{AR}$	Avalanche Current (note1)	7	A
$E_{AR}$	Repetitive Avalanche Energy (note1)	18	mJ
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	32.9	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55~+150	$^\circ C$
$R_{thJC}$	Thermal Resistance, Junction-to-Case	3.8	$^\circ C/W$
$R_{thJA}$	Thermal Resistance, Junction-to-Ambient	13.3	$^\circ C/W$

## 500V N-Channel Enhancement Mode MOSFET

### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

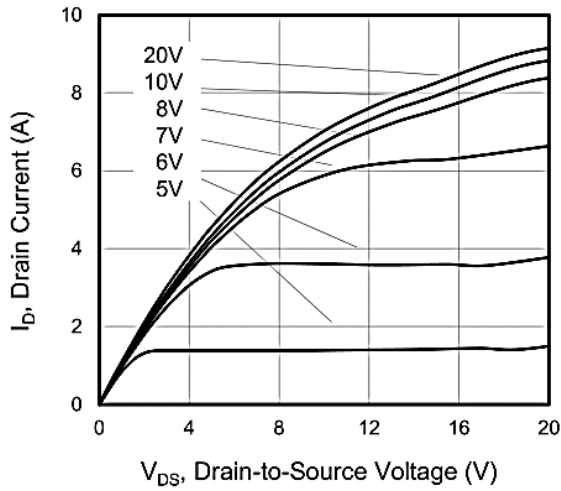
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	500	550	--	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V, T <sub>J</sub> =25°C	--	--	1	μA
IGSS	Gate-Source Leakage	V <sub>GS</sub> = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	--	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A	--	1.2	1.5	Ω
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz	--	700	--	pF
C <sub>oss</sub>	Output Capacitance		--	94	--	
C <sub>rss</sub>	Reverse Transfer Capacitance		--	12	--	
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =520V, I <sub>D</sub> = 7A, V <sub>GS</sub> = 10V	--	19	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.7	--	
Q <sub>gd</sub>	Gate-Drain Charge		--	11	--	
td(on)	Turn-on Delay Time	V <sub>DD</sub> =325V, I <sub>D</sub> = 7A, R <sub>G</sub> = 25Ω	--	13	--	ns
t <sub>r</sub>	Turn-on Rise Time		--	20	--	
td(off)	Turn-off Delay Time		--	76	--	
t <sub>f</sub>	Turn-off Fall Time		--	40	--	
I <sub>S</sub>	Continuous Body Diode Current	T <sub>C</sub> = 25 °C	--	--	7.0	A
I <sub>SM</sub>	Pulsed Diode Forward Current		--	--	28	A
V <sub>SD</sub>	Body Diode Voltage	T <sub>J</sub> = 25°C, I <sub>SD</sub> = 7A, V <sub>GS</sub> = 0V	--	--	1.4	V
trr	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A, di <sub>F</sub> /dt = 100A/μs	--	260	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	3.8	--	μC

#### Note :

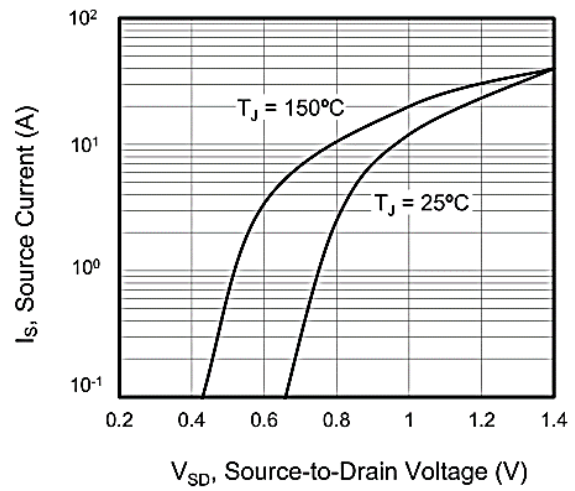
- 1、 The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . I<sub>AS</sub> = 4.5A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

**500V N-Channel Enhancement Mode MOSFET**

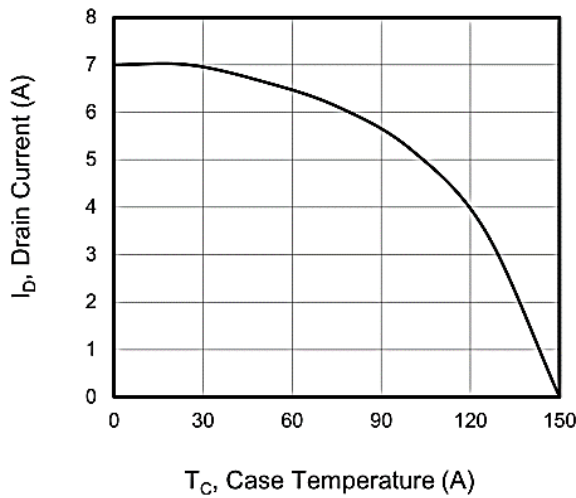
**Typical Characteristics**



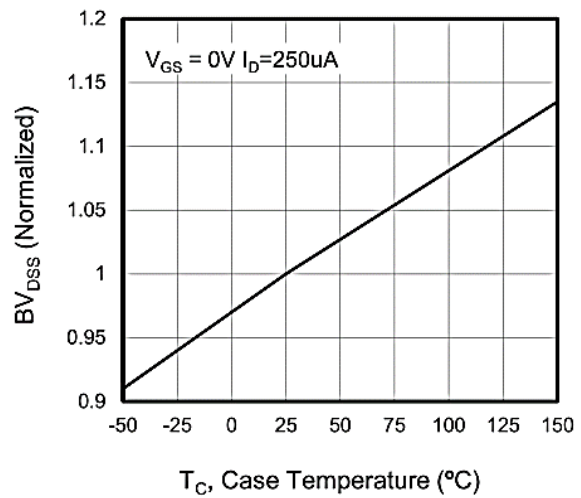
**Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )**



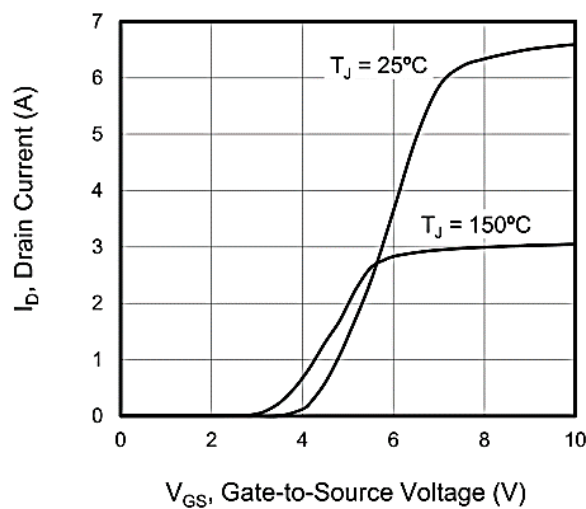
**Figure 2. Body Diode Forward Voltage**



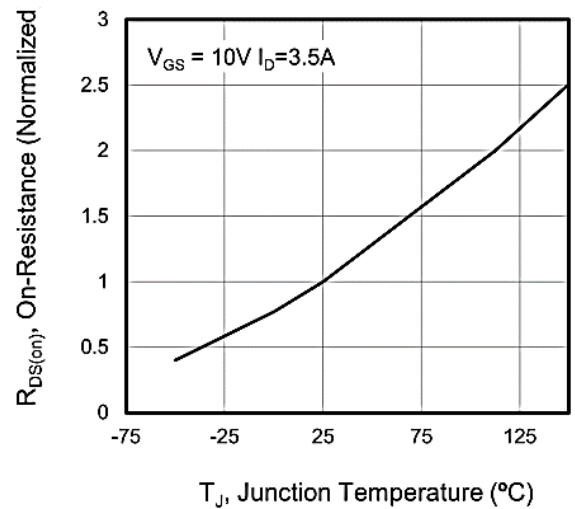
**Figure 3. Drain Current vs. Temperature**



**Figure 4.  $BV_{DSS}$  Variation vs. Temperature**



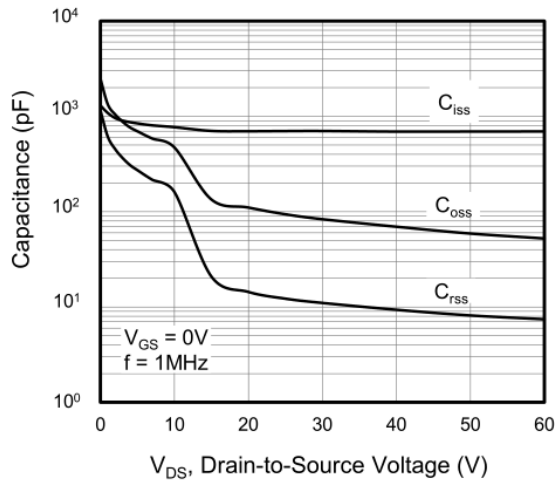
**Figure 5. Transfer Characteristics**



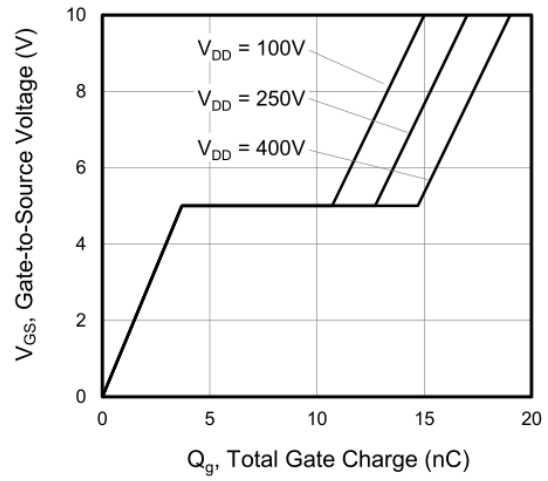
**Figure 6. On-Resistance vs. Temperature**



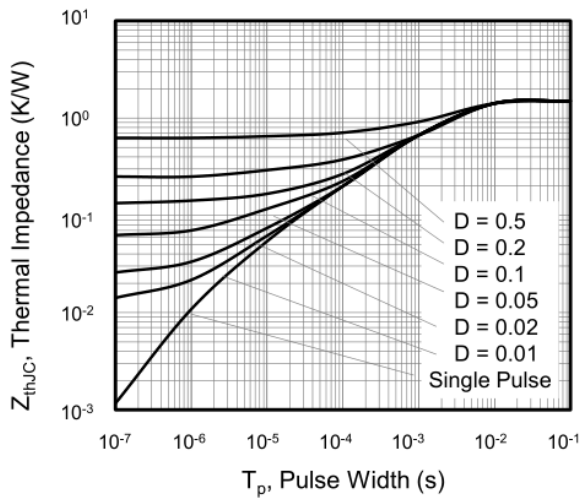
**500V N-Channel Enhancement Mode MOSFET**



**Figure 7. Capacitance**

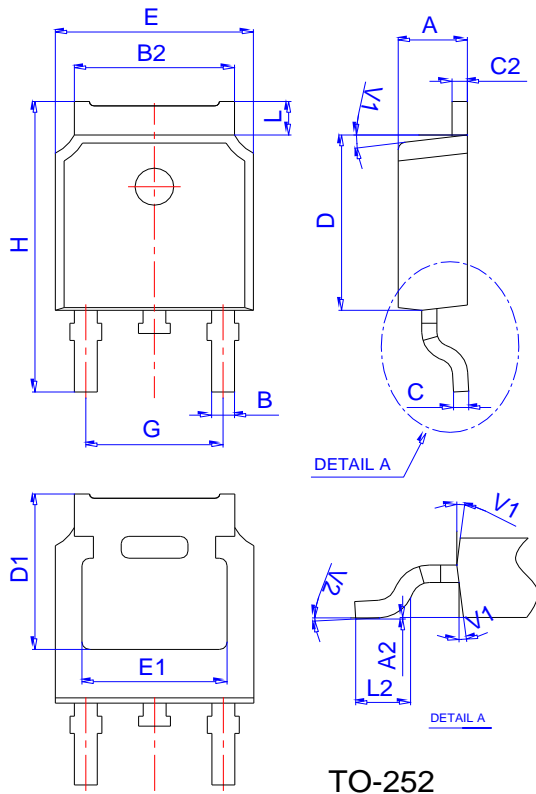


**Figure 8. Gate Charge**



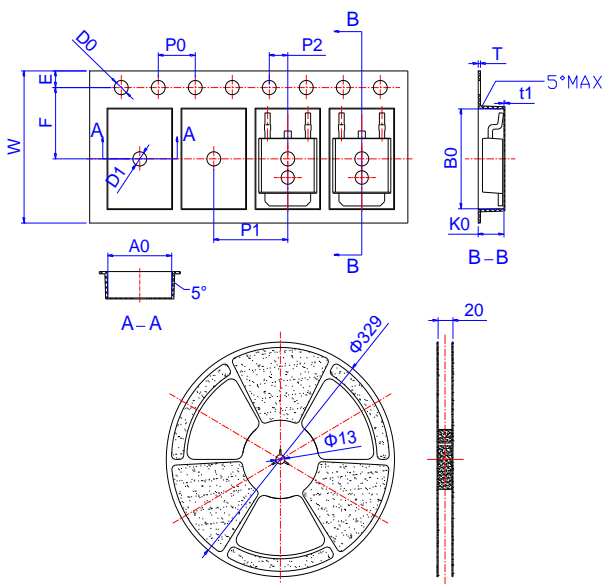
**Figure 9. Transient Thermal Impedance**

### Package Mechanical Data



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

### Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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**500V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2021/1/31	Initial release

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