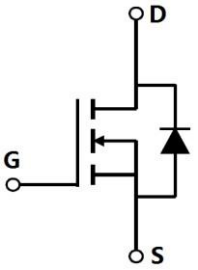
APG40N10NF

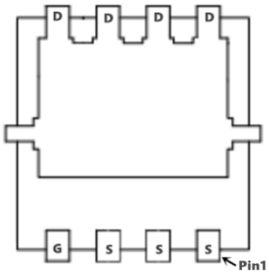
100V N-SGT Enhancement Mode MOSFET

General Description

APG40N10NF use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in





Features

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

Applications

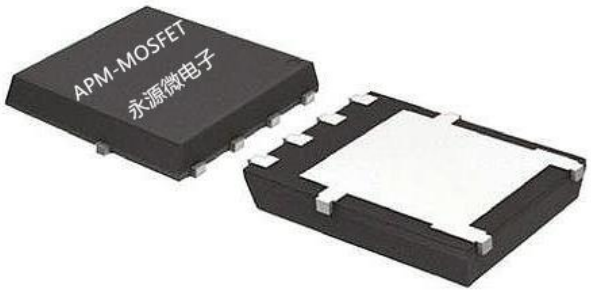
Consumer electronic power supply

Motor control

Synchronous-rectification

Isolated DC

Synchronous-rectification application



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG40N10NF	DFN5*6-8L	APG40N10NF XXX YYYY	5000

Absolute Maximum Ratings at T_j=25℃ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	100	V
Gate source voltage	VGS	±20	V
Continuous drain current[1], T_C=25 ℃	ID	40	A
Pulsed drain current[2], T_C=25 ℃	ID, pulse	120	A
Power dissipation[3], T_C=25 ℃	P_D	72	W
Single pulsed avalanche energy[5]	EAS	30	mJ
Operation and storage temperature	Tstg，Tj	-55 to 150	℃
Thermal resistance, junction-case	RθJC	1.74	℃/W

Thermal resistance, junction-ambient[4]	RθJA	62	℃/W

Electrical Characteristics at T_j=25 ℃ unless otherwise specified

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=250 μA	100			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 μA	1.0		2.5	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10 V, I_D=8 A		16	20	mΩ
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=4.5 V, I_D=6 A			26	mΩ
Gate-source leakage current	I_{GSS}	V_{GS}=20 V			100	nA
					-100	
Drain-source leakage current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V			1	μA
Input capacitance	Ciss	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz		1190.6		pF
Output capacitance	Coss			194.6		pF
Reverse transfer capacitance	Crss			4.1		pF
Turn-on delay time	td(on)	V_{GS}=10 V, V_{DS}=50 V, R_G=2.2 Ω, I_D=10 A		17.8		ns
Rise time	t_r			3.9		ns
Turn-off delay time	td(off)			33.5		ns
Fall time	t_f			3.2		ns
Total gate charge	Q_g	I_D=8 A, V_{DS}=50 V, V_{GS}=10 V		19.8		nC
Gate-source charge	Q_{gs}			2.4		nC
Gate-drain charge	Q_{gd}			5.3		nC
Gate plateau voltage	$V_{plateau}$			3.2		V
Diode forward current	I_S	V_{GS}<V_{th}			40	
Pulsed source current	I_{SP}				120	A
Diode forward voltage	V_{SD}	I_S=8 A, V_{GS}=0 V			1.3	V
Reverse recovery time	t_{rr}	I_S=8 A, di/dt=100 A/μs		50.2		ns
Reverse recovery charge	Q_{rr}			95.1		nC
Peak reverse recovery current	I_{rrm}			2.5		A

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 ℃.
5) V_{DD}=50 V, R_G=25 Ω, L=0.3 mH, starting T_j=25 ℃.

Electrical Characteristics Diagrams

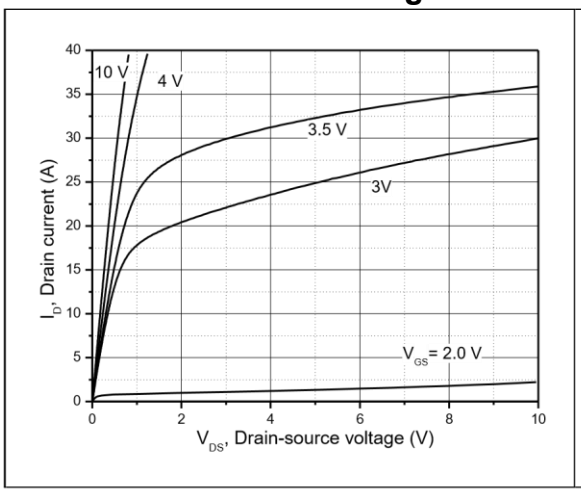


Figure 1, Typ. output characteristics

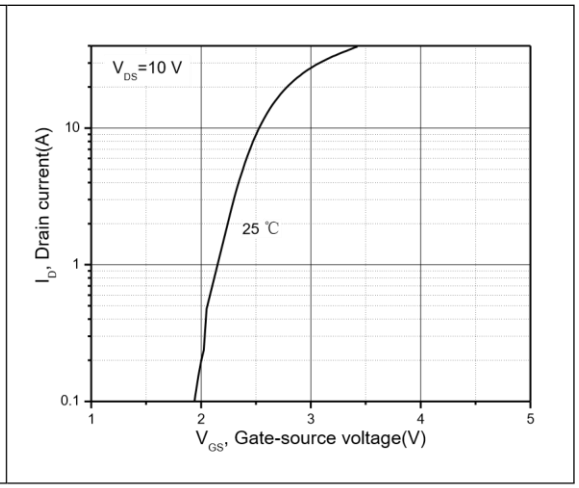


Figure 2, Typ. transfer characteristics

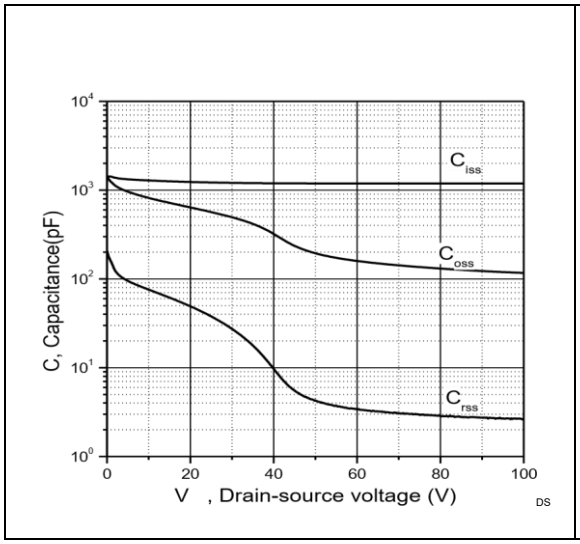


Figure 3, Typ. capacitances

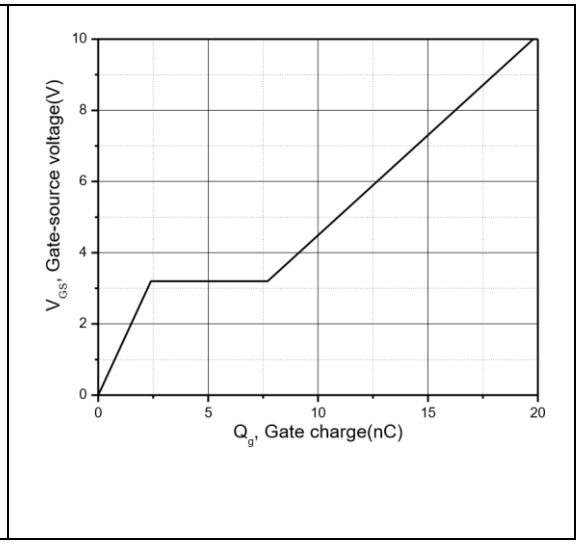


Figure 4, Typ. gate charge

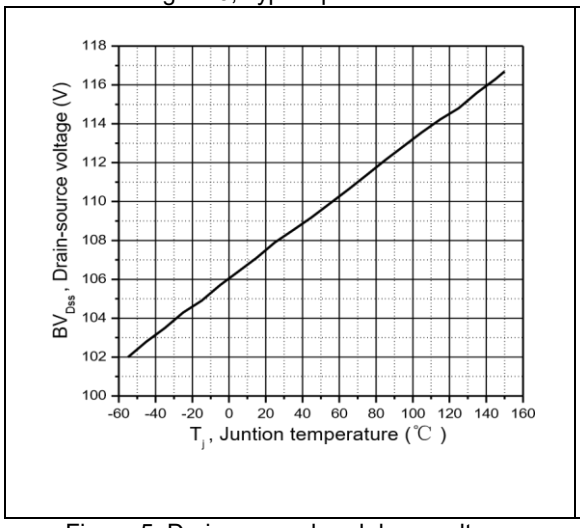


Figure 5, Drain-source breakdown voltage

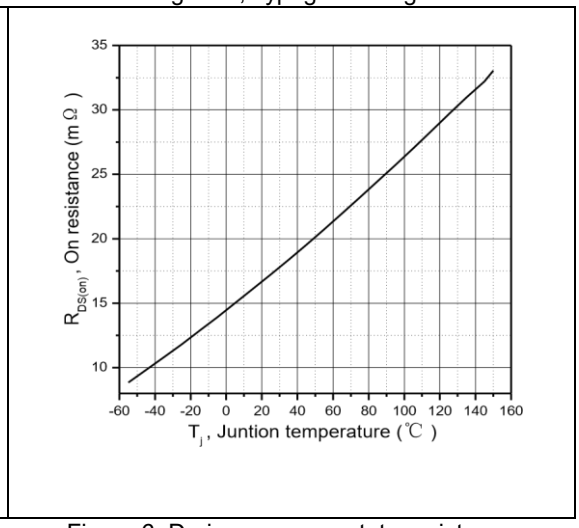


Figure 6, Drain-source on-state resistance

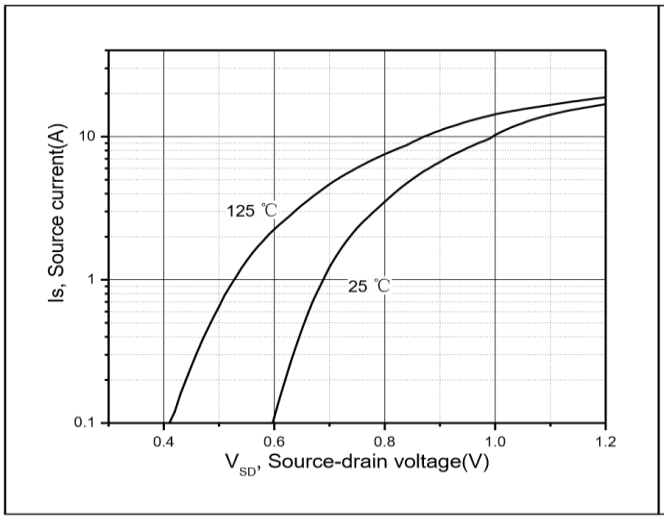


Figure 7, Forward characteristic of body diode

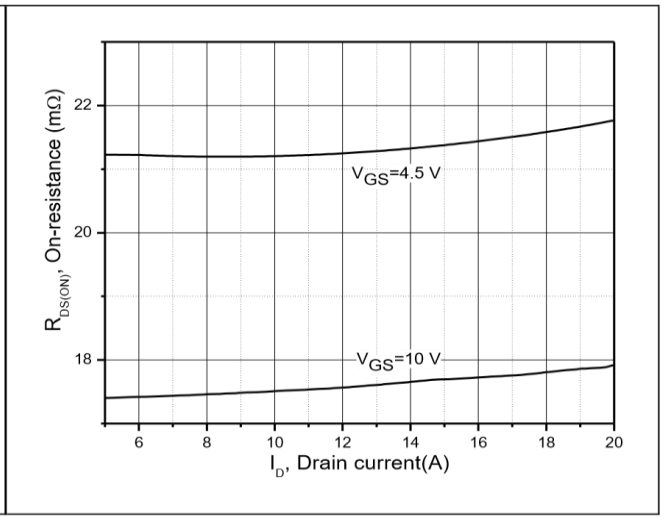


Figure 8, Drain-source on-state resistance

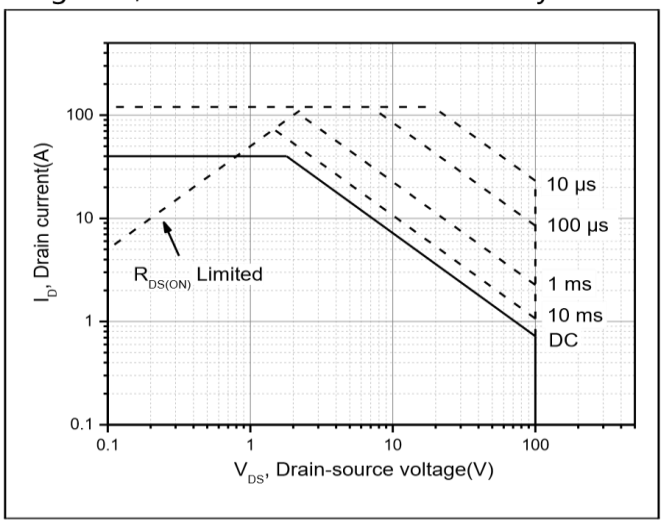


Figure 9, Safe operation area T_C=25 ℃

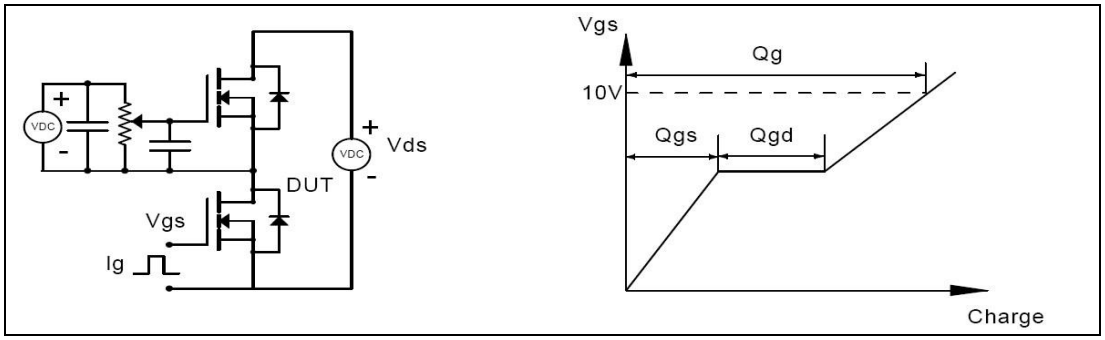


Figure 1, Gate charge test circuit & waveform

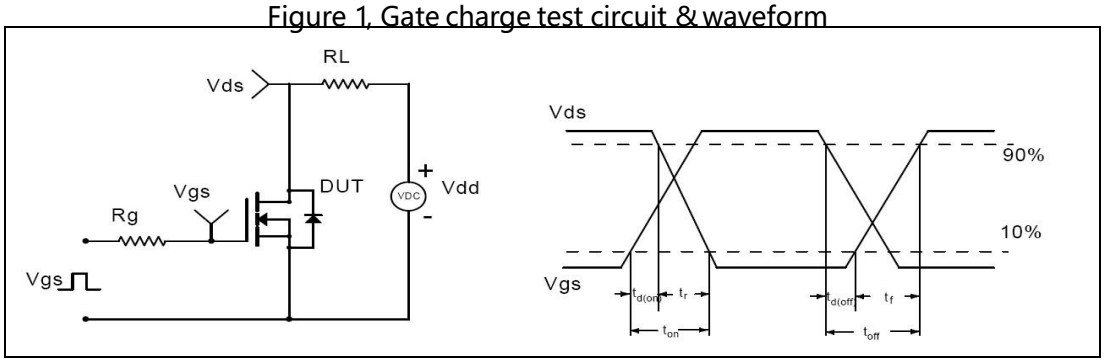


Figure 2, Switching time test circuit & waveforms

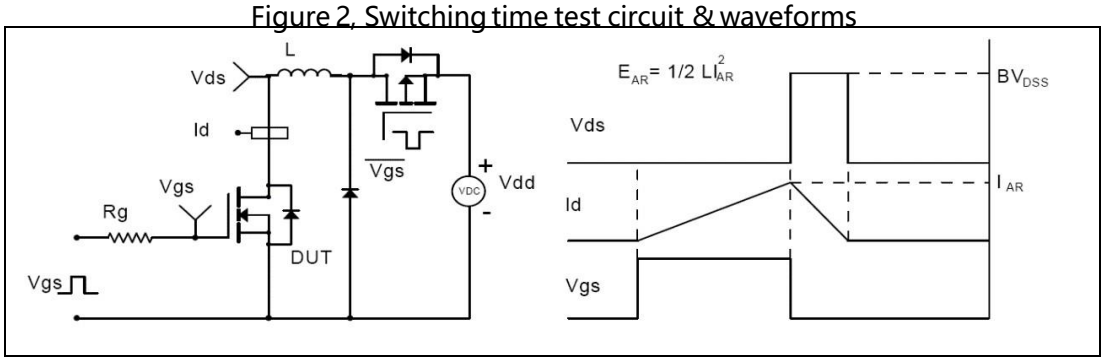


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

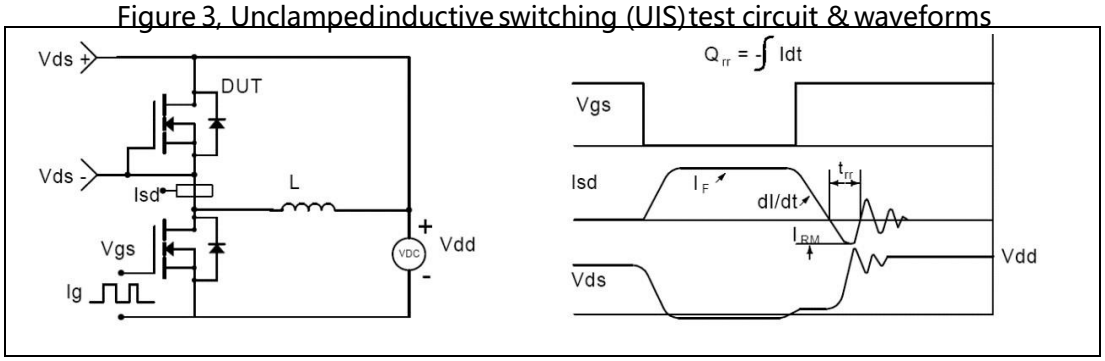
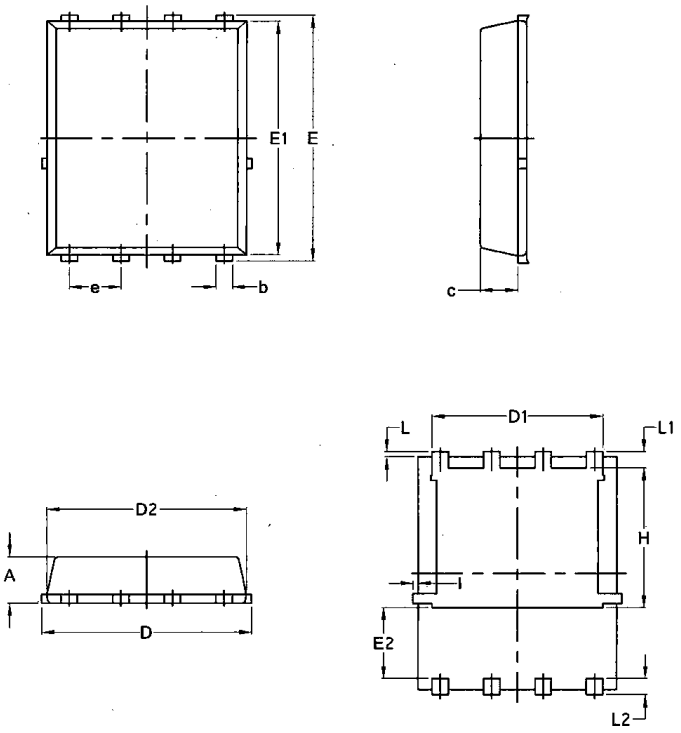


Figure 4, Diode reverse recovery test circuit & waveforms

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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100V N-SGT Enhancement Mode MOSFET

Edition	Date	Change
Rve3.8	2019/1/31	Initial release

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