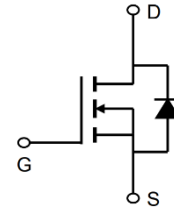


100V N-Channel Enhancement Mode MOSFET

Description

The APG40N10D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 100V$ $I_D = 40A$

$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=10V$



Application

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG40N10S	SOP-8	APG40N10S XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain source voltage	100	V
V_{GS}	Gate source voltage	± 20	V
I_D	Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	40	A
I_D , pulse	Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	120	A
P_D	Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	71	W
EAS	Single pulsed avalanche energy ⁵⁾	57	mJ
Tstg, T_j	Operation and storage temperature	-55 to 150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal resistance, junction-case	1.76	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal resistance, junction-ambient ⁴⁾	62	$^\circ\text{C/W}$



100V N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BVDSS	Drain-source breakdown voltage	V _{GS} =0 V, I _D =250 μA	100	107		V
VGS(th)	Gate threshold voltage	V _{DS} =V _{GS} , I _D =250 μA	1.2	1.5	2.5	V
RDS(ON)	Drain-source on-state resistance	V _{GS} =10 V, I _D =10 A		19.0	25.0	mΩ
RDS(ON)	Drain-source on-state resistance	V _{GS} =4.5 V, I _D =7 A		24.4	30.0	mΩ
IGSS	Gate-source leakage current	V _{GS} =±20 V			±100	nA
IDSS	Drain-source leakage current	V _{DS} =100 V, V _{GS} =0 V			1	uA
Ciss	Input capacitance	V _{GS} =0 V, V _{DS} =50 V, f=100 kHz		1003.9		pF
Coss	Output capacitance			185.4		pF
Crss	Reverse transfer capacitance			9.8		pF
td(on)	Turn-on delay time	V _{GS} =10 V, V _{DS} =50 V, R _G =10 Ω, I _D =5 A		16.6		ns
t _r	Rise time			3.8		ns
td(off)	Turn-off delay time			75.5		ns
t _f	Fall time			46		ns
Q _g	Total gate charge	I _D =5 A, V _{DS} =50V, V _{GS} =10V		16.2		nc
Q _{gs}	Gate-source charge			2.8		nc
Q _{gd}	Gate-drain charge			4.1		nc
Vplateau	Gate plateau voltage			3		V
I _s	Diode forward current	V _{GS} <V _{th}		30		A
ISP	Pulsed source current			90		A
trr	Reverse recovery time	I _S =1A, di/dt=100 A/μs	49			ns
Q _{rr}	Reverse recovery charge		61.8			nc
I _{rrm}	Peak reverse recovery current		2.4			A

Note :

- 1、 Calculated continuous current based on maximum allowable junction temperature.
- 2、 Repetitive rating; pulse width limited by max. junction temperature.
- 3、 Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4、 The value of R_{θja} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
- 5、 V_{DD}=50 V, R_G=25 Ω, L=0.3 mH, starting T_J=25 °C.

Typical Characteristics

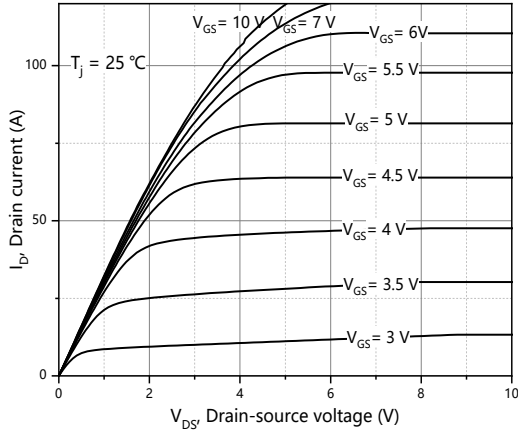


Figure 1, Typ. output characteristics

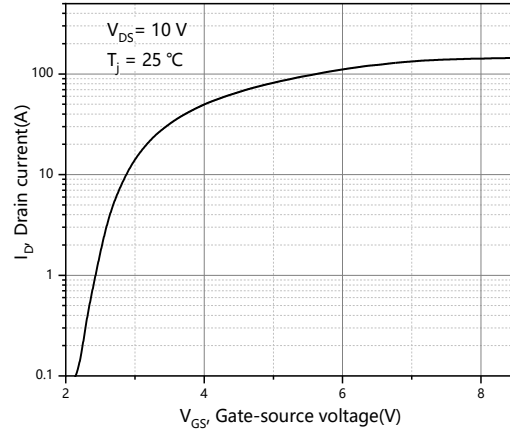


Figure 2, Typ. transfer characteristics

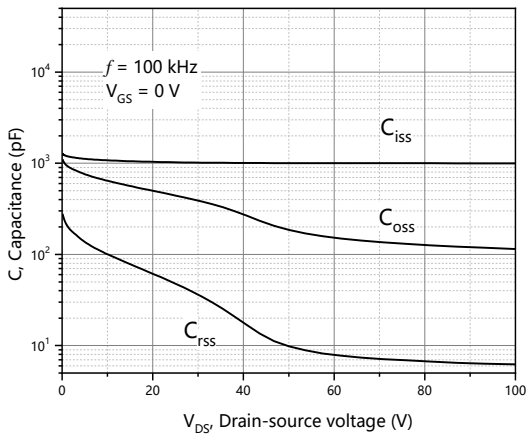


Figure 3, Typ. capacitances

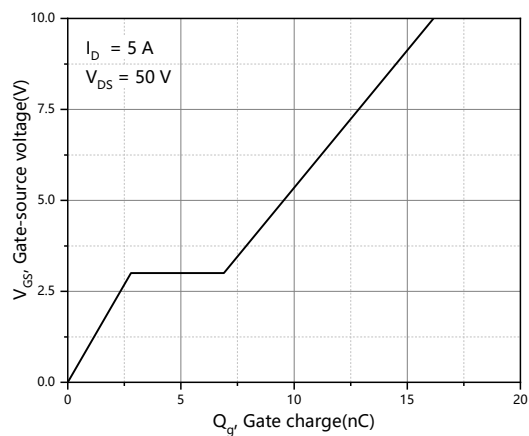


Figure 4, Typ. gate charge

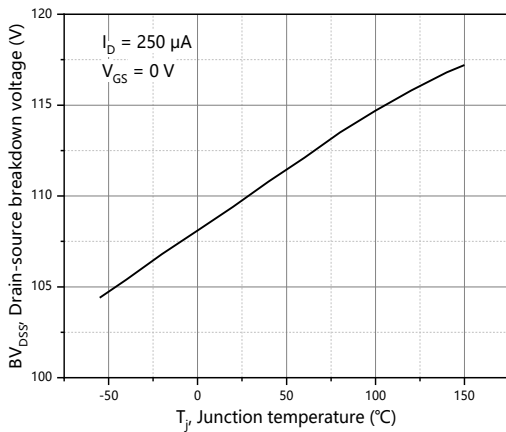


Figure 5, Drain-source breakdown voltage

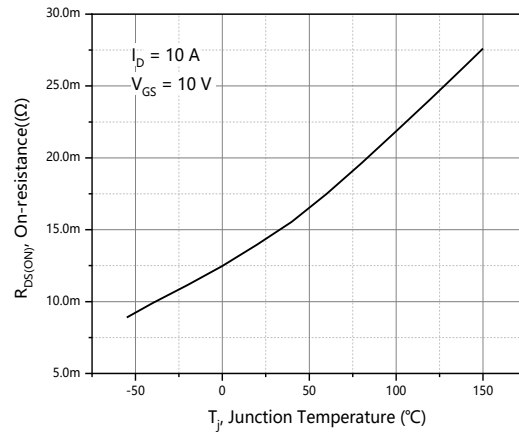


Figure 6, Drain-source on-state resistance

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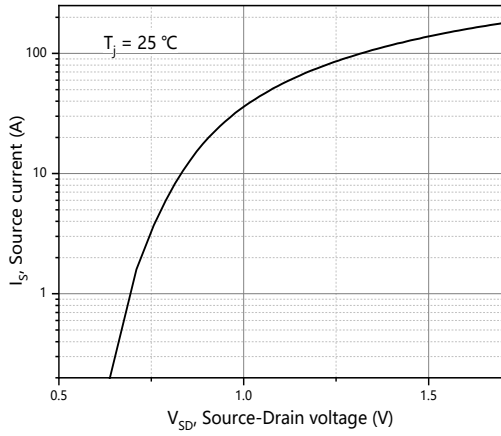


Figure 7, Forward characteristic of body diode

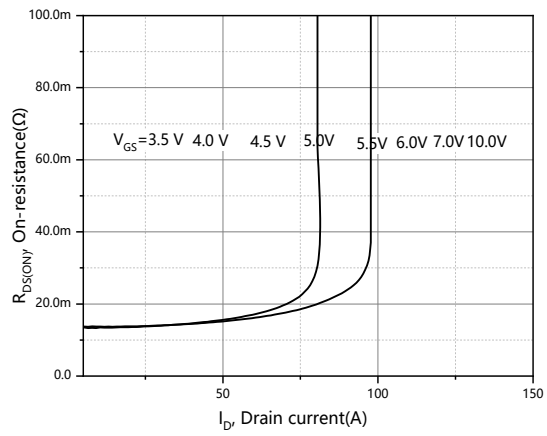


Figure 8, Drain-source on-state resistance

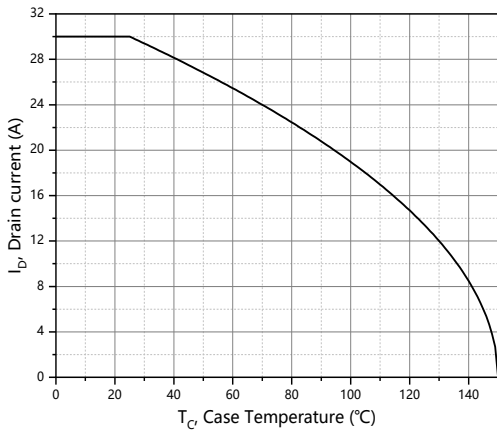


Figure 9, Drain current

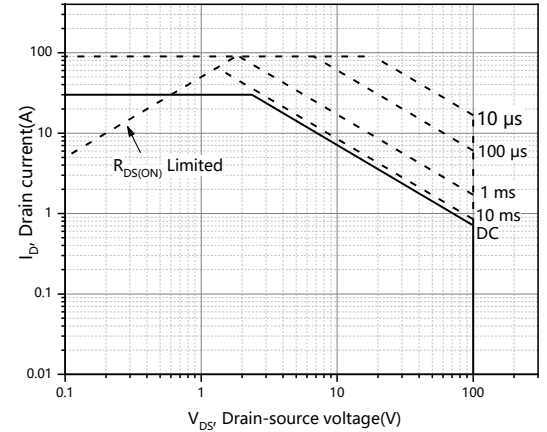


Figure 10, Safe operation area $T_C=25\text{ °C}$

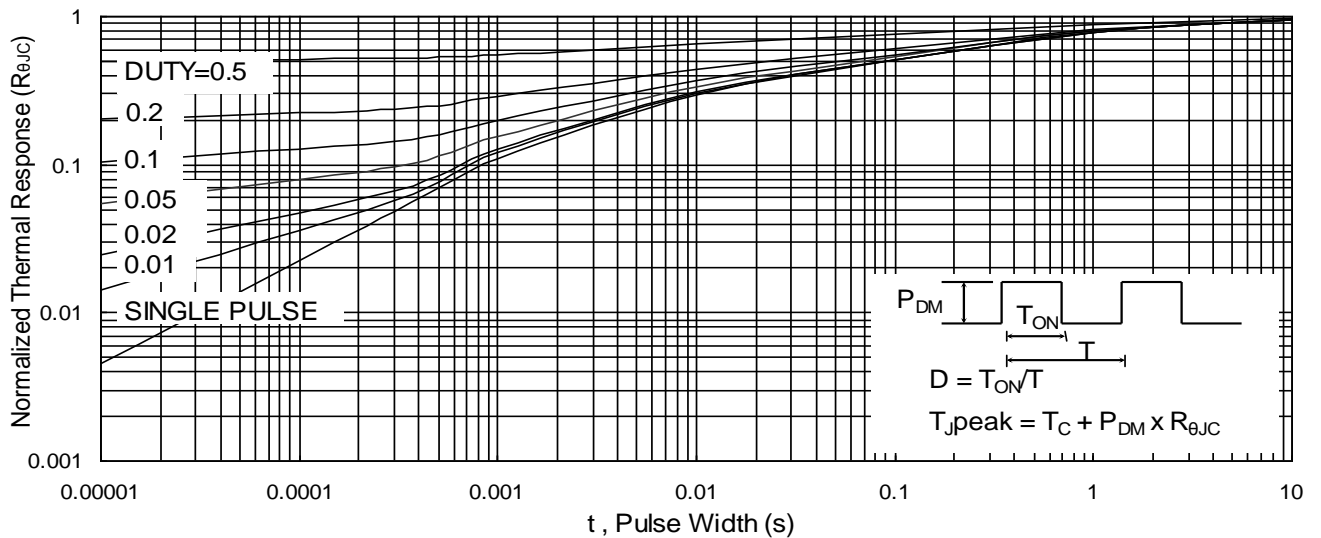
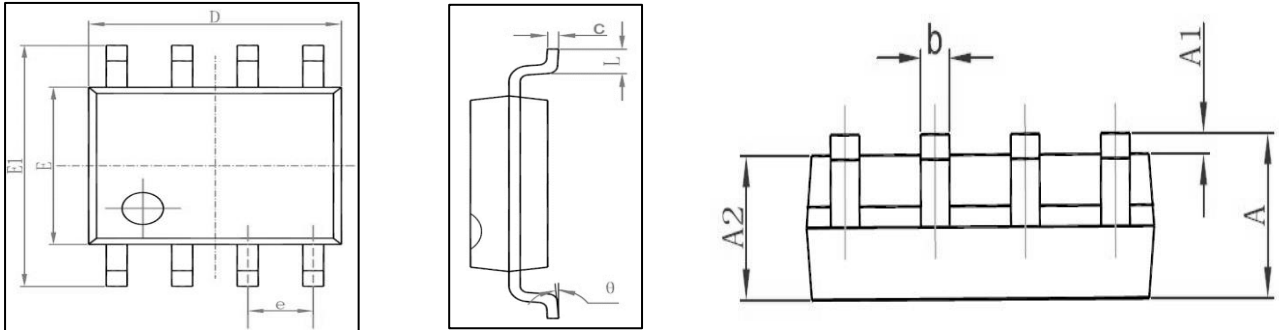
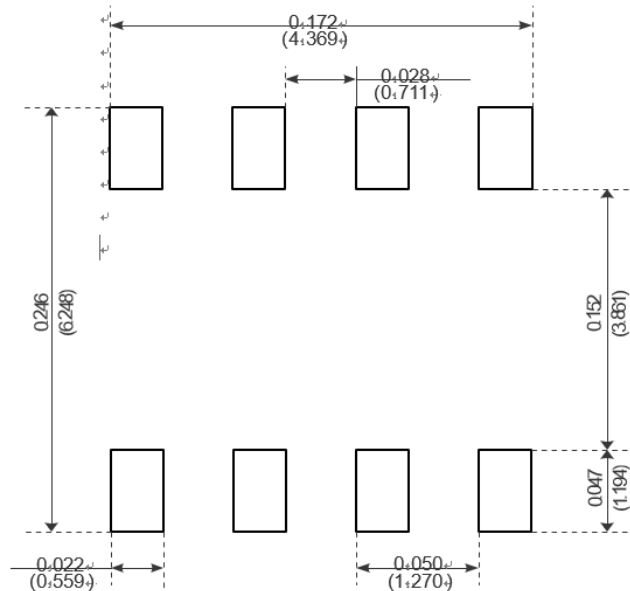


Fig11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOP-8/ESOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

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100V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2018/11/10	Initial release

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