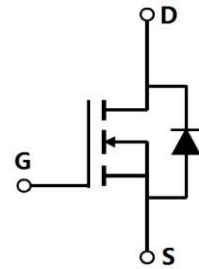


100V N-SGT Enhancement Mode MOSFET

General Description

APG60N10NF use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in



Features

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

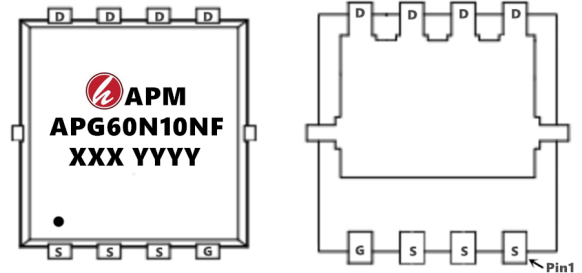
Applications

Consumer electronic power supply

Motor control

Synchronous-rectification

Isolated DC



Synchronous-rectification applications

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG60N10NF	DFN5*6-8	APG60N10NF XXX YYYY	5000

Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_D	60	A
Pulsed drain current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{D, pulse}$	210	A
Power dissipation ³⁾ $T_C=25^{\circ}\text{C}$	P_D	125	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	100	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^{\circ}\text{C}$
Thermal resistance, junction-case	$R_{\theta JC}$	1	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$

100V N-SGT Enhancement Mode MOSFET

Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(on)}$		8.5	10.0	m Ω	$V_{GS}=10\text{ V}, I_D=10\text{ A}$
Drain-source on-state resistance	$R_{DS(on)}$		9.5	12.0	m Ω	$V_{GS}=4.5\text{ V}, I_D=10\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		2604		pF	$V_{GS}=0\text{ V},$ $V_{DS}=50\text{ V}, f=1$ MHz
Output capacitance	C_{oss}		361.2		pF	
Reverse transfer capacitance	C_{rss}		6.5		pF	
Turn-on delay time	$t_{d(on)}$		20.6		ns	$V_{GS}=10\text{ V},$ $V_{DS}=50\text{ V},$ $R_G=2.2\text{ }\Omega,$ $I_D=25\text{ A}$
Rise time	t_r		5		ns	
Turn-off delay time	$t_{d(off)}$		51.8		ns	
Fall time	t_f		9		ns	
Total gate charge	Q_g		49.9		nC	$I_D=25\text{ A},$ $V_{DS}=50\text{ V},$ $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		6.5		nC	
Gate-drain charge	Q_{gd}		12.4		nC	
Gate plateau voltage	$V_{plateau}$		3.4		V	
Diode forward current	I_S			70	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			210		
Diode forward voltage	V_{SD}			1.3	V	$I_S=12\text{ A}, V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		60.4		ns	$I_S=12\text{ A}, di/dt=100$ A/ μs
Reverse recovery charge	Q_{rr}		106.1		nC	
Peak reverse recovery current	I_{rrm}		3		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.
- 5) $V_{DD}=50\text{ V}, R_G=25\text{ }\Omega, L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

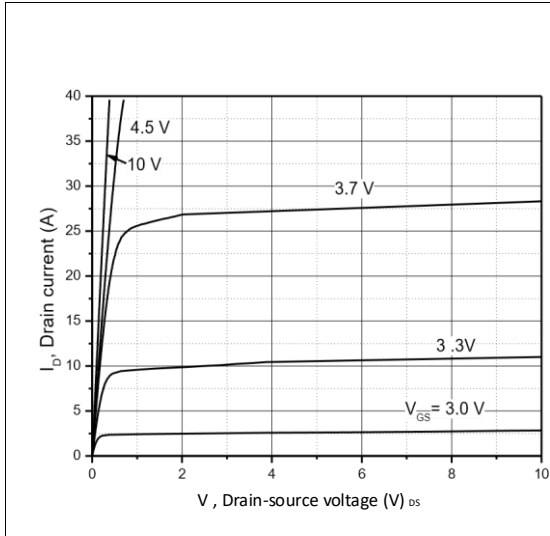


Figure 1, Typ. output characteristics

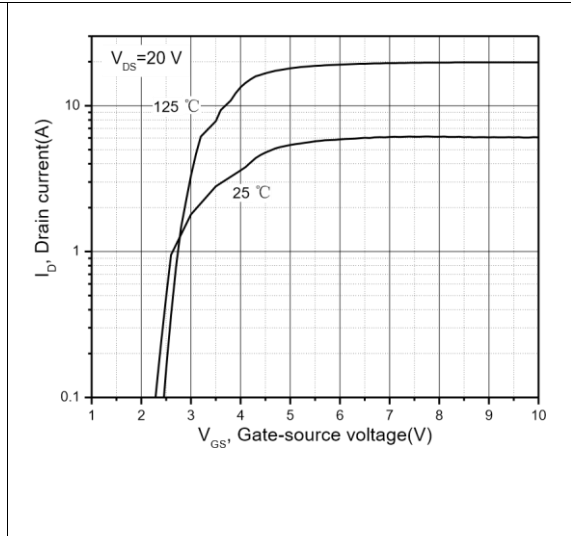


Figure 2, Typ. transfer characteristics

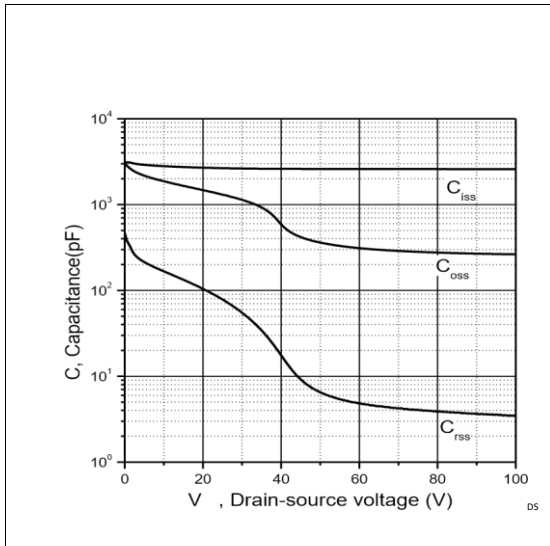


Figure 3, Typ. capacitances

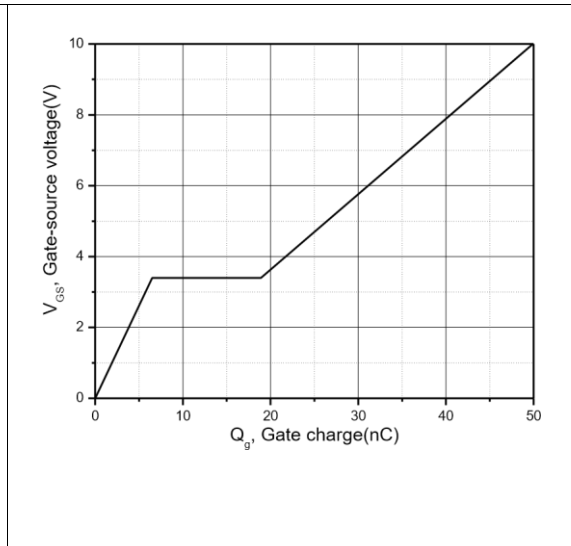


Figure 4, Typ. gate charge

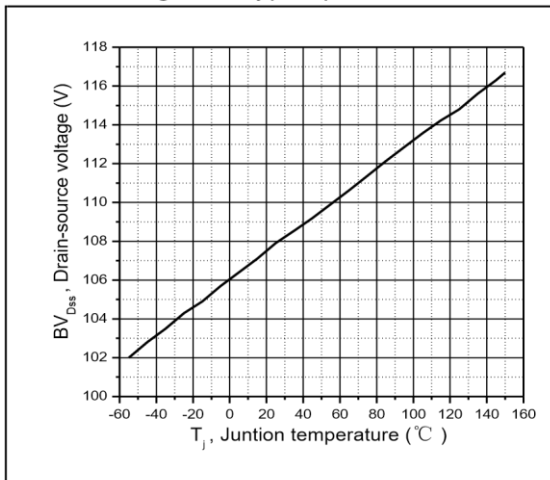


Figure 5, Drain-source breakdown voltage

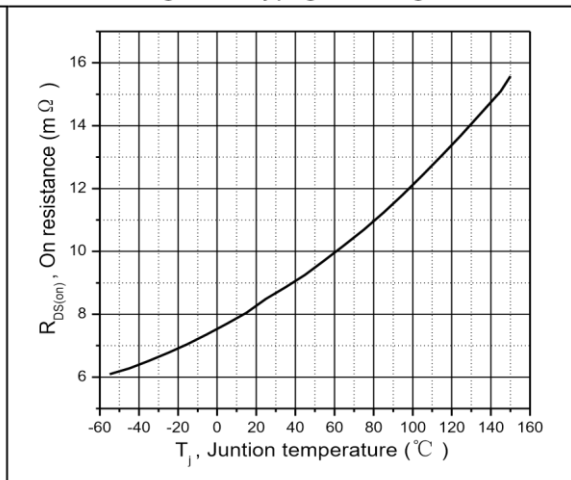


Figure 6, Drain-source on-state resistance



100V N-SGT Enhancement Mode MOSFET

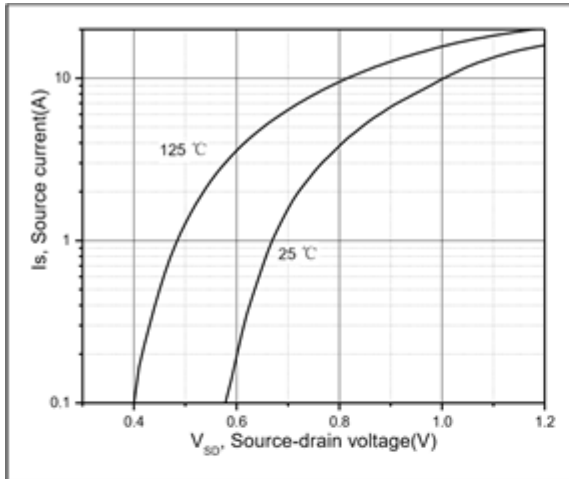


Figure 7, Forward characteristic of body diode

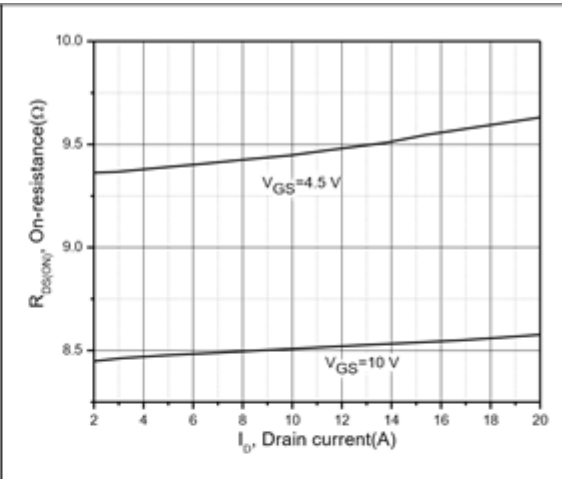
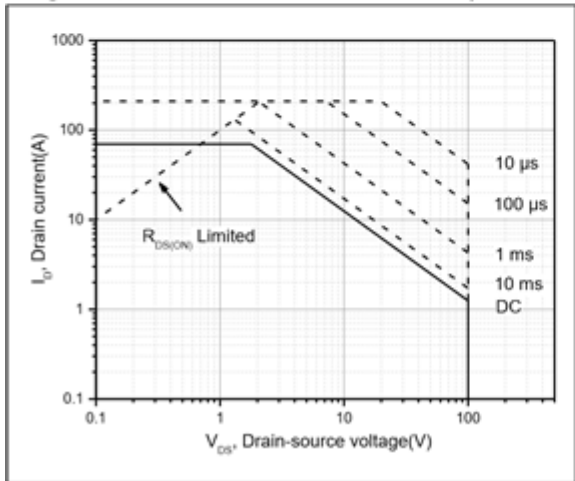


Figure 8, Drain-source on-state resistance



■ Test circuits and waveforms

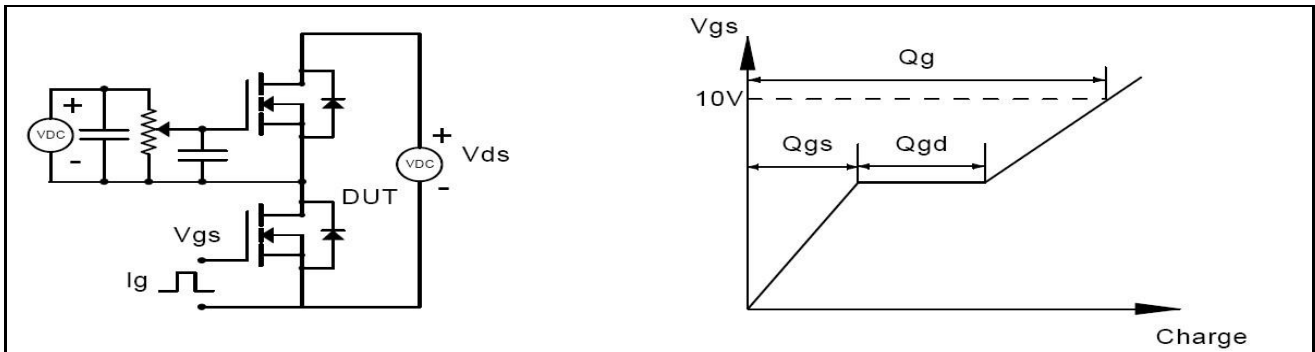


Figure 1, Gate charge test circuit & waveform

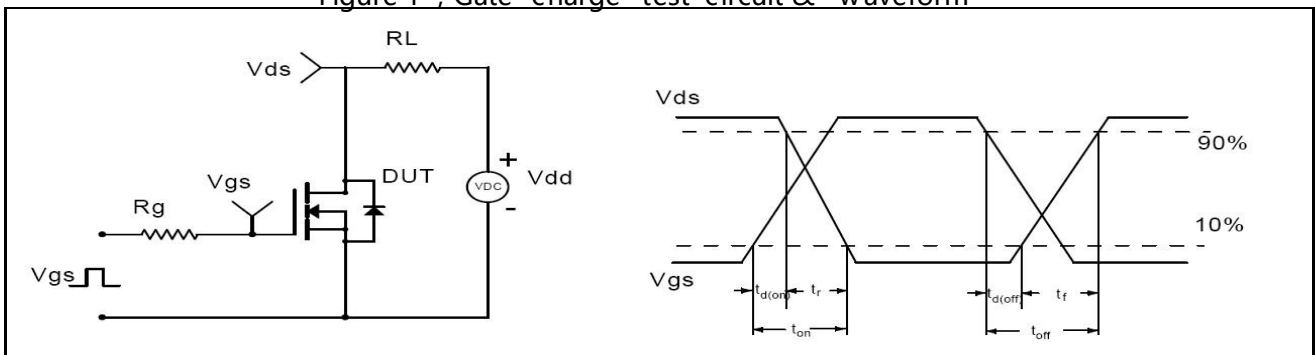


Figure 2, Switching time test circuit & waveforms

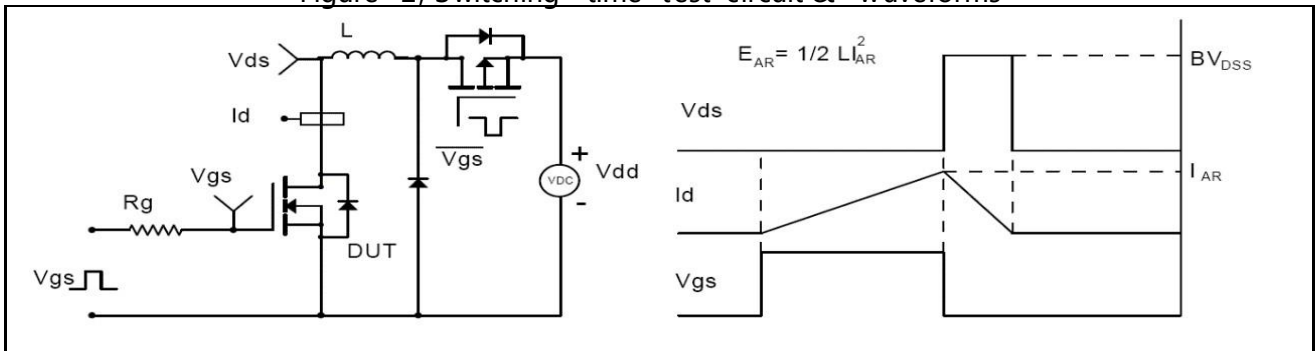


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

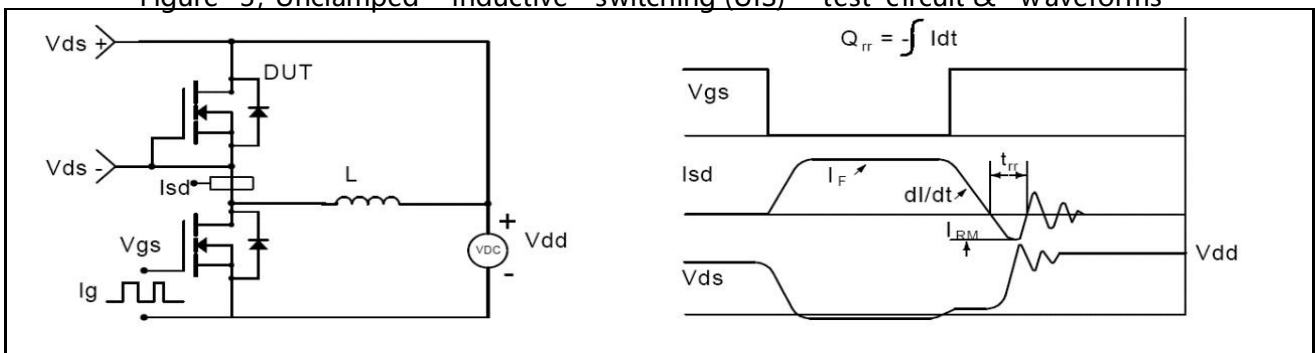
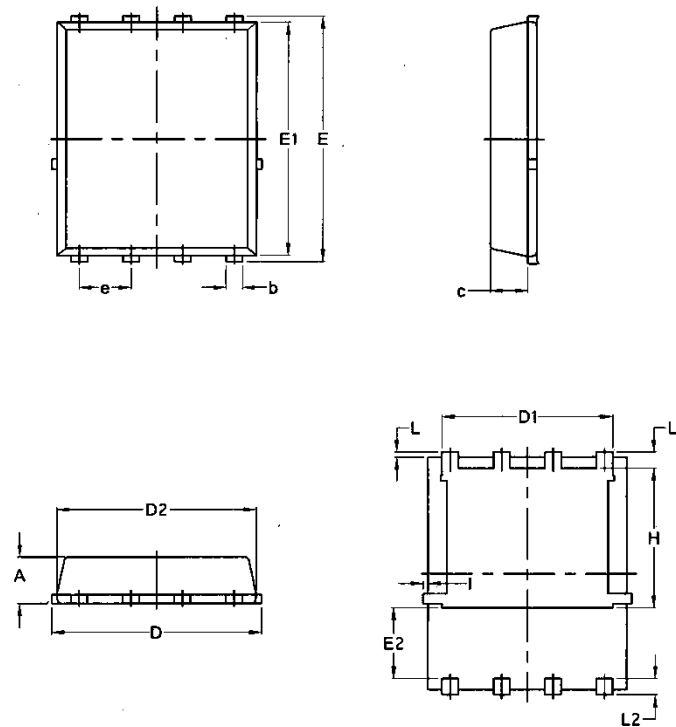


Figure 4, Diode reverse recovery test circuit & waveforms

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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