MLC

SDHC Card 6.1

PHANES-F Series

Document No. : 100-xPSDH-PFCSM

Version No. : 01V0

Date : Feb., 2022

ISO 9001 : 2015 CERTIFIED

Product Features

■ **Flash IC**

- SAMSUNG 14nm NAND Flash IC.

- Multi-Level Cell (MLC) technology

■ **Compatibility**

- Compliant with Part 1 Physical Layer Specification Ver. 6.10

- Compliant with Part 2 File System Specification Ver. 3.00

- Compliant with Part 3 Security Specification Ver. 7.00

- Standard Size SD Card Mechanical Addendum Ver . 7.0

■ **Additional Capabilities**

- S.M.A.R.T.*[1] (Self-Monitoring, Analysis and Reporting Technology) feature set support.

- Supports SD command Class 2/4/6/10

- Supports UHS-1

- Supports SD mode and SPI mode

- Supports CPRM (Content Protection for Recordable Media) of SD Card

- Supports Embedded Mode

- Support bad Block Management

- Support both Static and Dynamic Wear Leveling

■ **Mechanical**

- 9 exposed contact pins on one side.

- Dimension: 32.0mm x 24.0mm x 2.1mm.

- Weight: 2.5 g / 0.09 oz.

■ **Power Operating Voltage 2.7V to 3.6V**

- Power Up Current < 250uA

- Standby Current < 1000uA

- Read Current < 400mA

- Write Current < 400mA

■ **Performance (Maximum value) *[2]**

SDHC card performance

- Sequential Read: 93.0 MB/sec. (max.)

- Sequential Write: 34.0 MB/sec. (max.)

■ **Capacity**

- 8GB

■ **Reliability**

- **TBW:** Up to 23 TBW at 8GB Capacity. (Sequential Write)

- **ECC:** Designed with BCH ECC Algorithm.

- **MTBF:** > 3,000,000 hours

- **Temperature:** (Operating) Standard Grade: -25ºC ~ +85ºC

- **Vibration:** 80Hz~2000Hz/20G.

- **Shock:** 0.5ms, 1500 G, 3 axes.

- **Erase counts:** 3K

■ **Certifications and Declarations**

- **Certifications**: CE & FCC

- **Declarations**: RoHS & REACH

Remarks:

- 1. Support official S.M.A.R.T. Utility.

- 2. Sequential performance is based on CrystalDiskMark 5.1.2 with file size 1000MB

Order Information

I.   Part Number List

◆ **APRO MLC Secure Digital Memory Card PHANES-F Series**

Product Picture	Grade	Std. Temp Grade (-25ºC ~ +85ºC)
	8GB	SPSDH008G-PFCSM

II. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9—X11 X12 X13 X14 X15 X16

X1 : **Grade**

S: Standard Temp Grade- operating temp. -25º C ~ +85 º C

X2 : **The material of case**

P : Plastic casing

X3 X4 X5 : **Product category**

SDH : Secure Digital High Capacity (SDHC) memory card

X6 X7 X8 X9 : **Capacity**

  008G: 8GB

X11 : **Controller**

P : PHANES Series

X12 : **Controller version**

A, B, C…..

X13 : **Controller Grade**

C : Standard grade

X14 : **Flash IC**

S : SAMSUNG NAND Flash IC

X15 : **Flash IC grade / Type**

M : 14nm MLC **-**NAND Flash IC

Revision History

Revision	Description	Date
1.0	Initial release	2022/02/25

Contents

APRO

1. Introduction

APRO MLC Secure Digital Memory Card PHANES-F Series is specifically designed to meet the security, performance and environmental requirements of some significant applications such like networking, telecommunications and data-communications, mobile & embedded computing, medical instruments and industrial computing applications.

The main used Flash memory is MLC-NAND Type Flash memory chips is 8GB. APRO MLC Secure Digital Memory Cards include a copyright protection that complies with the security of the SDMI standard, and the physical form-factor, pin assignment.

1.1. Scope

This document describes the key features and specifications of APRO MLC Secure Digital Memory Cards.

1.2. Flash Management Technology – Static & Dynamic Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO MLC Secure Digital Memory Card PHANES-F Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3. Bad Block Management

➢ **Early Bad Block**

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

➢ **Later Bad Block**

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Latter Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO MLC Secure Digital Memory Card PHANES-F Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

1.4. Embedded Mode

Embedded mode is a function specially designed for operating systems that do not utilize FAT. Often under non Windows OS, for example Linux or customized host, wear leveling mechanism of APRO MLC SD cards will be affected or even disabled in some cases. With embedded mode activated, MLC SD cards ensure that under any circumstances, wear leveling mechanism can operate normally to keep the usage of blocks even throughout the SD card's life cycle. This is especially a great add-on for security cameras or drive recorders.

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2.   Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO Secure Digital Memory Card PHANES-F Series		SPSDH008G-PFCSM
Temperature	**Operating:**	-25ºC ~ +85ºC
	Non-operating:	-40ºC ~ +85ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing
Vibration	**Operating & Non-operating:**	80Hz~2000Hz/20G.
Shock	**Operating & Non-operating:**	0.5ms, 1500 G, 3 axes

2.2. System Power Requirements

Table 2: Power Requirement

APRO Secure Digital Memory Card PHANES-F Series		SPSDH008G-PFCSM
DC Input Voltage (VCC)		**2.7V to 3.6V**
Maximum average value	**Reading Mode :**	< 400 mA (max.)
	Writing Mode :	< 400 mA (max.)
	Standby Mode :	< 1000 uA (max.)

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting		SDA Specification Ver 3.0		
Capacity level		SDHC		
Speed level		UHS-1 (Grade-1)	UHS-1 (Grade-3)	
Maximum Performance	**Capacity**	**8GB**	**16GB**	**32GB**
	Sequential Read (MB/s)	93.0	N/A	N/A
	Sequential Write (MB/s)	34.0	N/A	N/A

Note:

➢ *All values quoted are typically at 25℃ and nominal supply voltage.*

➢ *Sequential performance is based on CrystalDiskMark 5.1.2 with file size 1000MB*

2.4. *System Reliability*

Table 4: System Reliability

Wear-leveling Algorithms		Static and Dynamic wear-leveling algorithms
Bad Block Management		Supportive
ECC Technology		BCH ECC
Erase counts		NAND MLC Flash Cell Level : 3K P/E Cycles
TBW (Tera Bytes Written)		
Capacity	8GB	23.0

Note:

➢ *Test by sequential write.*

➢ *The endurance of SD could be estimated based on users' behaviors, NAND endurance cycles, and write amplification factor.*

 It is not guaranteed by the flash vendor.

➢ *TBW may vary from flash configuration, customer patterns and platform.*

2.5. *System Reliability*

Table 4: System Reliability

Wear-leveling Algorithms	Static and Dynamic wear-leveling algorithms
Bad Blocks Management	Supportive
ECC Technology	BCH ECC
MTBF	> 3,000,000 hours
Endurance	NAND MLC Flash w/MLC Technology : 3K Erase counts
Durability	10,000 inserting cycles
Bending	>10N
Torque	0.1N +/- 2.5 deg.
Drop Test	1.5M free fall
Salt Spray	Concentration: 3% NaCl/35℃
Waterproof	1000mm submerge for 30 minutes.
Electrostatic Discharge (ESD)	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times
X-Ray Exposure Test	0.1 Gy of medium energy radiation (70 keV to 140keV, cumulative does per year) to both sides of the card.

Note:

➢ *The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.*

 It is not guaranteed by flash vendor.

2.6. *Physical Specifications*

Refer to Table 5 and see Figure 1 for APRO MLC Secure Digital Memory Card PHANES-F Series physical specifications and dimensions.

Table 5: Physical Specifications of APRO MLC Secure Digital Memory Card PHANES-F Series

Length:	32.00 mm
Width:	24.00 mm
Thickness:	2.10 mm
Weight:	2.5 g / 0.09 oz.

Figure 2: APRO MLC Secure Digital Memory Card PHANES-F Series Dimension
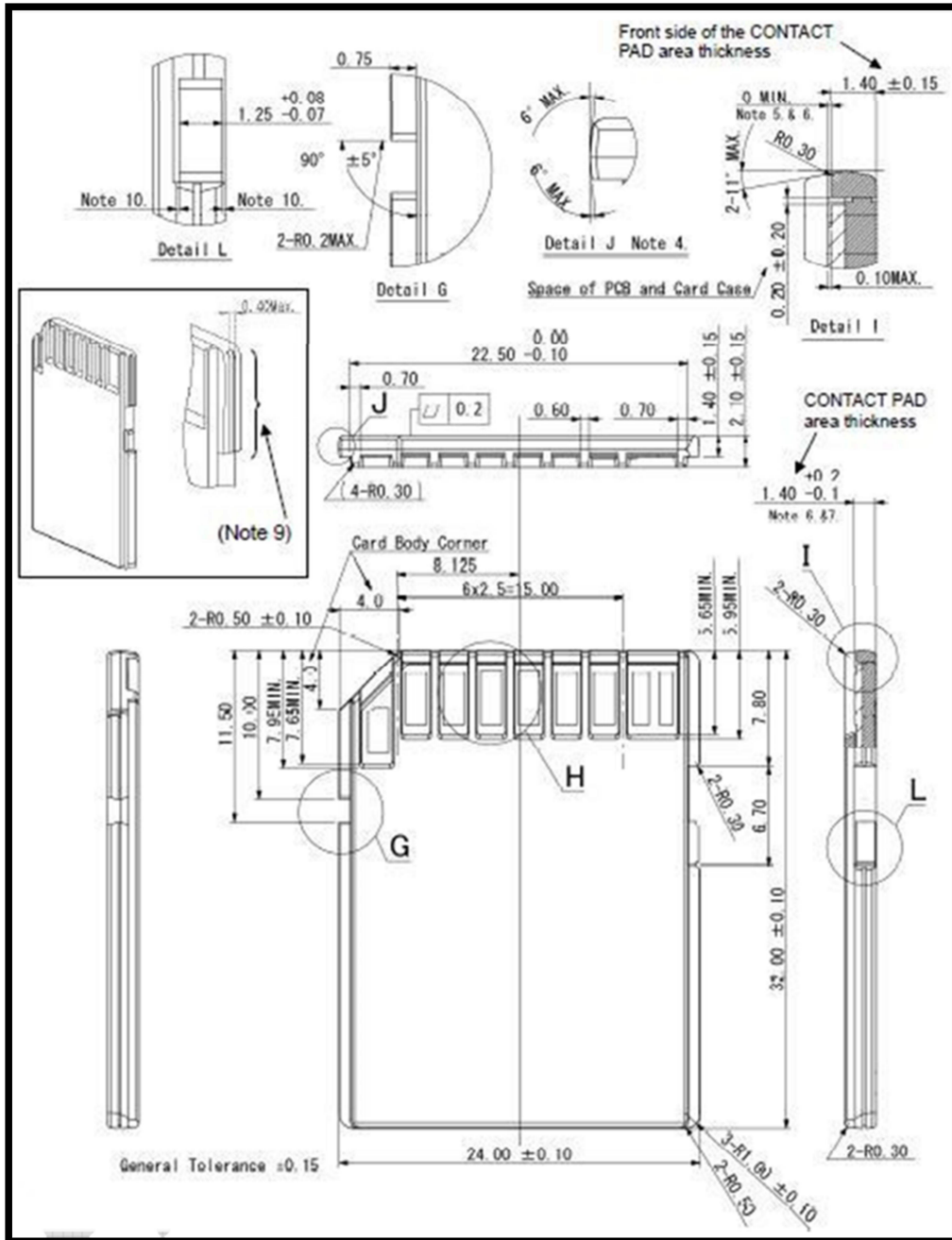
3. Interface Description

3.1. Secure Digital Memory Card interface

APRO MLC Secure Digital Memory Card has 9 exposed contacts on one side.
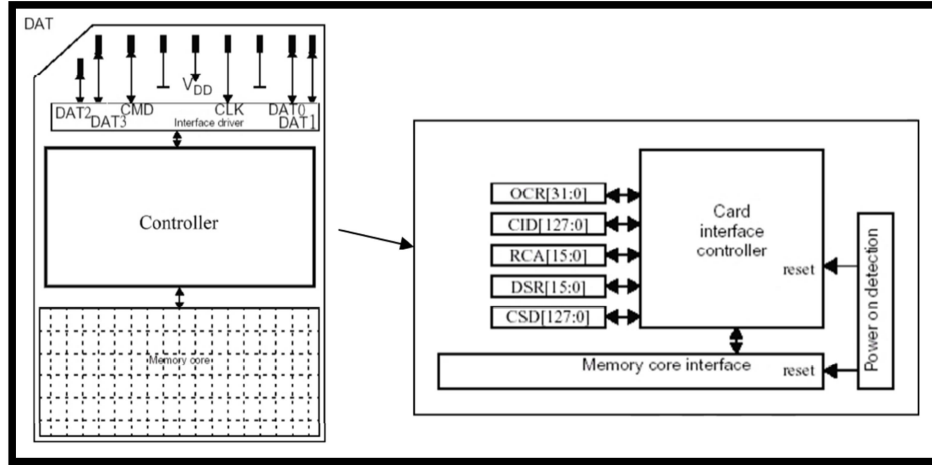

Figure 3: 9 Pins Connector

3.2. Pin Assignments

There are total of 9 pins in the SD Card Connector. The pin assignments are listed in below table 6.

Table 6 - Pin Assignments

Pin Number	SD Mode			SPI Mode		
	Pin Name	Type [1]	Description	Pin Name	Type	Description
Pin 1	CD / DAT3[2]	I/O/PP[3]	Card Detect / Data Line [bit3]	CS	I[3]	Chip Select
Pin 2	CMD	PP	Command / Response	DI	I	Data in
Pin 3	V_{SS1}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
Pin 4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
Pin 5	CLK	I	Clock	SCLK	I	Clock
Pin 6	V_{SS2}	S	Supply voltage ground	V_{SS2}	S	Supply voltage ground
Pin 7	DAT0	I/O/PP	Data Line [bit0]	DO	O/PP	Data Out
Pin 8	DAT1	I/O/PP	Data Line [bit1]	RSV		
Pin 9	DAT2	I/O/PP	Data Line [bit2]	RSV		

➢ S: power supply, I:input; O:output using push-pull drivers; PP:I/O using push-pull drivers.

➢ The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to Multi-Media Cards.

➢ At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, withSET_CLR_CARD_DETECT(ACMD42) command.

Appendix A: Limited Warranty

APRO warrants your MLC Secure Digital Memory Card PHANES-F Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **MLC (Standard grade / Wide temp. grade)   2 years / Within 3K Erasing Counts**

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