AK4332

Low-Power Advanced 32-bit Mono DAC with HP

1. General Description

The AK4332 is an advanced 32-bit high sound quality mono audio DAC with a built-in ground-referenced headphone amplifier. It has four types of 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range and operating ultra low power consumption. The AK4332 accepts PCM Data, PDM Data and DSD Data. It is available in a 30-pin CSP package, utilizing less board space than competitive offerings.

2. Features

1. High Sound Quality Low Power Advanced 32-bit Mono DAC
- **4 types of Digital Filter for Sound Color Selection in PCM Mode**
  - **Short Delay Sharp Roll-off, GD = 5.5 / fs**
  - **Short Delay Slow Roll-off, GD = 4.5 / fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**

2. Ground-referenced Class-G Stereo Headphone Amplifier
- **Output Power: 88 mW @ 8Ω**
- **THD+N: –101 dB**
- **S/N: 109 dB**
- **Output Noise Level: –114 dBV (Analog Volume = –10 dB)**
- **Analog Volume: +4 to –10 dB, 2 dB Step**
- **Ground Loop Noise Cancellation**

3. Low Power Consumption:2.8 mW

4. Digital Audio interface
- **PCM Interface Format: 32/24/16-bit I^2S/MSB justified**
  Master / Slave Mode
  Sampling Frequency:
  8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k, 192 kHz
- **PDM 1-bit Input Support**
- **DSD64 Input Support**

5. Power Management

6. PLL

7. µP Interface: I^2C-bus (400 kHz)

8. Operation Temperature Range: Ta = –40 to +85 °C

9. Power Supply:
- **AVDD (DAC, PLL): 1.7 to 1.9 V**
- **CVDD (Headphone Amplifier, Charge Pump): 1.7 to 1.9 V**
- **LVDD (Digital Interface & LDO2 for Digital Core): 1.7 to 1.9 V (built-in LDO)**

10. Pacage: 30-pin CSP (2.371 mm × 1.971 mm, 0.4 mm pitch)

3. Table of Contents

4. Block Diagram and Functions

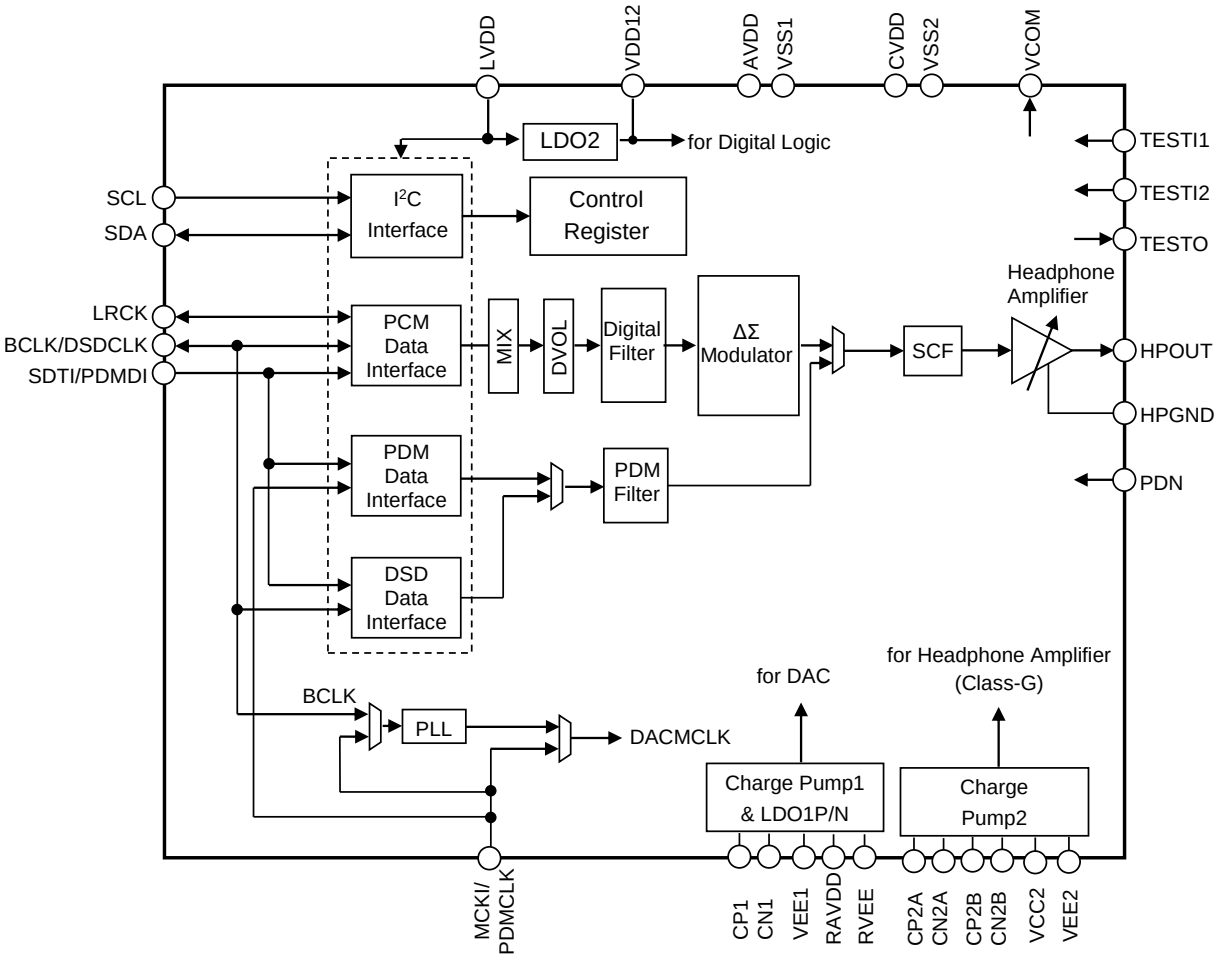
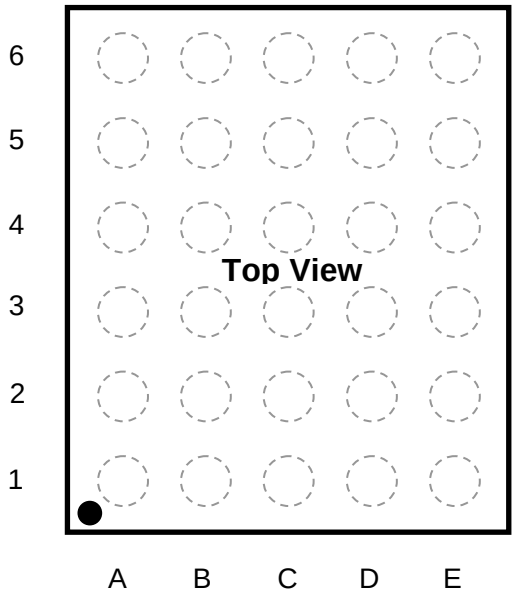


Figure 1. AK4332 Block Diagram

5. Pin Configurations and Functions

5-1. Pin Configurations

30-pin CSP



6	VDD12	CN1	CP1	CVDD	CN2B
5	VSS2	VEE1	BCLK/ DSDCLK	CP2B	CN2A
4	LVDD	LRCK	TESTI1	CP2A	VEE2
3	MCKI/ PDMCLK	SDA	TESTI2	VCC2	HPOUT
2	SDTI/ PDMDI	SCL	PDN	VSS1	HPGND
1	TESTO	RVEE	RAVDD	AVDD	VCOM
	A	**B**	**C**	**D**	**E**

Top View

5-2. Pin Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Power Supply					
D1	AVDD	-	Analog Power Supply Pin	-	AVDD
D2	VSS1	-	Ground1 Pin	-	-
D6	CVDD	-	Headphone Amplifier / Charge Pump Power Supply Pin	-	CVDD
A5	VSS2	-	Ground2 Pin	-	-
A4	LVDD	-	Digital Interface & LDO2 Power Supply Pin	-	LVDD
E1	VCOM	O	Common Voltage Output Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS1 pin. (Note 2)	AVDD/ VSS1	-
A6	VDD12	-	LDO2 (1.2 V) Output Power Supply Pin (Note 1) Connect a capacitor between this pin and the VSS2 pin. (Note 2)	LVDD/ VSS2	LVDD

Note 1. Capacitor value connected to the VDD12 pin should be selected from 2.2 µF ±50% to 4.7µF ±50%.

Note 2. Do not connect a load to the VCOM pin and the VDD12 pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Charge Pump & LDO					
D3	VCC2	O	Charge Pump Circuit Positive Voltage (CVDD or 1/2 × CVDD) Output Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS2 pin. (Note 3)	CVDD/ VSS2	CVDD
D4	CP2A	O	Positive Charge Pump Capacitor Terminal 2A Pin Connect a 2.2 µF ±50% capacitor between this pin and the CN2A pin.	CVDD/ VSS2	CVDD
E5	CN2A	I	Negative Charge Pump Capacitor Terminal 2A Pin Connect a 2.2 µF ±50% capacitor between this pin and the CP2A pin.	CVDD	CVDD
D5	CP2B	O	Positive Charge Pump Capacitor Terminal 2B Pin Connect a 2.2 µF ±50% capacitor between this pin and the CN2B pin.	CVDD/ VSS2	CVDD
E6	CN2B	I	Negative Charge Pump Capacitor Terminal 2B Pin Connect a 2.2 µF ±50% capacitor between this pin and the CP2B pin.	CVDD	CVDD
E4	VEE2	O	Charge Pump Circuit Negative Voltage (–CVDD or –1/2 × CVDD) Output 2 Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS2 pin. (Note 3)	CVDD/ VSS2	-
C6	CP1	O	Positive Charge Pump Capacitor Terminal 1 Pin Connect a 2.2 µF ±50% capacitor between this pin and the CN1 pin.	CVDD/ VSS2	CVDD
B6	CN1	I	Negative Charge Pump Capacitor Terminal 1 Pin Connect a 2.2 µF ±50% capacitor between this pin and the CP1 pin.	CVDD	CVDD
B5	VEE1	O	Charge Pump Circuit Negative Voltage (–CVDD) Output 1 Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS2 pin. (Note 3)	CVDD/ VSS2	-
C1	RAVDD	O	LDO1P (1.5 V) Output Pin (Note 3) Connect capacitor between this pin and the VSS1 pin. (Note 4)	AVDD/ VSS1	-
B1	RVEE	O	LDO1N (–1.5 V) Output Pin (Note 3) Connect capacitor between this pin and the VSS1 pin. (Note 4)	AVDD/ VSS1	-

Note 3. Do not connect a load to the VEE1 pin, VCC2 pin, VEE2 pin, RAVDD pin and the RVEE pin.
Note 4. Capacitor value connected to the RAVDD pin and the RVEE pin should be selected from 1.0 µF ±50% to 4.7 µF ±50%.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Control Interface					
B2	SCL	I	I^2C Serial Data Clock Pin	LVDD/ VSS2	LVDD
B3	SDA	I/O	I^2C Serial Data Input/Output Pin	LVDD/ VSS2	LVDD
Audio Interface					
A3	MCKI	I	External Master Clock Input Pin in PCM Mode (PDM bit = "0")	LVDD/ VSS2	LVDD
	PDMCLK	I	PDM Clock Pin in PDM Mode (PDM bit = "1" & PDMMODE bit = "0")		
C5	BCLK	I/O	Audio Serial Data Clock Pin in PCM Mode (PDM bit = "0")	LVDD/ VSS2	LVDD
	DSDCLK	I	DSD Clock Pin in DSD Mode (PDM bit = "1" & PDMMODE bit = "1")		
B4	LRCK	I/O	Frame Sync Clock Pin in PCM Mode	LVDD/ VSS2	LVDD
A2	SDTI	I	Audio Serial Data Input Pin in PCM Mode (PDM bit = "0")	LVDD/ VSS2	LVDD
	PDMDI	I	PDM Data Input Pin in PDM Mode and DSD Mode (PDM bit = "1")		
Analog Output					
E3	HPOUT	O	Headphone Amplifier Output Pin	CVDD/ VEE2	CVDD/ VEE2
E2	HPGND	I	Headphone Amplifier Ground Loop Noise Cancellation Pin	CVDD	-
Others					
C2	PDN	I	Power down Pin "L": Power-down, "H": Power-Up	LVDD/ VSS2	LVDD
C4	TESTI1	I	TEST Input 1 Pin It must be tied "L".	LVDD VSS2	LVDD
C3	TESTI2	I	TEST Input 2 Pin It must be tied "L".	LVDD/ VSS2	LVDD
A1	TESTO	O	TEST Output Pin	AVDD/ VSS1	AVDD

Note 5. The SCL pin, SDA pin, MCKI/PDMCLK pin, BCLK/DSDCLK pin, LRCK pin, SDTI/PDMDI pin, HPGND pin, PDN pin, TESTI1 pin, and the TESTI2 pin must not be allowed to float.

5-3. Handing of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Digital	MCKI/PDMCLK, BICK/DSDCLK, LRCK, TESTI1, TESTI2	Connect to VSS2
	TESTO	Open

6. Absolute Maximum Ratings

(VSS1 = VSS2 = 0 V; Note 6, Note 8)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies: (Note 7)	Analog	AVDD	–0.3	4.3	V
	Headphone Amplifier /Charge Pump	CVDD	–0.3	4.3	V
	Digital Interface & LDO2 for Digital Core	LVDD	–0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 9)		VIND	–0.3	LVDD+0.3 or 4.3	V
Ambient Temperature (powered applied)		Ta	–40	+85	°C
Storage Temperature		Tstg	–65	+150	°C

Note 6. All voltages with respect to ground.

Note 7. Charge pump 1 & 2 are not in operation. In the case that charge pump 1 & 2 are in operation, the maximum values of AVDD and CVDD become 2.15 V.

Note 8. VSS1 and VSS2 must be connected to the same analog plane.

Note 9. MCKI/PDMCLK, BCLK/DSDCLK, LRCK/FRCK, SDTI/PDMDI, SCL, SDA, PDN, TESTI1, TESTI2 pins
The maximum value of input voltage is lower value between (LVDD+0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal Operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = 0 V; Note 10)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies: (Note 11)	Analog	AVDD	1.7	1.8	1.9	V
	Headphone Amplifier / Charge Pump	CVDD	1.7	1.8	1.9	V
	Digital Interface & LDO2 for Digital Core	LVDD	1.7	1.8	1.9	V

Note 10. All voltages with respect to ground.

Note 11. Each power up/down sequence is shown below.

<Power-Up>

1. PDN pin = “L”
2. LVDD, AVDD and CVDD are powered up.
3. (AVDD must be powered up before or at the same time of CVDD. The power-up sequence of LVDD is not critical.)
4. The PDN pin is allowed to be “H” after all power supplies are applied and settled.

<Power-down>

1. PDN pin = “L”
2. AVDD, CVDD and LVDD are powered down.
   (CVDD must be powered down before or at the same time of AVDD. The power-down sequence of LVDD is not critical.)

8. Electrical Characteristics

8-1. DAC Analog Characteristics (PCM Mode)

(Ta = +25°C; AVDD = CVDD = LVDD = 1.8 V; VSS1 = VSS2 = HPGND = 0 V; Signal Frequency = 1 kHz; 24-bit Data; fs = 48 kHz, BCLK = 64fs; Measurement Bandwidth = 20 Hz to 20 kHz, OVC = 0 dB, R_L = 32Ω; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
DAC Characteristics:					
Resolution		-	-	32	Bits
Headphone-Amp Characteristics: DAC (Mono) → HPOUT pins					
Output Power					
0 dBFS, R_L = 32Ω, HPG = 0 dB		-	24	-	mW
R_L = 16Ω, HPG = +2 dB, THD+N < –60 dB		-	50	-	mW
R_L = 8Ω, HPG = +2 dB, THD+N < –20 dB		-	88	-	mW
Output Level (0 dBFS, R_L = 32Ω, HPG = –4 dB) (Note 12)		0.51	0.55	0.60	Vrms
THD+N					
0 dBFS, R_L = 32Ω, HPG = 0 dB	fs = 48 kHz BW = 20 kHz	-	–101	-	dB
0 dBFS, R_L = 32Ω, HPG = –4 dB	fs = 48 kHz BW = 20 kHz	-	–100	–90	dB
	fs = 96 kHz BW = 40 kHz	-	–97	-	dB
	fs = 192 kHz BW = 40 kHz	-	–97	-	dB
–60 dBFS, R_L = 32Ω, HPG = –4 dB	fs = 48 kHz BW = 20 kHz	-	–44	-	dB
	fs = 96 kHz BW = 40 kHz	-	–40	-	dB
	fs = 192 kHz BW = 40 kHz	-	–40	-	dB

Note 12. Output level is proportional to AVDD. Typ. 0.55 Vrms × AVDD / 1.8 V @headphone amplifier gain = –4 dB.

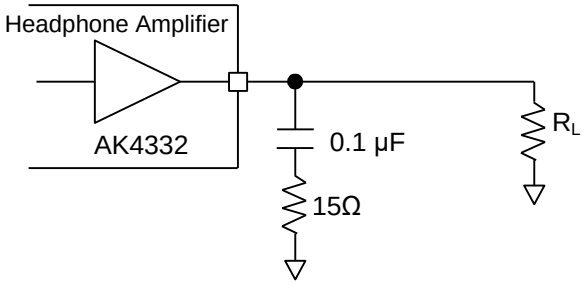


Figure 2. External Circuit for Headphone Amplifier

Parameter		Min.	Typ.	Max.	Unit
Dynamic Range (–60 dBFS, A-weighted, HPG = –4 dB)		-	107	-	dB
S/N (A-weighted) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS/ “0” Data) Po = 10 mW, HPG = –4 dB (Data = 0 dBFS/ “0” Data)		 - 99	 109 107	 - -	 dB dB
Output Noise Level (A-weighted, HPG = –10 dB)		-	–114	–106	dBV
Load Resistance		7.2	32	-	Ω
Load Capacitance		-	-	500	pF
Load Inductance		-	-	0.375	µH
PSRR (HPG = –4 dB) (Note 13) 217 Hz 1 kHz		 - -	 85 85	 - -	 dB dB
DC-offset (Note 14) HPG = 0 dB HPG = All gain		 –0.15 –0.2	 0 0	 +0.15 +0.2	 mV mV
Headphone Output Volume Characteristics:					
Gain Setting		–10	-	+4	dB
Step Width	Gain: +4 to –10 dB	1	2	3	dB

Note 13. PSRR is applied to all power supplies with 100 mVpp sine wave.
Note 14. When there is no gain change and temperature drift after headphone amplifier is powered up.

8-2. DAC Analog Characteristics（PDM 1-bit / DSD Mode)

(Ta = +25°C; AVDD = CVDD = LVDD = 1.8 V; VSS1 = VSS2 = HPGND = 0 V; Signal Frequency = 1 kHz; Input Signal Level = 0.5 × 0dBFS = 0dBr; Measurement bandwidth = 20 Hz to 20 kHz; R_L = 32Ω; unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics (Note 15)						
Patameter						
THD+N (HPG = –4 dB)		0dBr Input (Note 16)	-	–98	-	dB
S/N (A-weighted)	HPG = –4 dB	Digital “0” (Note 17)	-	104	-	dB
	HPG = +4 dB		-	107	-	dB
Output Level	HPG = +4dB	0dBr Input (Note 16)	-	1.01	-	Vrms
	HPG = 0 dB		-	0.64	-	Vrms
	HPG = –4 dB		-	0.40	-	Vrms

Note 15. Input signal should be in a range of 25 % to 75 % duty.

Note 16. This spec is defined in case that the signal source is a sine wave with 75 % duty for positive peak level and 25 % duty for negative peak level.

Note 17. Digital “0” is a digital zero code pattern (“01101001”).

8-3. PLL Characteristice

(Ta=−40 to +85°C; AVDD = CVDD = LVDD = 1.7V to 1.9V, VSS1 = VSS2 = HPGND = 0V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
PLL Characteristics				
Reference Clock (Figure 16)	76.8	-	768	kHz
PLLCLK Frequency (Figure 16)				
44.1 kHz × 256fs × 2	-	22.5792	-	MHz
48.0 kHz × 256fs × 2	-	24.576	-	MHz
Lock Time	-	-	2	msec

8-4. Charge Pump & LDO Circuit Power-Up Time

(Ta=−40 to +85°C; AVDD = CVDD = LVDD = 1.7V to 1.9V, VSS1 = VSS2 = HPGND = 0V; unless otherwise specified)

Parameter	Capacitor	Min.	Typ.	Max.	Unit
Block Power-Up Time					
CP1 (Note 18)	-	-	-	6.5	msec
CP2 (Class-G) (Note 18, Note 19)	-	-	-	4.5	msec
LDO1P (Note 20)	1 µF @RAVDD	-	-	0.5	msec
LDO1N (Note 20)	1 µF @RVEE	-	-	0.5	msec
LDO2 (Note 18)	-	-	-	1	msec

Note 18. Power-up time is a fixed value that is not affected by a capacitor.

Note 19. Power-up time is a value to −1/2 × CVDD, since CP2 starts with 1/2VDD Mode as part of Class-G operation.

Note 20. Power-up time is proportional to a capacitor value. For instance, if a 2.2 µF capacitor is connected to the RAVDD pin, LDO1P power-up time is 1.1 msec at maximum.

8-5. Power Supply Current

(Ta = +25°C; AVDD = CVDD = LVDD = 1.8 V; VSS1 = VSS2 = HPGND = 0 V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current:				
Power Up (PDN pin = "H", All Circuits Power-Up) (Note 21)				
AVDD + CVDD + LVDD	-	1.9	2.8	mA
Power Down (PDN pin = "L") (Note 22)				
AVDD + CVDD + LVDD	-	0	10	μA

Note 21. fs = 48 kHz, MCKI = 256fs, BCLK = 64fs; No data input, DAC, Headphone Amplifier, PLL Power-Up; PLL Slave Mode, R_L = 32Ω,

Note 22. All Digital input pins are fixed to LVDD or VSS2.

8-6. Current Consumptions for Each Operation Mode

(Ta = +25°C; AVDD = CVDD = LVDD = 1.8 V; VSS1 = VSS2 = HPGND = 0 V;
MCKI = 256fs@fs = 44.1kHz & 96kHz, 128fs@fs=192kHz, BCLK = 64fs, Signal Frequency = 1kHz,
HPG[2:0] bits = "011",CPMODE[1:0] bits = "00", LVDSEL[1:0] bits = "01", External Slave Mode, R_L = 32Ω)

Table 1. Current Consumption (Typ.) for Each Operation Mode

PCM Mode	AVDD [mA]	CVDD [mA]	LVDD [mA]	Total Power [mW]
DAC → HP (fs = 48 kHz), Digital "0" data Input	0.50	0.86	0.21	2.8
DAC → HP (fs = 96 kHz), Digital "0" data Input	0.50	0.86	0.30	3.0
DAC → HP (fs = 192 kHz), Digital "0" data Input	0.50	0.86	0.34	3.1
DAC → HP (fs = 48 kHz), Output Power = 0.1mW	0.50	1.64	0.32	4.4
DAC → HP (fs = 48 kHz), Output Power = 1mW	0.52	3.42	0.32	7.7

PDM 1-bit Mode / DSD Mode	AVDD [mA]	CVDD [mA]	LVDD [mA]	Total Power [mW]
DAC → HP Digital "0" data Input	0.50	0.86	0.17	2.8
DAC → HP Output Power = 0.1mW	0.50	1.59	0.17	4.1
DAC → HP Output Power = 1mW	0.52	3.37	0.17	7.3

8-7. DAC Sharp Roll-Off Filter Characteristics

8-7-1. DAC Sharp Roll-Off Filter (fs = 48 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 48 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 23)	–0.006 dB to +0.230 dB	PB	0	-	22.42	kHz
	–6.0 dB		-	24.02	-	kHz
Stopband (Note 23)		SB	26.2	-	-	kHz
Passband Ripple		PR	–0.006	-	+0.230	dB
Stopband Attenuation (Note 24)		SA	69.8	-	-	dB
Group Delay (Note 25)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 20.0 kHz		FR	–0.12	-	+0.1	dB

Note 23. The passband and stopband frequencies scale with fs (system sampling rate). PB = 0.467 × fs (@–0.006/+0.230 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 24. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 25. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-7-2. DAC Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 26)	–0.003 dB to +0.240 dB	PB	0	-	44.85	kHz
	–6.0 dB		-	48.04	-	kHz
Stopband (Note 26)		SB	52.5	-	-	kHz
Passband Ripple		PR	–0.003	-	+0.240	dB
Stopband Attenuation (Note 27)		SA	69.8	-	-	dB
Group Delay (Note 28)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 40.0 kHz		FR	–1.69	-	+0.11	dB

Note 26. The passband and stopband frequencies scale with fs (system sampling rate). PB = 0.4672 × fs (@–0.003/+0.240 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

Note 27. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 28. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-7-3. DAC Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 29)	–0.002 dB to +0.240 dB	PB	0	-	89.74	kHz
	–6.0 dB		-	96.08	-	kHz
Stopband (Note 29)		SB	104.9	-	-	kHz
Passband Ripple		PR	–0.002	-	+0.240	dB
Stopband Attenuation (Note 30)		SA	69.8	-	-	dB
Group Delay (Note 31)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 80.0 kHz		FR	–8.23	-	+0.35	dB

Note 29. The passband and stopband frequencies scale with fs (system sampling rate). PB = 0.4674 × fs (@–0.002/+0.240 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 30. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 31. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-8. DAC Slow Roll-Off Filter Characteristics

8-8-1. DAC Slow Roll-Off Filter (fs = 48 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 48 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 32)	–0.07 dB to +0.005 dB	PB	0	-	8.49	kHz
	–3.0 dB		-	20.15	-	kHz
Stopband (Note 32)		SB	42.59	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.005	dB
Stopband Attenuation (Note 33)		SA	72.8	-	-	dB
Group Delay (Note 34)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 20.0 kHz		FR	–3.21	-	+0.03	dB

Note 32. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1769 × fs (@–0.07/+0.005 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 33. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 34. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-8-2. DAC Slow Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 35)	–0.07 dB to +0.006 dB	PB	0	-	17.02	kHz
	–3.0 dB		-	40.3	-	kHz
Stopband (Note 35)		SB	85.15	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.006	dB
Stopband Attenuation (Note 36)		SA	72.8	-	-	dB
Group Delay (Note 37)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 40.0 kHz		FR	–4.84	-	+0.1	dB

Note 35. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1773 × fs (@–0.07/+0.006 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 36. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 37. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-8-3. DAC Slow Roll-Off Filter (fs = 192 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 38)	–0.07 dB to +0.006 dB	PB	0	-	34.17	kHz
	–3.0 dB		-	80.65	-	kHz
Stopband (Note 38)		SB	170.3	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.006	dB
Stopband Attenuation (Note 39)		SA	72.8	-	-	dB
Group Delay (Note 40)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 80.0 kHz		FR	–11.38	-	+0.35	dB

Note 38. The passband and stopband frequencies scale with fs (system sampling rate). PB = 0.178 × fs (@–0.07/+0.006 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 39. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 40. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-9. DAC Short Delay Sharp Roll-Off Filter Characteristics

8-9-1. DAC Short Delay Sharp Roll-Off Filter (fs = 48 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 48 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 41)	–0.009 dB to +0.232 dB	PB	0	-	22.41	kHz
	–6.0 dB		-	24.15	-	kHz
Stopband (Note 41)		SB	26.23	-	-	kHz
Passband Ripple		PR	–0.009	-	+0.232	dB
Stopband Attenuation (Note 42)		SA	69.8	-	-	dB
Group Delay (Note 43)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 20.0 kHz		FR	–0.12	-	+0.10	dB

Note 41. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4669 × fs (@–0.009/+0.232 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 42. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 43. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-9-2. DAC Short Delay Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 96 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 44)	–0.004 dB to +0.238 dB	PB	0	-	44.82	kHz
	–6.0 dB		-	48.32	-	kHz
Stopband (Note 44)		SB	52.5	-	-	kHz
Passband Ripple		PR	–0.004	-	+0.238	dB
Stopband Attenuation (Note 45)		SA	69.8	-	-	dB
Group Delay (Note 46)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 40.0 kHz		FR	–1.69	-	+0.11	dB

Note 44. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4669 × fs (@–0.004/+0.238 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 45. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 46. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-9-3. DAC Short Delay Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V;
fs = 192 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 47)	–0.002 dB to +0.247 dB	PB	0	-	89.68	kHz
	–6.0 dB		-	96.64	-	kHz
Stopband (Note 47)		SB	104.9	-	-	kHz
Passband Ripple		PR	–0.002	-	+0.247	dB
Stopband Attenuation (Note 48)		SA	69.8	-	-	dB
Group Delay (Note 49)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 80.0 kHz		FR	–8.23	-	+0.36	dB

Note 47 The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4671 × fs (@–0.002/+0.247 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 48. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 49. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10. DAC Short Delay Slow Roll-Off Filter Characteristics

8-10-1. DAC Short Delay Slow Roll-Off Filter (fs = 48 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 48 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 50)	–0.07 dB to +0.025 dB	PB	0	-	9.82	kHz
	–3.0 dB		-	20.57	-	kHz
Stopband (Note 50)		SB	42.98	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.025	dB
Stopband Attenuation (Note 51)		SA	75.1	-	-	dB
Group Delay (Note 52)		GD	-	4.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 20.0 kHz		FR	–2.96	-	+0.04	dB

Note 50. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2045 × fs (@–0.07/+0.025 dB), SB = 0.8955 × fs. Each frequency response refers to that of 1 kHz.

Note 51. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 52. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10-2. DAC Short Delay Slow Roll-Off Filter (fs = 96 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 96 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 53)	–0.07 dB to +0.027 dB	PB	0	-	19.7	kHz
	–3.0 dB		-	41.16	-	kHz
Stopband (Note 53)		SB	85.97	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.027	dB
Stopband Attenuation (Note 54)		SA	75.1	-	-	dB
Group Delay (Note 55)		GD	-	4.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 40.0 kHz		FR	–4.59	-	+0.10	dB

Note 53. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2052 × fs (@–0.07/+0.027 dB), SB = 0.8955 × fs. Each frequency response refers to that of 1 kHz.

Note 54. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 55. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10-3. DAC Short Delay Slow Roll-Off Filter (fs = 192 kHz)

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; fs = 192 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 56)	–0.07 dB to +0.028 dB	PB	0	-	39.54	kHz
	–3.0 dB		-	82.37	-	kHz
Stopband (Note 56)		SB	172	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.028	dB
Stopband Attenuation (Note 57)		SA	75.1	-	-	dB
Group Delay (Note 58)		GD	-	4.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp):						
Frequency Response: 0 to 80.0 kHz		FR	–11.13	-	+0.35	dB

Note 56. The passband and stopband frequencies scale with fs (system sampling rate) PB = 0.2059 × fs (@–0.07/+0.028 dB), SB = 0.8958 × fs. Each frequency response refers to that of 1 kHz.

Note 57. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 58. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-11. PDM Filter Characteristics

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V;
CM[1:0] bits = “00“, FS[4:0] bits = “01010”, PDM bit = “1”)

PDM 1-bit Mode / DSD Mode					
Parameter		**Min.**	**Typ.**	**Max.**	**Unit**
Digital Filter Response (Note 59)					
20 kHz		-	–0.63	-	dB
40 kHz		-	–2.64	-	dB
80 kHz		-	–14.37	-	dB
Group Delay (Note 60)	GD	-	12.5	-	µsec
Digital Filter + DACANA (Headphone Amplifier):					
20 kHz		-	–0.83	-	dB

Note 59. Input signal should be in a range of 25 % to 75 % duty.

Note 60. The calculated delay time is resulting from PDM Filter. This is the time from the point of data change at the PDMDI pin to the output of an analog signal.
In DSD Mode, this specification is 12.8 µsec.

8-12. DC Characteristics

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
I/O Pins (Note 61)					
High-Level Input Voltage	VIH	70 %LVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30 %LVDD	V
High-Level Output Voltage	VOH	LVDD – 0.2	-	-	V
Low-Level Output Voltage					
Except for SDA pin (Iout = 200 μA)	VOL1	-	-	0.2	V
SDA pin (Iout = 2 mA)	VOL2	-	-	20 %LVDD	V
Input Leakage Current	Iin	–5	-	+5	μA

Note 61. MCKI/PDMCLK, BCLK/DSDCLK, LRCK, SDTI/PDMDI, SCL, SDA, PDN, TESTI1, TESTI2, TESTO pins.

8-13. Switching Characteristics

(Ta = –40 to +85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; VSS1 = VSS2 = HPGND = 0 V; C_L = 80 pF; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCKI					
Input Frequency	fMCK	0.256	-	24.576	MHz
Pulse Width Low	tMCKL	0.4/fMCK	-	-	nsec
Pulse Width High	tMCKH	0.4/fMCK	-	-	nsec
PLL					
Output Frequency (PLLCLK) (Figure 16)					
44.1kHz × 256fs × 2	fPLL	-	22.5792	-	MHz
48.0kHz × 256fs × 2	fPLL	-	24.5760	-	MHz
Reference Clock (Figure 16)	rPLL	76.8	-	768	kHz
Lock Time	PLT	-		2	msec
PCM Audio Interface Timing					
Master Mode					
LRCK Output Timing					
Frequency (Note 62)	fs	-	8	-	kHz
		-	11.025	-	kHz
		-	12	-	kHz
		-	16	-	kHz
		-	22.05	-	kHz
		-	24	-	kHz
		-	32	-	kHz
		-	44.1	-	kHz
		-	48	-	kHz
		-	64	-	kHz
		-	88.2	-	kHz
		-	96	-	kHz
		-	128	-	kHz
		-	176.4	-	kHz
		-	192	-	kHz
Duty	LRDuty	-	50	-	%
BCLK Output Timing					
Period (BCKO bit = “0”)	tBCK	-	1/(64fs)	-	nsec
(BCKO bit = “1”)	tBCK	-	1/(32fs)	-	nsec
Duty	BCKDuty	-	50	-	%
BCLK “↓” to LRCK Edge	tBLR	–20	-	20	nsec
SDTI Setup Time	tBDS	10	-	-	nsec
SDTI Hold Time	tBDH	10	-	-	nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCM Audio Interface Timing					
Slave Mode					
LRCK Input Timing					
Frequency (Note 62)	fs	-	8	-	kHz
		-	11.025	-	kHz
		-	12	-	kHz
		-	16	-	kHz
		-	22.05	-	kHz
		-	24	-	kHz
		-	32	-	kHz
		-	44.1	-	kHz
		-	48	-	kHz
		-	64	-	kHz
		-	88.2	-	kHz
		-	96	-	kHz
		-	128	-	kHz
		-	176.4	-	kHz
		-	192	-	kHz
Duty	LRDuty	45	50	55	%
BCLK Input Timing					
Frequency (Note 63)	fBCK	0.256	-	12.288 or 512fs	MHz
Pulse Width Low	tBCKL	0.4/fBCK	-	-	nsec
Pulse Width High	tBCKH	0.4/fBCK	-	-	nsec
BCLK "↑" to LRCK Edge	tBLR	20	-	-	nsec
LRCK Edge to BCLK "↑"	tLRB	20	-	-	nsec
SDTI Setup Time	tBDS	10	-	-	nsec
SDTI Hold Time	tBDH	10	-	-	nsec

Note 62. Supported sampling rate are 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k and 192 kHz.

Note 63. The maximum value is lower frequency between "12.288 MHz" and "512fs".

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDM Interface Timing					
Sampling Frequency	PDMfs	-	-	3.072	MHz
PDMCLK Input Timing					
Period	tPDMCLK	-	1/(4PDMfs)	-	nsec
Pulse Width Low	tPDMCLKL	0.4×tPDMCLK	-	-	nsec
Pulse Width High	tPDMCLKH	0.4×tPDMCLK	-	-	nsec
PDM 1-bit mode					
PDMDI Setup Time	tPDMS	20	-	-	nsec
PDMDI Hold Time	tPDMH	20	-	-	nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
DSD64 Interface Timing (64fs mode)					
Sampling Frequency	fs	-	-	48	kHz
DSDCLK Input Timing					
Period	tDSCK	-	1/64fs	-	nsec
Pulse Width Low	tDSCKL	0.4×tDSCK	-	-	nsec
Pulse Width High	tDSCKH	0.4×tDSCK	-	-	nsec
DSD Data I/F Timing					
DSDCLK Edge to PDMDI Edge (Note 64)	tDDD	-20	-	20	nsec

Note 64. DSD data transmitting device must meet this time.
When DCKB bit = “0” (default), “tDDD” is defined from DSDCLK “↓” until PDMDI edge and from PDMDI edge until DSDCLK “↑” edge.
When DCKB bit = “1”, “tDDD” is defined from DSDCLK “↑” until PDMDI edge and from PDMDI edge until DSDCLK “↓” edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C-bus mode): (Note 65)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µsec
Clock Low Time	tLOW	1.3	-	-	µsec
Clock High Time	tHIGH	0.6	-	-	µsec
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µsec
SDA Hold Time from SCL Falling (Note 66)	tHD:DAT	0	-	-	µsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µsec
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µsec
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µsec
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µsec
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	nsec
Power-down & Reset Timing					
PDN accept pulse width (Note 67)	tPDN	1	-	-	msec
PDN Reject Pulse Width (Note 67)	tRPD	-	-	50	nsec

Note 65. I^2C-bus is a registered trademark of NXP B.V.

Note 66. Data must be held long enough to bridge the 300 nsec-transition time of SCL.

Note 67. The AK4332 will be reset by bringing the PDN pin = “L”. The PDN pin must held “L” for longer period than or equal to tPDN (Min.). The AK4332 will not be reset by the “L” pulse shorter than or equal to tRPD (Max.).

8-14. Timing Diagram (System Clock)

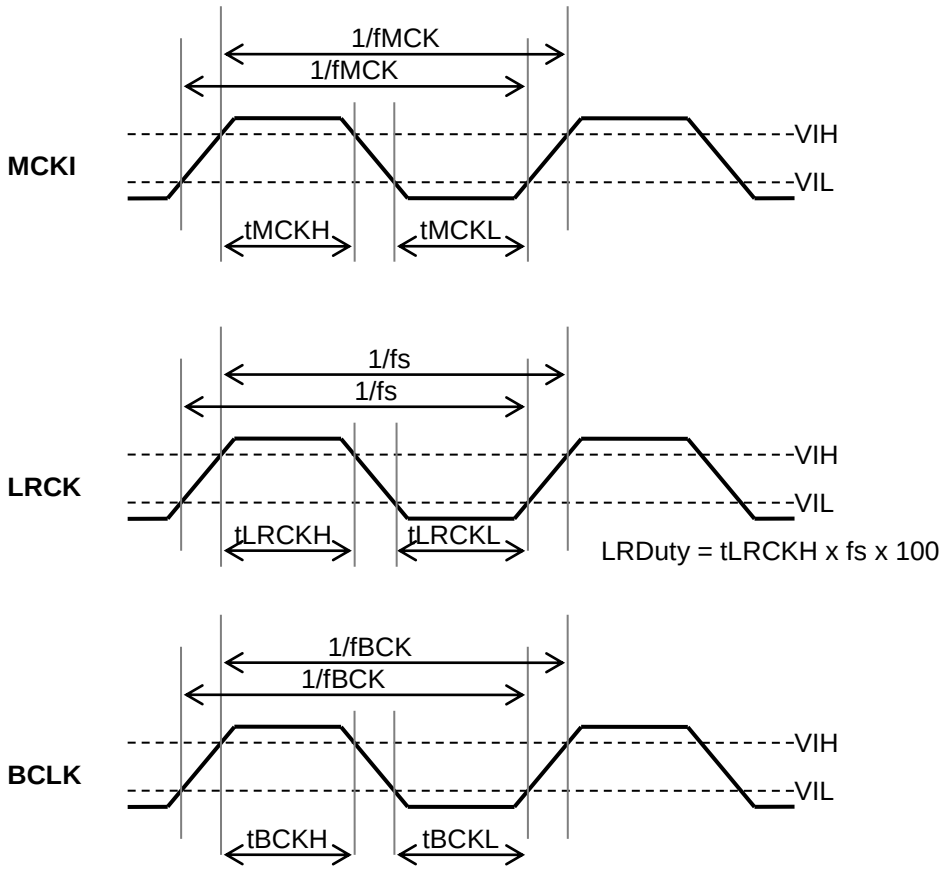


Figure 3. System Clock (Slave Mode)

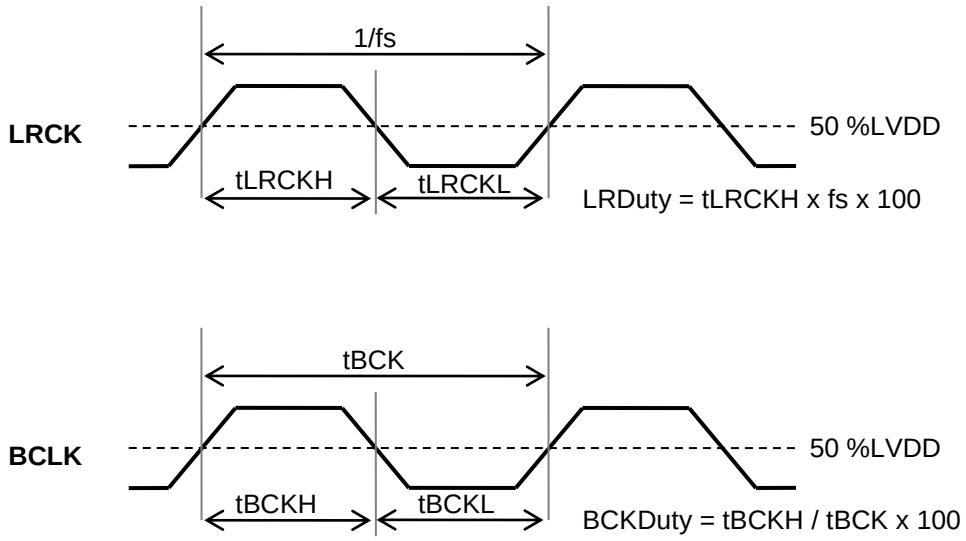


Figure 4. System Clock (Master Mode)

8-15. Timing Diagram (Serial Audio Interface)

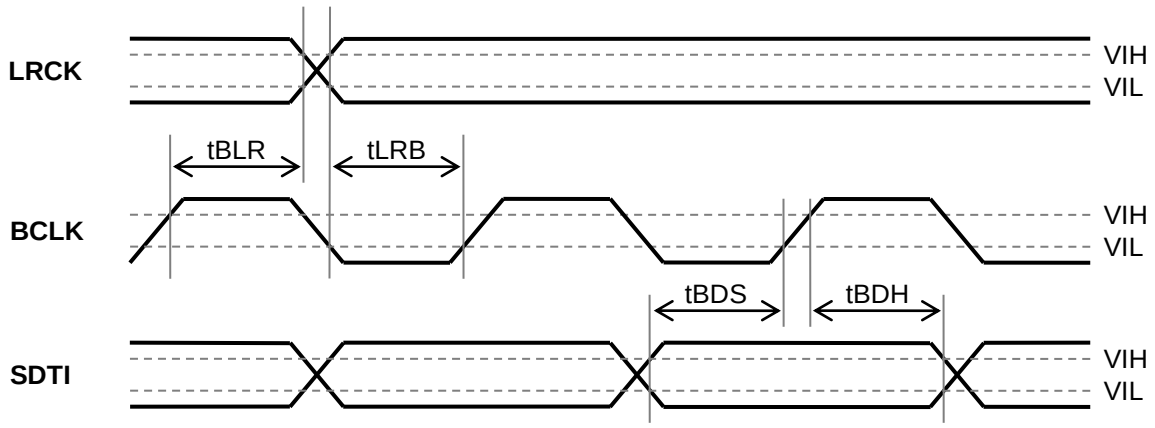


Figure 5. Serial Data Interface (Slave Mode)

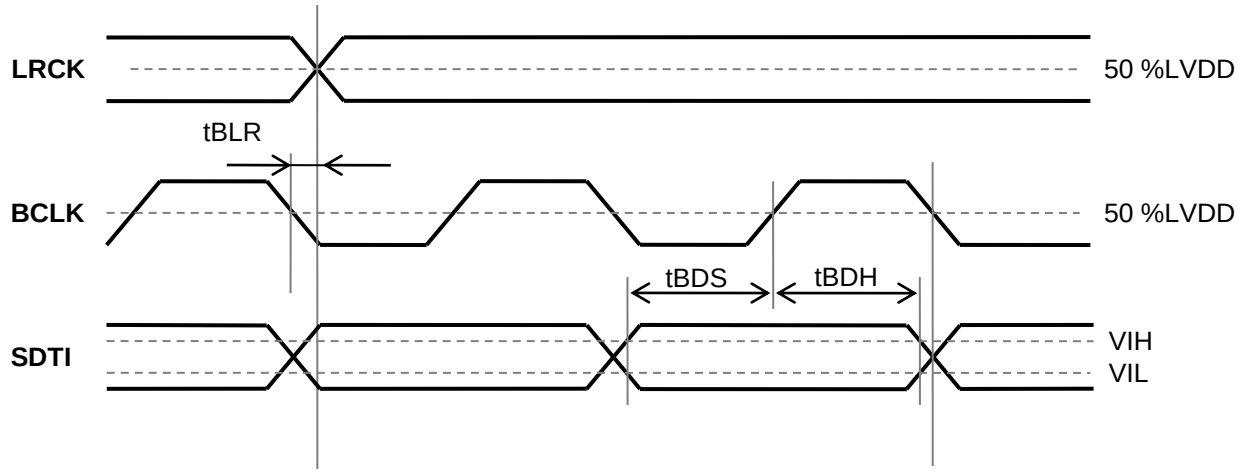


Figure 6. Serial Data Interface (Master Mode)

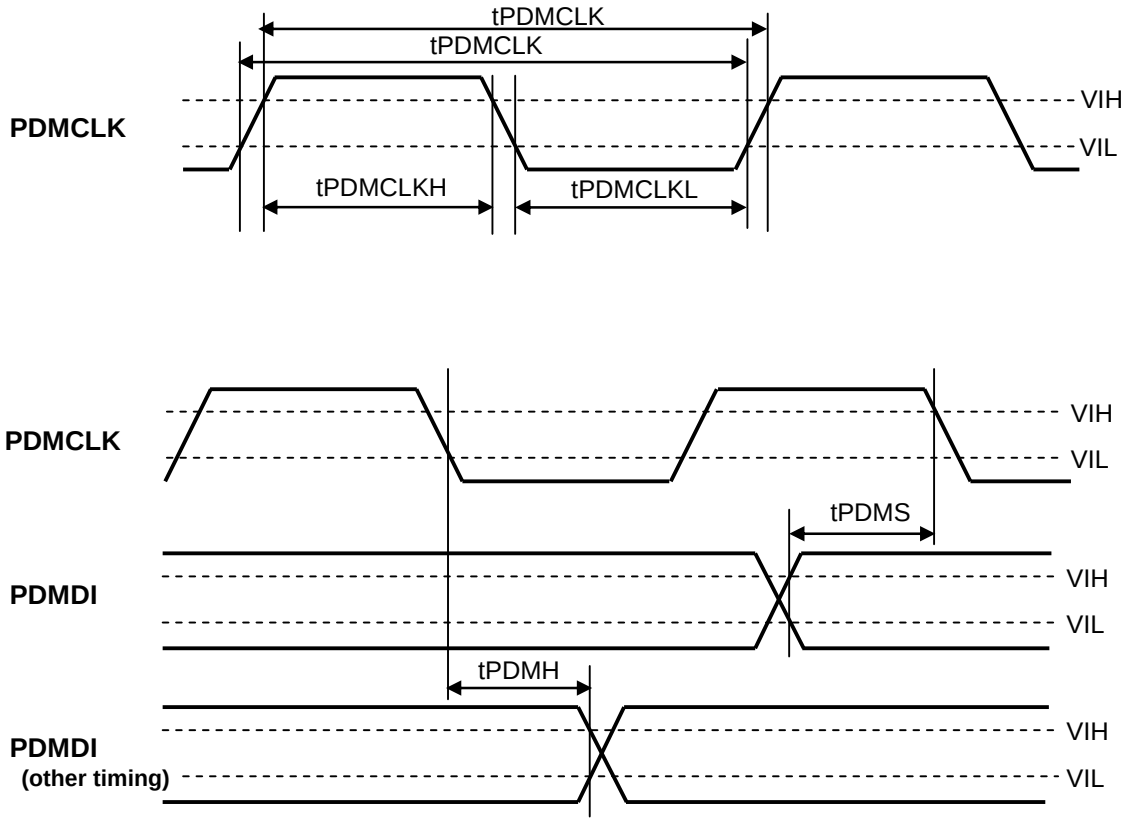


Figure 7. PDM 1-bit Interface Timing (PDMCKR bit = “0”)

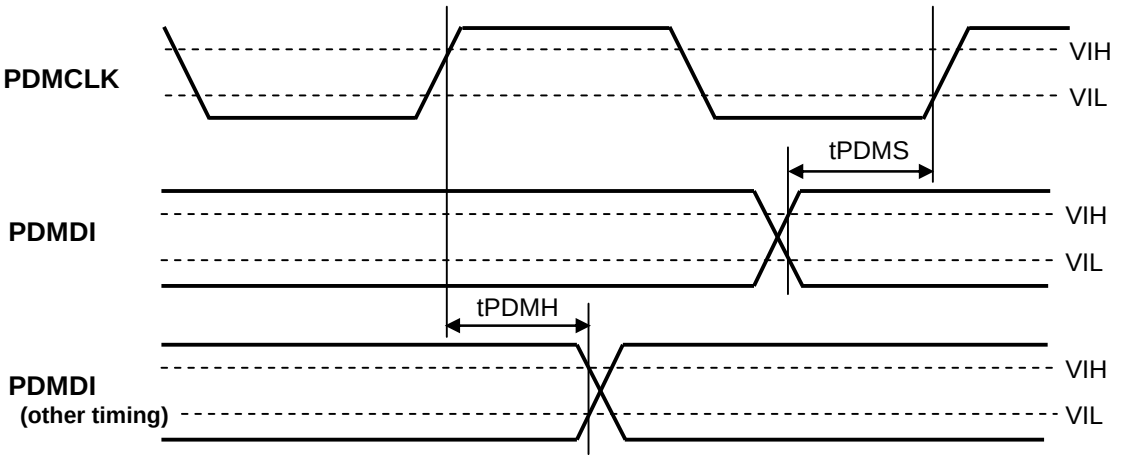


Figure 8. PDM 1-bit Interface Timing (PDMCKR bit = “1”)

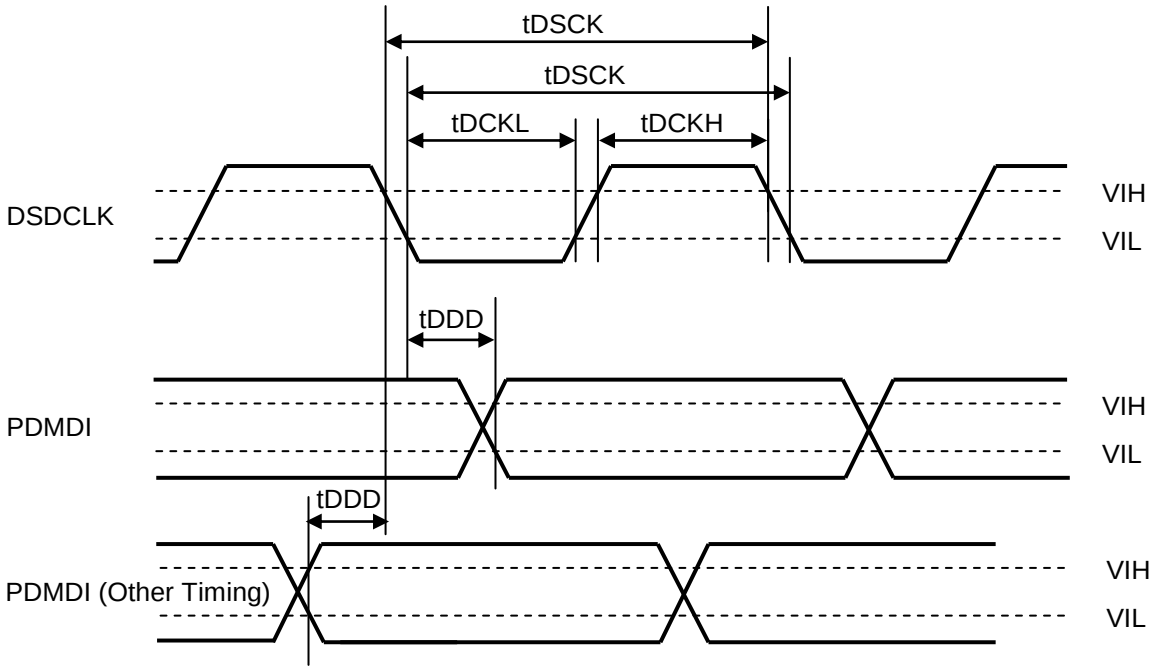


Figure 9. DSD Interface Timing (DCKB bit = “0”)

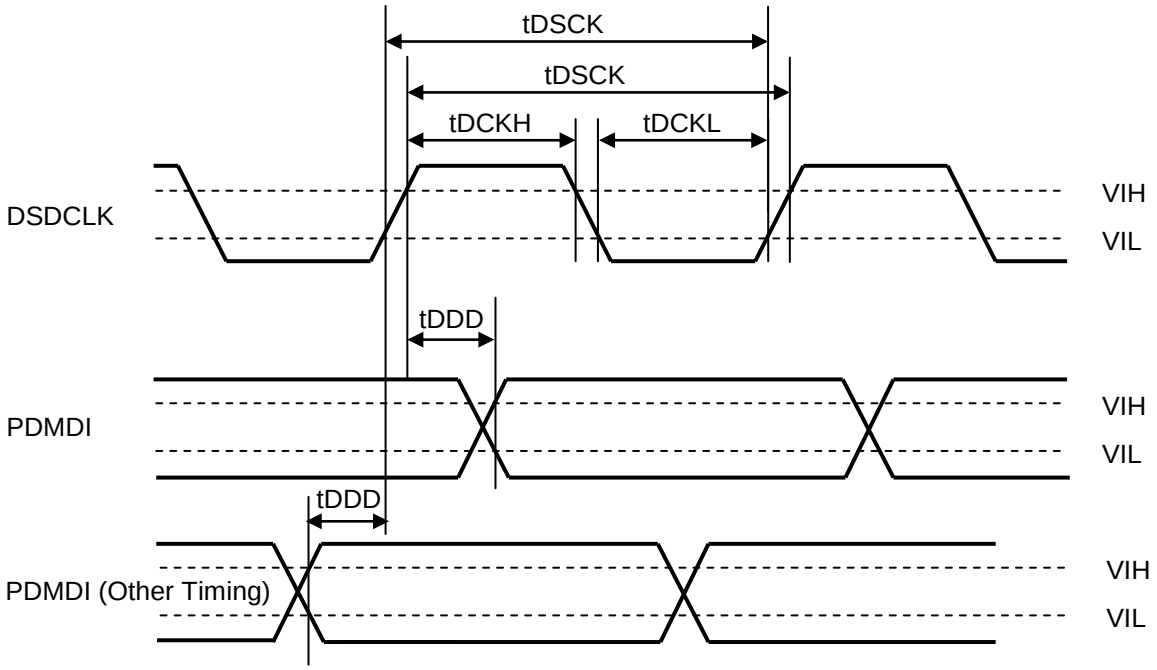


Figure 10. DSD Interface Timing (DCKB bit = “1”)

8-16. Timing Diagram (I²C-bus Interface)

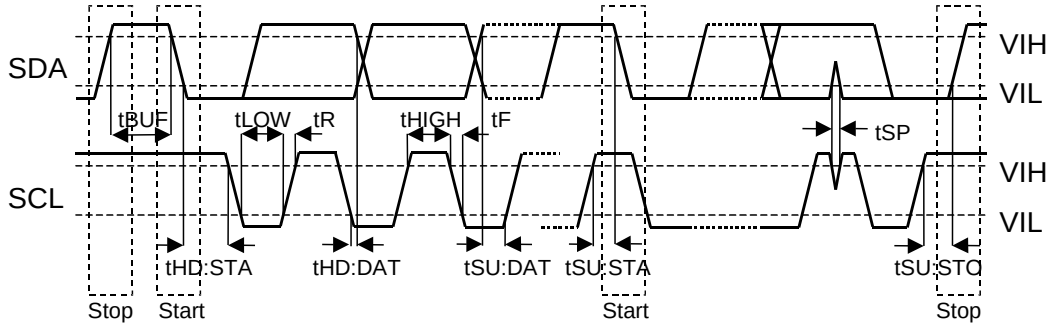


Figure 11. I²C-bus Mode Timing

8-17. Timing Diagram (Reset)

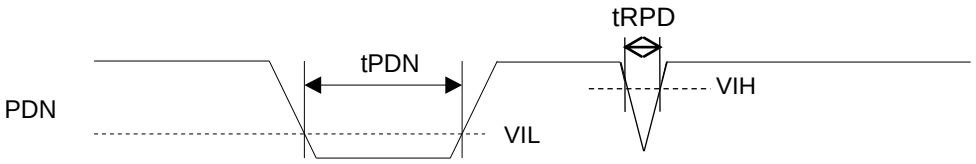


Figure 12. Power Down and Standby

9. Functional Description

9-1. Digital Data Input (PCM Mode, PDM 1-bit Mode / DSD Mode)

The AK4332 can perform D/A conversion for PCM data, PDM data and DSD data.
In PCM Mode, PCM data can be input to the BCLK, LRCK and SDTI pins. In PDM 1-bit Mode, PDM data can be input to the PDMCLK and PDMDI pins. In DSD Mode, DSD data can be input to the DSDCLK and PDMDI pins.
PCM Mode and PDM 1-bit Mode / DSD Mode can be selected by setting PDM bit (Table 2).

All power management bits (PMCP1, PMCP2, PMLDO1P, PMLDO1N, PMDA and PMHP bits) except for PMPLL bit must be "0" when setting PDM bit.

Table 2. Audio Interface Selection

PDM bit	Audio Interface	
0	PCM Mode	(default)
1	PDM 1-bit Mode / DSD Mode	

Table 3. Setting of Clock Selection (x: Do not Care)

Mode		PDM bit	PDMMODE bit	PMPLL bit	PLS bit	MS bit	MCKI / PDMCLK pins	BCLK / DSDCLK pins	LRCK pins	PLL Clock Source	DAC CLK
PCM Mode	1	0	x	0	0	0	MCKI Input	BCLK Input	LRCK Input	(PLL Disable)	MCKI
	2	0	x	0	0	1	MCLK Input	BCLK Output	LRCK Output	(PLL Disable)	MCKI
	3	0	x	1	0	0	MCKI Input	BCLK Input	LRCK Input	MCKI	PLLCLK
	4	0	x	1	0	1	MCLK Input	BCLK Output	LRCK Output	MCKI	PLLCLK
	5	0	x	1	1	0	VSS2	BCLK Input	LRCK Input	BCLK	PLLCLK
PDM 1-bit Mode		1	"0"	0	0	0	PDMCLK Input	VSS2	VSS2	(PLL Disable)	PDMCLK
DSD Mode	1	1	"1"	0	0	0	MCKI Input	DSDCLK	VSS2	(PLL Disable)	MCKI
	2	1	"1"	1	1	0	VSS2	DSDCLK	VSS2	DSDCLK	PLLCLK

Note 68. Inhibit to setting except of clock combinations shown in Table 3.

9-2. System Clock

9-2-1 PCM Mode

The DAC, Headphone Amplifier and Audio Interface blocks are operated by a clock generated by PLL or an external MCKI. Clock source can be selected by DACCKS bit. The sampling frequency and master clock frequency are set by CM[1:0] bits and FS[4:0] bits.

Table 4. DAC Master Clock Setting

DACCKS bit	DAC Master Clock	
0	MCKI	(default)
1	PLLCLK	

The AK4332 can be operated in both master and slave modes in PCM Mode. Clock mode of the LRCK pin and the BLCK pin can be selected by MS bit. When using master mode, the LRCK pin and the BCLK pin should be pulled down or pulled up with an external resistor (about 100 kΩ) because both pins are floating state until MS bit becomes “1”.

Table 5. Master / Slave Mode Selection

MS bit	LRCK (pin), BCLK (pin)	
0	Slave Mode	(default)
1	Master Mode	

Master / slave mode switching is not allowed while the AK4332 is in normal operation. The DAC and headphone amplifier must be powered down and PMTIM bit must be “0” before master / slave mode is switched. Furthermore, PLL and charge pump must also be powered down in case that sampling frequency is changed or DACCLK is stopped.

< MS bit Setting Sequence Example >
1. DAC, Headphone Amplifier (PLL, Charge Pump) Power-Down
2. Clock Mode of ACPU Setting (In case clock mode of ACPU is master, switch to slave.)
3. MS bit Selection
4. Clock Mode of ACPU Setting (In case clock mode of ACPU is slave, switch to master.)
5. DAC, Headphone Amplifier (PLL, Charge Pump) Power-Up

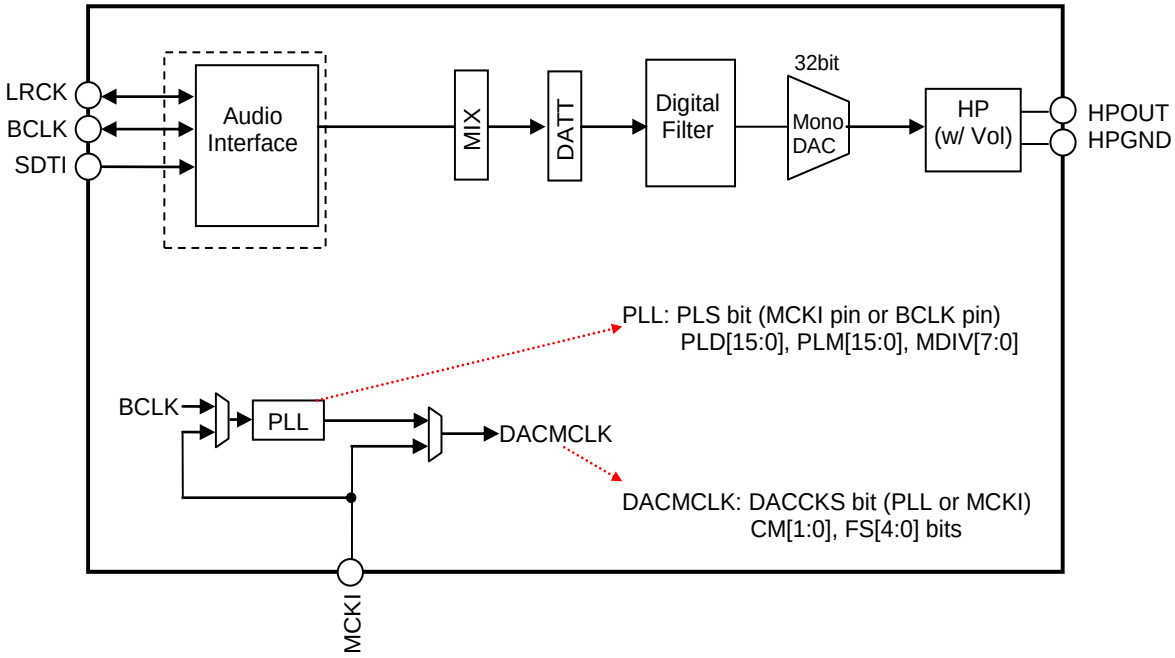


Figure 13. Internal configure diagram of AK4332

< Salve Mode: MS bit = “0” >
MS bit = “0”, PMPLL bit = “0”, DACCKS bit = “0”

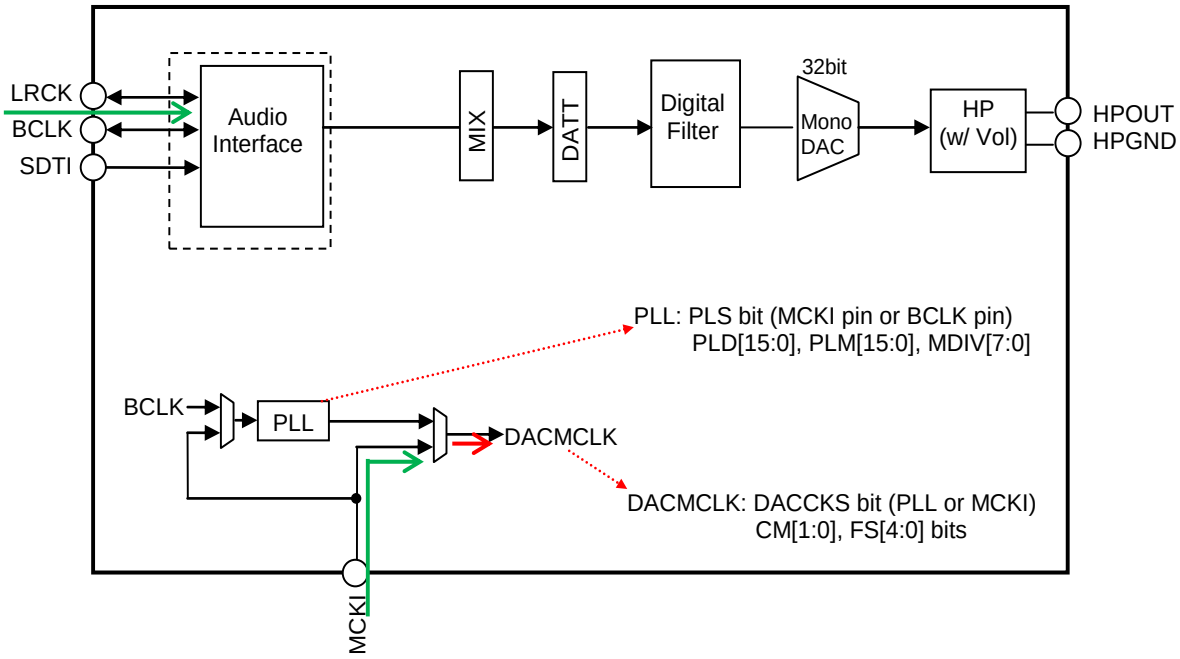


Figure 14. Example of Clock and Data Flow (Slave Mode, Not using PLL)

< Master Mode: MS bit = “1” >
MS bit = “1”, PMPLL bit = “1”, DACCKS bit = “0”

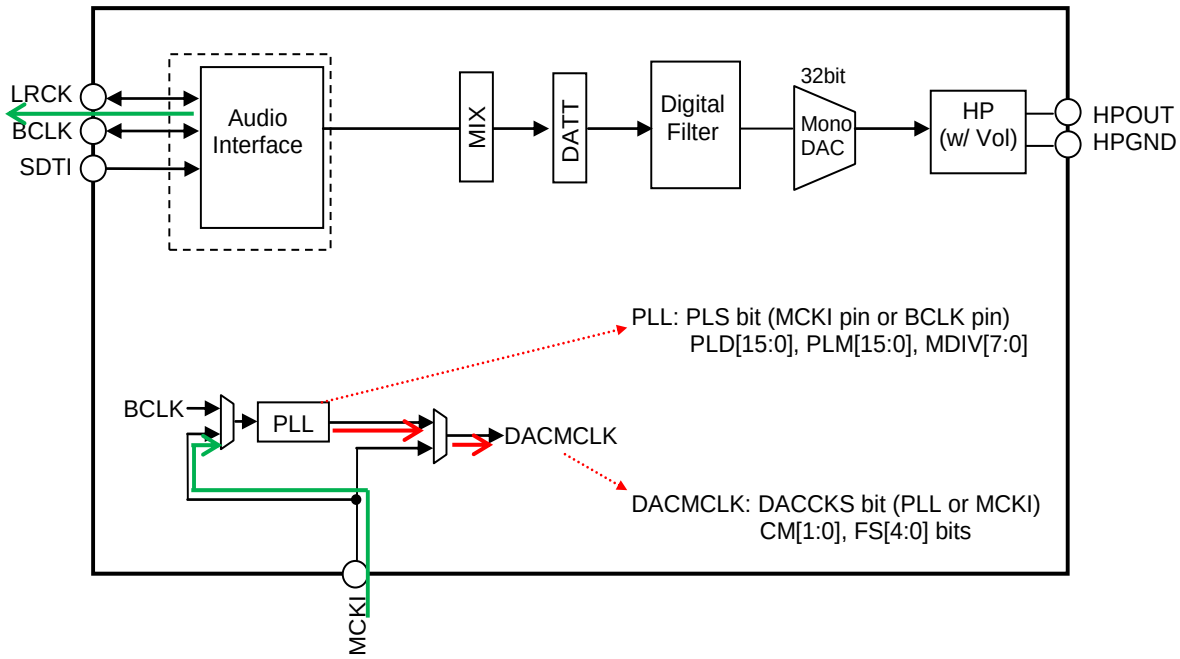


Figure 15. Example of Clock and Data Flow (Master Mode, Using PLL)

< Master Clock Frequency and Sampling Frequency Setting >

Table 6. Setting of Master Clock Frequency

CM1 bit	CM0 bit	Master Clock Frequency	Sampling Frequency Range	
0	0	256fs	8 to 96 kHz	(default)
0	1	512fs	8 to 48 kHz	
1	0	1024fs	8 to 24 kHz	
1	1	128fs	128 to 192 kHz	

Table 7. Setting of Sampling Frequency (N/A: Not available)

FS4 bit	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8 kHz	(default)
0	0	0	0	1	11.025 kHz	
0	0	0	1	0	12 kHz	
0	0	1	0	0	16 kHz	
0	0	1	0	1	22.05 kHz	
0	0	1	1	0	24 kHz	
0	1	0	0	0	32 kHz	
0	1	0	0	1	44.1 kHz	
0	1	0	1	0	48 kHz	
0	1	1	0	0	64 kHz	
0	1	1	0	1	88.2 kHz	
0	1	1	1	0	96 kHz	
1	0	0	0	0	128 kHz	
1	0	0	0	1	176.4 kHz	
1	0	0	1	0	192 kHz	
Others					N/A	

* Depending on setting of PLL's divider, the sampling frequency may differ. Please set PLD[15:0] and PLM[15:0] bits precisely.

9-2-2 PDM Mode

PDM 1-bit Mode and DSD Mode can be selected by setting PDM bit = “1” (Table 2).
PDM 1-bit Mode and DSD Mode can be selected by setting PDMMODE bit (Table 8).

In PDM 1-bit Mode or DSD Mode, CM[1:0] bits should be set to “00” (256fs), FS[4:0] bits should be set to “01001” (44.1 kHz) or “01010” (48 kHz) and MS bit should be set to “0” (Slave Mode).

All power management bits (PMCP1, PMCP2, PMLDO1P, PMLDO1N, PMDA and PMHP bits) except for PMPLL bit must be “0” when setting PDMMODE bit.

Table 8. PDM Mode Selection

PDM bit	PDMMODE bit	Mode	
1	0	PDM 1-bit Mode	(default)
	1	DSD Mode	

9-3. Master Counter Synchronization Control

Internal master counter starts when setting PMTIM bit = “1”. Phase difference can be controlled within 4/64fs by asserting PMTIM bit when using multiple AK4332’s. In case of using PLL output (PLLO) as system clock, set PMTIM bit to "1" in 2 msec or more after setting PMPLL bit to “1”. In case of using external clock as system clock, supply a stable clock and set PMTIM bit to "1". All power management bits (PMCP1, PMCP2, PMLDO1P, PMLDO1N, PMDA and PMHP bits) except for PMPLL bit must be “0” when PMTIM bit = “0”.

Table 9. Master Counter Power Control

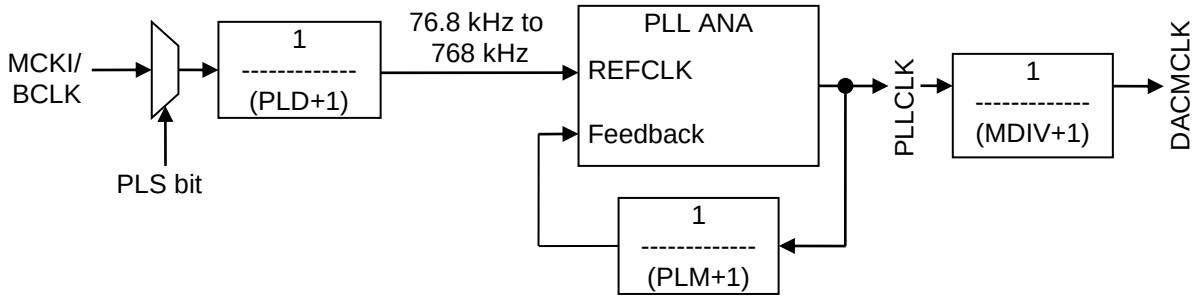
PMTIM bit	Master Counter Status	
0	Disable	(default)
1	Enable	

9-4. PLL

The PLL generates PLLCLK which can be used the operation clock for DAC (DACMCLK). The oscillation frequency of PLLCLK should be set to 22.5792 or 24.5760 MHz (Table 10 shows setting of 48 kHz, 44.1 kHz and 32 kHz base rates). Refer to Table 17 and Table 18 for PLL setting examples. Reference clock of PLL (REFCLK) should be set in a range from 76.8 kHz to 768 kHz.

Table 10. PLLCLK Setting

	48 kHz base rate / 32kHz base rate	44.1 kHz base rate
PLLCLK	24.5760 MHz	22.5792 MHz



REFCLK = PLL Source / (PLD+1)
PLLCLK = REFCLK x (PLM+1)
DACMCLK = PLLCLK / (MDIV+1)

Figure 16. PLL Block Diagram

9-4-1. Power Management (PMPLL)

PLL can be powered down by a control register setting.

Table 11. PLL Power Control

PMPLL bit	PLL Status	
0	Power-Down	(default)
1	Power-Up	

9-4-2. Input Clock Select Function

The PLL has a function that selects the input clock. The clock source pin is selected by PLS bit. PLS bit must be set at PMTIM bit = “0”.

Table 12. PLL Clock Source Selection

PLS bit	Clock Source	
0	MCKI pin	(default)
1	BCLK pin	

9-4-3. PLL Reference Clock Divider

The PLL can set the dividing number of the reference clock in 16-bit. The input clock is used as PLL reference clock by dividing by (PLD + 1). PLD[15:0] bits must be set at PMTIM bit = “0”.

Table 13. PLL Reference Clock Divider

PLD[15:0] bits	Dividing Number	
0x0000	1	(default)
0x0001-0xFFFF	1/(PLD+1)	

Note 69. The reference clock divided by PLD should be set in the range from 76.8 kHz to 768 kHz.

9-4-4. PLL Feedback Clock Divider

The dividing number of feedback clock can be set freely in 16-bit. PLLCLK is divided by (PLM +1) and used as PLL feedback clock. PLM[15:0] bits must be set at PMTIM bit = “0”.

Table 14. PLL Feedback Clock Divider

PLM[15:0] bits	Dividing Number	
0x0000	Clock Stop	(default)
0x0001-0xFFFF	1/(PLM+1)	

9-4-5. PLL Internal Mode Setting

PLLMD bit controls PLL internal mode. Set PLLMD bit by referring to Table 17 and Table 18. PLLMD bit must be set at PMPLL bit = “0”.

Table 15. PLL Internal Mode Setting

PLLMD bit	Reference Clock	
0	≥ 256 kHz	(default)
1	< 256 kHz	

9-4-7. PLLCLK Divider Setting

MDIV[3:0] bits control PLLCLK divider.
MDIV[3:0] bits must be set at PMTIM bit = “0”.

Table 16. PLLCLK Divider Setting

MDIV[3:0] bits	Divide By	
0H	1	(default)
1H ~ FH	1/(MDIV+1)	

Note 70. When set each registers as following, divider value is set to 1.5 at MDIV[3:0] bits = 0H.

- CM[1:0]=”10” , FS[4:0]=”00100” (1024fs, fs=16kHz)
- CM[1:0]=”01”, FS[4:0]=”01000” (512fs, fs=32kHz)
- CM[1:0]=”00” , FS[4:0]=”01100” (256fs, fs=64kHz)
- CM[1:0]=”11” , FS[4:0]=”10000” (128fs, fs=128kHz)

9-4-7. PLL Setting Examples

Table 17. PLL Setting Example (PLL reference source: MCKI)

CLKIN		PLL condition						Sampling Frequency [kHz]
Source	Frequency [kHz]	PLD+1	REFCLK [kHz]	PLM+1	PLLMD bit	PLLCLK [MHz]	MDIV+1 (Note 71)	
MCKI	9,600	25	384	64	0	24.5760	0	48
	19,200	25	768	32	0	24.5760	0	48
	12,288	16	768	32	0	24.5760	0	48
	24,576	32	768	32	0	24.5760	0	48
	12,000	125	96	256	1	24.5760	0	48
	24,000	125	192	128	1	24.5760	0	48
	9,600	125	76.8	294	1	22.5792	0	44.1
	19,200	125	153.6	147	1	22.5792	0	44.1
	11,289.6	16	705.6	32	0	22.5792	0	44.1
	22,579.2	32	705.6	32	0	22.5792	0	44.1

Note 71. At the case of CM[1:0] bits i set to “01” (512fs).

Table 18. PLL Setting Example (PLL reference source: BCLK)

CLKIN		PLL condition						Sampling
Source	Frequency [kHz]	PLD+1	REFCLK [kHz]	PLM+1	PLLMD bit	PLLCLK [MHz]	MDIV+1 (Note 71)	Frequency [kHz]
BCLK (32fs)	256	1	256	96	0	24.5760	5	8
	352.8	1	352.8	64	0	22.5792	3	11.025
	512	1	512	48	0	24.5760	2	16
	705.6	1	705.6	32	0	22.5792	1	22.05
	768	1	768	32	0	24.5760	1	24
	1,024	2	512	48	0	24.5760	0	32
	1,411.2	2	705.6	32	0	22.5792	0	44.1
	1,536	2	768	32	0	24.5760	0	48
BCLK (48fs)	384	1	384	64	0	24.5760	5	8
	529.2	3	176.4	128	1	22.5792	3	11.025
	768	1	768	32	0	24.5760	2	16
	1,058.4	3	352.8	64	0	22.5792	1	22.05
	1,152	3	384	64	0	24.5760	1	24
	1,536	2	768	32	0	24.5760	0	32
	2,116.8	3	705.6	32	0	22.5792	0	44.1
	2,304	3	768	32	0	24.5760	0	48
BCLK (64fs)	512	1	512	48	0	24.5760	5	8
	705.6	1	705.6	32	0	22.5792	3	11.025
	1,024	2	512	48	0	24.5760	2	16
	1,411.2	2	705.6	32	0	22.5792	1	22.050
	1,536	2	768	32	0	24.5760	1	24
	2,048	4	512	48	0	24.5760	0	32
	2,822.4	4	705.6	32	0	22.5792	0	44.1
	3,072	4	768	32	0	24.5760	0	48

9-5. DAC Digital Filter

AK4332 has four types of DAC digital filter in PCM Mode. The filter mode can be selected by DASD and DASL bits. The default setting is DASL = DASD bits = “0” (Sharp Roll-Off Filter). DASD bit and DASL bit must be set at PMDA bit = “0”.

Table 19. DAC Digital Filter Setting

DASD bit	DASL bit	DAC Filter Mode Setting	
0	0	Sharp Roll-Off Filter	(default)
0	1	Slow Roll-Off Filter	
1	0	Short Delay Sharp Roll-Off Filter	
1	1	Short Delay Slow Roll-Off Filter	

9-6. Digital Volume

The AK4332 has a 32-level digital volume control in the input stage of DAC. The volume control level ranges +3.0 dB to −12.0 dB in 0.5 dB step including Mute. The volume change is executed immediately by setting registers.
OVC [4:0] bits must be set when PMDA bit = “0”.

Table 20. Digital Volume Setting

OVC [4:0] bits	Volume (dB)	
1FH	+3.0	
1EH	+2.5	
1DH	+2.0	
1CH	+1.5	
1BH	+1.0	
1AH	+0.5	
19H	0.0	(default)
18H	−0.5	
17H	−1.0	
16H	−1.5	
15H	−2.0	
14H	−2.5	
13H	−3.0	
12H	−3.5	
11H	−4.0	
10H	−4.5	
0FH	−5.0	
0EH	−5.5	
0DH	−6.0	
0CH	−6.5	
0BH	−7.0	
0AH	−7.5	
09H	−8.0	
08H	−8.5	
07H	−9.0	
06H	−9.5	
05H	−10.0	
04H	−10.5	
03H	−11.0	
02H	−11.5	
01H	−12.0	
00H	MUTE	

9-7. Headphone Amplifier Output (HPOUT pin)

Headphone amplifiers are operated by positive and negative power that is supplied from internal charge pump circuit. The VEE2 pin output the negative voltage generated by the internal charge pump circuit from CVDD. This charge pump circuit is switched between VDD mode and 1/2VDD mode by the output level of the headphone amplifiers. The headphone amplifier output is single-ended and centered on HPGND (0 V). Therefore, a capacitor for AC-coupling is not necessary. The minimum load resistance is 7.2Ω. Ground loop noise cancelling function for headphone amplifier is available by connecting the HPGND pin to the ground of the jack.

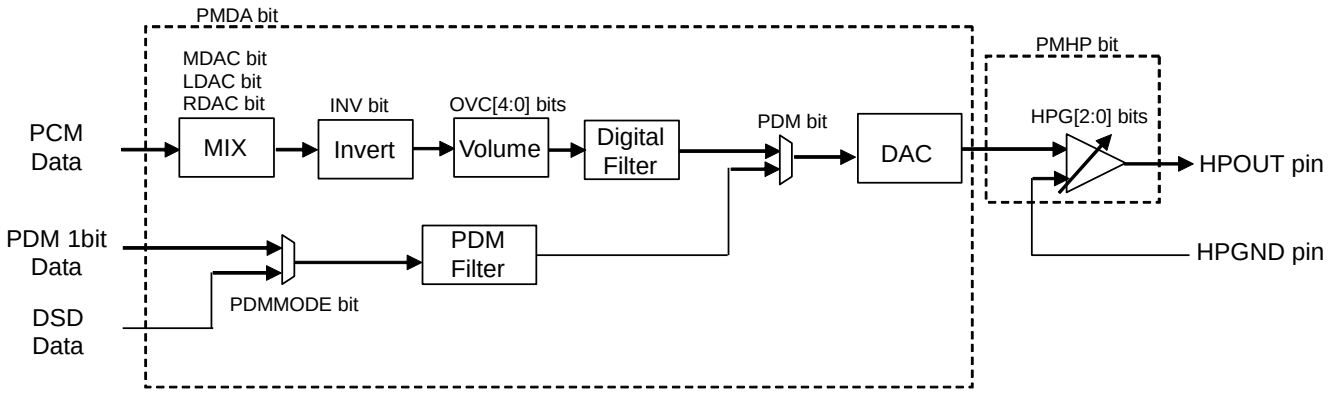


Figure 17. DAC & Headphone Amplifier Block Diagram

Charge Pump Mode can be selected by CPMODE[1:0]bits. Headphone amplifier operates Class-G Operation Mode when CPMODE[1:0] bits = “00”.

Table 21. Charge Pump Mode Setting (N/A: Not available)

CPMODE1 bit	CPMODE0 bit	Mode	Operation Voltage	
0	0	Class-G Operation Mode	Automatic Switching	(default)
0	1	VDD Operation Mode	± VDD	
1	0	1/2 VDD Operation Mode	±1/2 VDD	
1	1	N/A	N/A	

Note 72. Class-G Operation Mode is supported in PCM Mode, PDM 1-bit Mode and DSD Mode.

< Class-G Mode Switching Level >

<PCM Mode>
In PCM Mode, Class-G switching level of VDD and 1/2VDD modes can be set by LVDSEL[1:0] bits.
All power management bits (PMCP1, PMCP2, PMLDO1P, PMLDO1N, PMDA and PMHP bits) except for PMPLL bit must be “0” when setting LVDSEL[1:0] bits .

Table 22. Class-G Switching Level Setting (PCM Mode)

LVDSEL[1:0] bits	Class-G Switching Level	
00	1.05 mW @ 16Ω	(default)
01	1.05 mW @ 32Ω	
10	1.05 mW @ 11Ω	
11	1.05 mW @ 8Ω	

<PDM Mode / DSD Mode>
In PDM Mode and DSD Mode, Class-G switching level of VDD and 1/2VDD modes can be set by LVDSEL[1:0] bits and HPG[2:0] bits.
All power management bits (PMCP1, PMCP2, PMLDO1P, PMLDO1N, PMDA and PMHP bits) except for PMPLL bit must be “0” when setting LVDSEL[1:0] bits and HPG[2:0] bits .

Table 23. Class-G Switching Level Setting (PDM 1-bit Mode / DSD Mode)

LVDSEL[1:0] bits	Class-G Switching Level	
00	1.61 mW @ 16Ω	(default)
01	1.41 mW @ 32Ω	
10	1.65 mW @ 11Ω	
11	1.86 mW @ 8Ω	

Note 73. This specification is defined in case that HPG[2:0] bits is set to −4dB.

< Class-G Mode Switching Period >

When the charge pump operation mode is changed to VDD mode from 1/2VDD mode, an internal counter for holding VDD mode starts (Table 24). The charge pump changes to 1/2VDD mode if the output signal level is lower than the switching level and 1/2VDD mode detection time that is set by LVDTM[2:0] bits is passed after VDD mode hold time is finished.

Table 24. VDD Mode Holding Period Setting (x: Do not Care)

VDDTM[3:0] bits		VDD Mode Holding Period				
		8 kHz	48 kHz	96 kHz	192 kHz	
0000	1024/fs	128 msec	21.3 msec	10.7 msec	5.3 msec	(default)
0001	2048/fs	256 msec	42.7 msec	21.3 msec	10.7 msec	
0010	4096/fs	512 msec	85.3 msec	42.7 msec	21.3 msec	
0011	8192/fs	1024 msec	170.7 msec	85.3 msec	42.7 msec	
0100	16384/fs	2048 msec	341.3 msec	170.7 msec	85.3 msec	
0101	32768/fs	4096 msec	682.7 msec	341.3 msec	170.7 msec	
0110	65536/fs	8192 msec	1365.3 msec	682.7 msec	341.3 msec	
0111	131072/fs	16384 msec	2730.7 msec	1365.3 msec	682.7 msec	
1xxx	262144/fs	32768 msec	5461.3 msec	2730.7 msec	1365.3 msec	

When the output voltage becomes less than Class-G mode switching level, the internal detection counter for 1/2VDD mode which is set by LVDTM[2:0] bits starts. This counter is reset when the output voltage exceeds Class-G mode switching level. The charge pump operation mode is changed to 1/2VDD from VDD if the detection counter of 1/2VDD mode is finished and also the VDD mode hold period is passed.

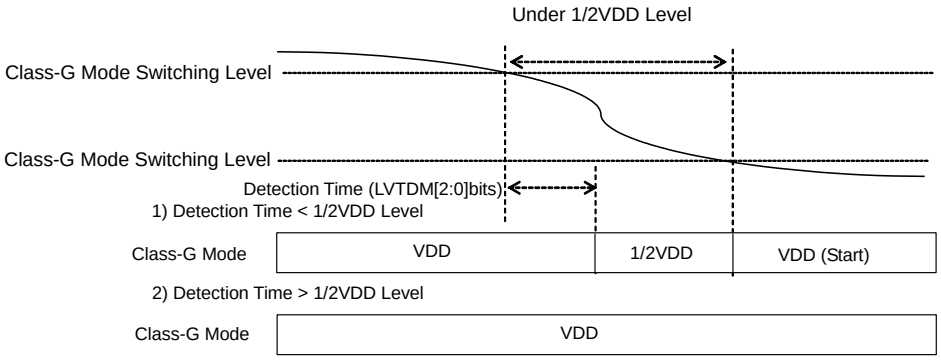


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Figure 18. Transition to 1/2VDD Mode from VDD Mode

Table 25. 1/2VDD Detection Period (Minimum frequency that is not detected)

LVDTM[2:0] bits		1/2VDD Mode Detection Time/ Minimum Frequency that is Not Detected				
		8 kHz	48 kHz	96 kHz	192 kHz	
000	64/fs	8 msec	1.3 msec	0.67 msec	0.33 msec	(default)
		62.5 Hz	375 Hz	750 Hz	1500 Hz	
001	128/fs	16 msec	2.7 msec	1.3 msec	0.67 msec	
		31.3 Hz	187.5 Hz	375 Hz	750 Hz	
010	256/fs	32 msec	5.3 msec	2.7 msec	1.3 msec	
		15.6 Hz	93.8 Hz	187.5 Hz	375 Hz	
011	512/fs	64 msec	10.7 msec	5.3 msec	2.7 msec	
		7.8 Hz	46.9 Hz	93.8 Hz	187.5 Hz	
100	1024/fs	128 msec	21.3 msec	10.7 msec	5.3 msec	
		3.9 Hz	23.4 Hz	46.9 Hz	93.8 Hz	
101	2048/fs	256 msec	42.7 msec	21.3 msec	10.7 msec	
		2.0 Hz	11.7 Hz	23.4 Hz	46.9 Hz	
110	4096/fs	512 msec	85.3 msec	42.7 msec	21.3 msec	
		1.0 Hz	5.9 Hz	11.7 Hz	23.4 Hz	
111	8192/fs	1024 msec	170.7 msec	85.3 msec	42.7 msec	
		0.5 Hz	2.8 Hz	5.9 Hz	11.7 Hz	

< Headphone Amplifier Volume Circuit >

The output level of the headphone amplifier can be controlled by HPG[2:0] bits. The volume setting is ranges from +4 dB to −10 dB in 2 dB step (Table 26). When the volume is changed, zero cross detection is executed. Zero cross timeout period is set by HPTM[2:0] bits (Table 27).

The headphone amplifier volume should be changed with an interval of zero cross timeout period after setting HPG[2:0] bits once. If the volume is changed continuously without the interval, the gain setting at the next zero crossing point will be applied.

Table 26. Headphone Amplifier Volume Setting

HPG[2:0] bits	Volume (dB)	
111	+4	
110	+2	
101	0	(default)
100	−2	
011	−4	
010	−6	
001	−8	
000	−10	

Table 27. Headphone Volume Zero Cross Timeout Setting (x: Do not care)

HPTM[2:0] bits		Zero Crossing Timeout Period				
		8 kHz	48 kHz	96 kHz	192 kHz	
000	128/fs	16 msec	2.7 msec	1.3 msec	0.67 msec	
001	256/fs	32 msec	5.3 msec	2.7 msec	1.3 msec	
010	512/fs	64 msec	10.7 msec	5.3 msec	2.7 msec	
011	1024/fs	128 msec	21.4 msec	10.7 msec	5.3 msec	(default)
1xx	2048/fs	256 msec	42.7 msec	21.4 msec	10.7 msec	

Note 74. Zero cross detection is not enabled in PDM 1-bit Mode and DSD Mode.

< Headphone Amplifier External Circuit >

It is necessary to put an oscillation prevention circuit (0.1 µF ±20% capacitor and 15Ω ±20% resistor) because there is a possibility that the headphone amplifier oscillates.

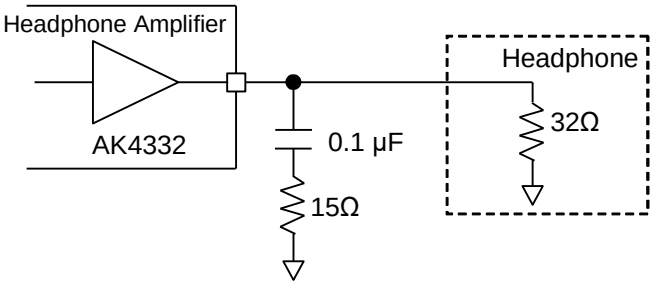


Figure 19. Example of Headphone Amplifier Oscillation Prevention Circuit

< Power-Up/Down Sequence of Headphone Amplifier >

After releasing DAC power-down state by PMDA bit, the headphone amplifier should be powered up by PMHP bit. A wait time from DAC power-up to headphone power-up is not necessary.

PMDA bit releases a power-down of the digital block of DAC, PMHP bit powers up the analog block of the DAC and the headphone amplifier. Then, initialization cycle of the headphone amplifier is executed. The gain setting (HPG[2:0] bits) should be done before PMHP bit is set to "1". Do not change the gain setting (HPG[2:0] bits) during the headphone initialization cycle. The gain setting can be changed after the headphone initialization cycle is finished. A wait time from the gain setting to PMHP bit = "1" is not necessary.

When the AK4332 is powered down, the headphone amplifier should be powered down first. The DAC should be powered down next. A wait time from a headphone power-down to a DAC power-down is not necessary.

When the headphone amplifier is powered down, the HPOUT pin is pulled down to HPGND via the internal pull-down register. The pulled-down resistor is 4Ω (Typ.) @ HPOHZ bit = "0".
The HPOUT pin is also pulled down to HPGND via 95 kΩ (Typ.) if HPOHZ bit is set to "1".

Table 28. Headphone Output Status (x: Do not Care)

PMHP bit	HPOHZ bit	HP-Amp Status
0	0	Pull-down by 4Ω (Typ.)
0	1	Pull-down by 95 kΩ (Typ.)
1	x	Normal Operation

To avoid pop noise, HPG[2:0] bits setting should not be changed at power-up and power-down of the headphone amplifier.

The power-up time of headphone amplifier is shown in Table 29. The HPOUT pin outputs 0V (HPGND) after powered up the headphone amplifier. The power-down is executed immediately

Table 29. Headphone Power-Up Time

Sampling Frequency [kHz]	Power-Up Time (Max)
8/12/16/24/32/48/64/96/128/192	23.9 msec
11.025/22.05/44.1/88.2/176.4	25.9 msec

< Over Current Protection Circuit >

If the headphone amplifier is in an overcurrent state, such as when output pin is shorted, the headphone amplifier limits the operation current. The headphone amplifier returns to a normal operation state if all causes are cleared.

9-8. Charge Pump & LDO Circuit

The charge pump circuits are operated by CVDD power supply voltage. CVDD is used to generate positive and negative voltage. The power-up/down sequence of charge pump and LDO circuits are as follows. CP1 should be powered up before LDO1P/N are powered up. CP2 should be powered up after LDO1P/N are powered up.

Power-Up Sequence: CP1 → LDO1P, LDO1N → CP2
Power-Down Sequence: CP2 → LDO1P, LDO1N → CP1

LDO1P and LDO1N have an overcurrent protection circuit. When overcurrent flows in a normal operation, the LDO1P and LDO1N circuits limit the operation current. If the overcurrent state is cleared, the overcurrent protection will be off and the LDO1P and LDO1N circuits will return to normal operation.

LDO2 has an overvoltage protection circuit. This overvoltage protection circuit powers the LDO2 down when the power supply becomes unstable by an instantaneous power failure, etc. during operation. The LDO2 circuit will not return to a normal operation until being reset by the PDN pin ("L" → "H") after removing the problems.

The charge pump and the LDO1 circuits, except for the LDO2, can be powered up again while they are in power-down state.

Table 30. Input/Output Voltage and Operation Block of the Charge Pump

Charge Pump	Power Management bit	Input Voltage	Output Voltage (Typ.)
CP1	PMCP1	CVDD	−1.8 V
CP2 (Class-G)	PMCP2	CVDD	±1.8 V / ±0.9 V

Table 31. Input/Output Voltage and Operation Block of the LDO

LDO	Power Management bit	Power Supply	Output Voltage (Typ.)
LDO1P	PMLDO1P	AVDD / VSS1	1.5 V
LDO1N	PMLDO1N	VSS1 / CP1 Output	−1.5 V
LDO2	-	LVDD / VSS2	1.2 V

9-9. Serial Audio Interface

9-9-1. PCM Mode

The serial audio interface format is set by DIF bit and its data length is controlled by DL[1:0] bits. In case that the input data length is less than the value which set by DL[1:0] bits, unused lower bits are filled with "0". When using master mode, DL[1:0] bits is set in accordance with the setting of BCKO bit. DIF bit and DL[1:0] bits must be set at PMTIM bit = "0".

Table 32. Digital I/F Format Setting

DIF bit	Digital I/F Format	
0	I²S Compatible	(default)
1	MSB justified	

Table 33. Data Length Setting (x: Do not Care, N/A: Not available)

DL1 bit	DL0 bit	Data Length	BCLK Frequency		
			Slave Mode	Master Mode	
0	0	24 bit linear	≥ 48fs	N/A	(default)
0	1	16 bit linear	≥ 32fs	32fs (BCKO bit = "1")	
1	x	32 bit linear	≥ 64fs	64fs (BCKO bit = "0")	

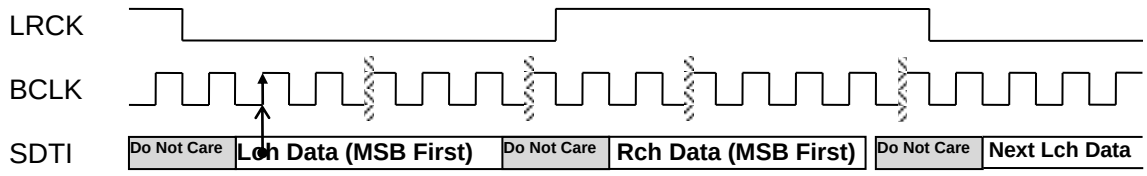


Figure 20. I²S Compatible Format (DIF bit = "0")

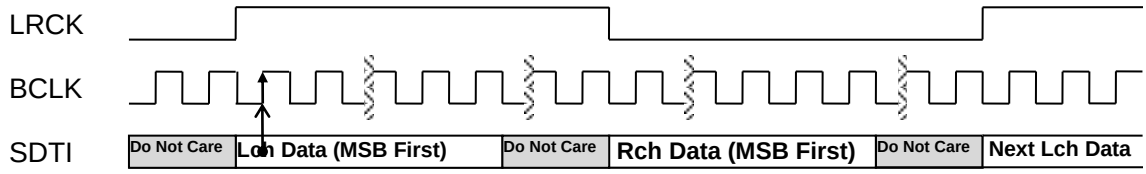


Figure 21. MSB justified format (DIF bit= "1")

9-9-2. Digital Mixing

The AK4332 has digital mixing circuit and signal polarity inversion function for “Lch Data” and “Rch Data” that are input to the SDTI pin in PCM Mode. The inverted data by this polarity inversion is calculated in 2’s complement format.
MDAC, RDAC, LDAC and INV bits must be set at PMDA bit = “0”.

Table 34. DAC Input Signal Selection

MDAC bit	RDAC bit	LDAC bit	DAC Input Data	
0	0	0	MUTE	(default)
0	0	1	Lch Data	
0	1	0	Rch Data	
0	1	1	Lch Data + Rch Data	
1	0	0	MUTE	
1	0	1	Lch Data /2	
1	1	0	Rch Data /2	
1	1	1	(Lch Data + Rch Data)/2	

Table 35. DAC Input Signal Polarity Selection

INV bit	Output Data	
0	Normal	(default)
1	Inverting	

9-9-3. PDM 1-bit Mode

In PDM 1-bit Mode, PDM data must be input to the PDMDI pin in synchronization with PDMCLK.
In this case, DIF bit and DL[1:0] bit settings are invalid.

Polarity of PDMCLK can be inverted by PDMCKR bit.

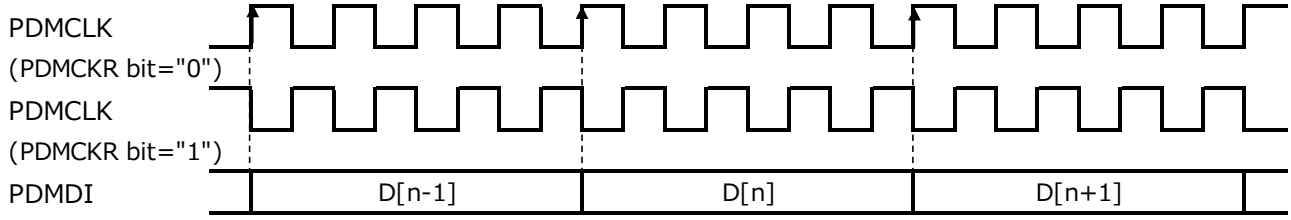


Figure 22. PDM 1-bit Format (PDMMODE bit = “0”)

9-9-4. DSD Mode

In DSD Mode, DSD data must must be input to the PDMDI pin in synchronization with DSDCLK.
In this case, DIF bit and DL[1:0] bit setting are invalid.

Polarity of DSDCLK can be inverted by DCKB bit.

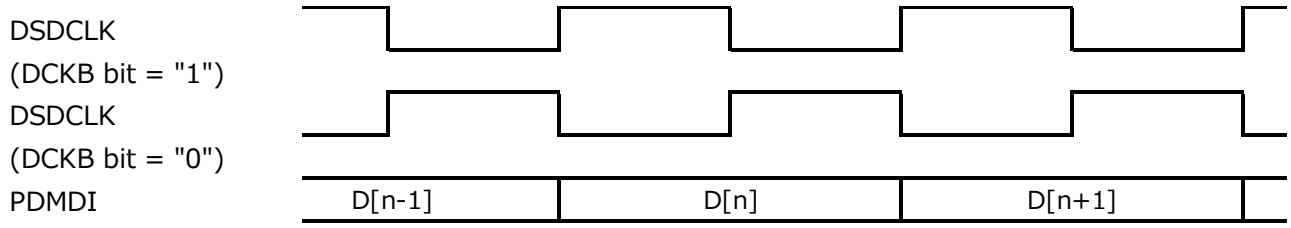


Figure 23. DSD Format (PDMMODE bit = “1”)

9-10. PDM&DSD Signal Full Scale (FS) Detection

The AK4332 has full scale detection function for PDM 1-bit signal and DSD signal. If the data is “0” (–FS) or “1” (+FS) in PDM 1-bit Mode or DSD Mode for 2048 bits (256 word: in case of 1byte = 8bit) times continuously, data full scale is detected and a corresponding FSDET bit becomes “1”. FSDET bit can be read out at the 17H register address (D4).
When the AK4332 detects full scale signal while PDMMUTEEN bit = “0”, the analog output is muted. (Pop noise may occur on a switching timing to the mute state.)
When setting PDMMUTEEN bit = “1”, full scale detection function is available but the analog output will not be muted.

9-11. Serial Control Interface (I²C-bus)

The AK4332 supports the fast-mode I²C-bus (Max: 400 kHz). Pull-up resistors at the SDA and SCL pins must be connected to (LVDD + 0.3) V or less voltage.

1. WRITE Operation

Figure 24 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 30). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010000". (Figure 25). If the slave address matches that of the AK4332, the AK4332 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 31). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4332. The format is MSB first 8 bits (Figure 26)。The data after the second byte contains control data. The format is MSB first, 8 bits (Figure 27). The AK4332 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 30).

The AK4332 can perform more than one byte write operation per sequence at address from 00H to 17H. After receipt of the third byte the AK4332 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 17H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. For the address 26H and 27H, the internal address counter is not incremented automatically.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 32) except for the START and STOP conditions.

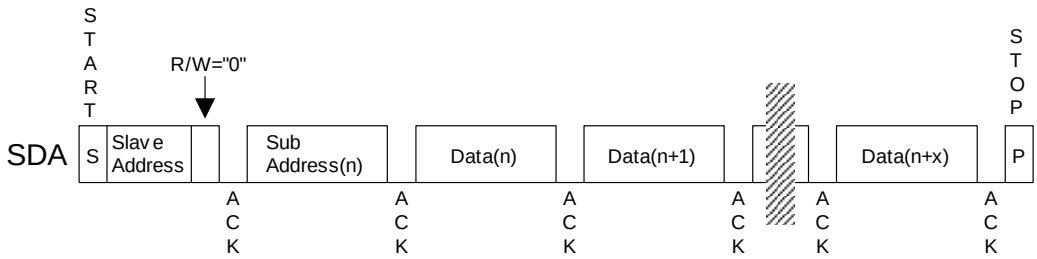


Figure 24. Data Transfer Sequence in I²C-bus Mode

0	0	1	0	0	0	0	R/W

Figure 25. The First Byte

A7	A6	A5	A4	A3	A2	A1	A0

Figure 26. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 27. The Third Byte

2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4332. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 17H prior to generating stop condition, the address counter will “roll over” to 00H and the data of 00H will be read out. For the address 26H and 27H, the internal address counter is not incremented automatically.

The AK4332 supports two basic read operations: Current Address READ and Random Address READ.

2-1. Current Address READ

The AK4332 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next Current READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4332 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4332 ceases the transmission.

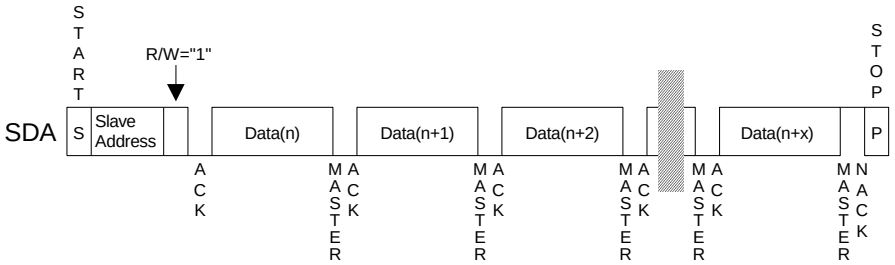


Figure 28. Data Transfer Sequence in I²C-bus Mode

2-2. Random Address READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4332 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4332 ceases the transmission.

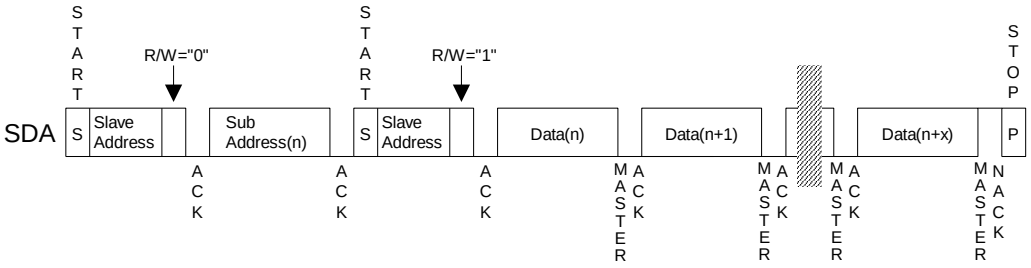


Figure 29. Random Address READ

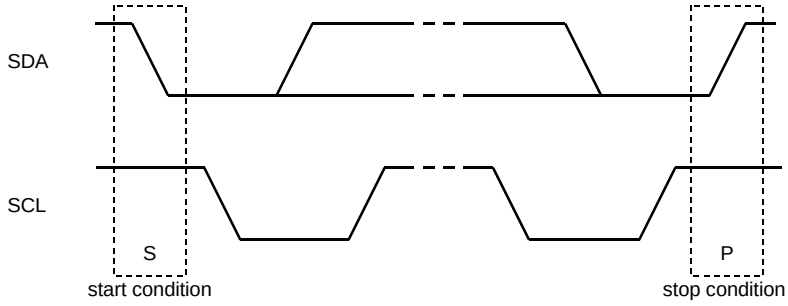


Figure 30. Start Condition and Stop Condition

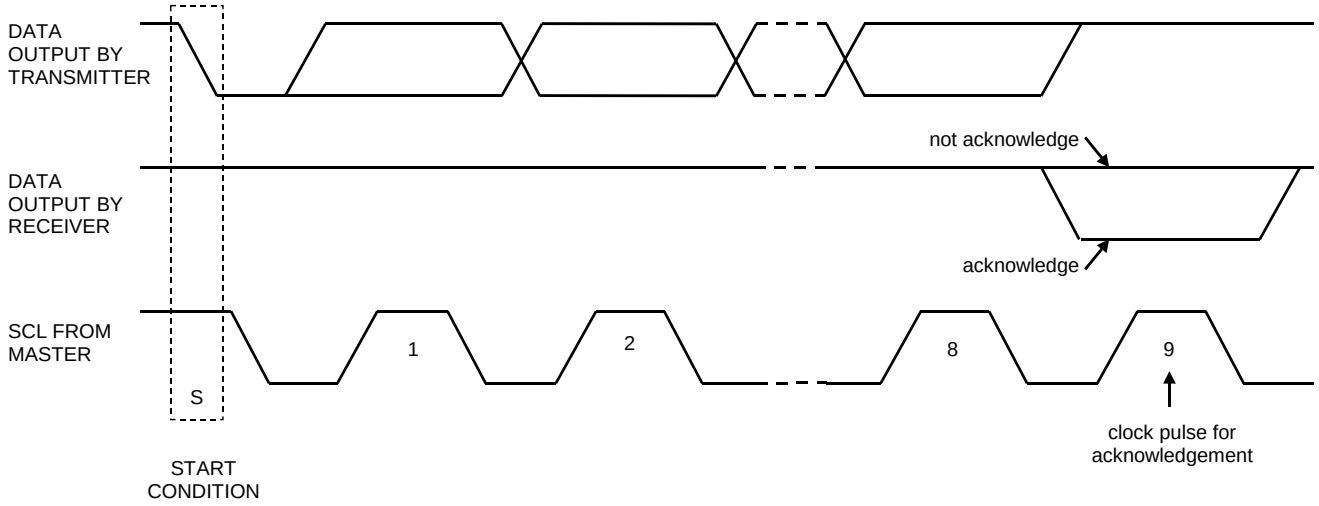


Figure 31. Acknowledge (I^2C-bus)

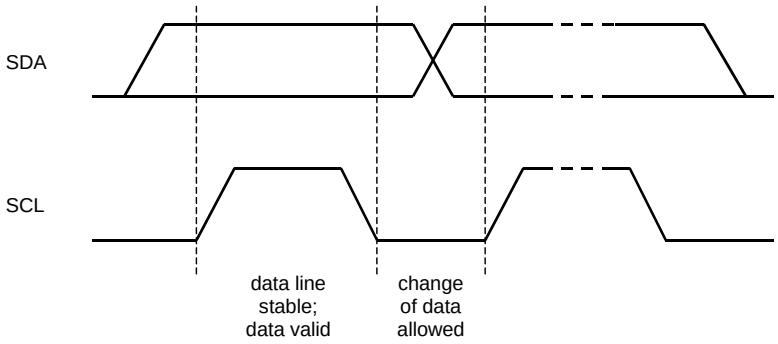


Figure 32. Bit Transfer (I^2C-bus)

9-12. Control Sequence

Figure 33 and Figure 34 show power-up sequence of DAC and headphone amplifier.
Figure 35 shows power-down sequence of headphone amplifier and DAC.

< Power-up Seaquence in PCM Mode>

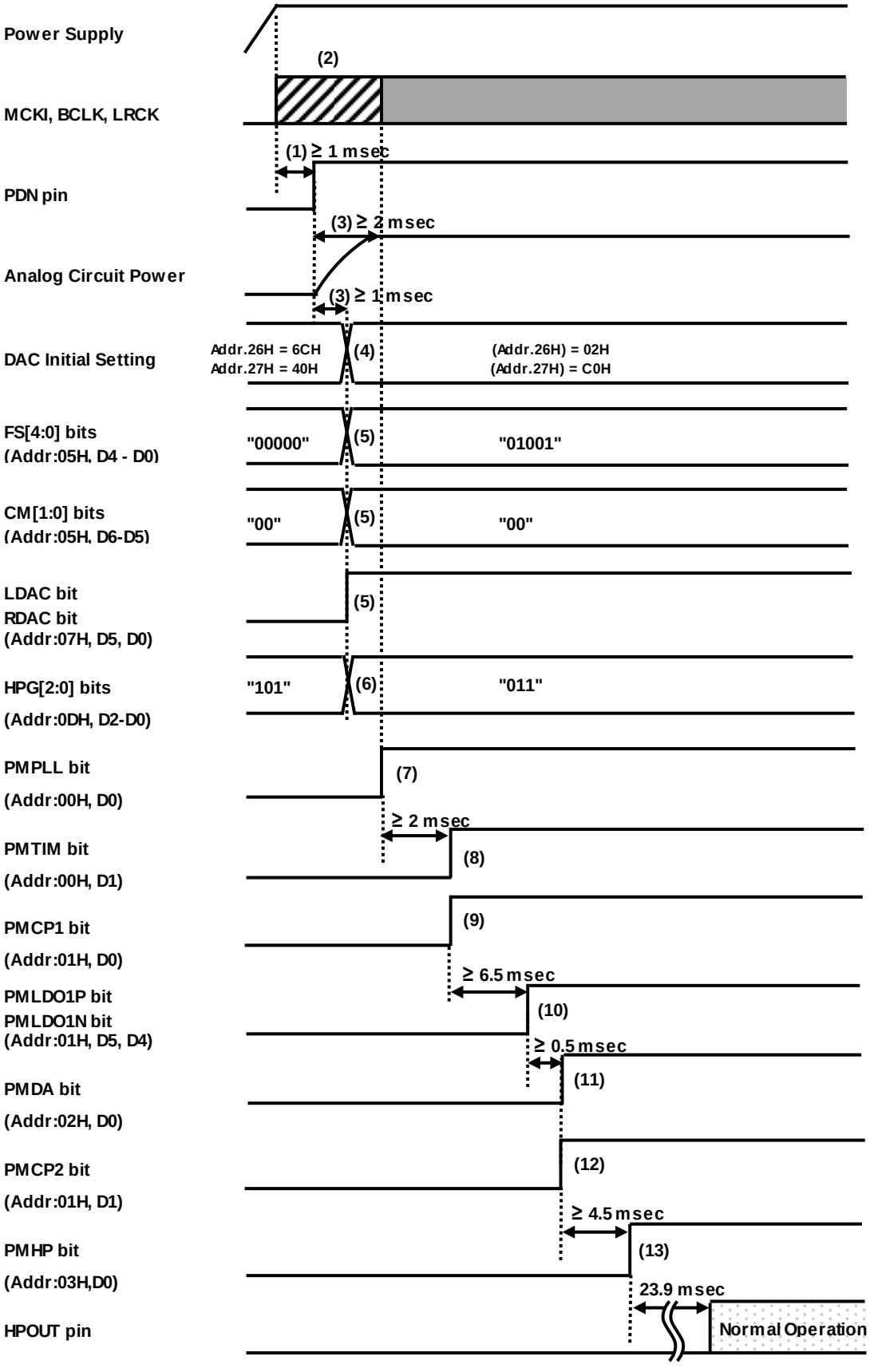


Figure 33. Power-Up Sequence Example of DAC and Headphone Amplifier in PCM Mode

(1) Set the PDN pin from “L” to “H” after turning on all power supplies. In this case, 1 msec or more “L” time is needed for a certain reset.
(2) After all power supplies are On, MCKI, BCLK and LRCK should be input before powering up PLL or CP1.
Refer to Table 3 for Input Clock Setting.
(3) Set the PDN pin = “H” to release the power-down. Register access will be valid in 1 msec at maximum. However, a wait time of 2 msec is needed to access PMTIM bit and power management bits of the analog circuit (PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit and PMHP bit) until the analog circuit is powered up.
(4) Set DAC initial settings. (Write 02H data into Address 26H and write C0H data into Address 27H)
(5) Set sampling frequency (FS[4:0] bits) and the input signal path of the DAC.
(LDAC bit or RDAC bit = “0” → “1”)
(6) Set headphone amplifier volume by HPG[2:0] bits.
(7) In case of using PLL, power-up PLL (PMPLL bit = “0” → “1”) and wait 2 msec for PLL output stabilization.
(8) Start internal master counter. (PMTIM bit = “0” → “1”)
PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit and PMHP bit must be powered up after PMTIM bit = “1”.
(9) Power-up CP1 (PMCP1 bit = “0” → “1”) and wait 6.5 msec (Note 75) for CP1 output voltage stabilization.
(10) Power-up LDO1P and LDO1N (PMLDO1P bit = PMLDO1N bit = “0” → “1”) and wait 0.5 msec (Note 75) for each LDO output voltage stabilization.
(11) Power-up DAC (PMDA bit = “0” → “1”)
(12) Power-up CP2 (PMCP2 bit = “0” → “1”) and wait 4.5 msec (Note 75) for CP2 output voltage stabilization.
(13) Power-up headphone amplifier (PMHP bit = “0” → “1”)
The power-up time of headphone amplifier is 23.9 msec (@ fs = 48 kHz). The HPOUT pin outputs 0 V until the headphone amplifier is powered up.

Note 75. Refer to “8-4. Charge Pump & LDO Circuit Power-Up Time”

< Power-up Seaquence in PDM 1-bit Mode and DSD Mode >

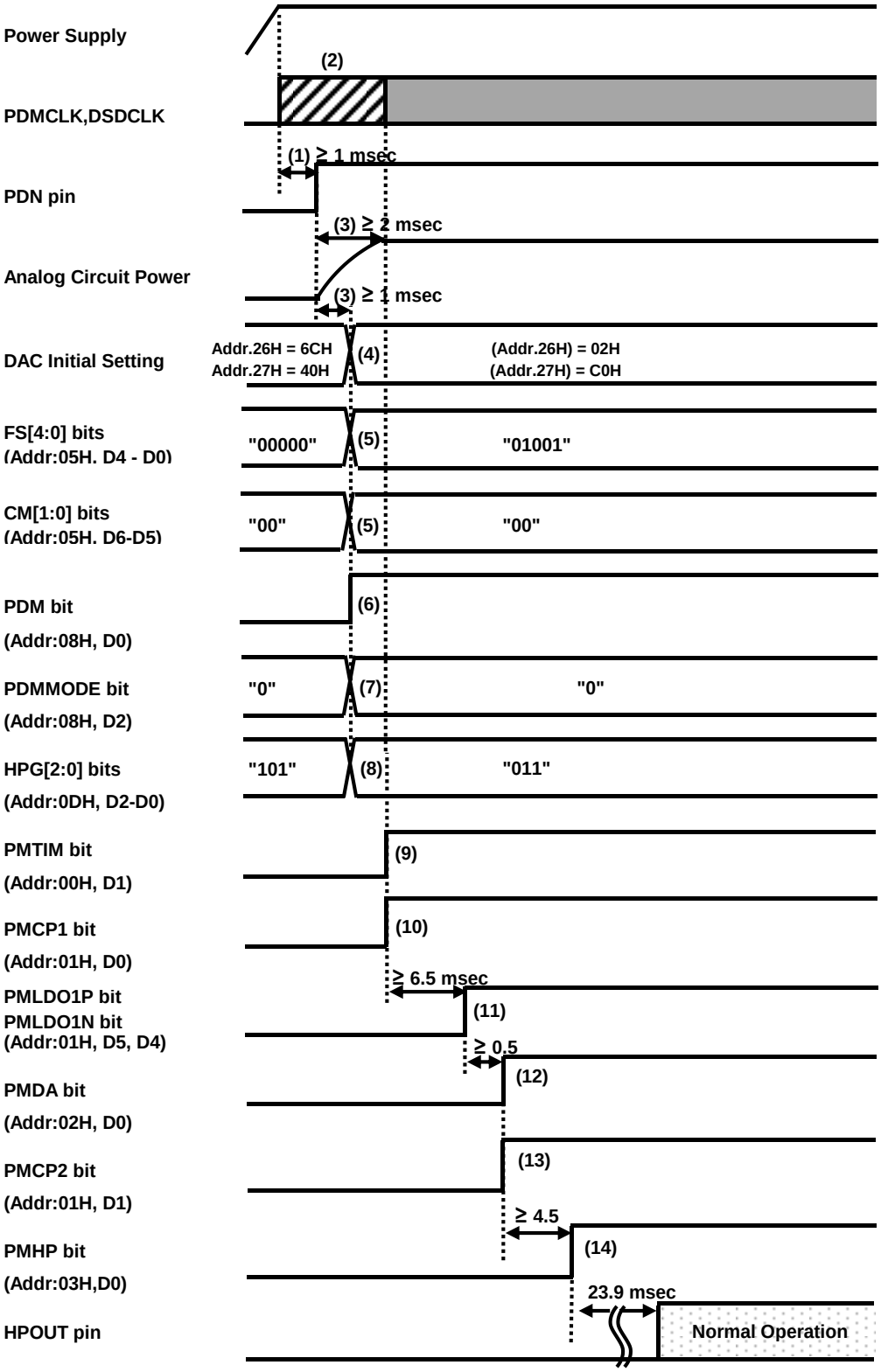


Figure 34. Power-Up Sequence Example of DAC and Headphone Amplifier in PCM 1-bit Mode and DSD Mode

(1) Set the PDN pin from “L” to “H” after turning on all power supplies. In this case, 1 msec or more “L” time is needed for a certain reset.
(2) After all power supplies are On, PDMCLK and DSDCLK should be input before powering up PLL or CP1.
Refer to Table 3 for Input Clock Setting.
(3) Set the PDN pin = “H” to release the power-down. Register access will be valid in 1 msec at maximum. However, a wait time of 2 msec is needed to access PMTIM bit and power management bits of the analog circuit (PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit and PMHP bit) until the analog circuit is powered up.
(4) Set DAC initial settings. (Write 02H data into Address 26H and write C0H data into Address 27H
(5) Set sampling frequency (FS[4:0] bits) and the input signal path of the DAC.
In PDM Mode and DSD Mode, CM[1:0] bits should be set to “00” (256fs) and FS[4:0] bits should be set to “01001” (44.1 kHz) or “01010” (48 kHz).
(6) Set PDM bit to PDM 1-bit Mode or DSD Mode.(PDM bit = “0” → “1”)
(7) Select the PDM 1-bit Mode or DSD Mode by PDMMODE bit.
(8) Set headphone amplifier volume by HPG[2:0] bits.
(9) Start internal master counter. (PMTIM bit = “0” → “1”)
PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit and PMHP bit must be powered up after PMTIM bit = “1”.
(10) Power-up CP1 (PMCP1 bit = “0” → “1”) and wait 6.5 msec (Note 75) for CP1 output voltage stabilization.
(11) Power-up LDO1P and LDO1N (PMLDO1P bit = PMLDO1N bit = “0” → “1”) and wait 0.5 msec (Note 75) for each LDO output voltage stabilization.
(12) Power-up DAC (PMDA bit = “0” → “1”)
(13) Power-up CP2 (PMCP2 bit = “0” → “1”) and wait 4.5 msec (Note 75) for CP2 output voltage stabilization.
(14) Power-up headphone amplifier (PMHP bit = “0” → “1”)
The power-up time of headphone amplifier is 23.9 msec (@ fs = 48 kHz). The HPOUT pin outputs 0 V until the headphone amplifier is powered up.

< Power-Down Sequence Example >

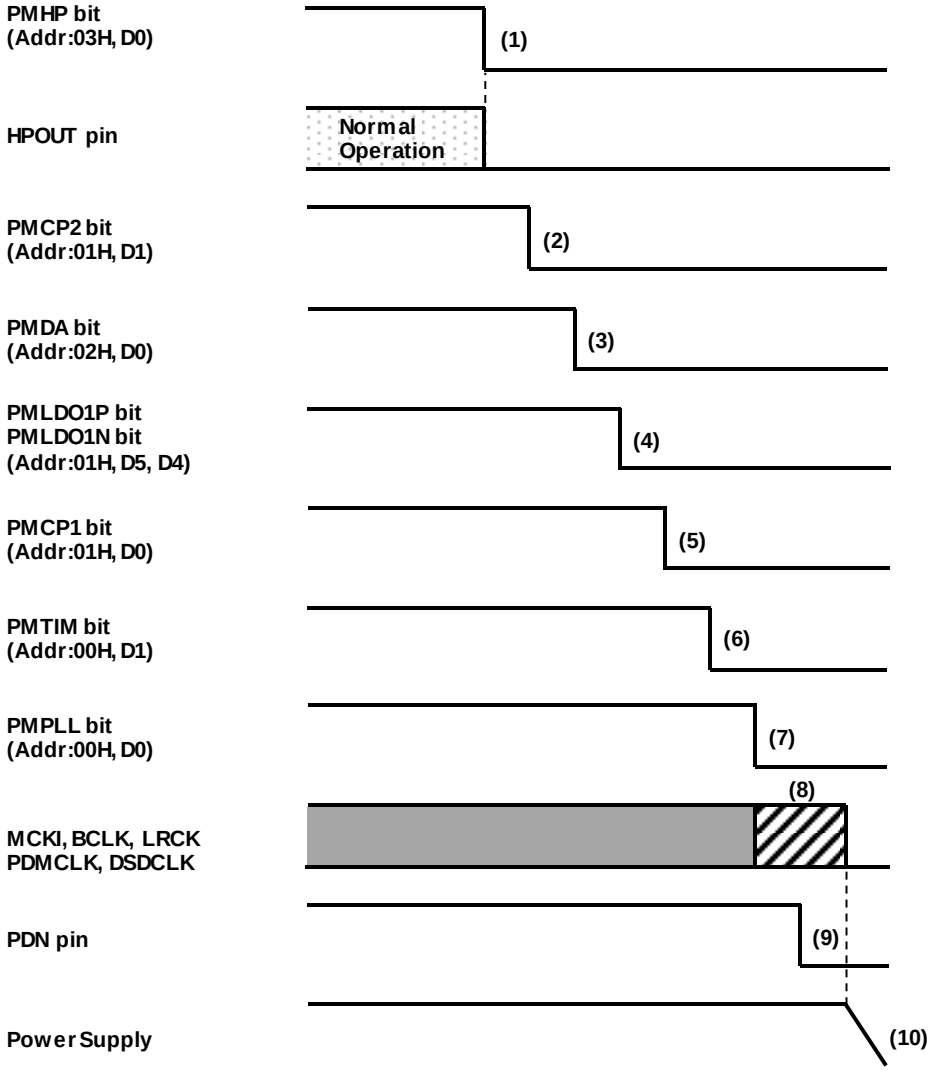


Figure 35. Power-Down Sequence Example of Headphone Amplifier and DAC

(1) Power-down headphone amplifier (PMHP bit = “1” → “0”)
When the headphone amplifier is powered down, the HPOUT pin is pulled down to HPGND via the internal pull-down register.
(2) Power-down CP2 (PMCP2 bit = “1” → “0”)
(3) Power-down DAC (PMDA bit = “1” → “0”)
(4) Power-down LDO1P, LDO1N (PMLDO1P bit = PMLDO1N bit = “1” → “0”)
(5) Power-down CP1 (PMCP1 bit = “1” → “0”)
(6) Stop internal master counter. (PMTIM bit = “1” → “0”)
PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit and PMHP bit must be powered off before PMTIM bit = “0”.
(7) In case of using PLL, power-down PLL. (PMPLL bit = “1” → “0”)
(8) Stop MCKI, BCLK, LRCK, PCMCLK and DSDCLK before turning off each of power supplies.
(9) Set the PDN pin from “H” to “L”.
(10) Turn off each of power supplies.

9-13. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	0	0	0	0	PMTIM	PMPLL
01H	Power Management 2	0	0	PMLDO1N	PMLDO1P	0	0	PMCP2	PMCP1
02H	Power Management 3	0	0	0	0	0	0	0	PMDA
03H	Power Management 4	0	LVDTM[2:0]			CPMODE[1:0]		0	PMHP
04H	Output Mode Setting	LVDSEL[1:0]		VDDTM[3:0]				0	HPOHZ
05H	Clock Mode Selection	0	CM[1:0]		FS[4:0]				
06H	Digital Filter Selection	DASD	DASL	0	0	0	0	0	0
07H	DAC Mono Mixing	0	0	0	0	INV	MDAC	RDAC	LDAC
08H	PDM I/F Control	0	PDMCKR	DCKB	PDM MUTEN	0	PDM MODE	0	PDM
09H	Reserved	0	0	0	0	0	0	0	0
0AH	Reserved	0	0	0	0	0	0	0	0
0BH	DAC Output Volume	0	0	0	OVC[4:0]				
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	HP Volume Control	HPTM[2:0]			0	0	HPG[2:0]		
0EH	PLL CLK Source Selection	0	0	0	PLLMD	0	0	0	PLS
0FH	PLL Ref CLK Divider 1	PLD[15:8]							
10H	PLL Ref CLK Divider 2	PLD[7:0]							
11H	PLL FB CLK Divider 1	PLM[15:8]							
12H	PLL FB CLK Divider 2	PLM[7:0]							
13H	DAC CLK Source	0	0	0	0	0	0	0	DACCKS
14H	DAC CLK Divider	0	0	0	0	MDIV[3:0]			
15H	Audio I/F Format	DEVICEID[2:0]			MS	BCKO	DIF	DL[1:0]	
16H	Reserved	0	0	0	0	0	0	0	0
17H	PDMERR	0	0	0	FSDET	0	0	0	0
26H	DAC Adjustment 1	T8	T7	T6	T5	T4	T3	T2	T1
27H	DAC Adjustment 2	T16	T15	T14	T13	T12	T11	T10	T9

Note 76. PDN pin = “L” resets the registers to their default values.
Note 77. The bits defined as “0” must contain a “0” value.
Note 78. Writing access to 18H to 25H, 28H to FFH is prohibited.

9-14. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	0	0	0	0	PMTIM	PMPLL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: Power-Down (default)
1: Power-Up

PMTIM: Synchronization Control Power Management
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	PMLDO1N	PMLDO1P	0	0	PMCP2	PMCP1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMCP1: Charge Pump 1 Power Management
0: Power-Down (default)
1: Power-Up

PMCP2: Charge Pump 2 Power Management
0: Power-Down (default)
1: Power-Up

PMLDO1P: LDO1P Power Management
0: Power-Down (default)
1: Power-Up

PMLDO1N: LDO1N Power Management
0: Power-Down (default)
1: Power-Up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management 3	0	0	0	0	0	0	0	PMDA
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMDA: DAC Power Management
0: Power-Down (default)
1: Power-Up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Power Management 4	0	LVDTM[2:0]			CPMODE[1:0]		0	PMHP
R/W		R/W	R/W			R/W		R/W	R/W
Default		0	000			00		0	0

PMHP: Headphone Amplifier Power Management
0: Power-Down (default)
1: Power-Up

CPMODE[1:0]: Charge Pump Mode Control (Table 21)
Default: “00” (Automatic Switching Mode)

LVDTM[2:0]: Class-G 1/2VDD Mode Detection Time Setting (Table 25)
Default: “000” (64/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Output Mode Setting	LVDSEL[1:0]		VDDTM[3:0]				0	HPOHZ
R/W		R/W		R/W				R/W	R/W
Default		00		0000				0	0

HPOHZ: GND Switch Setting for Headphone Amplifier Output
0: Pull-Down by 4Ω (Typ.) (default)
1: Pull-Down by 95kΩ (Typ.)

VDDTM[3-0]: Class-G VDD Hold Time Setting (Table 24)
Default: “0000” (1024/fs)

LVDSEL[1:0]: Switching Threshold between VDD Mode and 1/2VDD Mode of CP2 (Table 22)
Default: “00” (Load Resistance = 16Ω)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Clock Mode Selection	0	CM[1:0]		FS[4:0]				
R/W		R/W	R/W		R/W				
Default		0	00		00000				

FS[4:0]: Sampling Frequency Setting (Table 7)
Default: “00000” (fs=8kHz)

CM[1:0]: Master Clock Frequency Setting (Table 6)
Default: “00” (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Digital Filter Selection	DASD	DASL	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DASD, DASL: DAC Digital Filter Mode Setting (Table 19)
Default: “0”, “0” (Sharp Roll-Off Filter)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC Mono Mixing	0	0	0	0	INV	MDAC	RDAC	LDAC
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MDAC, RDAC, LDAC: DAC Channel Input Signal Selection (Table 34)
Default: “000” (MUTE)

INV: DAC Input Signal Polarity Selection
0: Normal (default)
1: Inverting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	PDM I/F Control	0	PDMCKR	DCKB	PDM MUTEN	0	PDM MODE	0	PDM
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PDM: Audio Interface Selection (Table 2)
0: PCM Mode (default)
1: PDM 1-bit Mode or DSD Mode

PDMMODE: PDM Mode Selection (Table 8)
0: PDM 1-bit Mode (default)
1: DSD Mode

PDMMUTEN: PDM Data / DSD Data Output Mute Function
0: Enable (default)
1: Disable

DCKB: Polarity of DSDCLK
0: DSD Data is output on a DSDCLK falling edge. (default)
1: DSD Data is output on a DSDCLK rising edge.

PDMCKR: Polarity of PDMCLK
0: PDM Data is output on a PDMCLK rising edge. (default)
1: PDM Data is output on a PDMCLK falling edge.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H 0AH	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Output Volume	0	0	0	OVC[4:0]				
R/W		R/W	R/W	R/W	R/W				
Default		0	0	0	11001				

OVC[4:0]: DAC Digital Volume Control; +3 dB to −12 dB & Mute, 0.5 dB step (Table 20)
Default: 19H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	HP Volume Control	HPTM[2:0]			0	0	HPG[2:0]		
R/W		R/W			R/W	R/W	R/W		
Default		011			0	0	101		

HPG[2:0]: Headphone Amplifier Analog Volume Control; +4 dB to −10 dB, 2 dB step (Table 26)
Default: “101” (0dB)

HPTM[2:0]: Zero Cross Time Output Period Setting for Analog Volume of Headphone Amplifier (Table 27)
Default: “011” (1024/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	PLL CLK Source Selection	0	0	0	PLLMD	0	0	0	PLS
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PLS: PLL Clock Source Selection (Table 12)
Default: “0” (MCKI)

PLLMD: PLL Mode Setting
Default: “0”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	PLL Ref CLK Divider 1	PLD[15:8]							
10H	PLL Ref CLK Divider 2	PLD[7:0]							
R/W		R/W							
Default		0000H							

PLD[15:0]: PLL Reference Clock Divider Setting (Table 13)
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	PLL FB CLK Divider 1	PLM[15:8]							
12H	PLL FB CLK Divider 2	PLM[7:0]							
R/W		R/W							
Default		0000H							

PLM[15:0]: PLL Feedback Clock Divider Setting (Table 14)
Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	DAC CLK Source	0	0	0	0	0	0	0	DACCKS
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACCKS: DAC Clock Source Selection (Table 4)
Default: “0” (MCKI)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	DAC CLK Divider	0	0	0	0	MDIV[3:0]			
R/W		R/W	R/W	R/W	R/W	R/W			
Default		0	0	0	0	0000			

MDIV[7:0]: MCKI Divider Setting (Table 16)
Default: “0000” (Divided by 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	CODEC I/F Format	DEVICEID[2:0]			MS	BCKO	DIF	DL[1:0]	
R/W		R			R/W	R/W	R/W	R/W	
Default		000			0	0	0	00	

DL[1:0]: Data Length Setting (Table 33)
Default: “00” (24 bit linear)

DIF: Digital I/F Format Setting (Table 32)
Default: “0” (I^2S Compatible)

BCKO: BCLK Output Frequency
0: 64fs (Default)
1: 32fs

MS: Master / Slave Mode Setting (Table 2)
Default: “0” (Slave Mode)

DEVICEID[2:0]: Device ID
Default: “000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	PDMERR	0	0	0	FSDET	0	0	0	0
R/W		R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FSDET: PDM Data or DSD Data Full Scale Detect
0: Not Full Scale Data (Default)
1: Full Scale Data

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	DAC Adjustment 1	T8	T7	T6	T5	T4	T3	T2	T1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	1	1	0	0

* 02H data must be written to DAC Adjustment 1 (Addr. 26H) before analog blocks (CP1, CP2, LDO1, DAC, headphone amplifier and PLL) are powered up.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	DAC Adjustment 2	T16	T15	T14	T13	T12	T11	T10	T9
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	0	0	0

* C0H data must be written to DAC Adjustment 2 (Addr. 27H) before analog blocks (CP1, CP2, LDO1, DAC, headphone amplifier and PLL) are powered up.

10. Recommended External Circuits

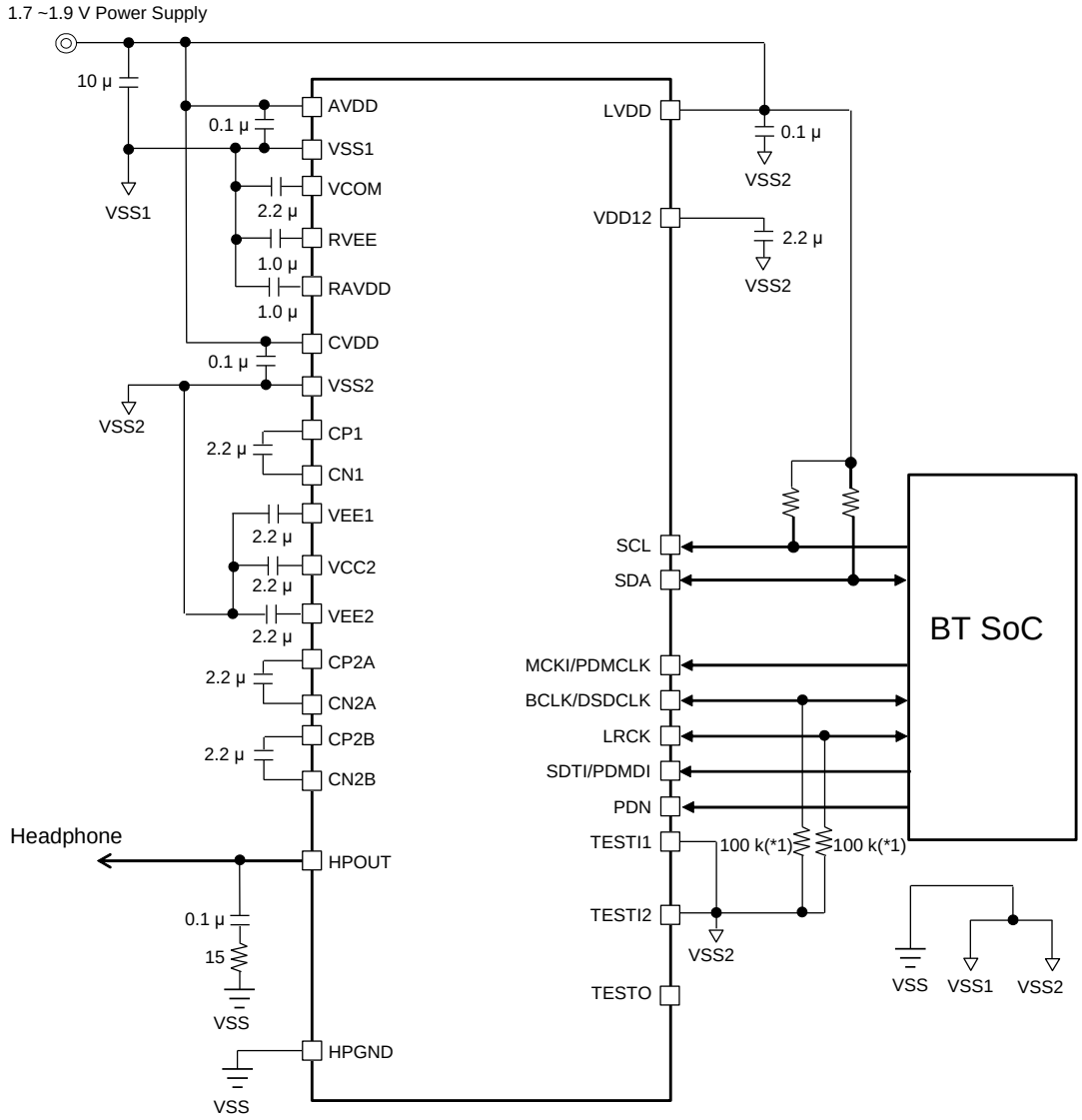


Figure 36. System Connection Diagram

*1: When the AK4332 is in master mode, a pull-down resistor (e.g. 100 kΩ) is needed.

1. Grounding and Power Supply Decoupling

The AK4332 requires careful attention to power supply and grounding arrangements. The PDN pin should be held “L” when power supplies are tuning on. AVDD should be powered up before or at the same time of CVDD. Power-up sequence of LVDD is not critical. The PDN pin is allowed to be “H” after all power supplies are applied and settled. To power down the AK4332, set the PDN pin to “L” and power down CVDD before or at the same time of AVDD. Power-down sequence of LVDD is not critical.

To avoid pop noise on analog output when power-up/down, the AK4332 should be operated along the following recommended power-up/down sequence.

1) Power-up
   - The PDN pin should be held “L” when power supplies are turning on. The AK4332 can be reset by keeping the PDN pin “L” for 1 msec or longer after all power supplies are applied and settled. Then release the reset by setting the PDN pin to “H”.

2) Power-down
   - Each of power supplies can be powered OFF after the PDN pin is set to “L”.

VSS1 and VSS2 of the AK4332 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2 µF ceramic capacitor attached between the VCOM pin eliminates the effects of high frequency noise. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4332.

3. Charge Pump and LDO Circuits

Capacitors for CP1 block (connected between the CP1 pin and the CN1 pin, between the VEE1 pin and the VSS2 pin) and for CP2 block (connected between the CP2A pin and the CN2A pin, between the CP2B pin and the CN2B pin, between the VCC2 pin and the VSS2 pin, between the VEE2 pin and the VSS2 pin) should be low ESR 2.2 µF ±50%.
Capacitors for LDO1P block (connected between the RAVDD pin and the VSS1 pin) and for LDO1N block (connected between the RVEE pin and the VSS1 pin) should be low ESR from 1.0 µF ±50% to 4.7 µF ±50%.
These capacitors must be connected as close as possible to the pins. No load current may be drawn from the Positive / Negative Power Output pin (VEE1, RAVDD, RVEE, VCC2 and VEE2 pins).

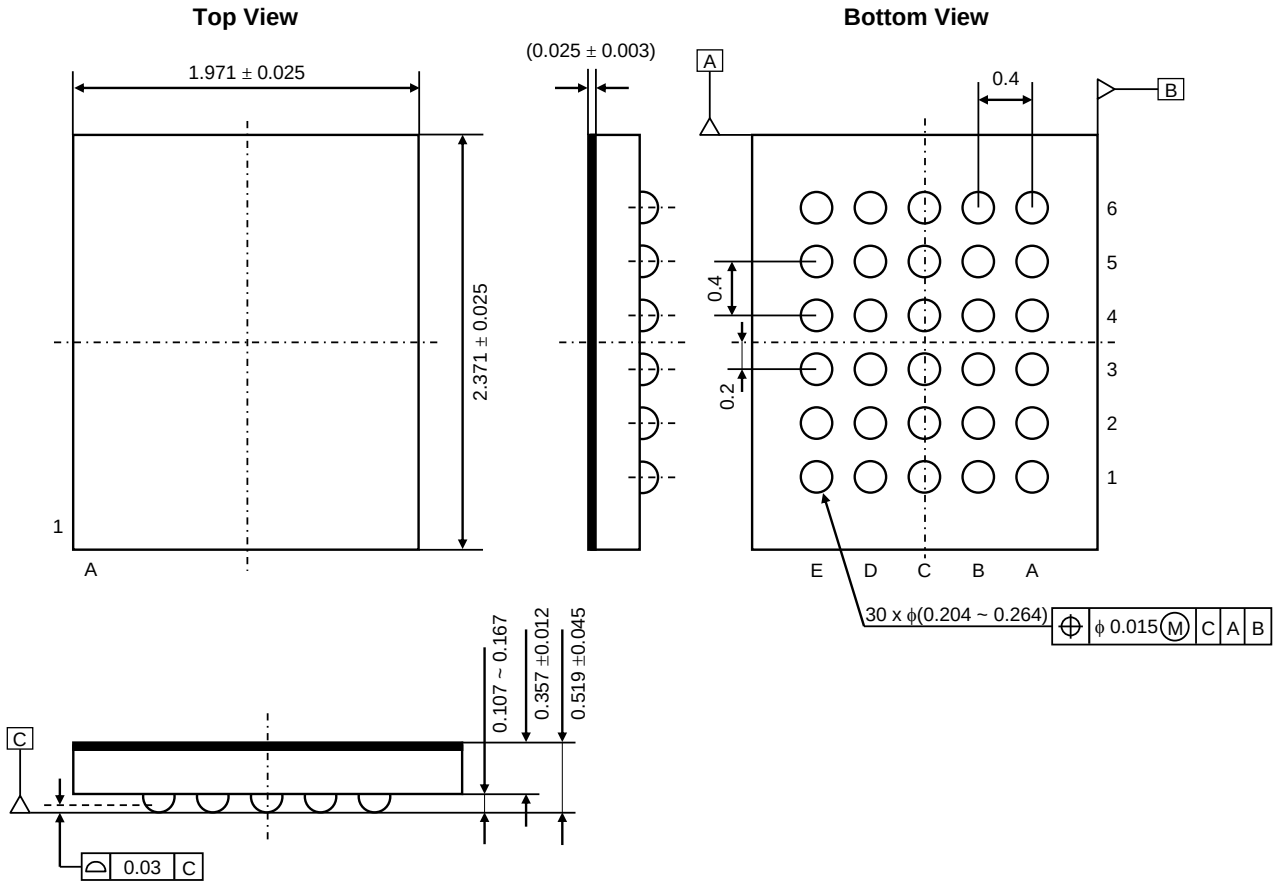
4. Analog Outputs

Headphone outputs are single-ended and centered at HPGND (0 V). They should be directly connected to a headphone without AC coupling.

11. Package

11-1. Outline Dimensions

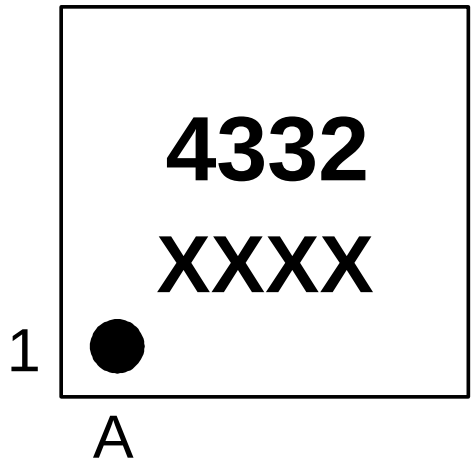
30-pin CSP (Unit: mm)



11-2. Material and Lead Finish

Package molding compound: Epoxy Resign, Halogen Free
Solder ball material: SnAgCu

11-3. Marking



XXXX: Date code (4 digits)
Pin #A1 indication

12. Ordering Guide

AK4332ECB	−40 to +85°C	30-pin CSP (0.4 mm pitch)
AKD4332	Evaluation board for AK4332	

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
19/04/10	00	First Edition		

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