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AK4619

192 kHz 4-ch Audio CODEC

1. General Description

The AK4619 is a 192 kHz audio codec. Its 4-channel, 24-bit ADC supports an analog gain amplifier. On the output side, the AK4619's 4-channel, 32-bit DAC supports single-ended analog output.
Pairing the AK4619 with one of AKM's automotive multi-core DSPs enables processing of both audio and voice, as required for modern car audio systems.
The AK4619 supports ambient temperatures from −40° C to 105° C and is available in a space-saving 32-pin QFN package, making it a perfect fit for automotive head units and amplifiers.

2. Features

4ch ADC: 24-bit ADC with MIC Gain Amplifiers
- Sampling Frequency: fs = 8 kHz to 192 kHz
- Channel-Independent MIC Gain Amplifiers: −6 to +27 dB, 3 dB Step
- Supports differential, single-ended, or pseudo-differential inputs
- ADC Characteristics S/N: 106 dB (fs = 48 kHz, Differential-Input, Gain = 0 dB,)
- Channel-Independent Digital Volume Control (+24 to −103 dB, 0.5 dB step, Mute)
- Digital HPF for DC Offset Cancellation
- 5 types of Digital Filter for Sound Color and Voice Selection

4ch DAC: Advanced 32-bit DAC
- Sampling Frequency: fs = 8 to 192 kHz
- Single-ended Output
- DAC Characteristics S/N: 108 dB (fs = 48 kHz)
- Channel Independent Digital Volume Control (+12 to −115 dB, 0.5 dB Step, Mute)
- 4 types of Digital Filter for Sound Color Selection

Digital Audio Interface:
- Slave operation
- Interface Data Format
  32 / 24 /20 / 16-bit I^2S/MSB justified, PCM Short/Long Frame
- 4-ch TDM Format Supported

Digital loop back path:
- Two 4:1 multiplexers (MUX)

Control Interface: SPI (7 MHz max), I^2C-bus (max 400 kHz, Fast Mode)
Power Supply:
- AVDD (Analog): 3.0 to 3.6 V (typ. 3.3 V)
- TVDD (Digital I/F, LDO): 1.7 to 3.6 V (typ. 3.3 V)

Operating Temperature Range: Ta = −40 to 105°C
Package: 32-pin QFN (5mm × 5mm, 0.5mm pitch)

3. Table of Contents

4. Block Diagram and Functions

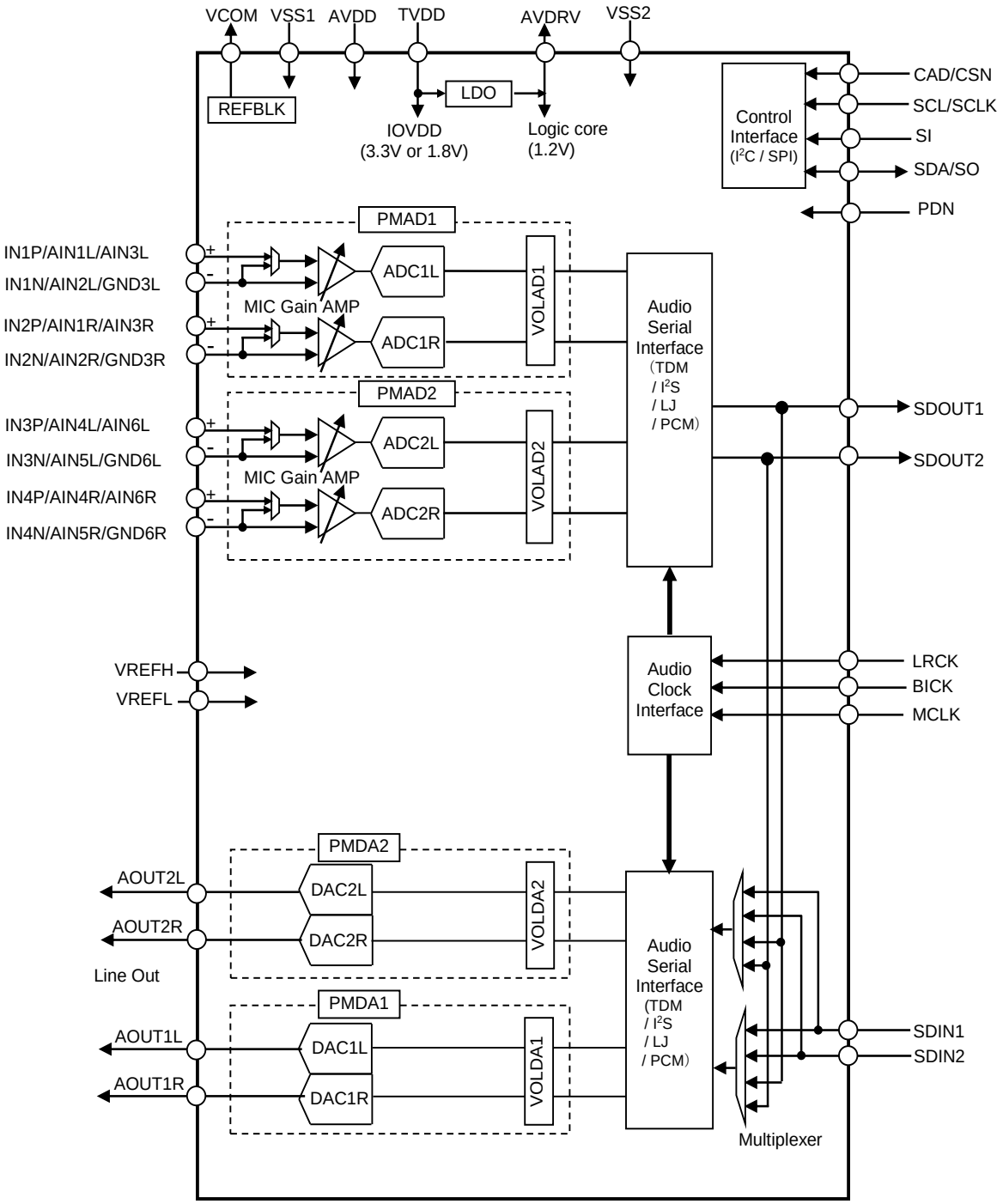


Figure 1. AK4619 Block Diagram

Block Function

Block	Function
REFBLK	Generate the internal reference voltage for analog block
LDO	Generate power for internal digital circuit (1.2 V typ.).
Control Interface	The interface for register access via I^2C bus or SPI.
MIC Gain AMP	Amplification for analog input signal.
ADC1/2	24-bit Analog to Digital converter
DAC1/2	32-bit Digital to Analog converter
VOLAD1,2 VOLDA1,2	Digital Volume for ADC and DAC
Multiplexer	Serial Data Multiplexers (4 : 1 multiplexers)
Audio Clock Interface	Clock interface for ADC and DAC
Audio Serial Interface	Serial data interface for ADC and DAC

5. Pin Configurations and Functions

5.1. Pin Configurations

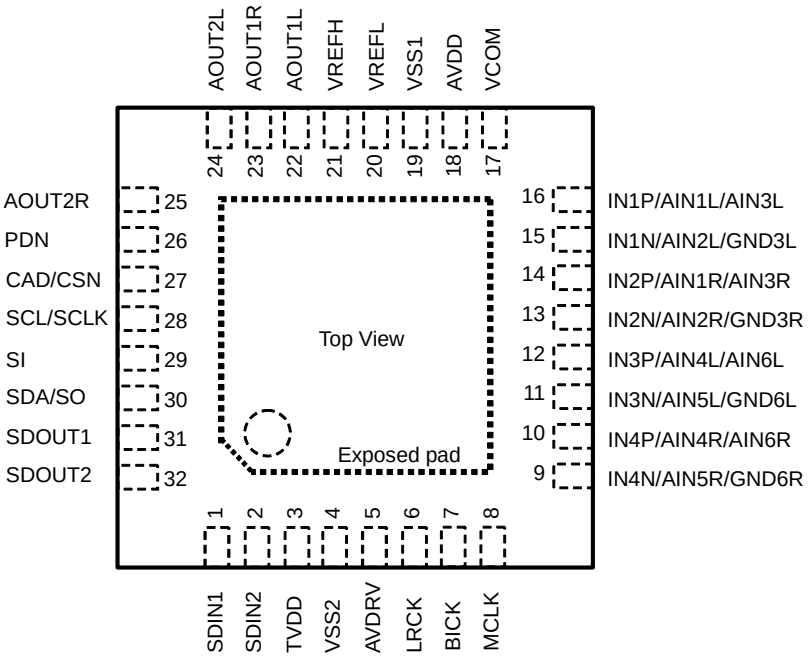


Figure 2. Pin Configuration

5.2. Pin Functions

No.	Pin Name	I/O	Function	Power Down State (PDN pin = "L")
1	SDIN1	I	Audio Serial Data Input 1 Pin	Hi-Z
2	SDIN2	I	Audio Serial Data Input 2 Pin	Hi-Z
3	TVDD	-	Digital I/F & LDO Power Supply Pin, 1.7 to 3.6V	-
4	VSS2	-	Digital Ground Pin	-
5	AVDRV	O	LDO (1.2 V) Output Pin This pin should be connected to VSS2 pin through a 2.2 µF (±50 %) capacitor in series. This pin must not be connected to any other devices.	Pull-down (500Ω)
6	LRCK	I	Audio Serial Frame Sync Clock Pin	Hi-Z
7	BICK	I	Audio Serial Data Clock Pin	Hi-Z
8	MCLK	I	External Master Clock Input Pin	Hi-Z
9	IN4N	I	Negative Analog Input 4 Pin	Hi-Z
	AIN5R	I	Single-ended Rch Analog Input 5 Pin	
	GND6R	I	Pseudo-differential Rch Ground Input 6 Pin	
10	IN4P	I	Positive Analog Input 4 Pin	Hi-Z
	AIN4R	I	Single-ended Rch Analog Input 4 Pin	
	AIN6R	I	Pseudo-differential Rch Analog Input 6 Pin	
11	IN3N	I	Negative Analog Input 3 Pin	Hi-Z
	AIN5L	I	Single-ended Lch Analog Input 5 Pin	
	GND6L	I	Pseudo-differential Lch Ground Input 6 Pin	
12	IN3P	I	Positive Analog Input 3 Pin	Hi-Z
	AIN4L	I	Single-ended Lch Analog Input 4 Pin	
	AIN6L	I	Pseudo-differential Lch Analog Input 6 Pin	
13	IN2N	I	Negative Analog Input 2 Pin	Hi-Z
	AIN2R	I	Single-ended Rch Analog Input 2 Pin	
	GND3R	I	Pseudo-differential Rch Ground Input 3 Pin	
14	IN2P	I	Positive Analog Input 2 Pin	Hi-Z
	AIN1R	I	Single-ended Rch Analog Input 1 Pin	
	AIN3R	I	Pseudo-differential Rch Analog Input 3 Pin	
15	IN1N	I	Negative Analog Input 1 Pin	Hi-Z
	AIN2L	I	Single-ended Lch Analog Input 2 Pin	
	GND3L	I	Pseudo-differential Lch Ground Input 3 Pin	
16	IN1P	I	Positive Analog Input 1 Pin	Hi-Z
	AIN1L	I	Single-ended Lch Analog Input 1 Pin	
	AIN3L	I	Pseudo-differential Lch Analog Input 3 Pin	

No.	Pin Name	I/O	Function	Power Down State (PDN pin = "L")
17	VCOM	O	Common Voltage Output Pin (1/2 × AVDD) This pin should be connected to VSS1 pin through a 2.2 µF (±50 %) ceramic capacitor in series. This pin must not be connected to other devices.	Pull-down (500Ω)
18	AVDD	-	Analog Power Supply Pin, 3.0 to 3.6V	-
19	VSS1	-	Analog Ground Pin	-
20	VREFL	I	Low Level Voltage Reference Input Pin, VREFL must be connected externally to VSS1	Hi-Z
21	VREFH	I	High Level Voltage Reference Input Pin, VREFH must be connected externally to AVDD	Hi-Z
22	AOUT1L	O	DAC1 Lch Analog Output Pin	Hi-Z
23	AOUT1R	O	DAC1 Rch Analog Output Pin	Hi-Z
24	AOUT2L	O	DAC2 Lch Analog Output Pin	Hi-Z
25	AOUT2R	O	DAC2 Rch Analog Output Pin	Hi-Z
26	PDN	I	Power down Pin "L": Power-down, "H": Power-Up	Hi-Z (Low)
27	CAD	I	I^2C Chip Address Pin	Hi-Z
	CSN	I	Chip Select Pin for SPI Interface	
28	SCL	I	I^2C Serial Data Clock Pin	Hi-Z
	SCLK	I	Serial Clock Input Pin for SPI Interface	
29	SI	I	Serial Data Input Pin for SPI Interface	Hi-Z
30	SDA	I/O	I^2C Serial Data Input/output Pin	Hi-Z
	SO	O	Serial Data Output Pin for SPI Interface	
31	SDOUT1	O	Audio Serial Data Output 1 Pin	Pull-down (50kΩ)
32	SDOUT2	O	Audio Serial Data Output 2 Pin	Pull-down (50kΩ)
-	Exposed Pad		The exposed pad on the bottom surface of the package must be open or connected to VSS1. It is recommended that the Exposed Pad be connected to VSS1.	-

Notes
*1. Do not connect a load to the AVDRV pin and VCOM pin.

5.3. Handling of Unused Pins

Unused I/O pins must be connected appropriately:

Classification	Pin Name	Setting
Analog	IN1P/AIN1L/AIN3L, IN1N/AIN2L/GND3L, IN2P/AIN1R/AIN3R, IN2N/AIN2R/GND3R IN3P/AIN4L/AIN6L, IN3N/AIN5L/GND6L, IN4P/AIN4R/AIN6R, IN4N/AIN5R/GND6R AOUT1L, AOUT1R, AOUT2L, AOUT2R	Open
Digital	SDOUT1, SDOUT2	Open
	SDIN1, SDIN2, SI	Connect to VSS2

6. Absolute Maximum Ratings

(VSS1 = VSS2 = 0 V; *2, *3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	−0.3	4.3	V
	Digital I/F & LDO	TVDD	−0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage *4		VINA	−0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage *5		VIND	−0.3	(TVDD+0.3) or 4.3	V
Ambient Temperature (powered applied) When Exposed Pad is connected to VSS1.		Ta	−40	105	°C
Ambient Temperature (powered applied) When Exposed Pad is open.		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Notes

*2. All voltages are with respect to ground.

*3. VSS1 and VSS2 must be connected to the same analog ground plane.

*4. IN1P/AIN1L/AIN3L, IN1N/AIN2L/GND3L, IN2P/AIN1R/AIN3R, IN2N/AIN2R/GND3R, IN3P/AIN4L/AIN6L, IN3N/AIN5L/GND6L, IN4P/AIN4R/AIN6R, IN4N/AIN5R/GND6R pins
The maximum input voltage on analog input pins is the lower of (AVDD+0.3) V and 4.3 V.

*5. MCLK, BICK, LRCK, SDIN1, SDIN2, CAD/CSN, SCL/SCLK, SI, SDA/SO, PDN pins.
The maximum input voltage on digital input pins is the lower of (TVDD+0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = 0 V;*6)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies *7	Analog	AVDD	3.0	3.3	3.6	V
	Digital I/F & LDO	TVDD	1.7	3.3	3.6	V

Notes

*6. All voltages are with respect to ground.

*7. The power-up sequence between AVDD and TVDD is not critical. The PDN pin should be held “L” while the power supplies ramp up. The PDN pin can be released to “H” after all power supplies have ramped and settled.

*8. Do not turn off the power supplies of the AK4619 if the power supply of the peripheral devices turned on when using the I^2C interface. The devices connected on the same I^2C Bus will not be able to communicate since the SDA and SCL pins go to 0V by the internal protection diode of the AK4619.

AKM assumes no responsibility for usage beyond the conditions in this datasheet.

8. Electrical Characteristics

8.1. Analog Characteristics

1. MIC Gain AMP

(Ta = 25 °C; AVDD = VREFH = TVDD = 3.3 V; VSS1 = VSS2 = VREFL = 0 V)

	Parameter	Min.	Typ.	Max.	Unit
MIC AMP	Gain Setting	-6	-	+27	dB
	Step Width	2	3	4	

2. MIC Gain AMP + ADC

(Ta = 25 °C; AVDD = VREFH = TVDD = 3.3 V; VSS1 = VSS2 = VREFL = 0 V; Signal frequency = 1 kHz; 24-bit Data; BICK = 64fs; Measurement frequncy BW = 20 Hz - 20 kHz @fs = 48 kHz, BW = 20 Hz - 40 kHz @fs = 96 kHz,192 kHz); MGNL/R[3:0] bits = 2h (0dB);

	Parameter		Min.	Typ.	Max.	Unit
ADC1 ADC2	Resolution				24	bit
	Input Impedance		17	25	33	kΩ
	Differential Input					
	Full-scale Input Voltage *13		±2.55	±2.83	±3.11	Vpp
	S/(N+D) (-1dBFS)	fs = 48 kHz	85	95		dB
		fs = 96 kHz		92		
		fs = 192 kHz		92		
	Dynamic Range (-60dBFS)	fs = 48 kHz (A-weighted)		106		dB
		fs = 96 kHz		99		
		fs = 192 kHz		99		
	S/N	fs = 48 kHz (A-weighted)	98	106		dB
		fs = 96 kHz		99		
		fs = 192 kHz		99		
	Interchannel Isolation *9		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	Power Supply Rejection Ratio (PSRR) *10			50		dB
	Common Mode Rejection Ratio (CMRR) *11		60	80		dB
	Single-ended Input, Pseudo-differential Input					
	Full-scale Input Voltage *14		2.55	2.83	3.11	Vpp
	S/(N+D) (-1dBFS)	fs = 48 kHz	85	95		dB
		fs = 96 kHz		92		
		fs = 192 kHz		92		
	Dynamic Range (-60dBFS)	fs = 48 kHz (A-weighted)		104		dB
		fs = 96 kHz		97		
		fs = 192 kHz		97		
	S/N	fs = 48 kHz (A-weighted)	96	104		dB
		fs = 96 kHz		97		
		fs = 192 kHz		97		
	Interchannel Isolation *9		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	Power Supply Rejection Ratio (PSRR) *10			50		dB
	Common Mode Rejection Ratio (CMRR) *12		55	75		dB

Notes

*9. Indicates Interchannel isolation between Lch and Rch when -1 dBFS signal is input

*10. PSRR measurement is based upon a 1 kHz, 50 mVpp signal applied to AVDD and VREFH.

*11. CMRR measurement is based upon a 1 kHz, 100 mVpp sine wave applied to both differential input pins.

*12. CMRR measurement is based upon a 1 kHz, 100 mVpp sine wave applied to both pseudo-differential input and pseudo-ground input pins.

*13. IN1P, IN1N, IN2P, IN2N, IN3P, IN3N, IN4P, IN4N pins. Input full-scale voltage is proportional to AVDD (0.858 x AVDD).

*14. AIN1L, AIN1R, AIN2L, AIN2R, AIN3L, AIN3R, AIN4L, AIN4R, AIN5L, AIN5R, AIN6L, AIN6R pins. Input full-scale voltage is proportional to AVDD (0.858 x AVDD).

3. DAC

(Ta = 25 °C; AVDD = VREFH = TVDD = 3.3 V; VSS1 = VSS2 = VREFL = 0 V;
Signal Frequency =1 kHz; 32-bit Data; BICK = 64fs; measurement bandwidth BW = 20 Hz to 20 kHz @fs = 48 kHz; measurement bandwidth BW = 20 Hz to 40 kHz @fs = 96 kHz,192 kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC1 DAC2	Resolution				32	bit
	Output Voltage *15		2.55	2.83	3.11	Vpp
	S/(N+D) (0dBFS)	fs = 48 kHz	80	91		dB
		fs = 96 kHz		89		
		fs = 192 kHz		89		
	Dynamic Range (-60dBFS)	fs = 48 kHz (A-weighted)		108		dB
		fs = 96 kHz		101		
		fs = 192 kHz		101		
	S/N	fs = 48 kHz (A-weighted)	100	108		dB
		fs = 96 kHz		101		
		fs = 192 kHz		101		
	Interchannel Isolation (fin = 1 kHz) *16		90	110		dB
	Channel Gain Mismatch			0.0	0.7	dB
	Load Resistance *17		10			kΩ
	Load Capacitance				30	pF
	Power Supply Rejection Ratio (PSRR) *10			50		dB

Notes:
*15. Full-scale output voltage. The output voltage is proportional to AVDD (AVDD x 0.858).
*16. Indicates DAC interchannel isolation between AOUT1L and AOUT1R, AOUT2L and AOUT2R when 0dBFS signal is input to the DAC.
*17. AC load.

4. Power Supplies

(Ta = 25°C; AVDD = VREFH = TVDD = 3.3V, VSS1 = VSS2 = VREFL = 0V; fs = 192kHz, MCLK = 128fs, BICK = 64fs, C_L = 20 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Normal operation (PDN pin= “H”)	AVDD		20	30	mA
	TVDD		10	20	mA
Power down (PDN pin= “L”, All digital input pins = VSS2)	AVDD		1	10	μA
	TVDD		1	10	μA

8.2. Digital Filter Characteristics

1. ADC 1/2

(Ta = −40 to 105°C; AVDD = VREFH = 3.0 to 3.6V, TVDD = 1.7 to 3.6V; VSS1 = VSS2 = VREFL = 0V)

1-1 Sharp Roll-Off Filter (ADxVO bit = "0", ADxSD bit = "0", ADxSL bit = "0", x=1, 2)

fs = 48 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband *18	0 dB/−0.06 dB	PB	0	-	22.1	kHz
	−3.0 dB	PB	-	23.7	-	kHz
Stopband *18		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 20 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	22	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	0.9	-	Hz

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband *18	0 dB/−0.06 dB	PB	0	-	44.2	kHz
	−3.0 dB	PB	-	47.5	-	kHz
Stopband *18		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	22	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	1.9	-	Hz

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband *18	0 dB/−0.04 dB	PB	0	-	83.7	kHz
	−3.0 dB	PB	-	96.0	-	kHz
Stopband *18		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	18	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	3.8	-	Hz

Notes:

*18. The passband and stopband frequencies scale with "fs" (sampling frequency). Frequency response is measured with respect to a 1 kHz input signal. The characteristic of the high pass filter is not included.

*19. The calculated delay time induced by digital filtering. This is the time measured from the input of an analog signal to the L channel MSB output on the SDTO pin. It may have an error of +1[1/fs] at maximum due to the serial output data via audio interfaces. This time includes the group delay of the HPF.

1-2 Slow Roll-Off Filter (ADxVO bit = "0", ADxSD bit = "0", ADxSL bit = "1", x=1, 2)

fs = 48 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband *18	0 dB/−0.074 dB	PB	0	-	12.5	kHz
	−3.0 dB		-	19.2	-	kHz
Stopband *18		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 20 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	10	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	0.9	-	Hz

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband *18	0 dB/−0.074 dB	PB	0	-	25	kHz
	−3.0 dB		-	38.5	-	kHz
Stopband *18		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	10	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	1.9	-	Hz

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband *18	0 dB/−0.1 dB	PB	0	-	31.1	kHz
	−3.0 dB		-	62.3	-	kHz
Stopband *18		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	11	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	3.8	-	Hz

1-3 Short Delay, Sharp Roll-Off Filter (ADxVO bit = "0", ADxSD bit = "1", ADxSL bit = "0" x=1, 2)

fs = 48 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SHARP ROLL-OFF						
Passband *18	0 dB/−0.06 dB	PB	0	-	22.1	kHz
	−3.0 dB		-	23.7	-	kHz
Stopband *18		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 20 kHz		ΔGD	-	-	2.6	1/fs
Group Delay *19		GD	-	8	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	0.9	-	Hz

fs = 96 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SHARP ROLL-OFF						
Passband *18	0 dB/−0.06 dB	PB	0	-	44.2	kHz
	−3.0 dB		-	47.5	-	kHz
Stopband *18		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	-	2.6	1/fs
Group Delay *19		GD	-	8	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	1.9	-	Hz

fs = 192 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SHARP ROLL-OFF						
Passband *18	0 dB/−0.04 dB	PB	0	-	83.7	kHz
	−3.0 dB		-	96.0	-	kHz
Stopband *18		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	0	0.2	1/fs
Group Delay *19		GD	-	9	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	3.8	-	Hz

1-4 Short Delay, Slow Roll-Off Filter (ADxVO bit = "0", ADxSD bit = "1", ADxSL bit = "1" x=1, 2)

fs = 48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SLOW ROLL-OFF						
Passband *18	0 dB/−0.074 dB	PB	0	-	12.5	kHz
	−3.0 dB		-	19.2	-	kHz
Stopband *18		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 20 kHz		ΔGD	-	-	2.6	1/fs
Group Delay *19		GD	-	8	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	0.9	-	Hz

fs = 96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SLOW ROLL-OFF						
Passband *18	0 dB/−0.074 dB	PB	0	-	25	kHz
	−3.0 dB		-	38.5	-	kHz
Stopband *18		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	-	2.6	1/fs
Group Delay *19		GD	-	8	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	1.9	-	Hz

fs = 192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SLOW ROLL-OFF						
Passband *18	0 dB/−0.1 dB	PB	0	-	31.1	kHz
	−3.0 dB		-	63.2	-	kHz
Stopband *18		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0 Hz to 40 kHz		ΔGD	-	-	0.6	1/fs
Group Delay *19		GD	-	9	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	3.8	-	Hz

1-5 Voice Filter (ADxVO bit = "1" x=1, 2)

fs = 16kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
VOICE						
Passband *18	−0.5 dB/+0.5 dB	PB	0	-	6.3	kHz
	−3.0 dB		-	6.9	-	kHz
Stopband *18		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay Distortion: 0 Hz to 8 kHz		ΔGD	-	0	-	1/fs
Group Delay *19		GD	-	22	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	−3.0 dB	FR	-	0.3	-	Hz

2. DAC 1/2

(Ta = −40 to 105°C; AVDD = VREFH = 3.0 to 3.6 V, TVDD = 1.7 to 3.6 V; VSS1 = VSS2 = VREFL = 0 V)

2-1 Sharp Roll-Off Filter (DAxSD bit = "0", DAxSL bit = "0" , x=1, 2)

fs = 48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband *20	±0.05 dB	PB	0		21.7	kHz
	−3.0 dB	PB		23.4		kHz
Passband Ripple		PR	−0.0032		0.0032	dB
Stopband *20		SB	26.3			kHz
Stopband Attenuation *22 *23		SA	80			dB
Group Delay *21		GD	-	29.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 20.0 kHz			-0.3		0.1	dB

fs = 96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband *20	±0.05 dB	PB	0		43.5	kHz
	−3.0 dB	PB		46.8		kHz
Passband Ripple		PR	-0.0032		0.0032	dB
Stopband *20		SB	52.5			kHz
Stopband Attenuation *22 *23		SA	80			dB
Group Delay *21		GD	-	29.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 40.0 kHz			-0.5		0.1	dB

fs = 192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband *20	±0.05 dB	PB	0		87.0	kHz
	−3.0 dB	PB		93.6		kHz
Passband Ripple		PR	-0.0032		0.0032	dB
Stopband *20		SB	105			kHz
Stopband Attenuation *22 *23		SA	80			dB
Group Delay *21		GD	-	29.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 80.0 kHz			-1.9		0.1	dB

Notes:

*20. The passband and stopband frequencies are proportional to "fs" (sampling frequency) and are expressed as PB=0.4535 × fs and SB=0.5465 × fs, respectively.

*21. The digital filter delay is calculated as the time elapsed from 16/20/24/32-bit digital data being written to the input register to the analog signal being output. It may have an error of +1[1/fs] at maximum due to audio interfaces via the serial input data.

*22. The output level is 0dB, with a 1 kHz, 0 dB Sine wave input.

*23. The measurement frequency range is from 0 Hz (DC) to fs.

2-2 Slow Roll-Off Filter (DAxSD bit = "0", DAxSL bit = "1" , x=1, 2)

fs = 48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband *25	±0.05 dB	PB	0		8.8	kHz
	−3.0 dB	PB		19.8		kHz
Passband Ripple		PR	−0.043		0.043	dB
Stopband *20		SB	42.7			kHz
Stopband Attenuation *22 *23		SA	73			dB
Group Delay *21		GD	-	8.8	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 20.0 kHz			−5.0		0.1	dB

fs = 96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband *25	±0.05 dB	PB	0		17.7	kHz
	−3.0 dB	PB		39.5		kHz
Passband Ripple		PR	−0.043		0.043	dB
Stopband *20		SB	85.3			kHz
Stopband Attenuation *22 *23		SA	73			dB
Group Delay *21		GD	-	8.8	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 40.0 kHz			−5.2		0.1	dB

fs = 192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband *25°	±0.05 dB	PB	0		35.5	kHz
	−3.0 dB	PB		79.0		kHz
Passband Ripple		PR	−0.043		0.043	dB
Stopband *20		SB	171			kHz
Stopband Attenuation *22 *23		SA	73			dB
Group Delay *21		GD	-	8.8	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 80.0 kHz			−5.9		0.1	dB

Note:

*24. The passband and stopband frequencies scale with fs.
For example, PB = 0.185 × fs, SB = 0.888 × fs.

2-3 Short Delay, Sharp Roll-Off Filter (DAxSD bit = "1", DAxSL bit = "0" , x=1, 2)

fs = 48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SHARP ROLL-OFF						
Passband *20	±0.05 dB	PB	0		21.7	kHz
	−3.0 dB	PB		23.4		kHz
Passband Ripple		PR	−0.0031		0.0031	dB
Stopband *20		SB	26.3			kHz
Stopband Attenuation *22 *23		SA	80			dB
Group Delay *21		GD	-	8.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 20.0 kHz			−0.3		0.1	dB

fs = 96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SHARP ROLL-OFF						
Passband *20	±0.05 dB	PB	0		43.5	kHz
	−3.0 dB	PB		46.8		kHz
Passband Ripple		PR	-0.0031		0.0031	dB
Stopband *20		SB	52.5			kHz
Stopband Attenuation *22 *23		SA	80			dB
Group Delay *21		GD	-	8.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 40.0 kHz			−0.5		0.1	dB

fs = 192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SHARP ROLL-OFF						
Passband *20	±0.05 dB	PB	0		87.0	kHz
	−3.0 dB	PB		93.6		kHz
Passband Ripple		PR	−0.0031		0.0031	dB
Stopband *20		SB	105			kHz
Stopband Attenuation *22 *23		SA	80			dB
Group Delay *21		GD	-	8.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 80.0 kHz			−1.9		0.1	dB

2-4 Short Delay, Slow Roll-Off Filter (DAxSD bit = "1", DAxSL bit = "1" , x=1, 2)

fs = 48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SLOW ROLL-OFF						
Passband *25	±0.05 dB	PB	0		12.0	kHz
	−3.0 dB	PB		21.1		kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband *20		SB	41.5			kHz
Stopband Attenuation *22 *23		SA	82			dB
Group Delay *21		GD	-	7.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 20.0 kHz			-4.8		0.1	dB

fs = 96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SLOW ROLL-OFF						
Passband *25	±0.05 dB	PB	0		24.2	kHz
	−3.0 dB	PB		42.1		kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband *20		SB	83.0			kHz
Stopband Attenuation *22 *23		SA	82			dB
Group Delay *21		GD	-	7.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 40.0kHz			-5.0		0.1	dB

fs = 192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY, SLOW ROLL-OFF						
Passband *25	±0.05 dB	PB	0		48.4	kHz
	−3.0 dB	PB		84.3		kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband *20		SB	165.9			kHz
Stopband Attenuation *22 *23		SA	82			dB
Group Delay *21		GD	-	7.3	-	1/fs
Digital Filter + SCF + SMF *22						
Frequency Response: 0 to 80.0 kHz			-5.7		0.1	dB

Note:

*25. The passband and stopband frequencies scale with fs.
For example, PB = 0.252 × fs, SB = 0.864 × fs.

8.3. DC Characteristics

(Ta = −40 to 105°C; AVDD = VREFH = 3.0 to 3.6 V, TVDD = 1.7 to 3.6 V; VSS1 = VSS2 = VREFL = 0 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage1 *26		VIH1	80%TVDD			V
Low-Level Input Voltage1 *26		VIL1			20%TVDD	V
SCL, SDA High-Level Input Voltage		VIH2	70%TVDD			V
SCL, SDA Low-Level Input Voltage		VIL2			30%TVDD	V
High-Level Output Voltage (Iout = −100 μA) *27		VOH1	TVDD−0.3			V
Low-Level Output Voltage (Iout = 100 μA) *27		VOL1			0.3	V
SDA Low-Level Output Voltage	Fast Mode					
	TVDD ≧ 2.0V (Iout = 3mA)	VOL2			0.4	V
	TVDD ＜ 2.0V (Iout = 3mA)	VOL2			20%TVDD	V
Input Leakage Current		Iin			±10	μA

Notes:
*26. MCLK, BICK, LRCK, SDIN1, SDIN2, CAD/CSN, SCLK, SI, PDN pins
*27. SDOUT1, SDOUT2, SO pins

8.4. Switching Characteristics

(Ta = −40 to 105°C; AVDD = VREFH = 3.0 to 3.6 V, TVDD = 1.7 to 3.6 V; VSS1 = VSS2 = VREFL = 0V; C_L = 20pF)

1. System Clocks

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
Frequency	fMCLK	2.027		24.822	MHz
Pulse Width Low	tMCLKL	0.4 / fMCLK			ns
Pulse Width High	tMCLKH	0.4 / fMCLK			ns
LRCK/BICK Input Timing					
LRCK Input Timing					
Stereo mode					
Frequency	fs	7.92		194	kHz
Pulse Width Low	tLRL	0.4 / fs			ns
Pulse Width High	tLRH	0.4 / fs			ns
PCM mode (PCM Long Frame, PCM Short Frame)					
Frequency	fs	7.92		194	kHz
Pulse Width Low	tLRL	1/(64fs)			ns
Pulse Width High	tLRH	1/(64fs)			ns
TDM128 mode					
Frequency	fs	7.92		194	kHz
Pulse Width Low	tLRL	1/(128fs)			ns
Pulse Width High	tLRH	1/(128fs)			ns
TDM256 mode					
Frequency	fs	7.92		97	kHz
Pulse Width Low	tLRL	1/(256fs)			ns
Pulse Width High	tLRH	1/(256fs)			ns
BICK Input Timing					
Frequency *28	fBICK	0.253		24.822	MHz
Pulse Width Low	tBICKL	0.4 / fBICK			ns
Pulse Width High	tBICKH	0.4 / fBICK			ns

Note:

*28. The BICK frequency must be set to fBICK ≥ (2 x fs x Slot length).

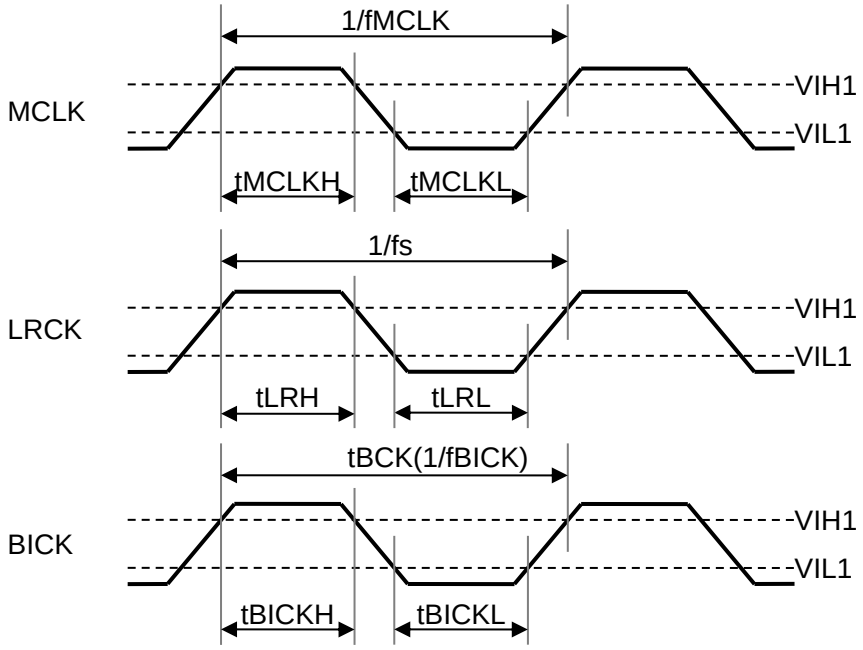


Figure 3. System Clock Timing

2. Power down

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width *29	tRST	600			ns

Note:
*29. The PDN pin must be held “L” upon applying power to the device.

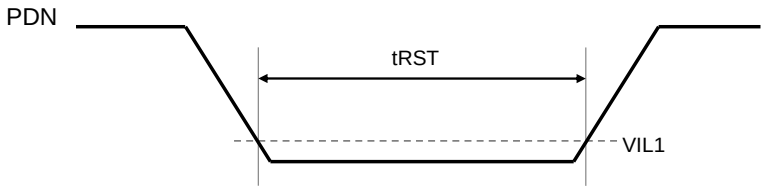


Figure 4. Power-down & Reset Timing

3. Audio Serial Data interface (SDIN1, SDIN2, SDOUT1, SDOUT2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Delay Time from BICK "↑" to LRCK *30	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" *30	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from BICK "↓"to Serial Data Output *31 *32	tBSOD1			20	ns
Delay Time from BICK "↑"to Serial Data Output *30	tBSOD2	5		30	ns

Notes:

*30. Measured from BICK "↓" when the BICK polarity is inverted (BCKP bit = "1").".

*31. Measured from BICK "↑" when the BICK polarity is inverted (BCKP bit = "1").".

*32. Set SDOPH bit to "1" when BICK is faster than 12.288 MHz. (e.g. TDM256 mode with 96 kHz sampling frequency.) The data should be output based on BICK " ↑ "

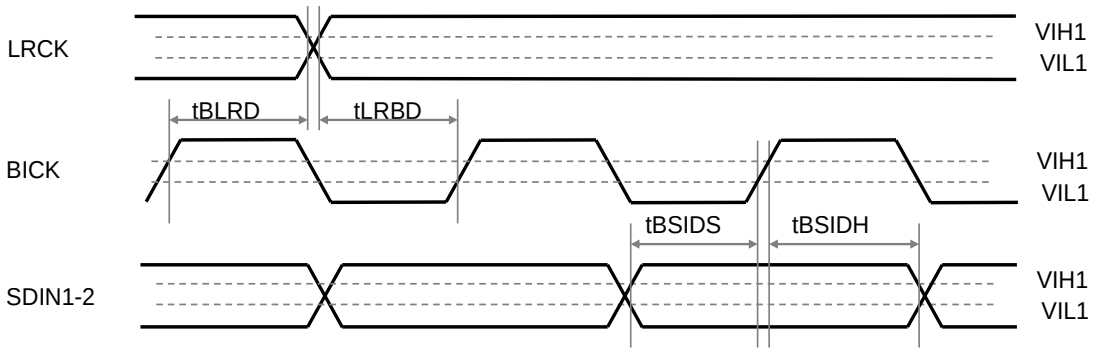


Figure 5. Audio Interface Timing (SDIN1-2)

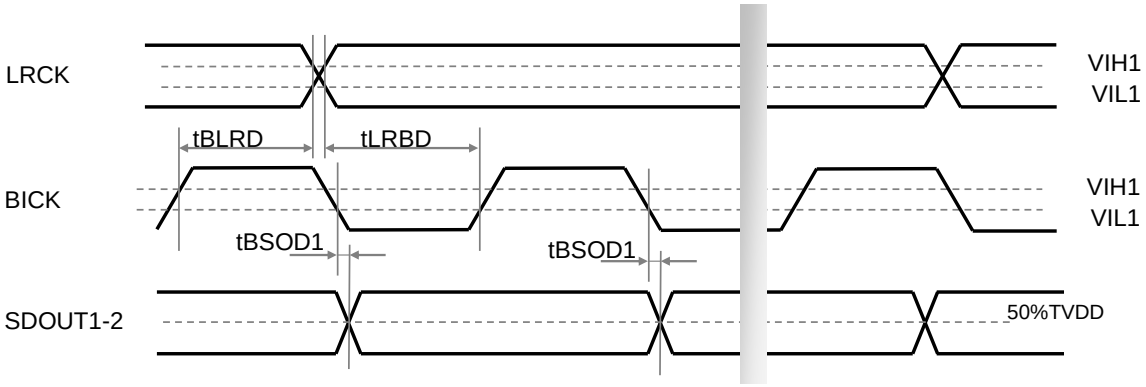


Figure 6. Audio Interface Timing (SDOUT1-2, SDOPH bit = “0”)

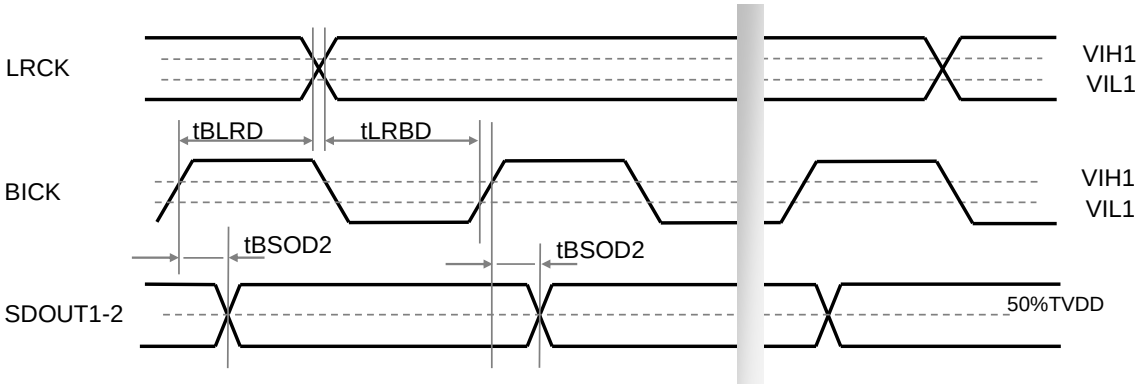


Figure 7. Audio Interface Timing (SDOUT1-2, SDOPH bit = “1”)

4. SPI Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency	fSCLK			7	MHz
SCLK Low-level Width	tSCLKL	60			ns
SCLK High-level Width	tSCLKH	60			ns
Microcontroller →AK4619					
CSN High-level Width	tWRQH	150			ns
From CSN "↑" to PDN "↑"	tRST1	180			ns
From PDN "↑" to CSN "↓"	tIRRQ	10			ms
From CSN "↓" to SCLK "↓"	tWSC	150			ns
From SCLK "↑" to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	20			ns
SI Latch Hold Time	tSIH	20			ns
AK4619→ **Microcontroller**					
Delay Time from SCLK "↓" to SO Output	tSOS			40	ns
SO Output Hold Time from SCLK "↑"	tSOH	60			ns

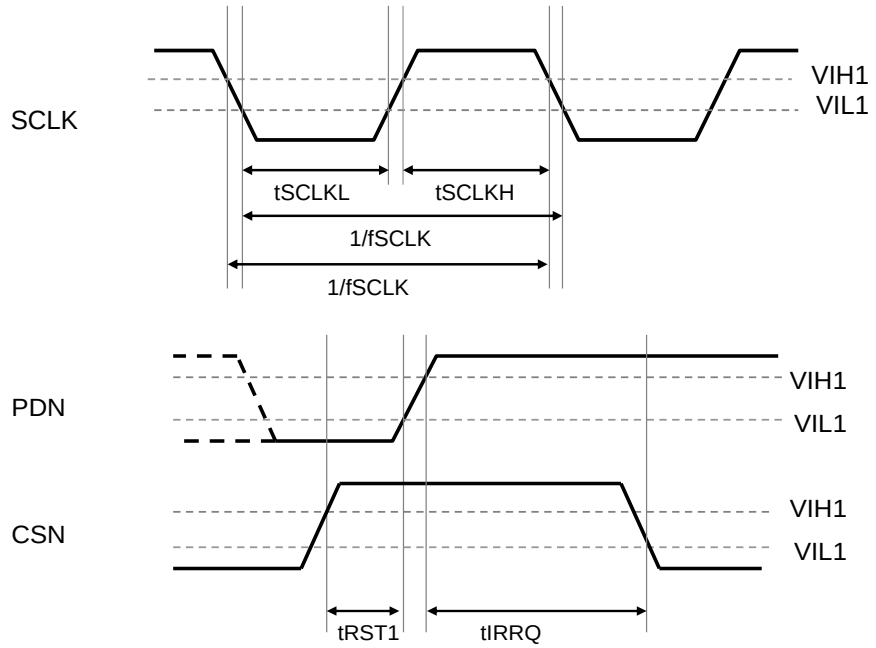


Figure 8. SPI Interface Timing1

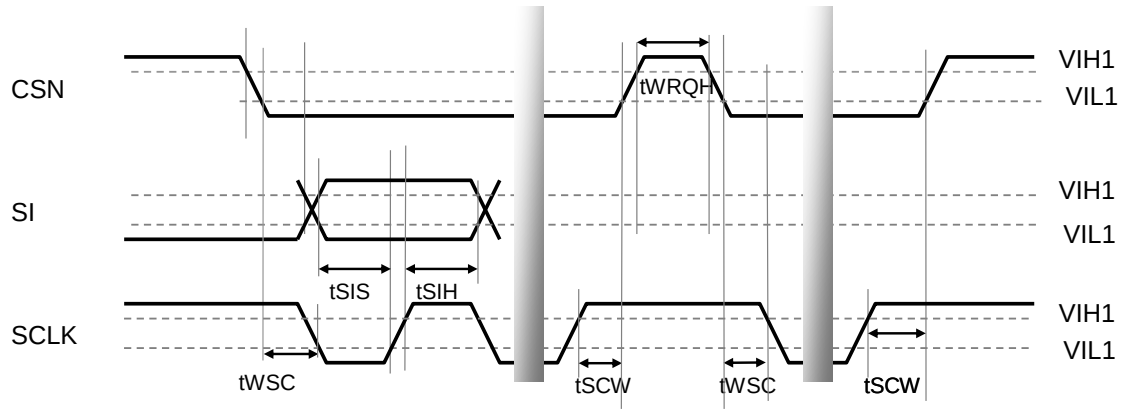


Figure 9. SPI Interface Timing 2（Microcontroller→ AK4619）

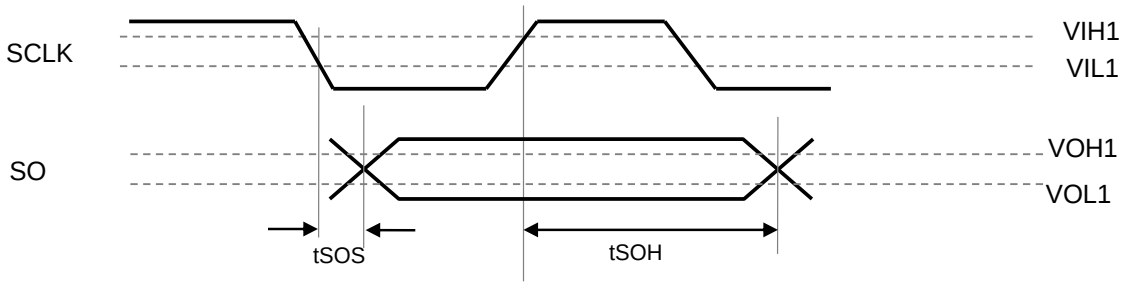


Figure 10. SPI Interface Timing 3（AK4619→Microcontroller）

5. I²C Interface

<I²C-bus: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling *32	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

Notes:

*33. The SDA data must provide a hold time of at least 300 ns with respect to the falling of SCL.

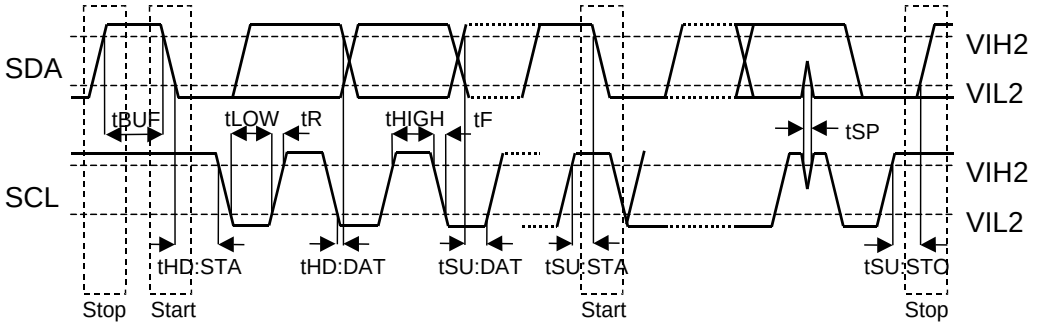


Figure 11. I²C Bus Timing

9. Functional Descriptions

9.1. LDO

The AK4619 has an on-chip LDO regulator for driving internal digital circuits. When using the LDO, connect a 2.2 µF (±50%) capacitor in series between the AVDRV pin and VSS2. The LDO starts operation when the device is released from power-down mode (PDN pin = "H"), and control register write/read operations can be performed 10 ms after PDN is deasserted.

The AK4619 has an overcurrent protection circuit to avoid the overheating that may be caused by a short of the AVDRV pin to VSS2 etc., and an overvoltage protection circuit to protect from excessexceeded voltage supplied to the AVDRV pin. When these protection circuits are engaged, internal circuits are powered down, SDA/SO pins are Hi-Z, and the control interface does not generate the ACK signal in I^2C mode nor serial data output in SPI mode. Internal circuits will not return to normal operation until the device is reset by bringing the PDN pin "L" after addressing the problem conditions.

9.2. System Clock

The external clocks required to operate the AK4619 are MCLK, BICK, and LRCK. MCLK, BICK, and LRCK should be synchronous with respect to each other, but the phase of MCLK is not critical. A clock with the frequency 128fs, 256fs, 384fs or 512fs must be input to the MCLK pin and a clock of 32fs, 48fs, 64fs, 128fs or 256fs must be input to BICK pin. The FS [2: 0] bits must be configured based upon the MCLK, BICK, and LRCK provided to the device. (Table 1)

Table 1. MCLK/BICK and Sampling Frequency Range Setting Example

FS[2:0] bits	MCLK	BICK	Sampling Frequency Range	
000	256fs	32fs, 48fs, 64fs, 128fs, 256fs	8 kHz ≦ fs ≦ 48 kHz	(default)
001	256fs	32fs, 48fs, 64fs, 128fs, 256fs	fs = 96 kHz	
010	384fs	32fs, 48fs, 64fs, 128fs, 256fs	8 kHz ≦ fs ≦ 48 kHz	
011	512fs	32fs, 48fs, 64fs, 128fs, 256fs	8 kHz ≦ fs ≦ 48 kHz	
1xx	128fs	32fs, 48fs, 64fs, 128fs	fs = 192 kHz	

x:Don't Care

9.3. Audio Interface Format

The serial audio interface format is configured via the TDM, SLOT, DCF[2:0], BCKP, DSL[1:0], BCKP, DIDL[1:0] and DODL[1:0] bits (Table 2 to Table 7) .

The slot length of the word is set by DSL [1: 0] bits (Table 4).
The input word length is set by DIDL [1: 0] bits (Table 6).
The output word length is set by DODL [1: 0] bits (Table 7). The relationship between slot length and word length is shown on Figure 12. BCKP bit controls the edge relationship of BICK and LRCK (Table 5).

When AK4619 is functioning in TDM mode, only the SDIN1 pin and SDOUT1 pin are supported. The multiplexed data is input onto SDIN1 pin, and output data on the SDOUT1 pin. At this time, input data on the SDIN2 pin is ignored and the SDOUT2 pin becomes “L” output.

The start position for consecutive audio words is set by the SLOT bit (Table 3). In Stereo mode, the SLOT bit should be set to “0” because it operates based on the LRCK edge. In PCM mode and TDM mode, audio words are separated by slot length so set the SLOT bit = “1” (slot length basis).

The LRCK clock requires a high/low time of 1xBICK or more per LRCK cycle in PCM mode and TDM mode.

In all modes, the serial data format is MSB first, 2's complement. The AK4619 does not support settings other than those listed in Table 2.

Table 2. Audio Interface Format

Mode	TDM bit	SLOT bit	DCF[2:0] bits	Audio Interface Format	Slot Length	DSL[1:0] bits	BICK	Figure	
0	0	0	000	Stereo mode I²S compatible	16/20/ 24/32 bit	xx	32fs, 48fs, 64fs	Figure 13	(default)
1			101	Stereo mode MSB justified		xx	32fs, 48fs, 64fs	Figure 14	
2		1	110	Stereo mode PCM Short Frame	16bit	10	32fs	Figure 15	
3					24bit	00	48fs		
4					32bit	11	64fs		
5			111	Stereo mode PCM Long Frame	16bit	10	32fs	Figure 16	
6					24bit	00	48fs		
7					32bit	11	64fs		
8	1		010	TDM128 mode I²S compatible	32bit	11	128fs	Figure 17	
9			111	TDM128 mode MSB justified	32bit	11	128fs	Figure 18	
10			010	TDM256 mode I²S compatible	32bit	11	256fs	Figure 19	
11			111	TDM256 mode MSB Justified	32bit	11	256fs	Figure 20	

x:Don’t Care

Table 3. Start Position Setting for next Slot

SLOT bit	Start Position	
0	LRCK Edge Basis	(default)
1	Slot Length Basis	

If the data transmission timing is set to LRCK edge basis, the next channel's data will not be transmitted until the next LRCK edge occurs.

If the data transmission timing is set to Slot length basis, the next channel's data is transmitted immediately, without waiting for an LRCK edge after the previous slot has been transmitted.

Table 4. Slot Length setting

DSL[1:0] bits	Slot Length	
00	24bit	
01	20bit	
10	16bit	
11	32bit	(default)

Table 5. BICK Edge Setting

BCKP bit	BICK edge referenced to LRCK edge	
0	Falling Edge	(default)
1	Rising Edge	

Table 6. SDIN1/2 Word Length Setting

DIDL[1:0] bits	SDIN Word Length	
00	24-bit	
01	20-bit	
10	16-bit	
11	32-bit	(default)

Table 7. SDOUT1/2 Word Length Setting (N/A: Not available)

DODL[1:0] bits	SDOUT Word Length	
00	24-bit	(default)
01	20-bit	
10	16-bit	
11	N/A	

Data difinitions

A serial data that is transmitted or received has the structure of the slot, word and bit.

Bit : It is a smallest component in a serial data(SDIN/SDOUT). The bit duration is one BICK clock cycle.

Word : It is a group of multiple bits that composes sampled data. Figure 12 shows an example of a word consists of 24 bits length.

Slot : It is composed of a word and adequate additional bits (P: Padding) to move serial data from/to an external device.

In Figure 12, the audio word is 24-bit valid data. In order to make 32-bit slot length, additional eight "P" adds to satisfy an interface protocol of the external device. Zeros are inserted into "P" when sending SDOUT serial data, and "P" data is ignored when receiving SDIN serial data.

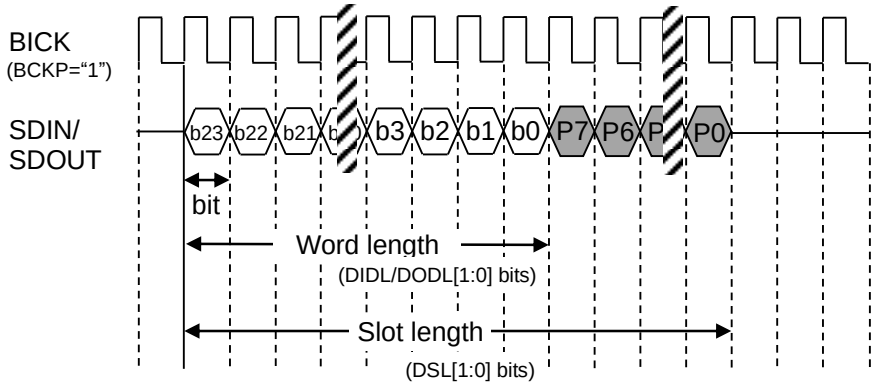


Figure 12.The definition of Bit, Word and Slot

Figure 12 is an example of the sample word aligned to the beginning of the slot(MSB justified).

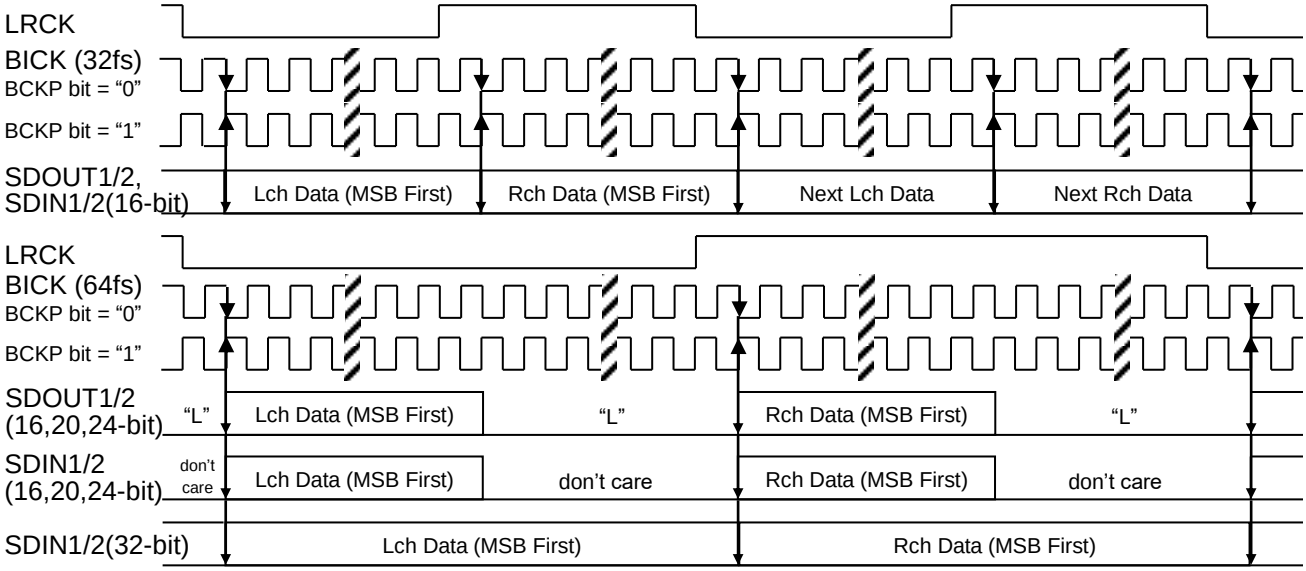


Figure 13. Mode 0 Timing (Stereo mode, I^2S Compatible)

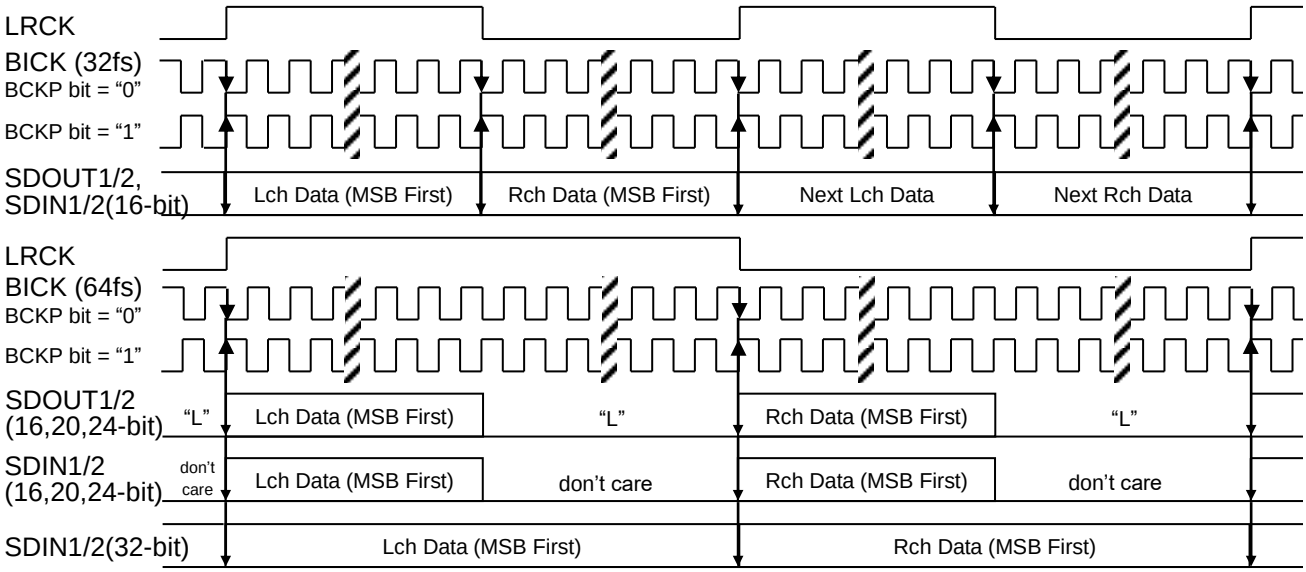


Figure 14. Mode 1 Timing (Stereo mode, MSB Justified)

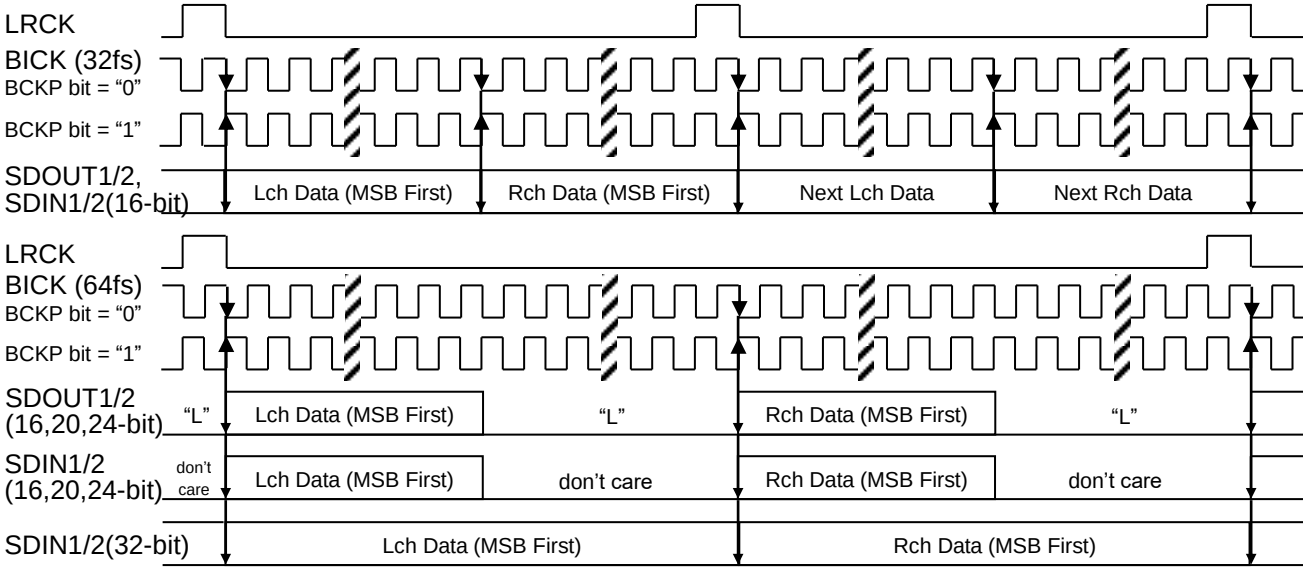


Figure 15. Mode 2/3/4 Timing (Stereo mode PCM Short Frame)

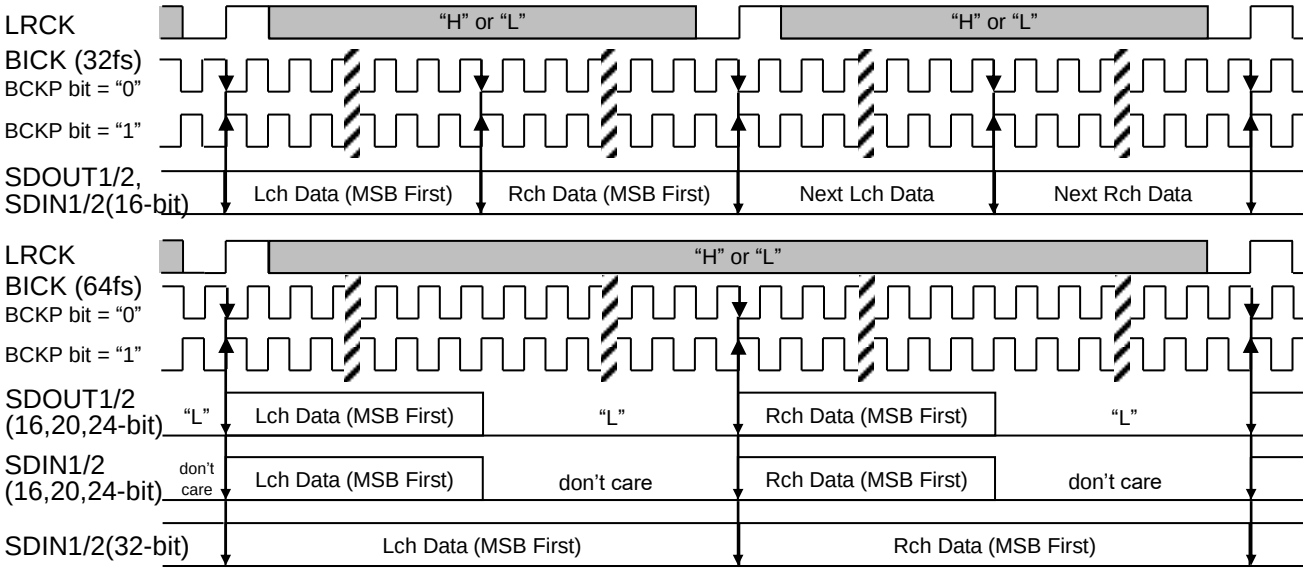


Figure 16. Mode 5/6/7 Timing (Stereo mode PCM Long Frame)

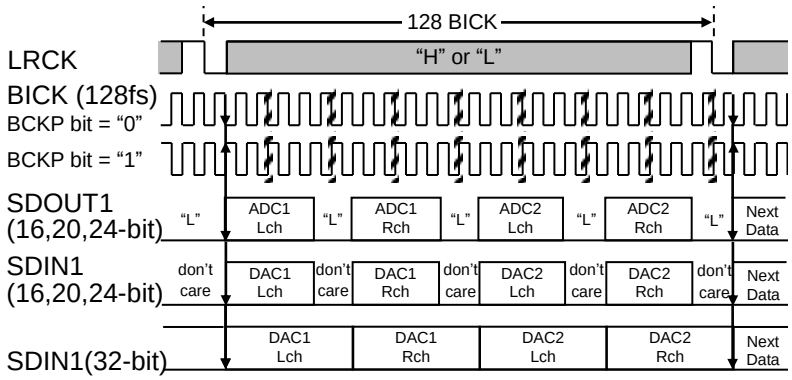


Figure 17. Mode 8 Timing (TDM128 mode, I²S Compatible)

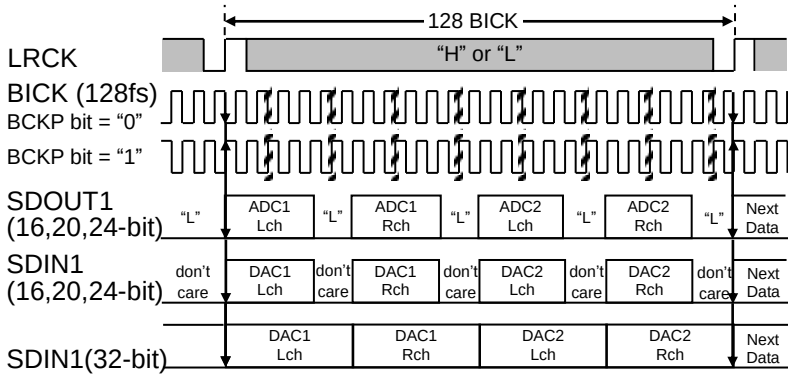


Figure 18. Mode 9 Timing (TDM128 mode, MSB Justified)

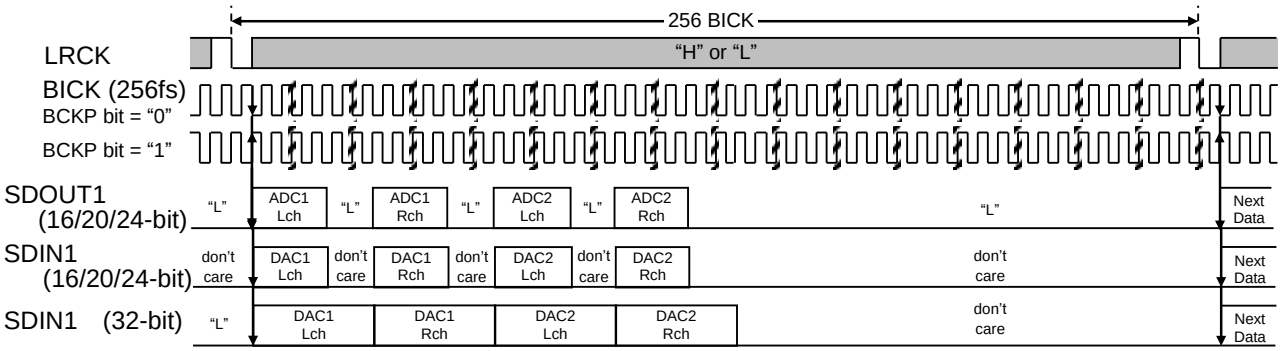


Figure 19. Mode 10 Timing (TDM256 mode, I²S Compatible)

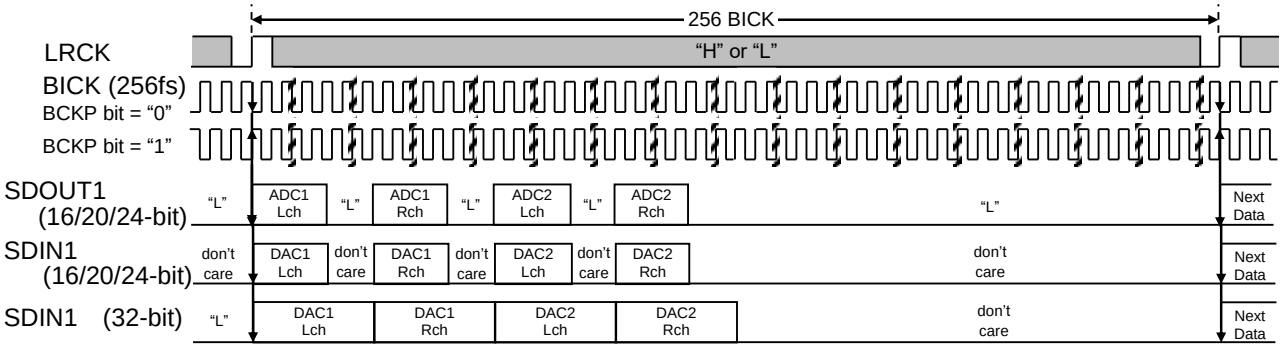


Figure 20. Mode 11 Timing (TDM256 mode, MSB Justified)

9.4. Power state, Power-up/down Sequence

1. Power state

There are four power state (power-down, standby, reset and normal operation) which are set via the PDN pin, PMAD1/2, PMDA1/2 bits, and RSTN bit. (Table 8).

Table 8. Power Down, Standby, Reset & Normal operation

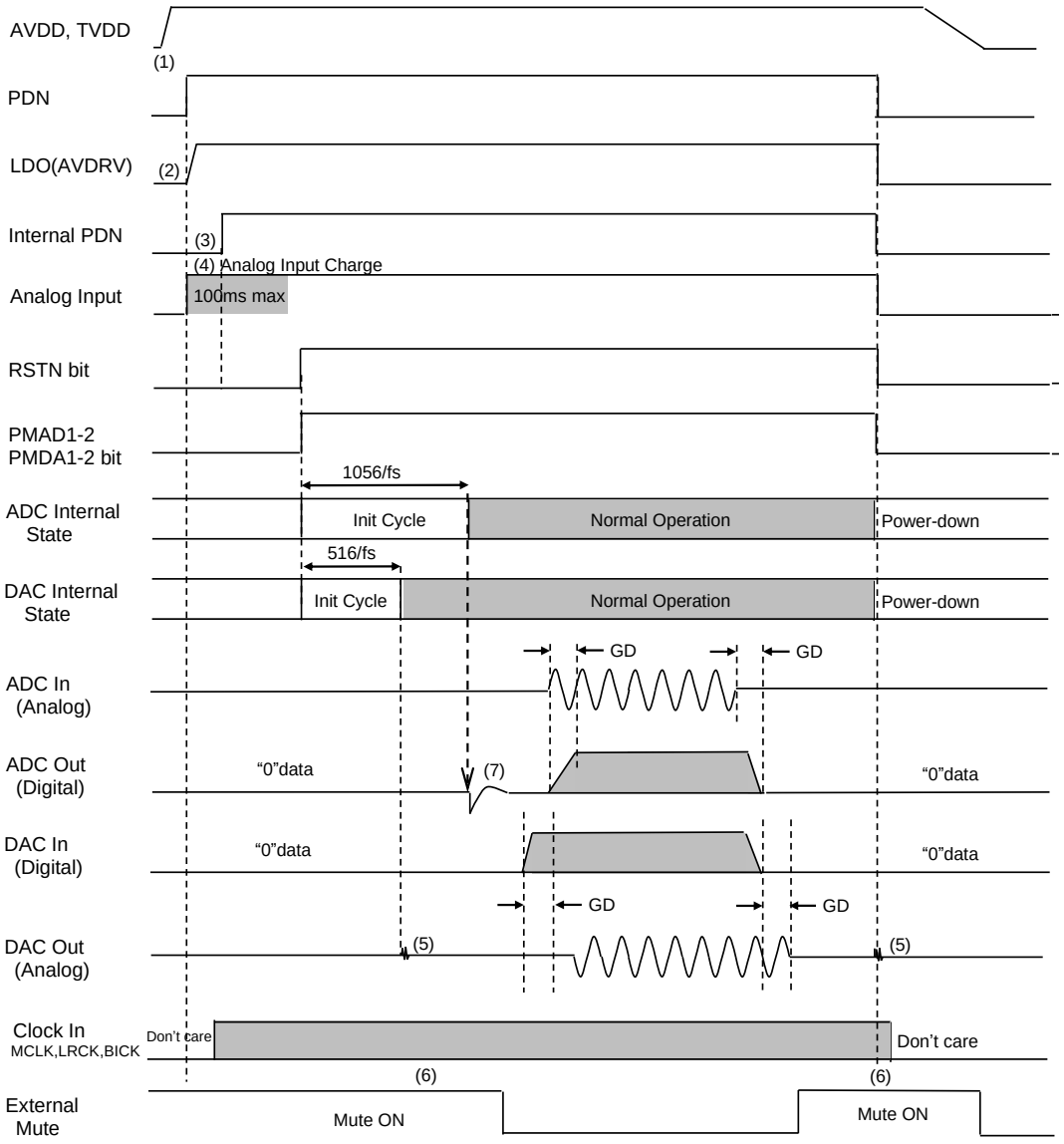
Mode	PDN pin	MCLK BICK LRCK	PMAD 1/2 bits	PMDA 1/2 bits	RSTN bit	Pin State	
						Digital Output	Analog Output
Power Down	L	x	0	0	0	L	Hi-Z
Standby	H	Input	0	0	0	L	Hi-Z
Reset	H	Input	1	0	0	L	Hi-Z
			0	1		L	AVDD/2
Normal operation	H	Input	1	1	1	Signal Output	Signal Output

x : Don't Care

2. Power-up/down Sequence

The AK4619 should be powered up when the PDN pin = “L”. The PDN pin should be set “H” after all power supplies have ramped up. At that point, the reference voltage generator block (REFBLK) and LDO (AVDRV) circuit are powered up and the control registers are initialized. Control register settings should be no less than 10ms after PDN pin = “H”.

After power-down is released (PDN pin = “H”), the state of PMAD1 bit = PMAD2 bit = PMDA1 bit = PMDA2 bit = RSTN bit = “0” is defined as the standby state. At this state, all internal blocks are in the power-down state except for the REFBLK and the LDO. After setting the control register, supply the necessary system clock (MCLK, BICK, LRCK) and then release the standby state. Once the power management bit (PMADx, PMDAx, x=1, 2) of the required block has been changed from “0” to “1” and the reset bit (RSTN bit) is changed from “0” to “1”, the normal operational state is established.



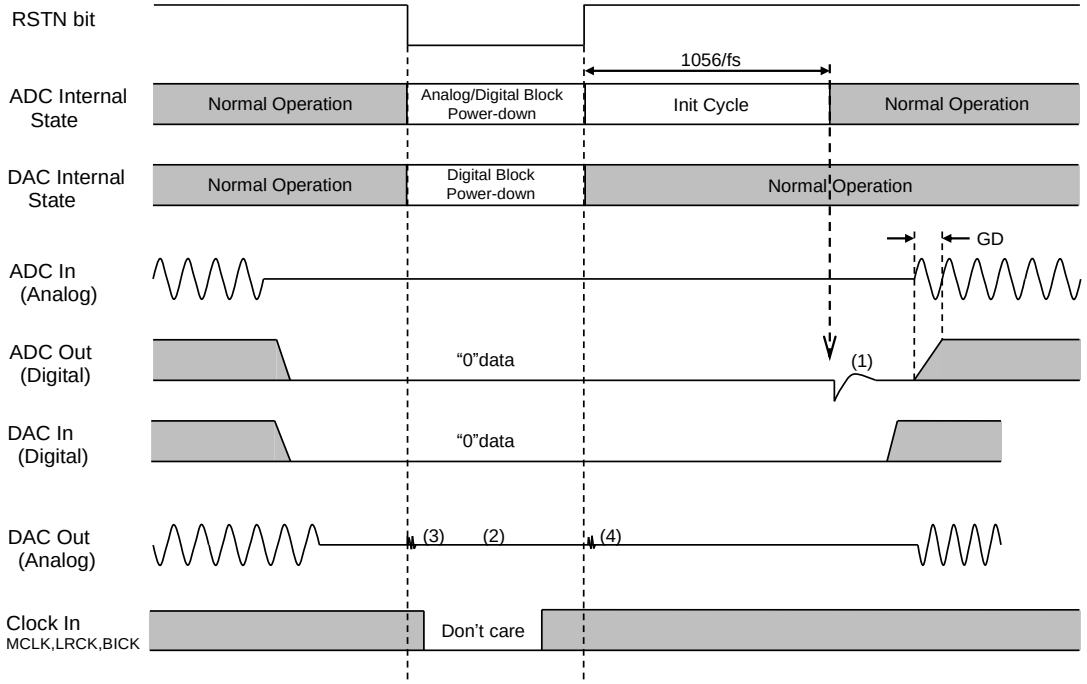
Notes:
(1) The PDN pin must be “L” when initially supplying AVDD and TVDD. PDN pin must be held “L” for more than 600 ns after AVDD and TVDD are powered up. The power-up sequence between AVDD and TVDD is not critical.
(2) The AVDRV output (generated by Internal LDO) is powered up after PDN pin is set “H”
(3) The internal PDN signal will rise within 10 ms (max.) after the PDN pin = “H,” at which point the host may access the control registers.
(4) External analog inputs can be provided after these input pins reach the analog common level (half of AVDD). It is necessary to wait for the HPF’s charge-up time. When the external capacitor is 1μF and the input impedance is 25 kΩ(typ.), τ = 25 ms. When ADC is powered up by setting PMAD1/2 bit = “0” →“1” it takes more than 100 ms (4 times of τ) for the HPF block to be fully charged .
(5) Pop noise from DAC analog output may occur after completing the initial cycle even if “0” data is input onto the audio serial interface.
(6) Mute the analog output externally if Pop noise (5) adversely affects system performance.
(7) Pop noise from ADC serial output may also occur after completing the initial cycle.

Figure 21. Power up/down sequence

3. The sequence on changing system clocks and registers

The system clock should be changed during standby, reset state or power-down (PDN pin = “L”) mode. It is possible to change the register values during the reset state. Release RSTN bit to “1” after the system clock is stable during reset state.

The digital blocks of ADC and DAC that operate the internal clock are powered down at reset state. ADC digital output is “L” and DAC analog output is half of AVDD at this state.



Notes:
(1) Pop noise may occur at the end of the initial cycle of the ADC.
(2) DAC output level is the half of AVDD at reset state.
(3) Pop noise may occur on the edge of RSTN bit = “1” →“0”. This noise is output even if “0” data is input.
(4) Pop noise may occur on the edge of RSTN bit = “0” →“1”. This noise is output even if “0” data is input.

Figure 22. reset sequence

9.5. MIC Gain AMP seting

The AK4619 has MIC Gain AMP for analog input. The gain for L and R channels can be independently selected by MGN1L[3:0], MGN1R[3:0], MGN2L[3:0] and MGN2R[3:0] bits. The volume is changed immediately upon changing the register setting. The maximum input voltage of the analog input pin could be 3.3 Vpp or less at AVDD = 3.3V. The setting of MIC Gain AMP should be adjusted not to exceed the input full-scale voltage of the ADCs.

Table 9. MIC Gain AMP Setting

Mode	MGN1L[3:0] MGN1R[3:0] MGN2L[3:0] MGN2R[3:0]	Input Gain	
0	0000	-6dB	
1	0001	-3dB	
2	0010	0dB	(default)
3	0011	3dB	
4	0100	6dB	
5	0101	9dB	
6	0110	12dB	
7	0111	15dB	
8	1000	18dB	
9	1001	21dB	
10	1010	24dB	
11	1011	27dB	
	others	N/A	

(N/A: Not available)

9.6. Start-up time on Analog input pin

The AK4619 starts charging coupling capacitors of analog input pins after setting PDN pin = “L” → “H”. The time constant will be 25 ms when the coupling capacitor is 1 μF and the input impedance is 25kΩ. Wait about 100 ms to fully charge, then power up ADC1/2 with PMAD1/2 bit = "0" →"1". If the wait time is less than 100 ms, a pop noise may appear immediately after the ADC start-up.

9.7. Analog input mode

Three analog input modes are available: single-ended input, differential input, and pseudo-differential input. These modes are selected by ADxLSEL[1:0], ADxRSEL[1:0] bits(x = 1, 2), (Table 10).

IN single-ended mode, 2:1 multiplexer is used to select which pin to route to each ADC input.

Pseudo-differential signals may not be applied in differential input mode.

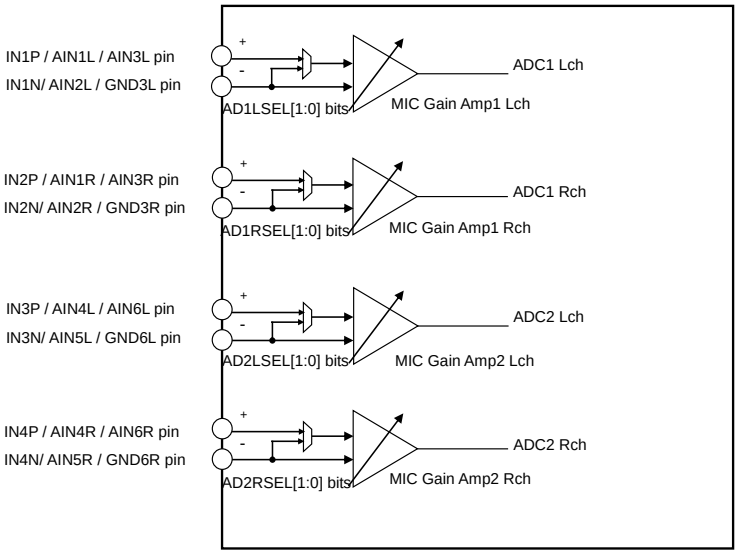


Figure 23. Analog Input Mode

Table 10. Analog Input Mode

Input Mode	AD1LSEL[1:0] bits	Input Pins	
Differential	00	IN1P, IN1N	(default)
Single-Ended1	01	AIN1L	
Single-Ended2	10	AIN2L	
Pseudo Differential	11	AIN3L, GND3L	

Input Mode	AD1RSEL[1:0] bits	Input Pins	
Differential	00	IN2P, IN2N	(default)
Single-Ended1	01	AIN1R	
Single-Ended2	10	AIN2R	
Pseudo Differential	11	AIN3R, GND3R	

Input Mode	AD2LSEL[1:0] bits	Input Pins	
Differential	00	IN3P, IN3N	(default)
Single-Ended1	01	AIN4L	
Single-Ended2	10	AIN5L	
Pseudo Differential	11	AIN6L, GND6L	

Input Mode	AD2RSEL[1:0] bits	Input Pins	
Differential	00	IN4P, IN4N	(default)
Single-Ended1	01	AIN4R	
Single-Ended2	10	AIN5R	
Pseudo Differential	11	AIN6R, GND6R	

Differential mode: A non-inverted analog signal is input to the INxP (x=1 to 4) pins and inverted analog signal is input to the INxN pins via coupling capacitors (Figure 24).

Single-ended mode: Analog signal is input to the AIN1L/R, AIN2L/R, AIN4L/R, AIN5L/R pins via coupling capacitors. (Figure 25) These inputs are connected to 2:1 multiplexers and can be selected with Single-Ended1 or Single-Ended2 inputs. Unused input pins should be left open.

Pseudo-differential mode: Analog signal is input to the AIN3L/R, AIN6L/R pins via coupling capacitors, and the GND3L/R, GND6L/R pins should be connected to ground via coupling capacitors (Figure 26). In pseudo-differential input mode, the common signal superimposed on the analog input and ground pin is eliminated.

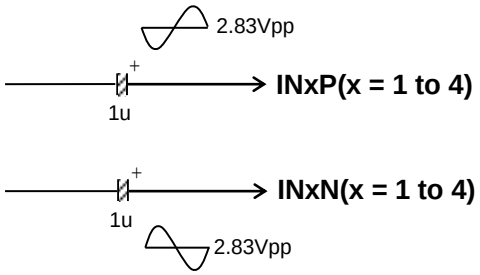


Figure 24. Differential Input Mode
(AD1LSEL[1:0] = AD1RSEL[1:0] = AD2LSEL[1:0] = AD2RSEL[1:0] = ”00”)

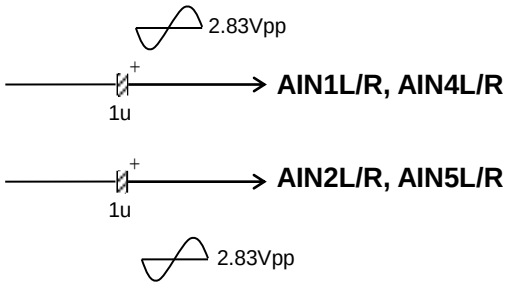


Figure 25. Single-ended Input Mode
(AD1LSEL[1:0] = AD1RSEL[1:0] = AD2LSEL[1:0] = AD2RSEL[1:0] = ”01” or “10”)

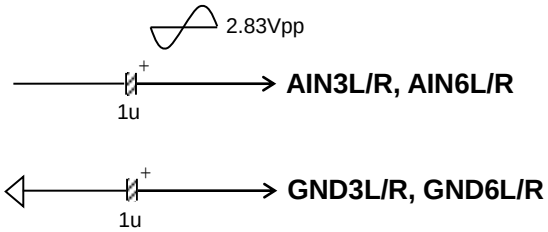


Figure 26. Pseudo-differential Input Mode
(AD1LSEL[1:0] = AD1RSEL[1:0] = AD2LSEL[1:0] = AD2RSEL[1:0] = ”11”)

9.8. ADC (ADC1, ADC2)

1. ADC Block high pass filter

The AK4619 has a digital high pass filter (HPF) for DC offset cancelling of both ADC inputs. The cut-off frequency of the HPF is about 0.9 Hz (fs = 48kHz), depending on operating frequency.

2. ADC digital volume

The AK4619 has digital volume controls (256 levels, 0.5dB steps) for the Lch and Rch of each ADC.

Table 11. ADC Digital Volume Setting

VOLAD1L[7:0], VOLAD1R[7:0] VOLAD2L[7:0], VOLAD2R[7:0]	Attenuation Level	
00h	+24.0dB	
01h	+23.5dB	
02h	+23.0dB	
:	:	
2Fh	+0.5dB	
30h	0.0dB	(default)
31h	−0.5dB	
:	:	
FDh	−102.5dB	
FEh	−103.0dB	
FFh	Mute (−∞)	

The transition interval time per 1 step (e.g. 30h to 31h) is selected by ATSPAD bit.

Table 12. ADC Volume Level Transition Time

Mode	ATSPAD bit	ATT speed	
0	0	4/fs	(default)
1	1	16/fs	

The transition process between setting values is a soft transition thus no switching noise occurs. It takes 1020/fs (21.3 ms at fs= 48 kHz) to go from 0x00 to 0xFF (MUTE) in Mode 0. If the PDN pin goes to “L”, the digital volume setting for both ADC channels is initialized to 0x30.

Table 13. ADC Volume Transition Time from 0x00 to 0xFF

ATSPAD bit	00h ↔ FFh Transition Time			
	LRCK Cycle	fs = 48 kHz	fs = 8 kHz	
0	1020/fs	21.3 ms	127.5 ms	(default)
1	4080/fs	85.0 ms	510.0 ms	

Table 14. ADC Digital Volume Settings

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB
00h	24.0	20h	8.0	40h	-8.0	60h	-24.0	80h	-40.0	A0h	-56.0	C0h	-72.0	E0h	-88.0
01h	23.5	21h	7.5	41h	-8.5	61h	-24.5	81h	-40.5	A1h	-56.5	C1h	-72.5	E1h	-88.5
02h	23.0	22h	7.0	42h	-9.0	62h	-25.0	82h	-41.0	A2h	-57.0	C2h	-73.0	E2h	-89.0
03h	22.5	23h	6.5	43h	-9.5	63h	-25.5	83h	-41.5	A3h	-57.5	C3h	-73.5	E3h	-89.5
04h	22.0	24h	6.0	44h	-10.0	64h	-26.0	84h	-42.0	A4h	-58.0	C4h	-74.0	E4h	-90.0
05h	21.5	25h	5.5	45h	-10.5	65h	-26.5	85h	-42.5	A5h	-58.5	C5h	-74.5	E5h	-90.5
06h	21.0	26h	5.0	46h	-11.0	66h	-27.0	86h	-43.0	A6h	-59.0	C6h	-75.0	E6h	-91.0
07h	20.5	27h	4.5	47h	-11.5	67h	-27.5	87h	-43.5	A7h	-59.5	C7h	-75.5	E7h	-91.5
08h	20.0	28h	4.0	48h	-12.0	68h	-28.0	88h	-44.0	A8h	-60.0	C8h	-76.0	E8h	-92.0
09h	19.5	29h	3.5	49h	-12.5	69h	-28.5	89h	-44.5	A9h	-60.5	C9h	-76.5	E9h	-92.5
0Ah	19.0	2Ah	3.0	4Ah	-13.0	6Ah	-29.0	8Ah	-45.0	AAh	-61.0	CAh	-77.0	EAh	-93.0
0Bh	18.5	2Bh	2.5	4Bh	-13.5	6Bh	-29.5	8Bh	-45.5	ABh	-61.5	CBh	-77.5	EBh	-93.5
0Ch	18.0	2Ch	2.0	4Ch	-14.0	6Ch	-30.0	8Ch	-46.0	ACh	-62.0	CCh	-78.0	ECh	-94.0
0Dh	17.5	2Dh	1.5	4Dh	-14.5	6Dh	-30.5	8Dh	-46.5	ADh	-62.5	CDh	-78.5	EDh	-94.5
0Eh	17.0	2Eh	1.0	4Eh	-15.0	6Eh	-31.0	8Eh	-47.0	AEh	-63.0	CEh	-79.0	EEh	-95.0
0Fh	16.5	2Fh	0.5	4Fh	-15.5	6Fh	-31.5	8Fh	-47.5	AFh	-63.5	CFh	-79.5	EFh	-95.5
10h	16.0	30h	0.0	50h	-16.0	70h	-32.0	90h	-48.0	B0h	-64.0	D0h	-80.0	F0h	-96.0
11h	15.5	31h	-0.5	51h	-16.5	71h	-32.5	91h	-48.5	B1h	-64.5	D1h	-80.5	F1h	-96.5
12h	15.0	32h	-1.0	52h	-17.0	72h	-33.0	92h	-49.0	B2h	-65.0	D2h	-81.0	F2h	-97.0
13h	14.5	33h	-1.5	53h	-17.5	73h	-33.5	93h	-49.5	B3h	-65.5	D3h	-81.5	F3h	-97.5
14h	14.0	34h	-2.0	54h	-18.0	74h	-34.0	94h	-50.0	B4h	-66.0	D4h	-82.0	F4h	-98.0
15h	13.5	35h	-2.5	55h	-18.5	75h	-34.5	95h	-50.5	B5h	-66.5	D5h	-82.5	F5h	-98.5
16h	13.0	36h	-3.0	56h	-19.0	76h	-35.0	96h	-51.0	B6h	-67.0	D6h	-83.0	F6h	-99.0
17h	12.5	37h	-3.5	57h	-19.5	77h	-35.5	97h	-51.5	B7h	-67.5	D7h	-83.5	F7h	-99.5
18h	12.0	38h	-4.0	58h	-20.0	78h	-36.0	98h	-52.0	B8h	-68.0	D8h	-84.0	F8h	-100.0
19h	11.5	39h	-4.5	59h	-20.5	79h	-36.5	99h	-52.5	B9h	-68.5	D9h	-84.5	F9h	-100.5
1Ah	11.0	3Ah	-5.0	5Ah	-21.0	7Ah	-37.0	9Ah	-53.0	BAh	-69.0	DAh	-85.0	FAh	-101.0
1Bh	10.5	3Bh	-5.5	5Bh	-21.5	7Bh	-37.5	9Bh	-53.5	BBh	-69.5	DBh	-85.5	FBh	-101.5
1Ch	10.0	3Ch	-.6.0	5Ch	-22.0	7Ch	-38.0	9Ch	-54.0	BCh	-70.0	DCh	-86.0	FCh	-102.0
1Dh	9.5	3Dh	-6.5	5Dh	-22.5	7Dh	-38.5	9Dh	-54.5	BDh	-70.5	DDh	-86.5	FDh	-102.5
1Eh	9.0	3Eh	-7.0	5Eh	-23.0	7Eh	-39.0	9Eh	-55.0	BEh	-71.0	DEh	-87.0	FEh	-103.0
1Fh	8.5	3Fh	-7.5	5Fh	-23.5	7Fh	-39.5	9Fh	-55.5	BFh	-71.5	DFh	-87.5	FFh	Mute

3. ADC Soft Mute Operation

The ADC block has a digital soft mute circuit. The output signal is attenuated to -∞ by setting AD1MUTE bit or AD2MUTE bit to “1”. When the AD1MUTE bit or AD2MUTE bit returns to “0”, mute is cancelled, and the output attenuation level gradually changes to the ATT setting level in “ATT setting level x ATT transition time”. If the soft mute is cancelled before attenuating all the way to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to the original volume setting level during the same cycle. The soft mute is useful for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 828/fs (ATT speed: 4/fs) to go from 0dB to -∞ and from -∞ to 0dB. The soft mute function is available while an ADC is in operation. Setting the PDN pin = “L” initializes the attenuation value.

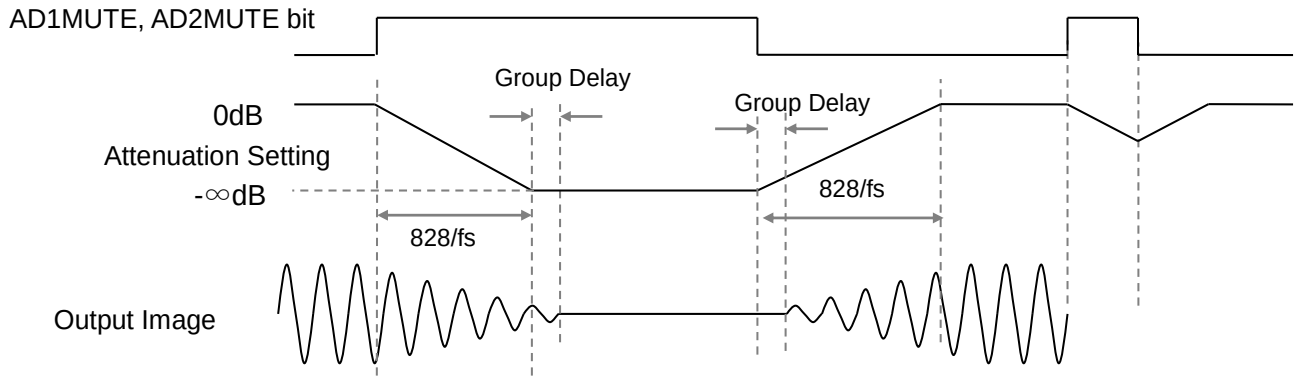


Figure 27. ADC Soft Mute

The input channel should be switched only after enabling the soft mute function, in order to avoid the switching noise of the input selector.

e.g.) ADC Input Channel Switching Sequence (Transition Time for 1 step = 4/fs, fs = 48kHz)

(1) Enable Soft Mute AD1/2MUTE bit = “0” → “1”

(2) Wait until −∞ dB Attenuation Level (0xFF−0x36) × 4/fs = (255−54) × 4 / (48×10$^{3)}$ = 16.75 ms

(3) Switch Input channel ADxL/RSEL[1:0] bits = “01” → “10”(x=1, 2)

(4) Wait until Stable ADC Input 200 ms min.

(5) Release Soft Mute AD1/2MUTE bit = “1” → “0”

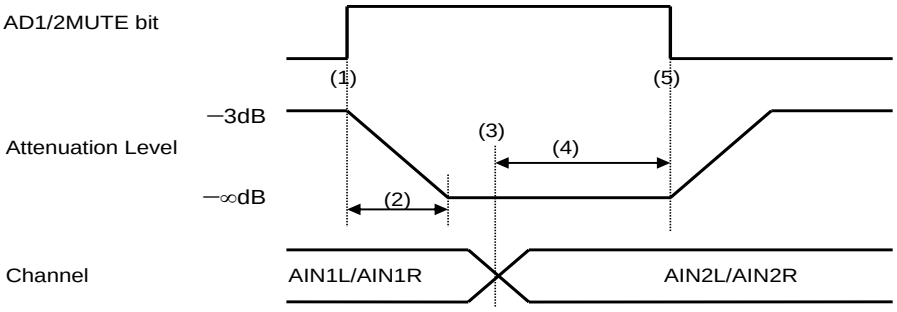


Figure 28. ADC Input Channel Switching Example

4. ADC Digital Filter

The AK4619's ADC block has five kinds of digital filters (Table 15, Table 16). AD1VO bit, AD1SD bit and AD1SL are used to configure ADC1's digital filter. AD2VO bit, AD2SD bit and AD2SL bit are used for ADC2 digital filter settings. Note that when Voice Filter is selected, maximum fs = 48 kHz.

Table 15. ADC1 Digital Filter Selection

Mode	AD1VO bit	AD1SD bit	AD1SL bit	Digital filter	
0	0	0	0	Sharp Roll-Off Filter	(default)
1	0	0	1	Slow Roll-Off Filter	
2	0	1	0	Short Delay Sharp Roll-Off Filter	
3	0	1	1	Short Delay Slow Roll-Off Filter	
4	1	x	x	Voice Filter	

x:Don't Care

Table 16. ADC2 Digital Filter Selection

Mode	AD2VO bit	AD2SD bit	AD2SL bit	Digital filter	
0	0	0	0	Sharp Roll-Off Filter	(default)
1	0	0	1	Slow Roll-Off Filter	
2	0	1	0	Short Delay Sharp Roll-Off Filter	
3	0	1	1	Short Delay Slow Roll-Off Filter	
4	1	x	x	Voice Filter	

x:Don't Care

9.9. DAC source multiplexers

The AK4619 has two 4:1 multiplexers, one at the input to each DAC. These multiplexers may be used to route audio from the SDIN pins to the DAC input, or to loop audio data directly from ADC outputs to DAC inputs. (Figure 29)

These DAC source multiplexers are controllable via their respective DAC1SEL[1:0] bits (Table 17) DAC2SEL[1:0] bits (Table 18).

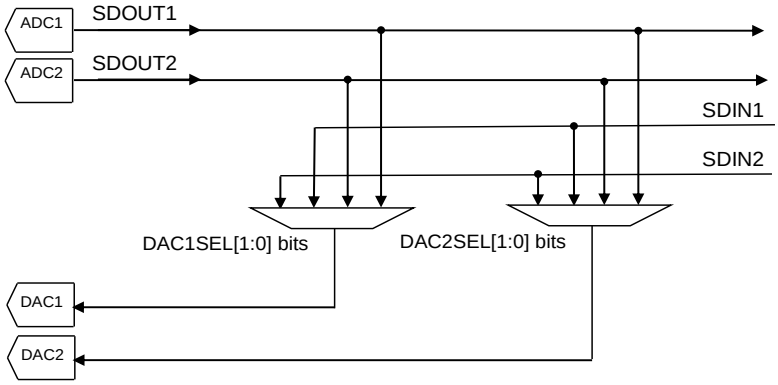


Figure 29. DAC1/2 source multiplexer

Table 17. DAC1 source multiplexer setting

DAC1SEL[1:0] bits	DAC1 Input	
00	SDIN1	(default)
01	SDIN2	
10	SDOUT1	
11	SDOUT2	

Table 18. DAC2 source multiplexer setting

DAC2SEL[1:0] bits	DAC2 Input	
00	SDIN1	
01	SDIN2	(default)
10	SDOUT1	
11	SDOUT2	

9.10. DAC (DAC1, DAC2)

1. DAC Digital Volume

The AK4619 has digital volume controls (256 levels, 0.5dB steps) for the Lch and Rch of each DAC.

Table 19. DAC Digital Volume Setting

VOLDA1L[7:0], VOLDA1R[7:0] VOLDA2L[7:0], VOLDA2R[7:0]	Attenuation Level	
00h	+12.0 dB	
01h	+11.5 dB	
02h	+11.0 dB	
:	:	
17h	+0.5 dB	
18h	0.0 dB	(default)
19h	−0.5 dB	
:	:	
FDh	−114.5 dB	
FEh	−115.0d B	
FFh	Mute (−∞)	

The transition interval time per 1 step (e.g. 18h to 19h) is selected by ATSPDA bit.

Table 20. DAC Volume Transition Time Setting

MODE	ATSPDA	ATT speed	
0	0	4/fs	(default)
1	1	16/fs	

The transition process between setting values is a soft transition, thus no switching noise. It takes 1020/fs (21.3ms at fs=48kHz) to go from 0x00 to 0xFF(MUTE) in Mode 0. If the PDN pin goes to “L”, the digital volume setting for both DAC channels is initialized to default (0x18).

Table 21. DAC Volume Transition Time (0x00 ↔ 0xFF)

ATSPDA	00h ↔ FFh Transition Time			
	LRCK cycle	fs = 48 kHz	fs = 8 kHz	
0	1020/fs	21.3 ms	127.5 ms	(default)
1	4080/fs	85.0 ms	510.0 ms	

Table 22. DAC Digital Volume Level Setting

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB
00h	12.0	20h	-4.0	40h	-20.0	60h	-36.0	80h	-52.0	A0h	-68.0	C0h	-84.0	E0h	-100.0
01h	11.5	21h	-4.5	41h	-20.5	61h	-36.5	81h	-52.5	A1h	-68.5	C1h	-84.5	E1h	-100.5
02h	11.0	22h	-5.0	42h	-21.0	62h	-37.0	82h	-53.0	A2h	-69.0	C2h	-85.0	E2h	-101.0
03h	10.5	23h	-5.5	43h	-21.5	63h	-37.5	83h	-53.5	A3h	-69.5	C3h	-85.5	E3h	-101.5
04h	10.0	24h	-.6.0	44h	-22.0	64h	-38.0	84h	-54.0	A4h	-70.0	C4h	-86.0	E4h	-102.0
05h	9.5	25h	-6.5	45h	-22.5	65h	-38.5	85h	-54.5	A5h	-70.5	C5h	-86.5	E5h	-102.5
06h	9.0	26h	-7.0	46h	-23.0	66h	-39.0	86h	-55.0	A6h	-71.0	C6h	-87.0	E6h	-103.0
07h	8.5	27h	-7.5	47h	-23.5	67h	-39.5	87h	-55.5	A7h	-71.5	C7h	-87.5	E7h	-103.5
08h	8.0	28h	-8.0	48h	-24.0	68h	-40.0	88h	-56.0	A8h	-72.0	C8h	-88.0	E8h	-104.0
09h	7.5	29h	-8.5	49h	-24.5	69h	-40.5	89h	-56.5	A9h	-72.5	C9h	-88.5	E9h	-104.5
0Ah	7.0	2Ah	-9.0	4Ah	-25.0	6Ah	-41.0	8Ah	-57.0	AAh	-73.0	CAh	-89.0	EAh	-105.0
0Bh	6.5	2Bh	-9.5	4Bh	-25.5	6Bh	-41.5	8Bh	-57.5	ABh	-73.5	CBh	-89.5	EBh	-105.5
0Ch	6.0	2Ch	-10.0	4Ch	-26.0	6Ch	-42.0	8Ch	-58.0	ACh	-74.0	CCh	-90.0	ECh	-106.0
0Dh	5.5	2Dh	-10.5	4Dh	-26.5	6Dh	-42.5	8Dh	-58.5	ADh	-74.5	CDh	-90.5	EDh	-106.5
0Eh	5.0	2Eh	-11.0	4Eh	-27.0	6Eh	-43.0	8Eh	-59.0	AEh	-75.0	CEh	-91.0	EEh	-107.0
0Fh	4.5	2Fh	-11.5	4Fh	-27.5	6Fh	-43.5	8Fh	-59.5	AFh	-75.5	CFh	-91.5	EFh	-107.5
10h	4.0	30h	-12.0	50h	-28.0	70h	-44.0	90h	-60.0	B0h	-76.0	D0h	-92.0	F0h	-108.0
11h	3.5	31h	-12.5	51h	-28.5	71h	-44.5	91h	-60.5	B1h	-76.5	D1h	-92.5	F1h	-108.5
12h	3.0	32h	-13.0	52h	-29.0	72h	-45.0	92h	-61.0	B2h	-77.0	D2h	-93.0	F2h	-109.0
13h	2.5	33h	-13.5	53h	-29.5	73h	-45.5	93h	-61.5	B3h	-77.5	D3h	-93.5	F3h	-109.5
14h	2.0	34h	-14.0	54h	-30.0	74h	-46.0	94h	-62.0	B4h	-78.0	D4h	-94.0	F4h	-110.0
15h	1.5	35h	-14.5	55h	-30.5	75h	-46.5	95h	-62.5	B5h	-78.5	D5h	-94.5	F5h	-110.5
16h	1.0	36h	-15.0	56h	-31.0	76h	-47.0	96h	-63.0	B6h	-79.0	D6h	-95.0	F6h	-111.0
17h	0.5	37h	-15.5	57h	-31.5	77h	-47.5	97h	-63.5	B7h	-79.5	D7h	-95.5	F7h	-111.5
18h	0.0	38h	-16.0	58h	-32.0	78h	-48.0	98h	-64.0	B8h	-80.0	D8h	-96.0	F8h	-112.0
19h	-0.5	39h	-16.5	59h	-32.5	79h	-48.5	99h	-64.5	B9h	-80.5	D9h	-96.5	F9h	-112.5
1Ah	-1.0	3Ah	-17.0	5Ah	-33.0	7Ah	-49.0	9Ah	-65.0	BAh	-81.0	DAh	-97.0	FAh	-113.0
1Bh	-1.5	3Bh	-17.5	5Bh	-33.5	7Bh	-49.5	9Bh	-65.5	BBh	-81.5	DBh	-97.5	FBh	-113.5
1Ch	-2.0	3Ch	-18.0	5Ch	-34.0	7Ch	-50.0	9Ch	-66.0	BCh	-82.0	DCh	-98.0	FCh	-114.0
1Dh	-2.5	3Dh	-18.5	5Dh	-34.5	7Dh	-50.5	9Dh	-66.5	BDh	-82.5	DDh	-98.5	FDh	-114.5
1Eh	-3.0	3Eh	-19.0	5Eh	-35.0	7Eh	-51.0	9Eh	-67.0	BEh	-83.0	DEh	-99.0	FEh	-115.0
1Fh	-3.5	3Fh	-19.5	5Fh	-35.5	7Fh	-51.5	9Fh	-67.5	BFh	-83.5	DFh	-99.5	FFh	Mute

2. DAC Soft Mute Operation

The DAC block has a digital soft mute circuit. Setting DA1MUTE bit or DA2MUTE bit to “1” attenuates the signal to −∞. When the DA1MUTE bit or DA2MUTE bit returns to “0”, the mute is cancelled, and the output attenuation level gradually changes to the ATT setting level in “ATT setting level x ATT transition time”. If the soft mute is cancelled before attenuating to −∞ after starting the operation, the attenuation is discontinued and the volume level returns to the original volume setting level during the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 924/fs (ATT speed: 4/fs) from 0dB to −∞ and from −∞ to 0dB. The soft-mute function is available while the DACs are in operation. Setting the PDN pin “L” initializes the attenuation value.

The DAC block is reset by setting RSTN bit = “0” or PMDA1 bit = PMDA2 bit = “0”. A pop noise may occur when resetting the DAC block and releasing the reset. The output should therefore be muted externally if the pop noise adversely affects the system performance.

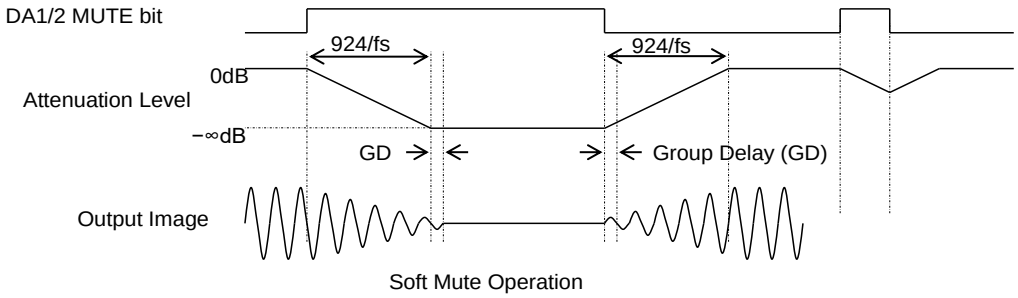


Figure 30. DAC Soft Mute Operation

3. DAC Digital Filter

The AK4619's DAC block has four kinds of digital filters. DA1SD and DA1SL bits are used for DAC1 digital filter selection. DA2SD and DA2SL bits are used for DAC2 digital filter selection.

Table 23. DAC1 Digital Filter Selection

Mode	DA1SD bit	DA1SL bit	Digital Filter	
0	0	0	Sharp Roll-Off Filter	
1	0	1	Slow Roll-Off Filter	
2	1	0	Short Delay Sharp Roll-Off Filter	(default)
3	1	1	Short Delay Slow Roll-Off Filter	

Table 24. DAC2 Digital Filter Selection

Mode	DA2SD bit	DA2SL bit	Digital Filter	
0	0	0	Sharp Roll-Off Filter	
1	0	1	Slow Roll-Off Filter	
2	1	0	Short Delay Sharp Roll-Off Filter	(default)
3	1	1	Short Delay Slow Roll-Off Filter	

4. De-emphasis Filter

The AK4619 has digital de-emphasis filters (tc=50/15μs) - implemented as IIR filters – for three sampling frequencies (32 kHz, 44.1 kHz, 48 kHz). A de-emphasis filter is enabled for each DAC in the selected frequency by DEMx[1:0] bits (Table 25). De-emphasis filters operate correctly only for the frequencies shown in Table 25. De-emphasis filters should be set to the default setting (DEMx[1:0]="01", x=1, 2) for other sampling frequencies.

When operating De-emphasis Filter in a sampling frequency other than those shown below, the selected filter frequency characteristics will track the actual sampling frequency.

e.g. The cutoff frequency is around 1kHz when the filter mode is 48 kHz mode. It will be around 2 kHz if the actual sampling frequency is 96 kHz and will be around 0.5 kHz if the actual sampling frequency is 24 kHz.

Table 25. De-emphasis Filter Control

DEMx[1] bit	DEMx[0] bit	Mode	
0	0	44.1 kHz	
0	1	OFF	(default)
1	0	48 kHz	
1	1	32 kHz	

9.11. µP Interface Setting and Pin State

The AK4619 supports SPI, I²C interfaces.

When using I²C interface, the CSN pin must be pulled up or down since it becomes a chip address pin. After a power-down release, the AK4619 is set to I²C interface mode.

When using SPI interface, release the power-down state of the AK4619 while the CSN pin is "H". SPI interface mode becomes enabled by sending the dummy command mentioned below. To send the dummy command, input "0xDE → 0xADDA → 0x7A" to the SI pin after a falling edge of CAD/CSN (while it is kept "L"). The data is in MSB first format.

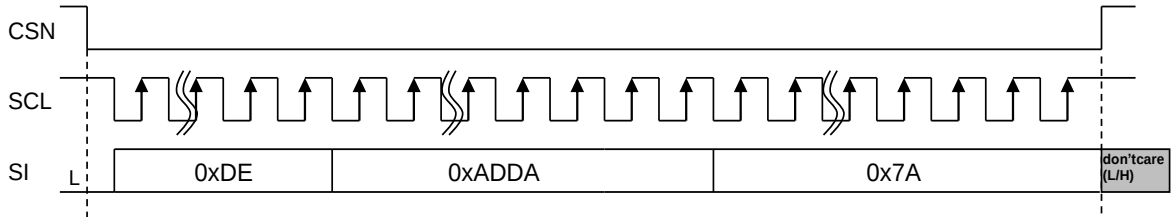


Figure 31. Dummy command switching SPI mode

Status of the SDA/SO, SCL/SCLK and SI pins are shown on Table 26 depending on PDN pin and the CAD/CSN state.

Table 26. µP Pin State

	PDN pin	CAD/CSN pin	SDA/SO pin	SCL/SCLK pin	SI pin
I²C Interface	L	CAD pin = "L" or "H"	Hi-Z	Input	SI pin = "L"
	H	CAD pin = "L"	function	function	
		CAD pin = "H"			
SPI Interface	L	CSN pin = "H"	Hi-Z	input	input
	H	CSN pin = "L"	function	function	function
		CSN pin = "H"	Hi-Z	input	input

9.12. SPI Interface

1. Configuration

The access format consists of Command code (8bits) + Address (16bits) + Data (MSB first).
The SO pin output should be pulled-down/pulled-up externally when using the AK4619 in SPI mode.

Table 27. µP Interface Format

	Bit Length	Description
Command code	8	MSB bit is an R/W flag. The following 7 bits indicate access area
Address	16	Address is fixed to 16bits.
Data	8-bit x N	Read/Write Data N: Cycle number of byte to Write/Read cycle.

Write Operation

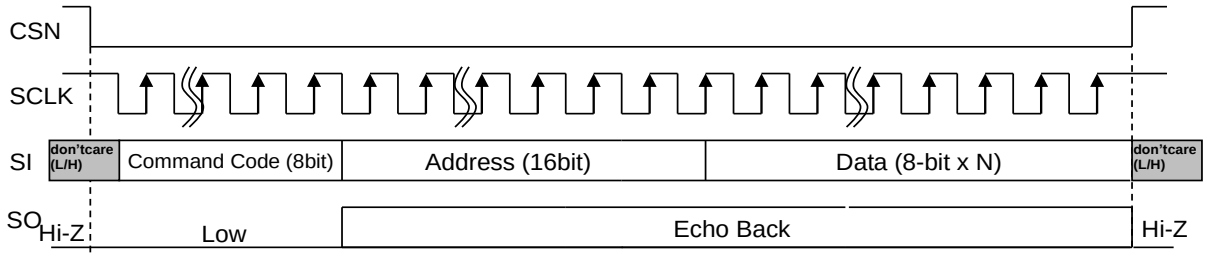


Figure 32. SPI Interface Format (Write)

Read operation

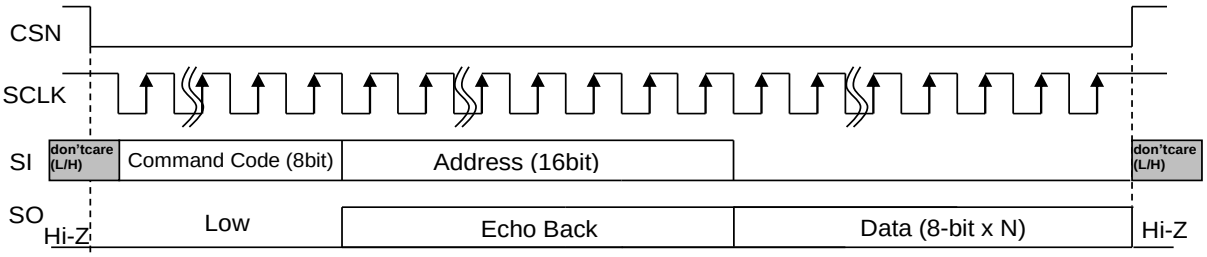


Figure 33. SPI Interface Format (Read)

2. Command Code

Command Code Format

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R/W flag	100			0011			

R/W flag: write “1”, read “0”
Command codes other than the above cannot be set.

3. Register Write and Read

Register Write

(1) Control Register Write

Field	Write data
COMMAND Code	0xC3
ADDRESS HIGH	0x00
ADDRESS_LOW	A7 to A0
DATA	D7 to D0
	When data larger than 1 byte is written, the address is incremented.

Register Read

(1) Control Register Read

Field	Write data	Readout data
COMMAND Code	0x43	
ADDRESS_HIGH	0x00	
ADDRESS LOW	A7 to A0	
DATA		D7 to D0
	When data larger than 1 byte is read, the address is incremented.	

4. Echo-back

The AK4619 has an echo-back function that outputs the written data sequentially on the SO pin.

1. Write

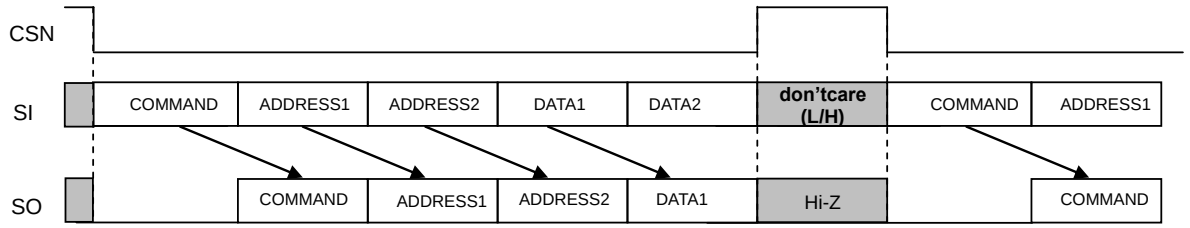


Figure 34. Echo-back Writing (SPI)

The input data driven into the SI pin is echoed out on the SO pin by shifting 1-byte to the right. The last 1- byte written data is not echoed-back.

2. Read

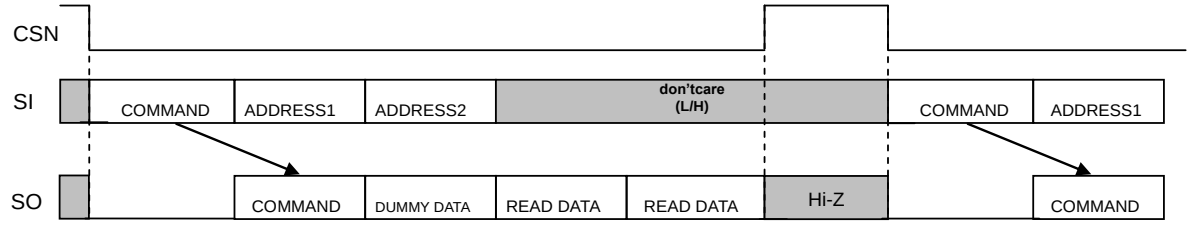


Figure 35. Echo-back Reading (SPI)

Data is not echoed back completely in read operation. Read data is output with priority over write data.

9.13. I²C bus control interface

The AK4619 registers may be accessed via the I²C bus. The AK4619 supports fast-mode I²C-bus (max: 400kHz). Connect the pull-up resistors on the SDA and SCL pins to TVDD or less.

1. WRITE Operation

Figure 36 shows the data transfer sequence of the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 42). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit , which is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0010000”. If the slave address matches that of the AK4619, the AK4619 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 43). R/W bit = “1” indicates that a read operation is to be executed. “0” indicates that a write operation is to be executed.

The second byte consists of the control register address of the AK4619. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 38). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 39). The AK4619 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 42).

The AK4619 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4619 generates an acknowledge and awaits the next data. The master can transmit more than one byte (as opposed to terminating the write cycle after the first data byte is transferred). After receiving each data packet, the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 14H prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 44) except for the START and STOP conditions.

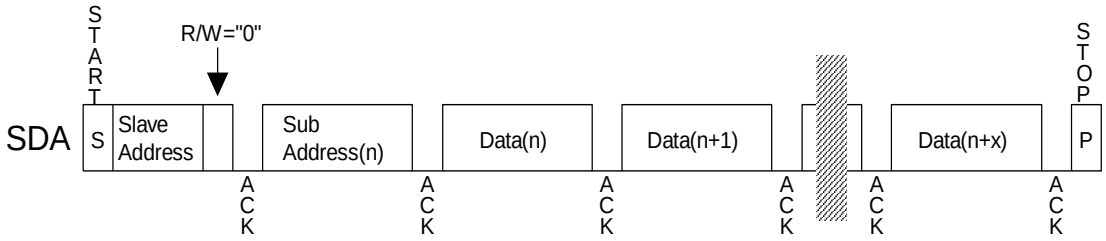


Figure 36. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	CAD	R/W

(CAD bit is set by CAD pin)

Figure 37. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 38. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 39. Byte Structure after the second byte

2. READ operation

Set the R/W bit = “1” for READ operation of the AK4619. After the transmission of data, the master can read the next address’ data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet, the internal 7-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 14H prior to generating the stop condition, the address counter will “roll over” to 00H and the data of 00H will be read out.

The AK4619 supports two basic read operations: the CURRENT ADDRESS READ, the RANDOM ADDRESS READ.

2-1. Current Address Read

The AK4619 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4619 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4619 ceases transmission.

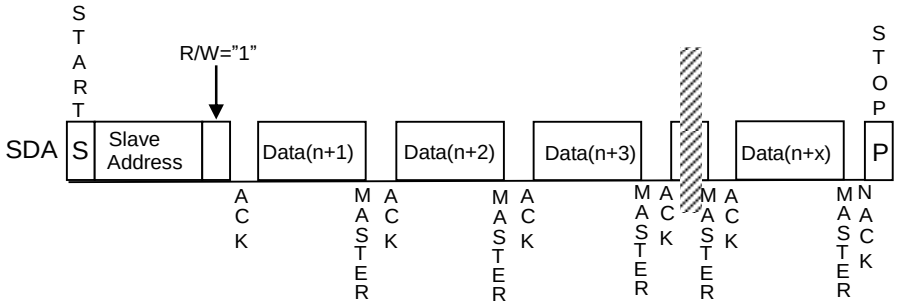


Figure 40. CURRENT ADDRESS READ

2-2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit = “1”, the master must execute a “dummy” write operation first in order to identify the control register address. The master issues a start condition request, a slave address (R/W bit = “0”) and then the sub address (control register address) to read. After the register address is acknowledged, the master immediately reissues another start condition request as well as the slave address with the R/W bit = “1”. The AK4619 then generates an acknowledge, 1 byte of data, and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4619 ceases transmission.

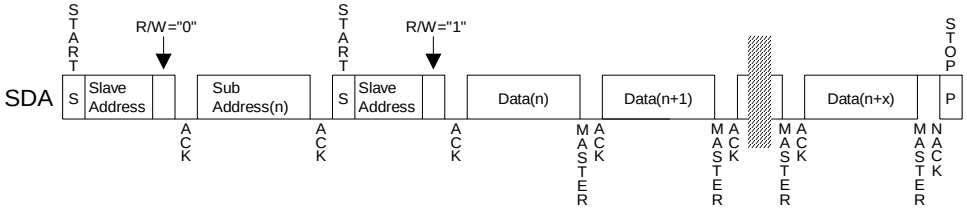


Figure 41. RANDOM ADDRESS READ

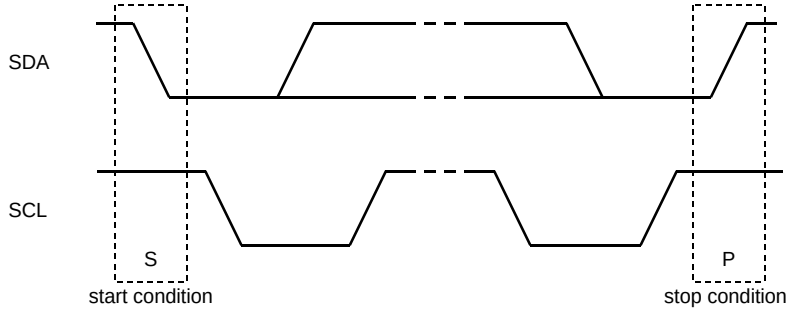


Figure 42. START and STOP Conditions

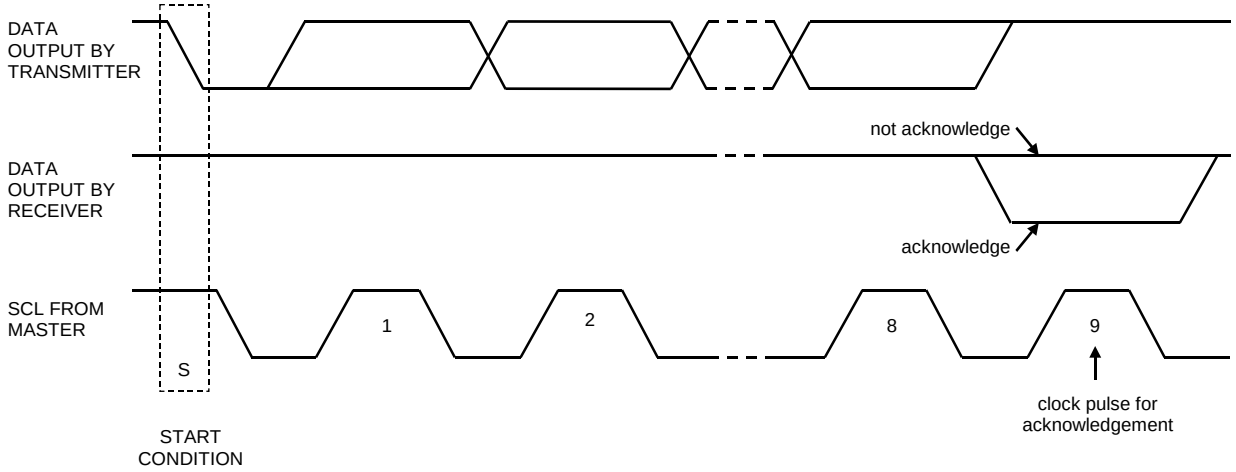


Figure 43. Acknowledge on the I^2C-Bus

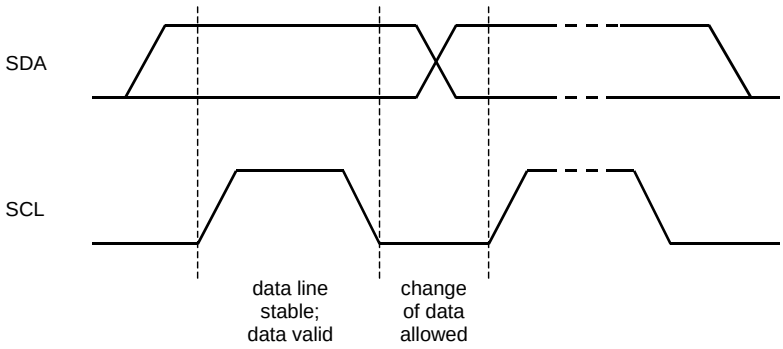


Figure 44. Bit Transfer on the I^2C-Bus

9.14. Register Map

1. Description of Register Map

When the PDN pin goes to “L” → “H”, the registers are initialized to their default values.
The bits listed “0” must write “0”.
Writing to addresses from 15H to 7FH is prohibited.

2. Register Map Table

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default [Hex]
00	Power Management	0	0	PMAD2	PMAD1	0	PMDA2	PMDA1	RSTN	00
01	Audio I/F Format	TDM	DCF[2:0]			DSL[1:0]		BCKP	SDOPH	0C
02	Audio I/F Format	0	0	0	SLOT	DIDL[1:0]		DODL[1:0]		0C
03	System Clock Setting	0	0	0	0	0	FS[2:0]			00
04	MIC AMP Gain	MGN1L[3:0]				MGN1R[3:0]				22
05	MIC AMP Gain	MGN2L[3:0]				MGN2R[3:0]				22
06	ADC1 Lch Digital Volume	VOLAD1L[7:0]								30
07	ADC1 Rch Digital Volume	VOLAD1R[7:0]								30
08	ADC2 Lch Digital Volume	VOLAD2L[7:0]								30
09	ADC2 Rch Digital Volume	VOLAD2R[7:0]								30
0A	ADC Digital Filter Setting	0	AD2VO	A2DSD	AD2SL	0	AD1VO	AD1SD	AD1SL	00
0B	ADC Analog Input Setting	AD1LSEL[1:0]		AD1RSEL[1:0]		AD2LSEL[1:0]		AD2RSEL[1:0]		00
0C	Reserved	0	0	0	0	0	0	0	0	00
0D	ADC Mute & HPF Control	ATSPAD	AD2MUTE	AD1MUTE	0	0	AD2HPFN	AD1HPFN	0	00
0E	DAC1 Lch Digital Volume	VOLDA1L[7:0]								18
0F	DAC1 Rch Digital Volume	VOLDA1R[7:0]								18
10	DAC2 Lch Digital Volume	VOLDA2L[7:0]								18
11	DAC2 Rch Digital Volume	VOLDA2R[7:0]								18
12	DAC Input Select Setting	0	0	0	0	DAC2SEL[1:0]		DAC1SEL[1:0]		04
13	DAC De-Emphasis Setting	0	0	0	0	DEM2[1:0]		DEM1[1:0]		05
14	DAC Mute & Filter Setting	ATSPDA	0	DA2MUTE	DA1MUTE	DA2SD	DA2SL	DA1SD	DA1SL	0A

3. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00	Power Management	0	0	PMAD2	PMAD1	0	PMDA2	PMDA1	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMAD2: Power management of ADC2
0: Power-down (default)
1: Normal Operation

PMAD1: Power management of ADC1
0: Power-down (default)
1: Normal Operation

PMDA2: Power management of DAC2
0: Power-down (default)
1: Normal Operation

PMDA1: Power management of DAC1
0: Power-down (default)
1: Normal Operation

RSTN: Internal timing reset
0: Reset (default) ADC1, ADC2, DAC1, DAC2 held in reset state.
1: Release reset state (Normal Operation)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01	Audio I/F Format	TDM	DCF[1:0]			DSL[1:0]		BCKP	SDOPH
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

TDM: TDM Mode Setting (Table 2)
Default: “0” (Stereo Mode)

DCF [2:0]: Audio I/F Format Setting (Table 2)
Default: “000” (I^2S compatible)

DSL [1:0]: Slot Length Setting (Table 4)
Default: “11” (32bit)

BCKP: BICK Edge Setting (Table 5)
0: Falling (default)
1: Rising

SDOPH: Fast Mode Setting of SDOUT1/2 Output (*32)
0: Slow mode (default)
1: Fast mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02	Reset Control	0	0	0	SLOT	DIDL[1:0]		DODL[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

SLOT: Start Position Setting of Word Transferring for Second and Succeeding slot of SDIN1/2, SDOUT1/2
0: LRCK Edge Basis (default)
1: Slot Length Basis

DIDL [1:0]: SDIN1/2 Word Length Setting (Table 6)
Default: “11” (32-bit)

DODL [1:0]: SDOUT1/2 Word Length Setting (Table 7)
Default: “00” (24-bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03	System Clock Setting	0	0	0	0	0	FS[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	000		

FS [2:0]: Master Clock frequency mode and sampling Frequency range setting (Table 1)
Default: “000” (MCLK = 256fs, 8 kHz ≦ fs ≦ 48 kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04	MIC AMP Gain	MGN1L[3:0]				MGN1R[3:0]			
05	MIC AMP Gain	MGN2L[3:0]				MGN2R[3:0]			
R/W		R/W				R/W			
Default		0010				0010			

MGN1L[3:0]: ADC1 Lch MIC Gain AMP setting (Table 9)
Default: “0010” (0dB)

MGN1R[3:0]: ADC1 Rch MIC Gain AMP setting(Table 9)
Default: “0010” (0dB)

MGN2L[3:0]: ADC2 Lch MIC Gain AMP setting(Table 9)
Default: “0010” (0dB)

MGN2R[3:0]: ADC2 Rch MIC Gain AMP setting(Table 9)
Default: “0010” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06	ADC1 Lch Digital Volume	VOLAD1L[7:0]							
07	ADC1 Rch Digital Volume	VOLAD1R[7:0]							
08	ADC2 Lch Digital Volume	VOLAD2L[7:0]							
09	ADC2 Rch Digital Volume	VOLAD2R[7:0]							
R/W		R/W							
Default		30H							

VOLAD1L[7:0]: ADC1 Lch Digital Volume setting (Table 11)
Default: 30H (0dB)

VOLAD1R[7:0]: ADC1 Rch Digital Volume setting (Table 11)
Default: 30H (0dB)

VOLAD2L[7:0]: ADC2 Lch Digital Volume setting (Table 11)
Default: 30H (0dB)

VOLAD2R[7:0]: ADC2 Rch Digital Volume setting (Table 11)
Default: 30H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0A	ADC Digital Filter Setting	0	AD2VO	AD2SD	AD2SL	0	AD1VO	AD1SD	AD1SL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AD2VO: AD2SD, AD2SL: ADC2 Audio/Voice digital filter setting (Table 16)
000: Audio Sharp Roll-off Filter (default)

AD1VO: AD1SD, AD1SL: ADC1 Audio/Voice digital filter setting (Table 15)
000: Audio Sharp Roll-off Filter (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0B	ADC Analog Input Setting	AD1LSEL[1:0]		AD1RSEL[1:0]		AD2LSEL[1:0]		AD2RSEL[1:0]	
R/W		R/W	R/W	R/W		R/W		R/W	
Default		00		00		00		00	

AD1LSEL[1:0]: ADC1 Lch input mode setting (Table 10)
Default: “00” (IN1P, IN1N)

AD1RSEL[1:0]: ADC1 Rch input mode setting (Table 10)
Default: “00” (IN2P, IN2N)

AD2LSEL[1:0]: ADC2 Lch input mode setting (Table 10)
Default: “00” (IN3P, IN3N)

AD2RSEL[1:0]: ADC2 Rch input mode setting (Table 10)
Default: “00” (IN4P, IN4N)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0C	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Write “0” data on each bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0D	ADC Mute & HPF Control	ATSPAD	AD2MUTE	AD1MUTE	0	0	AD2HPFN	AD1HPFN	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATSPAD: ADC Digital Volume Transition Time Setting (Table 12)
0: 4/fs (default)
1: 16/fs

AD2MUTE: ADC2 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

AD1MUTE: ADC1 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

AD2HPFN: ADC2 DC Offset Cancel HPF Enable
0: HPF Enable (default)
1: HPF Disable

AD1HPFN: ADC1 DC Offset Cancel HPF Enable
0: HPF Enable (default)
1: HPF Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0E	DAC1 Lch Digital Volume	VOLDA1L[7:0]							
0F	DAC1 Rch Digital Volume	VOLDA1R[7:0]							
10	DAC2 Lch Digital Volume	VOLDA2L[7:0]							
11	DAC2 Rch Digital Volume	VOLDA2R[7:0]							
R/W		R/W							
Default		18H							

VOLDA1L[7:0]: DAC1 Lch Digital Volume setting (Table 19)
Default: 18H (0dB)

VOLDA1R[7:0]: DAC1 Rch Digital Volume setting (Table 19)
Default: 18H (0dB)

VOLDA2L[7:0]: DAC2 Lch Digital Volume setting (Table 19)
Default: 18H (0dB)

VOLDA2R[7:0]: DAC2 Rch Digital Volume setting (Table 19)
Default: 18H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12	DAC Input Select Setting	0	0	0	0	DAC2SEL[1:0]		DAC1SEL[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W		R/W	
Default		0	0	0	0	01		00	

DAC2SEL[1:0]: DAC2 input select setting (Table 18)
Default: “01” (SDIN2)

DAC1SEL[1:0]: DAC1 input select setting(Table 17)
Default: “00” (SDIN1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13	DAC De-Emphasis Setting	0	0	0	0	DEM2[1:0]		DEM1[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W		R/W	
Default		0	0	0	0	01		01	

DEM2[1:0]: DAC2 De-emphasis Filter Setting (Table 25)
Default: “01” (off)

DEM1[1:0]: DAC1 De-emphasis Filter Setting (Table 25)
Default: “01” (off)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14	DAC Mute & Filter Setting	ATSPDA	0	DA2MUTE	DA1MUTE	DA2SD	DA2SL	DA1SD	DA1SL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	1	0

ATSPDA: DAC Digital Volume Transition Time Setting (Table 20)
0: 4/fs (default)
1: 16/fs

DA2MUTE: DAC2 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

DA1MUTE: DAC1 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

DA2SD, DA2SL: DAC2 digital filter setting (Table 24)
Default: “10” (Short Delay, Sharp Roll-Off Filter)

DA1SD, DA1SL: DAC2 digital filter setting (Table 23)
Default: “10” (Short Delay, Sharp Roll-Off Filter)

10. Recommended External Circuits

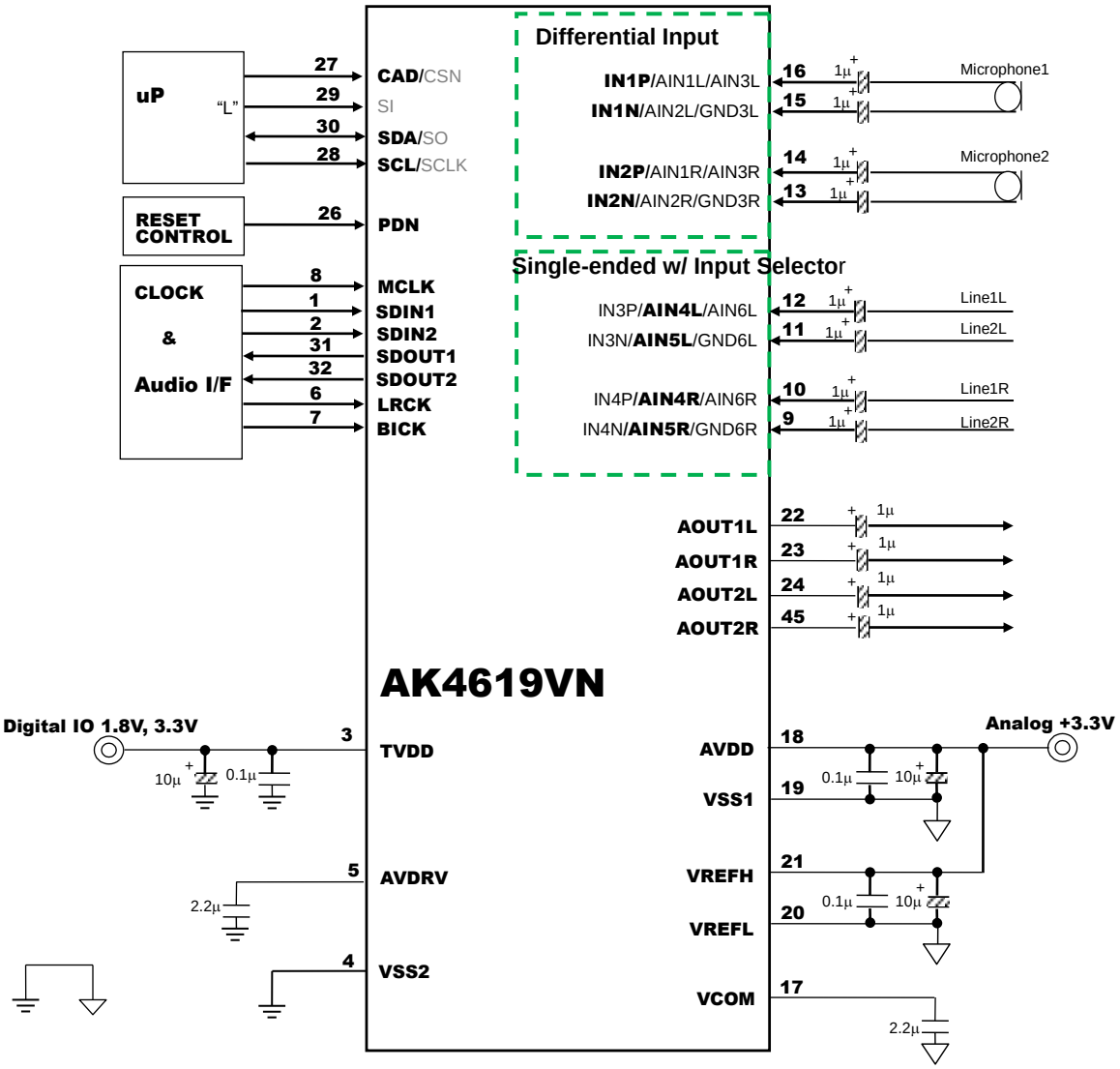


Figure 45. Differential Input 2ch and single-ended 2ch input with multiplexer (I^2C)

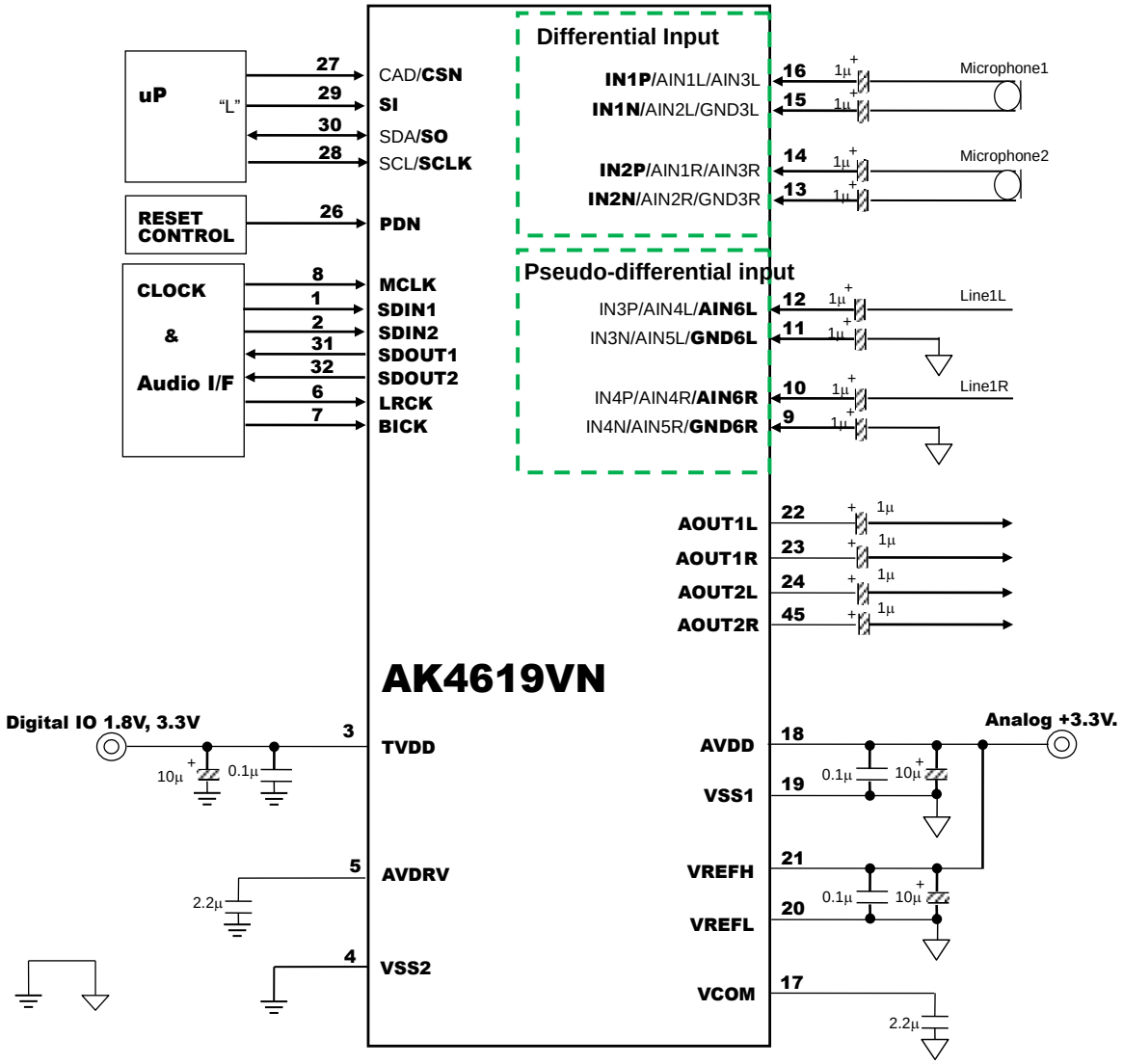


Figure 46. Differential Input 2ch and Pseudo-differential input 4ch (SPI)

1. Ground

VSS1, VSS2 should be connected to the same ground plane. Bypass capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as closed as possible to this device.

2. Reference Voltage

The AVDD voltage sets the analog signal range. VCOM is the common voltage for this device and the VCOM pin outputs AVDD/2. A 2.2µF ceramic capacitor should be connected between the VCOM pin and AVSS.
Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal lines, should be kept away as far as possible from this pin to avoid unwanted noise coupling into the device.

The voltage difference between VREFH and VREFL determines the full scale of the analog input and output range.

The VREFH pin is externally connected to AVDD, and the VREFL pin is externally connected to the analog ground (VSS1). Connect a 0.1 µF ceramic and a 10 µF electrolytic capacitors between VREFH and VREFL. Especially the ceramic capacitors should be connected as near as possible to the device pin.
All digital signals, especially clocks, should be kept away from the VREFH and VREFL pins to avoid unwanted noise coupling into the AK4619.

3. Analog Inputs

The operating common level of the analog input pins IN1P/N, IN2P/N, IN3P/N, and IN4P/N is the VCOM voltage (half of AVDD). A VCOM output amplifier is connected to INxP and INxN pins with an impedance of 25 kΩ (typ). After power-down is released, each analog input pin level becomes VCOM with the time constant of the AC coupling capacitor and the above impedance.
The output code format is 2's complement. The internal HPF removes the DC offset.

Voltage of AVDD + 0.3V or larger, voltage of VSS1 - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuits and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15 V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

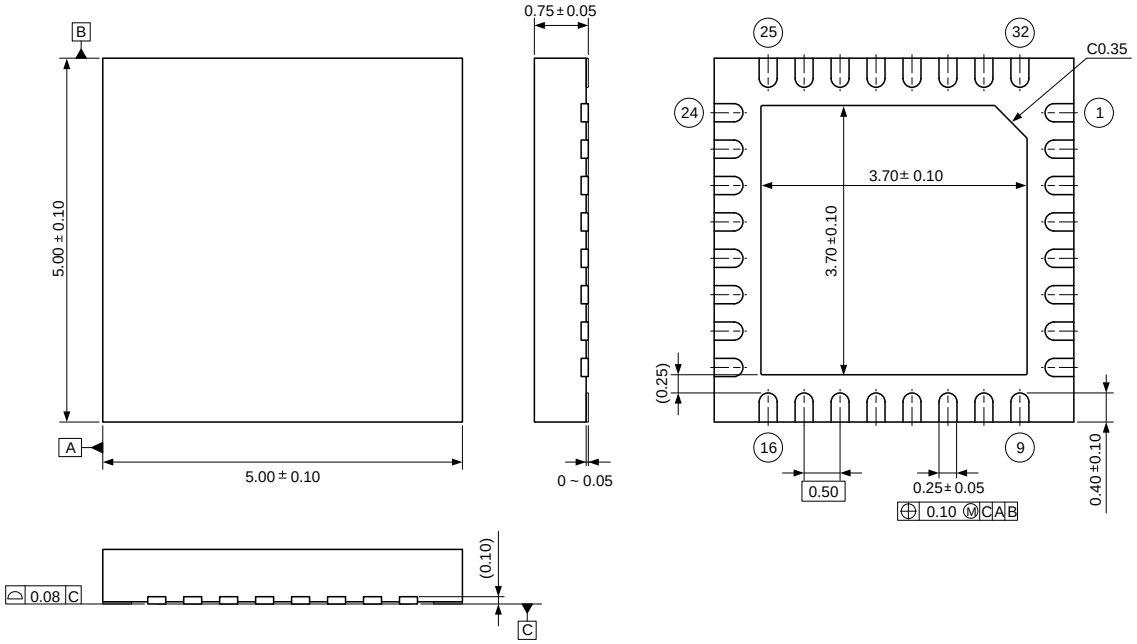
4. Analog Output

The analog output is single-ended, and the output signal range is typically 0.858 x AVDD Vpp, centered on VCOM. The digital input data format is two’s compliment. Positive full-scale output corresponds to 0x7FFFFFFF (@32bit) input code, Negative full scale is 0x80000000 (@32bit) and VCOM voltage ideally is 0x00000000 (@32bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an on-chip filter.

11. Package

11.1. Outline Dimensions (Unit: mm)

32-pin QFN

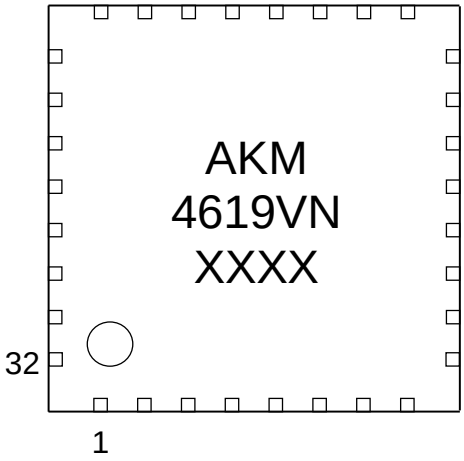


* The exposed pad on the bottom surface of the package is recommended to connect to the VSS1 pin.

11.2. Material & Lead Finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free
Lead frame material: Cu Alloy
Pin surface treatment: Solder (Pb free) plate

11.3. Marking



1) Pin #1 indication
2) Date Code: XXXX(4 digits)
3) Marking Code: 4619VN
4) Asahi Kasei Logo

12. Ordering Guide

AK4619VN -40 to 105ºC 32-pin QFN (0.5mm pitch)
AKD4619 Evaluation board for AK4619

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
21/06/04	00	First Edition		

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