

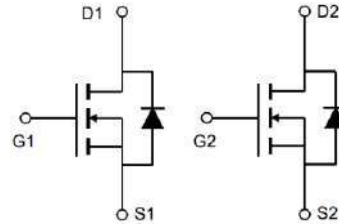
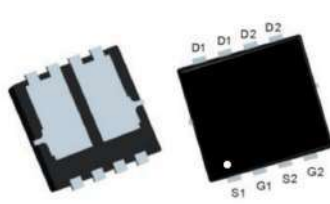


Features

- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- Fast Switching and High efficiency
- Pb-free lead plating; RoHS compliant

Product Summary

V_{DS}	30	V
$R_{DS(on),TYP}$ @ $V_{GS}=10\text{ V}$	8	m Ω
I_D	30	A



PDFN 3.3x3.3-8

NMOS

Maximum ratings, at $T_A=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	30	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_A=25\text{ }^\circ\text{C}$	30 A
I_D	Continuous drain current @ $V_{GS}=10\text{ V}$	$T_C=25\text{ }^\circ\text{C}$	30 A
		$T_C=100\text{ }^\circ\text{C}$	19 A
I_{DM}	Pulse drain current tested ①	$T_C=25\text{ }^\circ\text{C}$	120 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{ V}$	$T_A=25\text{ }^\circ\text{C}$	11 A
		$T_A=70\text{ }^\circ\text{C}$	9 A
EAS	Avalanche energy, single pulsed ②		16 mJ
P_D	Maximum power dissipation	$T_C=25\text{ }^\circ\text{C}$	20 W
		$T_C=100\text{ }^\circ\text{C}$	8 W
P_{DSM}	Maximum power dissipation ③	$T_A=25\text{ }^\circ\text{C}$	2.8 W
		$T_A=70\text{ }^\circ\text{C}$	1.8 W
T_{STG}, T_J	Storage and junction temperature range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	45	$^\circ\text{C/W}$



Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =30V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =30V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.5	2.4	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =20A	--	8	13	mΩ
		V _{GS} =4.5V, I _D =10A	--	12	18	mΩ
		T _j =100°C	--	13	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	--	830	--	pF
C _{oss}	Output Capacitance		--	110	--	pF
C _{rss}	Reverse Transfer Capacitance		--	105	--	pF
R _g	Gate Resistance	f=1MHz	--	4.7	--	Ω
Q _g (10V)	Total Gate Charge	V _{DS} =15V, I _D =20A, V _{GS} =10V	--	23	--	nC
Q _g (4.5V)	Total Gate Charge		--	11	--	nC
Q _{gs}	Gate-Source Charge		--	4.2	--	nC
Q _{gd}	Gate-Drain Charge		--	5.6	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V, I _D =20A, R _G =3Ω, V _{GS} =10V	--	5.8	--	ns
t _r	Turn-on Rise Time		--	56	--	ns
t _{d(off)}	Turn-Off Delay Time		--	26	--	ns
t _f	Turn-Off Fall Time		--	12	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =20A, V _{GS} =0V	--	0.9	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{SD} =20A, V _{GS} =0V di/dt=100A/μs	--	6.8	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.0	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 8A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.



Typical Characteristics

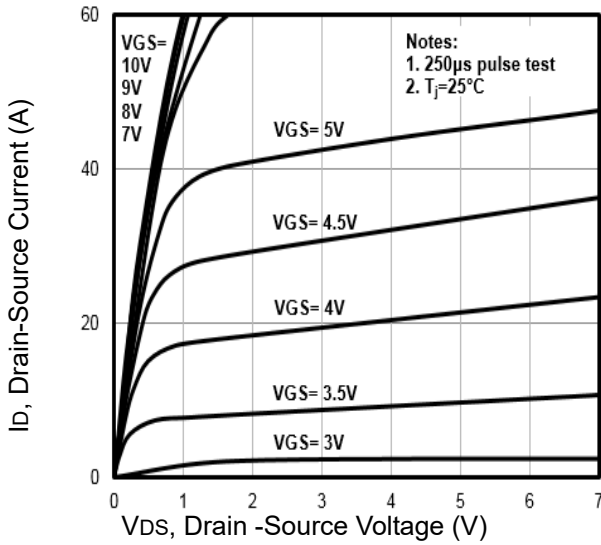


Fig1. Typical Output Characteristics

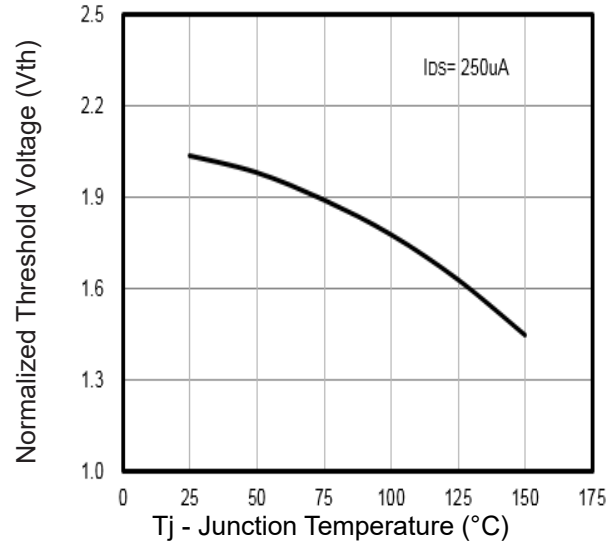


Fig2. Normalized Threshold Voltage Vs. Temperature

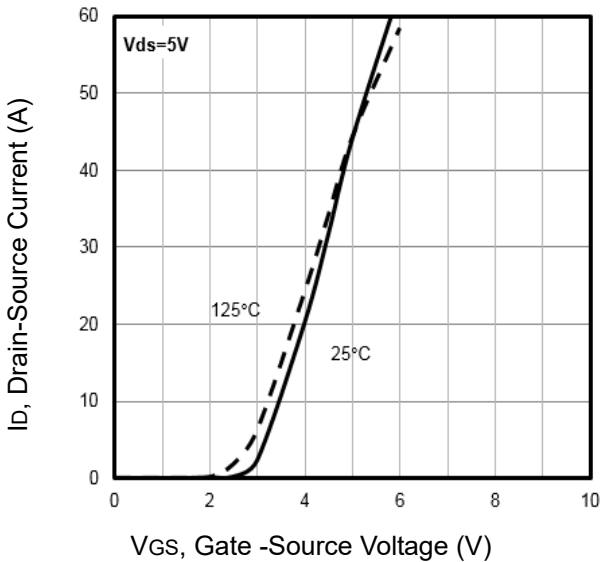


Fig3. Typical Transfer Characteristics

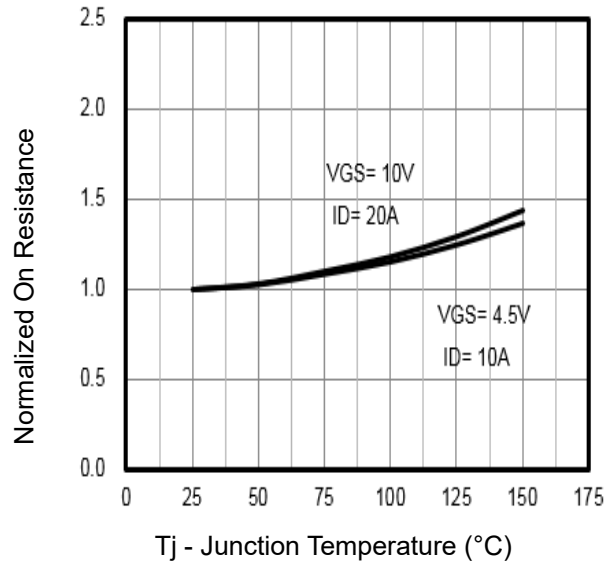


Fig4. Normalized On-Resistance Vs. Temperature

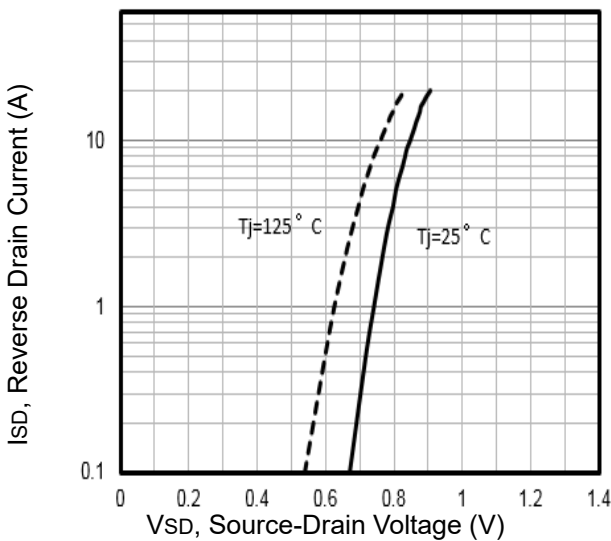


Fig5. Typical Source-Drain Diode Forward Voltage

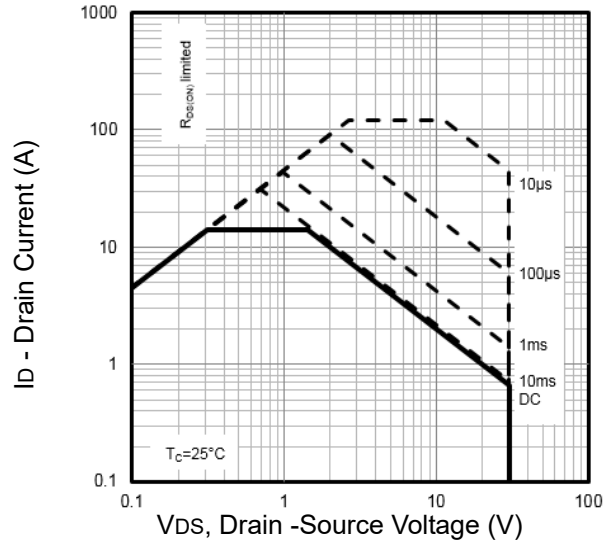


Fig6. Maximum Safe Operating Area



Typical Characteristics

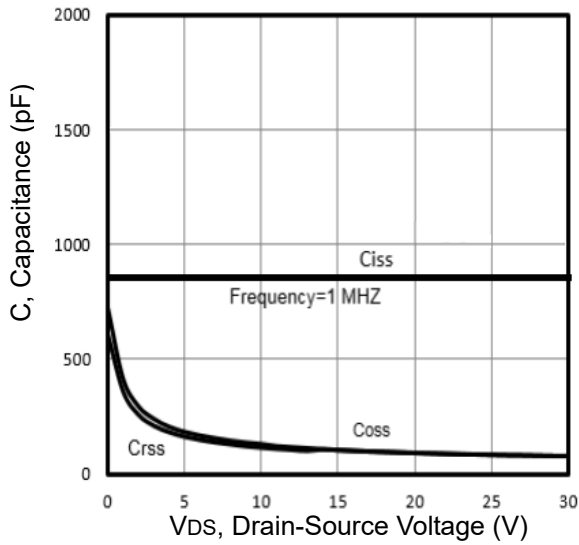


Fig7. Typical Capacitance Vs. Drain-Source Voltage

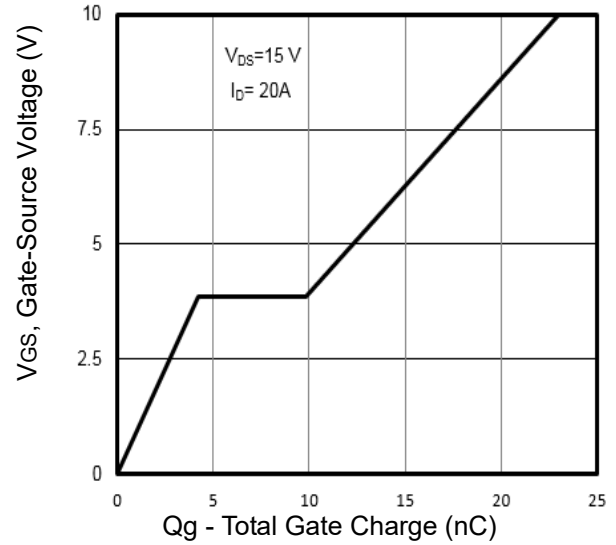


Fig8. Typical Gate Charge Vs. Gate-Source

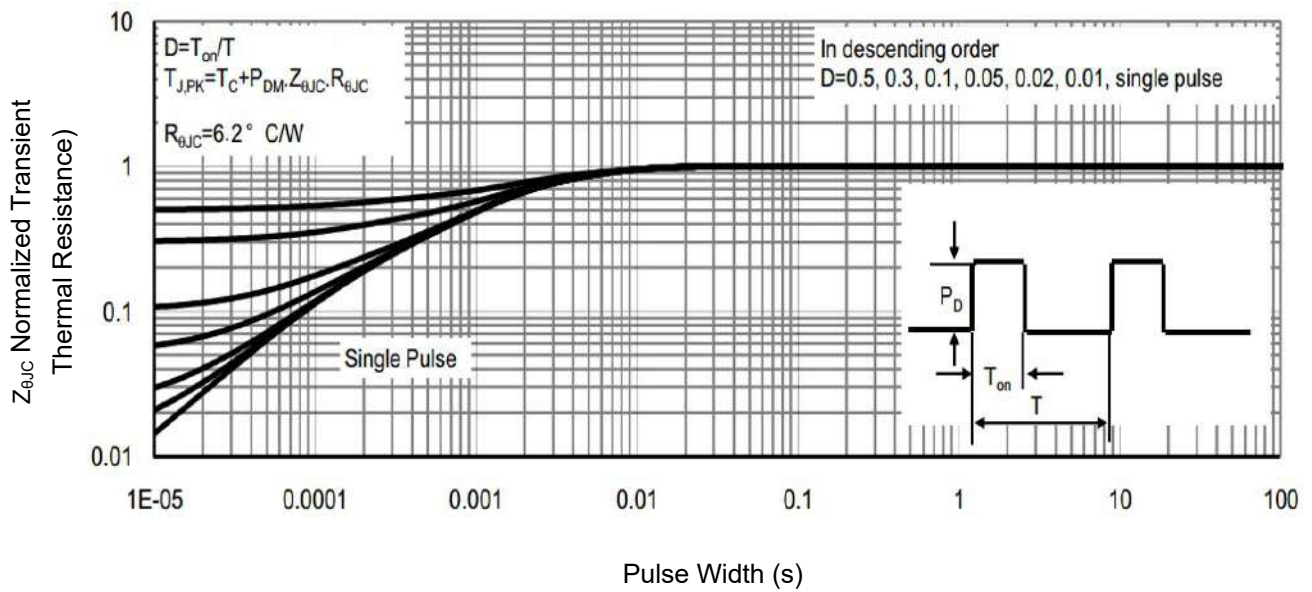


Fig9. Normalized Maximum Transient Thermal Impedance

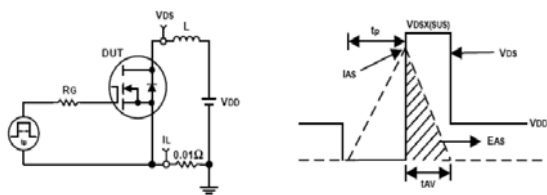


Fig10. Unclamped Inductive Test Circuit and waveforms

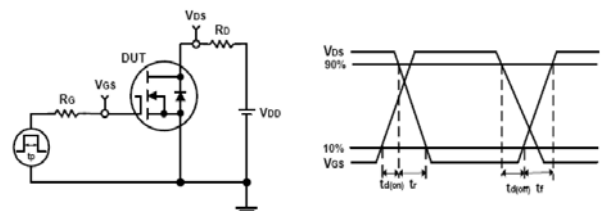
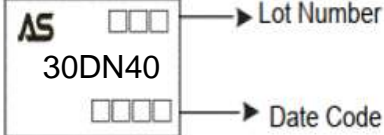
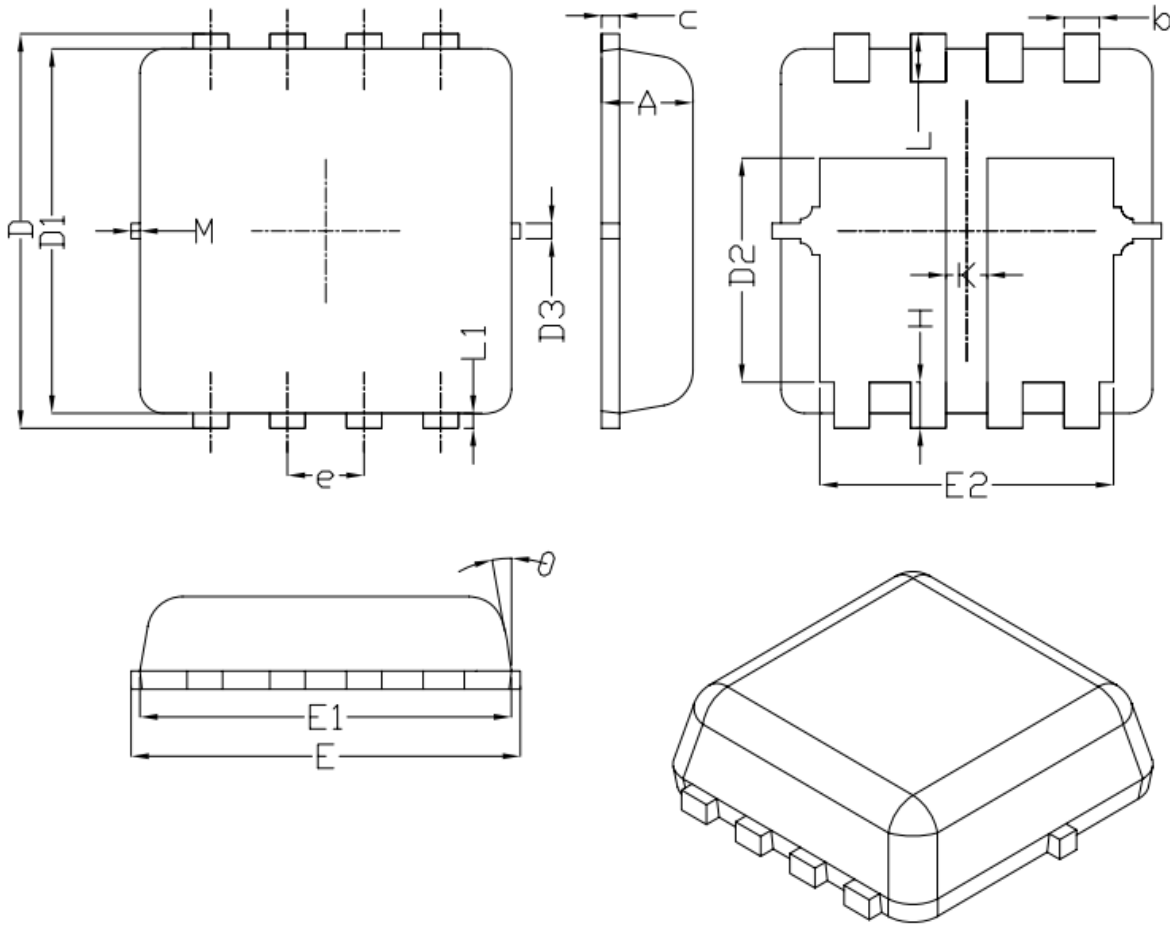


Fig11. Switching Time Test Circuit and waveforms

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM30DN40E-R	30DN40	PDFN3.3*3.3-8	Tape&Reel	5000/Reel

PACKAGE	MARKING
PDFN3.3*3.3-8	 <p>The marking diagram shows a rectangular package with the following markings: 'AS' logo in the top left, '30DN40' in the center, a three-digit Lot Number (□□□) to the right of the top, and a four-digit Date Code (□□□□) to the right of the bottom.</p>

**Dual PDFN3.3*3.3 Package Outline Data**

Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

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[SSM6P54TU,LF](#) [DMP22D4UFO-7B](#) [IPS60R3K4CEAKMA1](#) [DMN1006UCA6-7](#) [DMN16M9UCA6-7](#) [STF5N65M6](#) [STU5N65M6](#)
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