

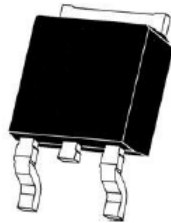


General Features

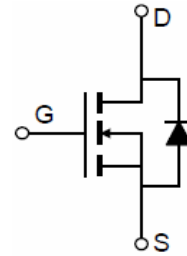
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply



TO-252-2L top view



Schematic diagram

Product Summary

V_{DS}	60	V
$R_{DS(on), Typ} @ V_{GS}=10V$	12	m Ω
I_D	45	A

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	45	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	35	A
Pulsed Drain Current	I_{DM}	180	A
Maximum Power Dissipation	P_D	80	W
Derating factor		0.53	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	115	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

**Electrical Characteristics (T_C=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	12	15	mΩ
		V _{GS} =4.5V, I _D =20A	-	14	17	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V, I _D =20A	24	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	1920	-	PF
Output Capacitance	C _{oss}		-	221	-	PF
Reverse Transfer Capacitance	C _{rss}		-	70	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	-	25	-	nS
Turn-on Rise Time	t _r		-	5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	50	-	nS
Turn-Off Fall Time	t _f		-	6	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =50A, V _{GS} =10V	-	30	-	nC
Gate-Source Charge	Q _{gs}		-	10	-	nC
Gate-Drain Charge	Q _{gd}		-	5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =40A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	45	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 40A	-	50	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs (Note 3)	-	100	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T_J=25°C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25Ω

Typical Electrical and Thermal Characteristics (Curves)

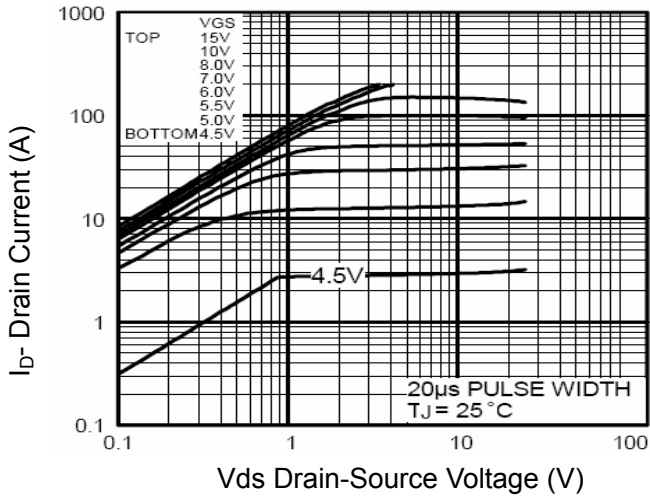


Figure 1 Output Characteristics

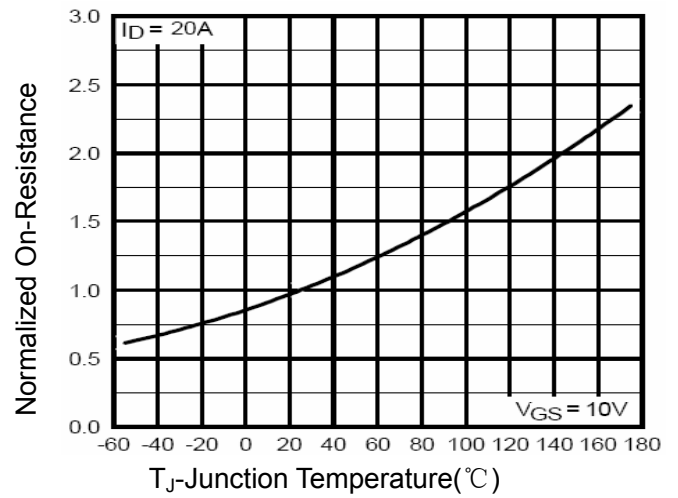


Figure 4 R_{dson} -Junction Temperature

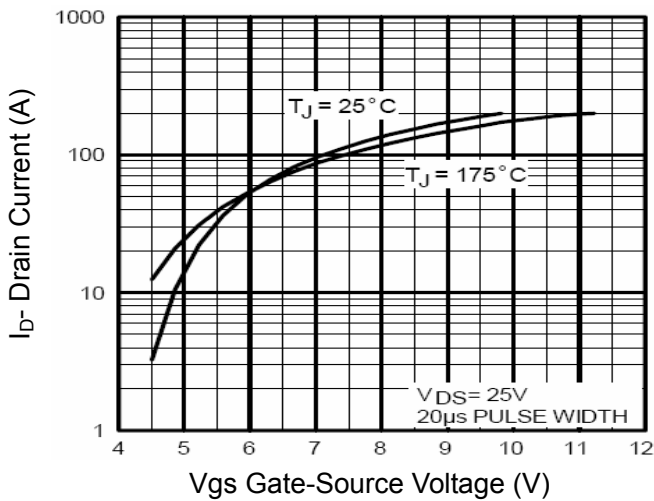


Figure 2 Transfer Characteristics

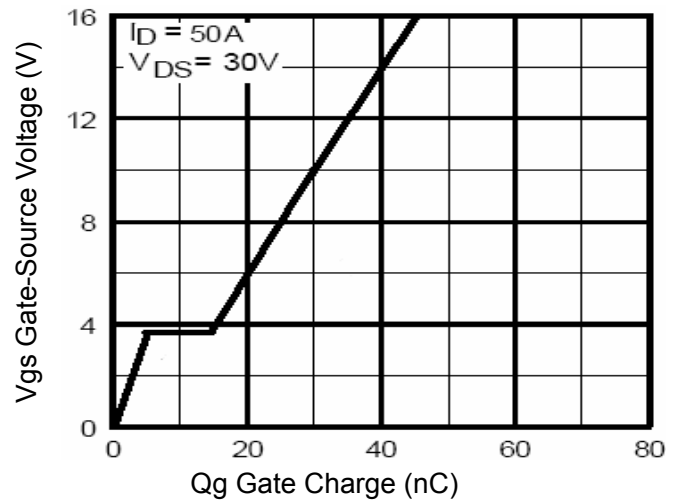


Figure 5 Gate Charge

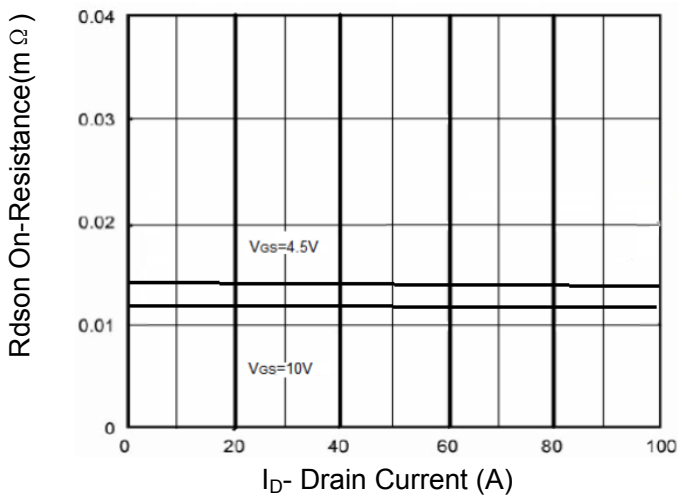


Figure 3 R_{dson} - Drain Current

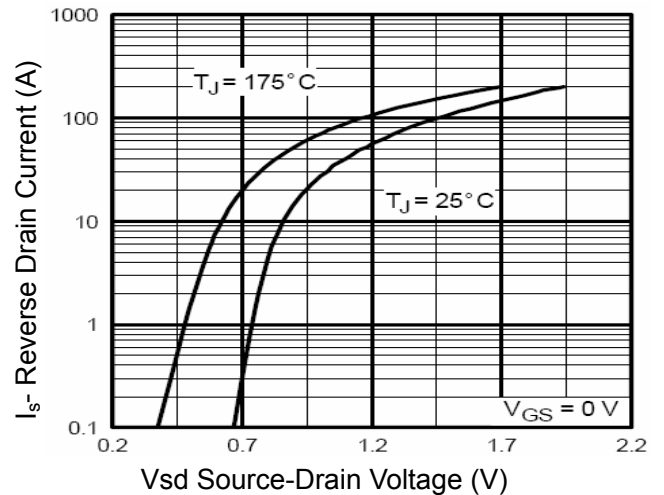


Figure 6 Source- Drain Diode Forward

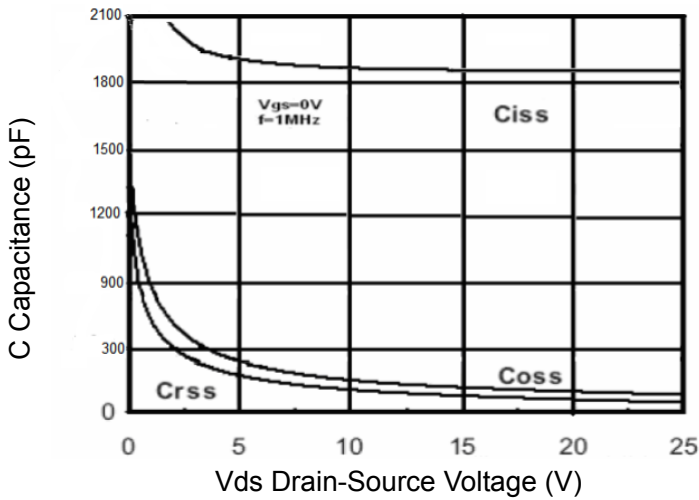


Figure 7 Capacitance vs Vds

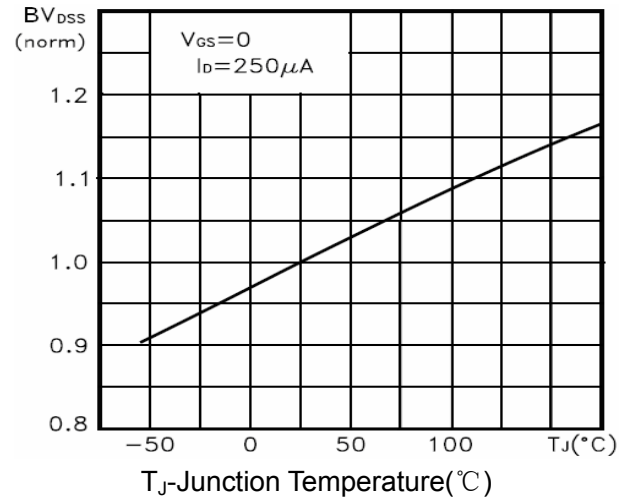


Figure 9 BV_{DSS} vs Junction Temperature

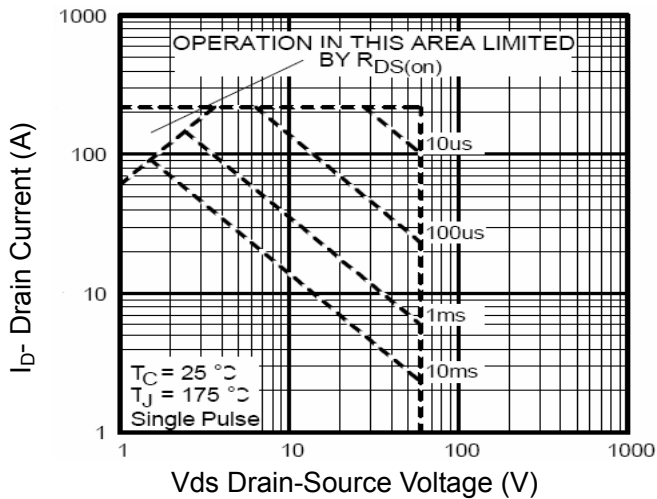


Figure 8 Safe Operation Area

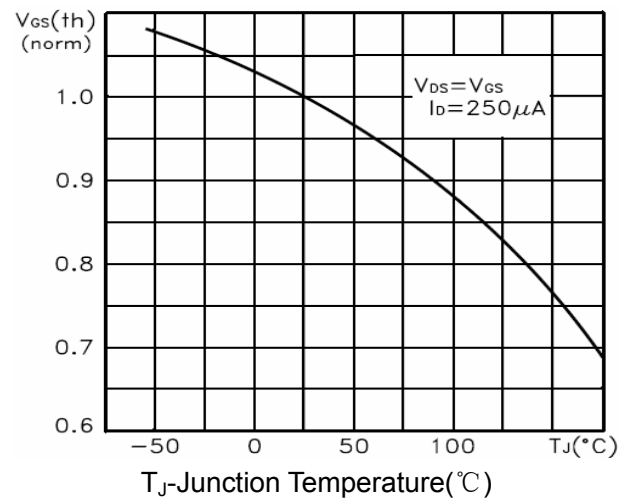


Figure 10 $V_{GS(th)}$ vs Junction Temperature

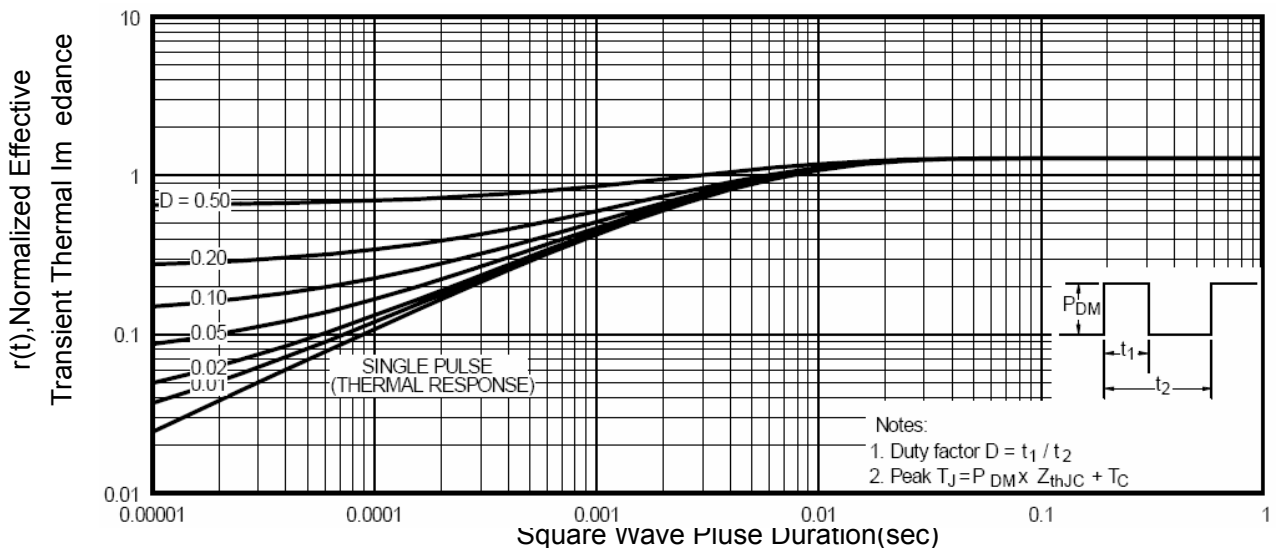
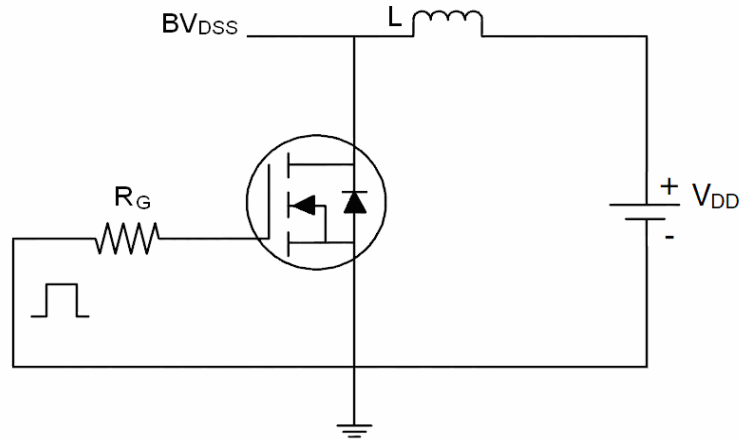


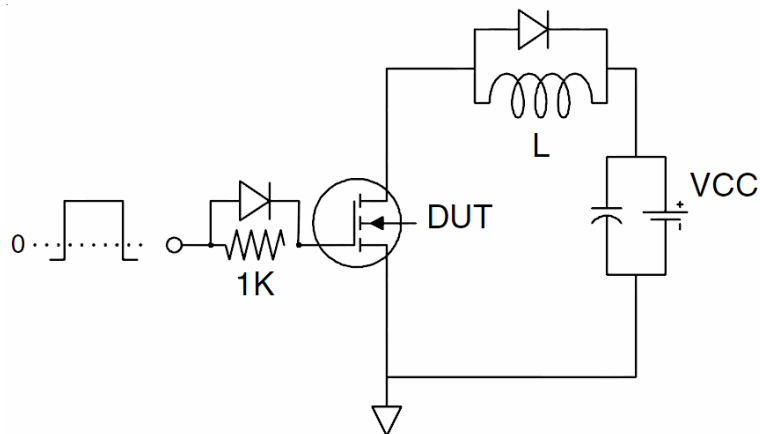
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

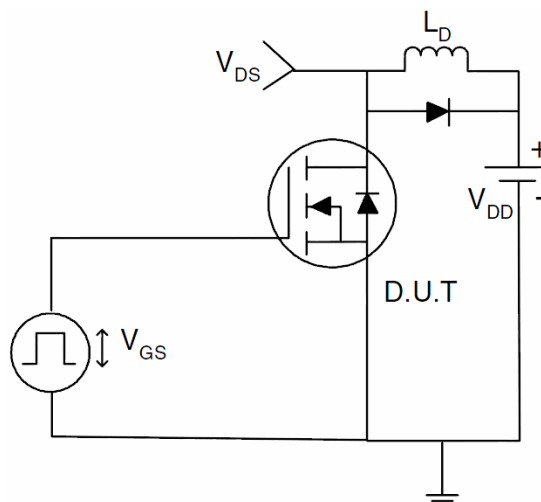
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



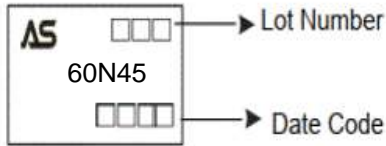
3) Switch Time Test Circuit





Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM60N45KQ-R	60N45	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 <p>The diagram shows a rectangular marking area for a TO-252 package. It contains the following elements from top to bottom: the letters 'AS' in a bold font; a horizontal row of three small squares; the text '60N45' in a bold font; and another horizontal row of three small squares. To the right of the top row of squares is an arrow pointing to the text 'Lot Number'. To the right of the bottom row of squares is an arrow pointing to the text 'Date Code'.</p>

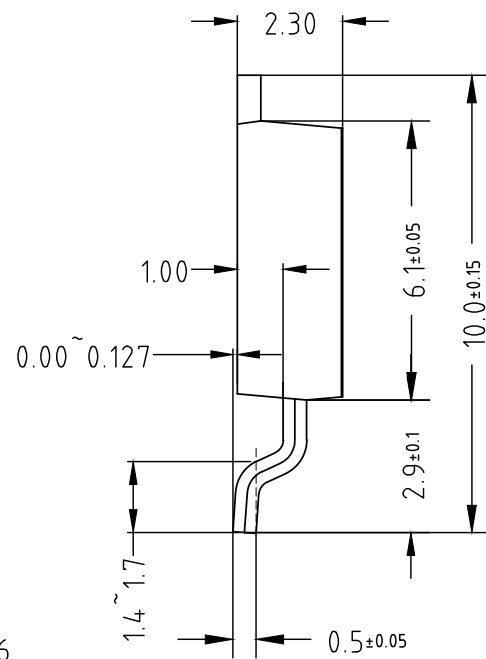
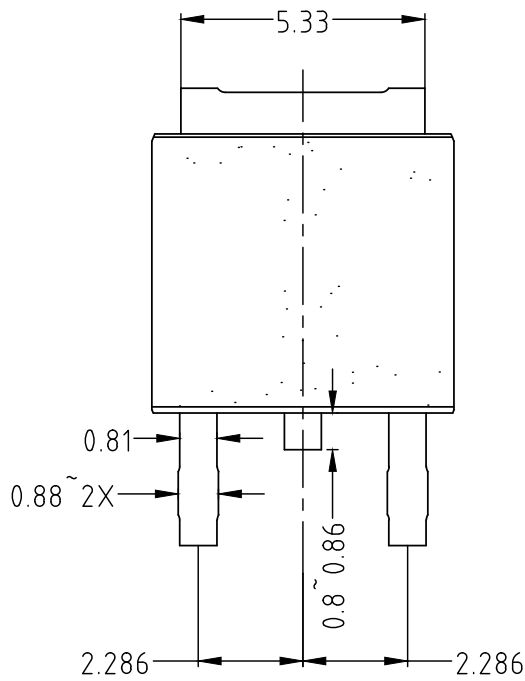
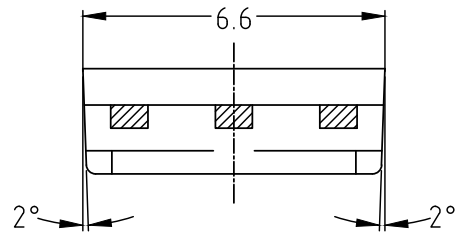


ASCENDSEMI

ASDM60N45KQ

60V N-Channel MOSFET

TO-252



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