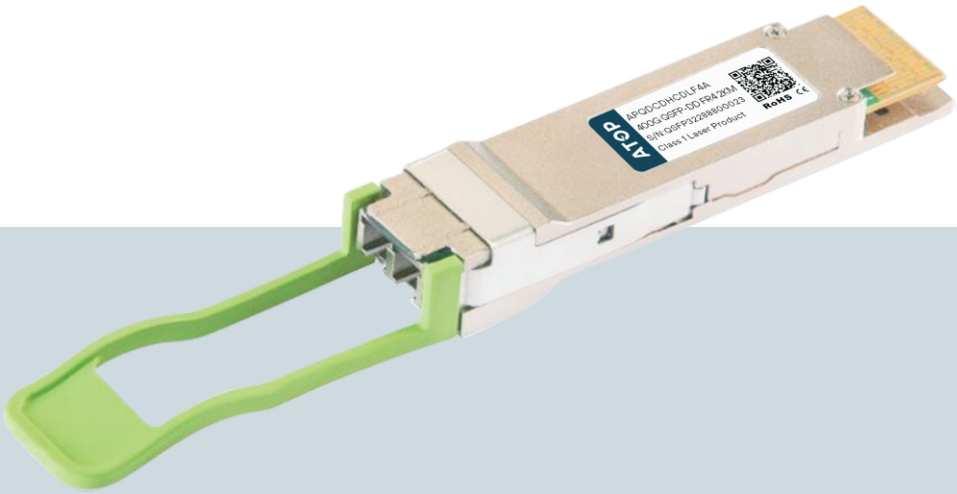
400Gb/s QSFP-DD FR4 Transceiver

APQDCDHCDLF4A



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Product Features

- ✓ QSFP-DD MSA compliant
- ✓ Compliant to 100G Lambda MSA and 802.3cu
- ✓ 400G FR4 Specification compliant
- ✓ Non-hermetic package design
- ✓ 4 CWDM lanes MUX/DEMUX design 8x53.125Gb/s PAM4 electrical interface (400GAUI-8)
- ✓ Maximum power consumption 12W
- ✓ LC duplex connector
- ✓ Supports 425Gb/s aggregate bit rate
- ✓ Up to 2km transmission on single mode fiber with FEC
- ✓ Single 3.3V power supply
- ✓ RoHS-6 compliant

Applications

- ✓ Data Center Interconnect

Product Selection

Part Number	Operating Case temperature	DDMI
APQDCDHCDLF4A	Commercial(0~70℃)	Yes

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- ESD to the Duplex LC Receptacle: compatible with EN 61000-4-2
- Immunity compatible with EN 61000-4-3
- EMI compatible with FCC Part 15 Class B
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and 1040.11 IEC 60950, IEC60825-1,2
- RoHS compliant with RoHS 2.0(2015/863/EU)-amending.

Pin Descriptions

Pin	Logic	Symbol	Description	Plug	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6		Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-I	Mod-PrsL	Module Present	3B	
28	LVTTL-I	IntL	Interrupt	3B	1
29		VccTx	+3.3V Power supply transmitter	2B	
30		Vcc1	+3.3V Power supply	2B	
31	LVTTL-I	Init-Mode	Initialization mode, In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-O	Rx4n	Receiver Inverted Data Output	3B	
34	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
35		GND	Ground	1B	1

Pin Descriptions

Pin	Logic	Symbol	Description	Plug	Notes
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data output	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		Vs2	Module Vendor Specific 2	3A	3
50		Vs3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5n	Receiver Inverted Data Output	3A	
56	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Non-Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69		Reserved	For Future Use	3A	3

Pin	Logic	Symbol	Description	Plug	Notes
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Non-Inverted Data input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	3A	
75		Tx5n	Transmitter Non-Inverted Data output	3A	
76		GND	Ground	1A	1

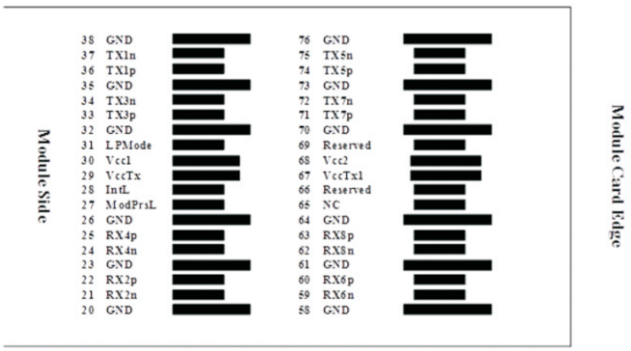
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

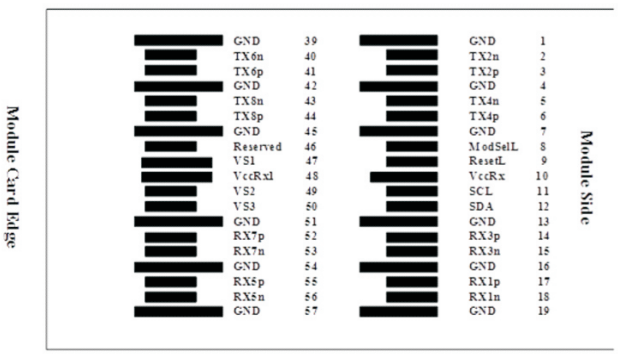
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

4.Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see Figure 3 for pad locations) Contact sequence A will make, then break con- tact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

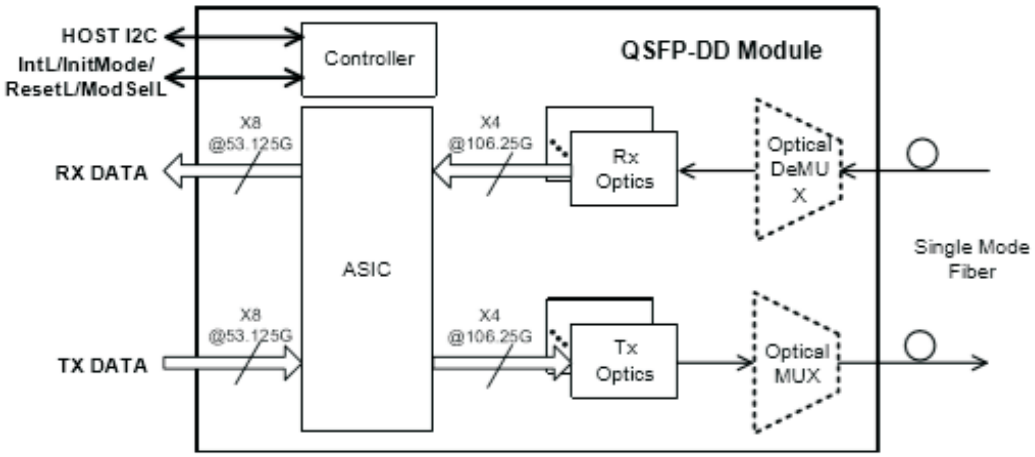


Top Side Viewed from Top

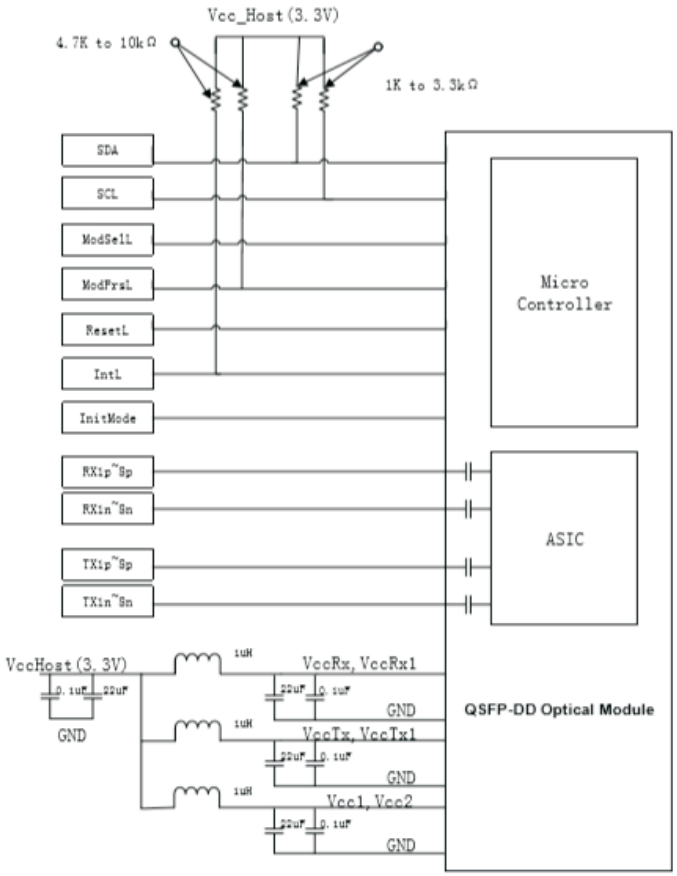


Bottom Side Viewed from Bottom

Recommend Circuit Schematic



Recommend Circuit Schematic



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		+3.6	V	
Storage Temperature	TS	-40		+85	℃	
Operating Humidity	RH	0		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Power Supply Current	Icc			3.63	A	
Case Operating Temperature	Tc	0		+70	℃	Commercial
Power dissipation	P			12	w	
9/125um G.652 SMF	Lmax			2	km	
Data Rate Accuracy		-100		100	ppm	

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Data Rate, each lane			26.5625±100ppm		Gbd	
Differential input Voltage pk-pk	Vpp	900			mV	1
Common Mode Voltage	Vcm	-350	700	2850	mV	2
Differential Termination Resistance Mismatch		Vee		10	%	
Single-ended Voltage Tolerance Range (Min)		-0.4		3.3	V	
Differential Input Return Loss		IEEE 802.3-2015 Equation(83E-5)			dB	
Differential to Common Mode Input Return Loss		IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test		IEEE 802.3cu				3

Receiver					
Data Rate, each lane		26.5625±100ppm		Gbd	
Differential Termination Resistance Mismatch			10	%	
Differential output Voltage	Vpp	Vcc-0.8	900	mV	
Common Mode Voltage	Vcm	-350	2850	mV	
Common Mode Noise RMS	Vrms		17.5	mV	
Transition time (min)	Vpp	9.5		ps	20% to 80%
Near-end Eye height, differential (min)		70		mV	
Near-end ESMW (Eye symmetry mask width)		0.2		UI	
Far-end Eye height, differential (min)		30		mV	
Far-end pre-cursor ISI ratio		-4.5	2.5	%	
Differential output return Loss		IEEE 802.3-2015 Equation (83E-2)			
Common to differential mode conversion return loss		IEEE 802.3-2015 Equation (83E-3)			

Notes:

1.With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

2.DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

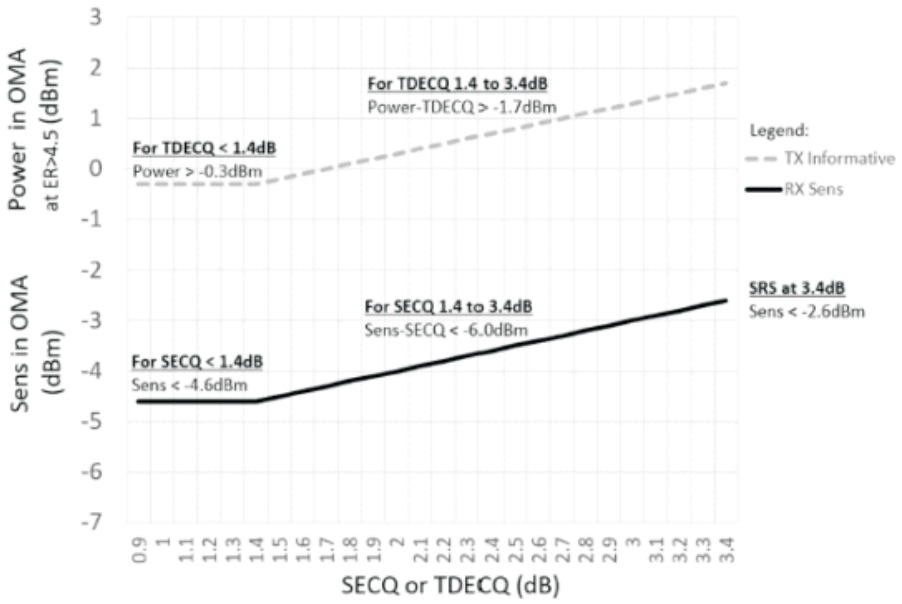
3.BER specified in IEEE 802.3bs 120E.1.1

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Receiver						
Data Rate, each Lane	Gbd		53.125±100		ppm	
Modulation Format			PAM4			
Damage Threshold, each lane		4.5			dBm	
Average receiver sensitivity, each lane	SENS	-7.3		3.5	dBm	
Receiver sensitivity, each lane (OMA)	SENS1			3.7	dBm	
Difference in Receiver Power between any Two Lanes (OMA)				4.1	dB	
LOS De-Assert	LOSD			-8.6	dBm	
LOS Assert	LOSA	-15			dBm	
LOS Hysteresis		0.5			dB	

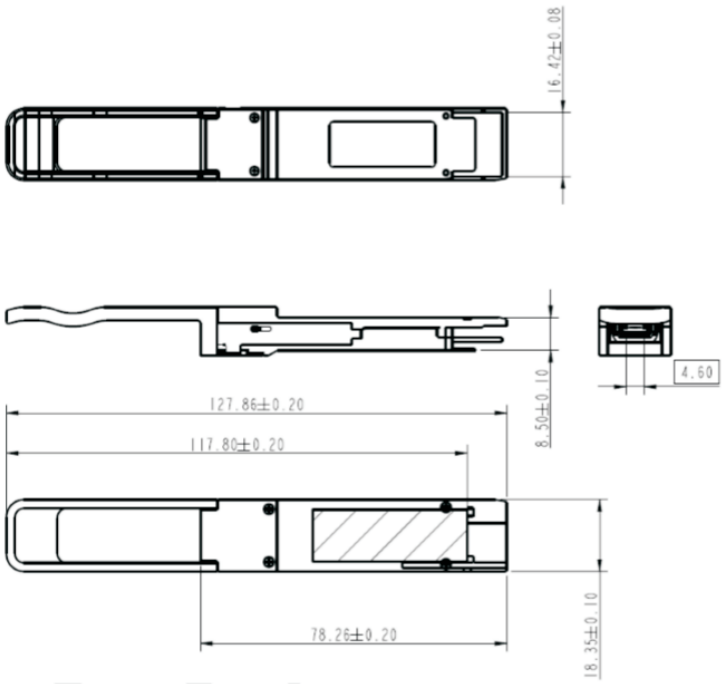
Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Data Rate, each Lane			53.125±100 ppm		Gbd	
Modulation Format			PAM4			
Total Average Launch Power	PT			9.5	dBm	
Average Launch Power, each Lane		-3.3		3.5	dBm	
Optical Modulation Amplitude, each Lane	OMA	-0.3		3.7	dBm	
Optical Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side-mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5			dB	
Launch power in OMA minus TDECQ, each lane, for ER⩾ 4.5dB		-1.6			dB	
Launch power in OMA minus TDECQ, each lane, for ER <4.5dB		-1.7			dB	
Transmitter and Dispersion Eye Clouser for PAM4, each Lane (TDECQ)		-1.6		3.4	dB	
Difference in Launch Power between any Two Lanes (OMAouter)				4	dB	
RIN17.1OMA				-136	dB/Hz	
Optical Return Loss Tolerance				17.1	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of OFF Transmitter, each Lane				-20	dBm	
Conditions of Stressed Receiver Sensitivity						
Stressed eye closure for PAM4 (SECQ), lane under test		0.9		3.4	dB	
OMAouter of each aggressor lane			1.5		dBm	



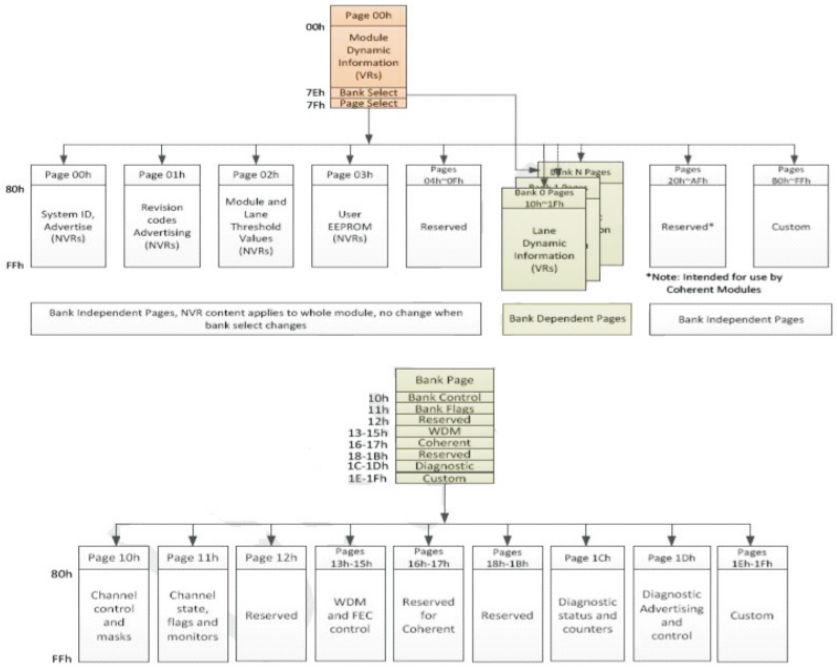
Stressed receiver sensitivity mask for 400G-FR4

Mechanical Specifications



APQDCDHCDLF4A

EEPROM Information



Digital Diagnostic Monitoring Interface

Five transceiver parameter values are monitored. The following table defines the monitory parameter's accuracy.

Parameter	Range	Accuracy	Calibration
Temperature	0 to +70°C	±3°C	Internal
Voltage	2.97 to 3.63V	±3%	Internal
Bias Current	0 to 100mA	±10%	Internal
RX Power	-11 to 4.5dBm	±3dB	Internal
TX Power	-3.3~+3.5dBm	±3dB	Internal

Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Billy Tang	Xuming Di	Dingzheng	New Released.	Apr 21, 2019
Version1.1	Carmen Zhou	Xuming Di	Dingzheng	Update the new template	Aug 7, 2020

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