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ATP AH28K72F8BJE6S

1GB DDR2-667 REGISTERED ECC DIMM

DESCRIPTION

The ATP AH28K72F8BJE6S is a high performance 1GB DDR2-667 Registered ECC SDRAM memory module. It is organized as 128M x 72 in a 240-pin Dual-In-Line Memory Module (DIMM) package. The module utilizes nine 128Mx8 DDR2 SDRAMs in FBGA package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 1GB (128M x 72)
- DIMM Rank: 1 Rank
- Cycle Time: 3ns (333MHz)
- CAS Latency: 5
- Bi-directional differential data-strobe
- Power supply: 1.8V±0.1V
- RoHS compliant
- Burst lengths: 4, 8
- Auto & Self refresh
- 7.8 μs refresh interval at lower than T_{CASE} 85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- On Die Termination
- PCB Height: 1.18 inches
- Support address and command signals parity function

Part No.	Max Freq	Interface
AH28K72F8BJE6S	333 MHz (3ns@CL=5) x2	SSTL_1.8

PIN DESCRIPTION

Pin Name	Description	Pin Name	Description
A0~A9, A11~A13	Address Inputs	ODT0	On die termination
A10/AP	Address Input/Auto precharge	$\overline{RAS}$	Row Address Strobe
BA0~BA2	DDR2 SDRAM Bank Address	$\overline{RESET}$	Register and PLL control pin
$\overline{CAS}$	Column Address Strobe	RFU	Reserved for Future Use
CB0~CB7	Data check bits Input/Output	$\overline{CS0}$	Chip Selects
CK0	Clock Inputs, positive line	SA0~SA2	SPD address
$\overline{CK0}$	Clock inputs, negative line	SCL	Serial Presence Detect (SPD) Clock Input
CKE0	Clock Enables	SDA	SPD Data Input/Output
DM0~DM8	Data Masks	TEST	Memory bus test tool (Not Connect and Not Useable on DIMMs)
DQ0~DQ63	Data Input/Output	VDD	Core Power
DQS0~DQS8	Data strobes	VDDQ	I/O Power
$\overline{DQS0}$ ~ $\overline{DQS8}$	Data strobes, negative line	VDDSPD	SPD Power
DQS9~DQS17	Data strobes (Read)	VREF	Input/Output Reference
$\overline{DQS9}$ ~ $\overline{DQS17}$	Data strobes (Read), negative line	VSS	Ground
Par_In	Parity bit for the Address and Control bus	Err_Out	Parity error found in the Address and Control bus
NC	No Connect	$\overline{WE}$	Write Enable

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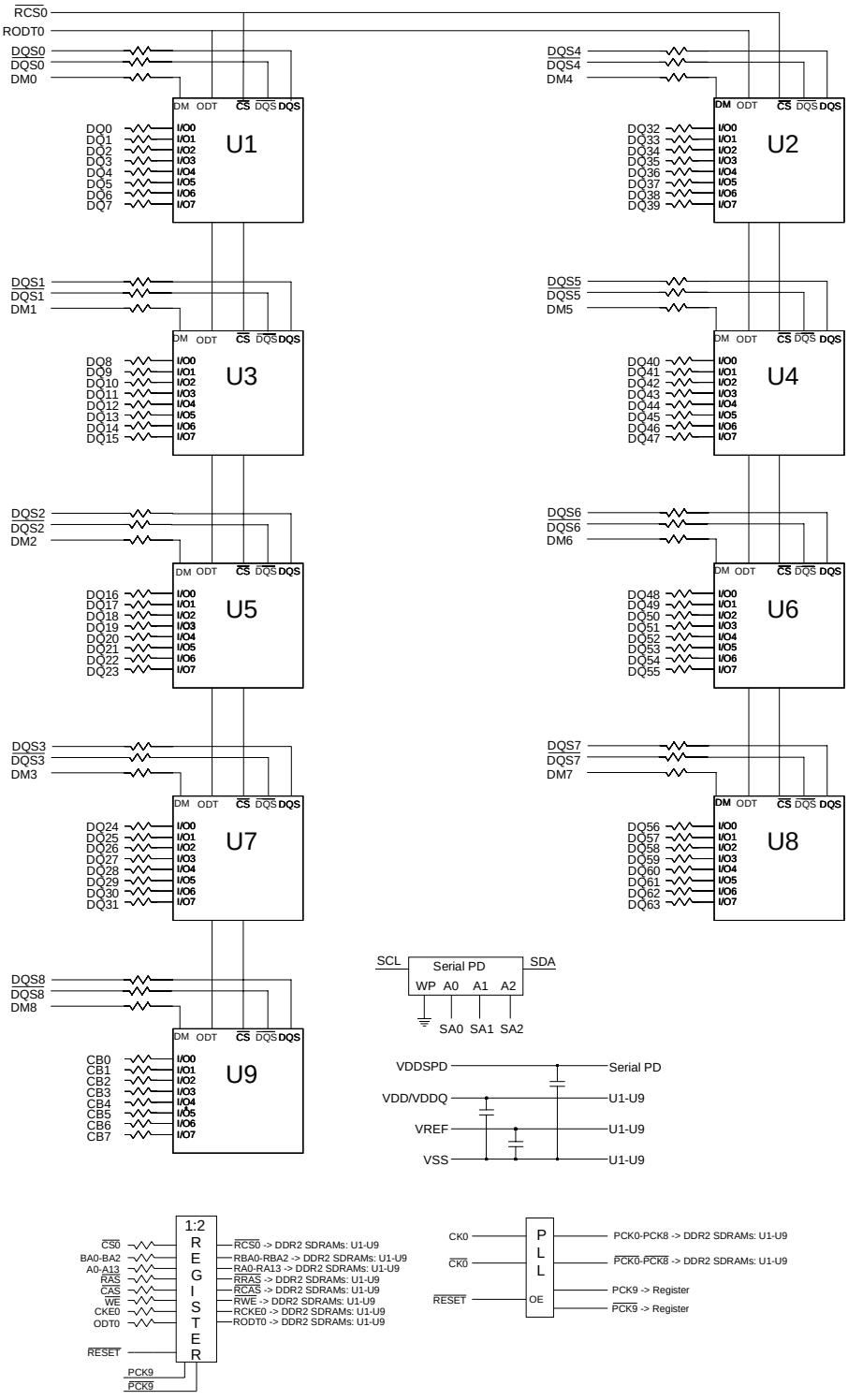
PIN ASSIGNMENT

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREF	121	VSS	61	A4	181	VDDQ
2	VSS	122	DQ4	62	VDDQ	182	A3
3	DQ0	123	DQ5	63	A2	183	A1
4	DQ1	124	VSS	64	VDD	184	VDD
5	VSS	125	DM0 or DQS9	KEY			
6	$\overline{\text{DQS0}}$	126	NC or $\overline{\text{DQS9}}$	65	VSS	185	CK0
7	DQS0	127	VSS	66	VSS	186	$\overline{\text{CK0}}$
8	VSS	128	DQ6	67	VDD	187	VDD
9	DQ2	129	DQ7	68	Par_In[3]	188	A0
10	DQ3	130	VSS	69	VDD	189	VDD
11	VSS	131	DQ12	70	A10/AP	190	BA1
12	DQ8	132	DQ13	71	BA0	191	VDDQ
13	DQ9	133	VSS	72	VDDQ	192	$\overline{\text{RAS}}$
14	VSS	134	DM1 or DQS10	73	$\overline{\text{WE}}$	193	$\overline{\text{CS0}}$
15	$\overline{\text{DQS1}}$	135	NC or $\overline{\text{DQS10}}$	74	$\overline{\text{CAS}}$	194	VDDQ
16	DQS1	136	VSS	75	VDDQ	195	ODT0
17	VSS	137	RFU	76	NC	196	A13
18	$\overline{\text{RESET}}$[1]	138	RFU	77	NC	197	VDD
19	NC	139	VSS	78	VDDQ	198	VSS
20	VSS	140	DQ14	79	VSS	199	DQ36
21	DQ10	141	DQ15	80	DQ32	200	DQ37
22	DQ11	142	VSS	81	DQ33	201	VSS
23	VSS	143	DQ20	82	VSS	202	DM4 or DQS13
24	DQ16	144	DQ21	83	$\overline{\text{DQS4}}$	203	NC or $\overline{\text{DQS13}}$
25	DQ17	145	VSS	84	DQS4	204	VSS
26	VSS	146	DM2 or DQS11	85	VSS	205	DQ38
27	$\overline{\text{DQS2}}$	147	NC or $\overline{\text{DQS11}}$	86	DQ34	206	DQ39
28	DQS2	148	VSS	87	DQ35	207	VSS
29	VSS	149	DQ22	88	VSS	208	DQ44
30	DQ18	150	DQ23	89	DQ40	209	DQ45
31	DQ19	151	VSS	90	DQ41	210	VSS
32	VSS	152	DQ28	91	VSS	211	DM5 or DQS14
33	DQ24	153	DQ29	92	$\overline{\text{DQS5}}$	212	NC or $\overline{\text{DQS14}}$
34	DQ25	154	VSS	93	DQS5	213	VSS
35	VSS	155	DM3 or DQS12	94	VSS	214	DQ46
36	$\overline{\text{DQS3}}$	156	NC or $\overline{\text{DQS12}}$	95	DQ42	215	DQ47
37	DQS3	157	VSS	96	DQ43	216	VSS
38	VSS	158	DQ30	97	VSS	217	DQ52
39	DQ26	159	DQ31	98	DQ48	218	DQ53
40	DQ27	160	VSS	99	DQ49	219	VSS
41	VSS	161	CB4	100	VSS	220	RFU
42	CB0	162	CB5	101	SA2	221	RFU
43	CB1	163	VSS	102	NC(TEST)[2]	222	VSS
44	VSS	164	DM8 or DQS17	103	VSS	223	DM6 or DQS15
45	$\overline{\text{DQS8}}$	165	NC or $\overline{\text{DQS17}}$	104	$\overline{\text{DQS6}}$	224	NC or $\overline{\text{DQS15}}$
46	DQS8	166	VSS	105	DQS6	225	VSS
47	VSS	167	CB6	106	VSS	226	DQ54
48	CB2	168	CB7	107	DQ50	227	DQ55
49	CB3	169	VSS	108	DQ51	228	VSS
50	VSS	170	VDDQ	109	VSS	229	DQ60
51	VDDQ	171	NC	110	DQ56	230	DQ61
52	CKE0	172	VDD	111	DQ57	231	VSS
53	VDD	173	NC	112	VSS	232	DM7 or DQS16
54	BA2	174	NC	113	$\overline{\text{DQS7}}$	233	NC or $\overline{\text{DQS16}}$
55	Err_Out[3]	175	VDDQ	114	DQS7	234	VSS
56	VDDQ	176	A12	115	VSS	235	DQ62
57	A11	177	A9	116	DQ58	236	DQ63
58	A7	178	VDD	117	DQ59	237	VSS
59	VDD	179	A8	118	VSS	238	VDDSPD
60	A5	180	A6	119	SDA	239	SA0
				120	SCL	240	SA1

1. RESET (Pin 18) is connected to both OE of PLL and Reset of register.
2. The Test pin (Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)
3. Err_Out (Pin 55) and Par_In (Pin 68) are for function to check address and command parity.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-1.0V ~ 2.3V	V	1
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.5V ~ 2.3V	V	1
Voltage on V_{DDL} pin relative to V_{SS}	V_{DDL}	-0.5V ~ 2.3V	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5V ~ 2.3V	V	1
Storage Temperature	T_{STG}	-55 to +100	^{o}C	1,2
Operating Temperature	T_{CASE}	0 to +95	^{o}C	1,2,3

Note:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. At 85 - 95 ^{o}C operation temperature range, doubling refresh commands in frequency to a 32ms period (Refresh interval =3.9 µs) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

AC & DC OPERATING CONDITIONS (SSTL- 1.8)

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
Supply Voltage for Output [4]	V_{DDQ}	1.7	1.8	1.9	V
Supply Voltage for DLL [4]	V_{DDL}	1.7	1.8	1.9	V
Input Reference Voltage[1,2]	V_{REF}	0.49 * V_{DDQ}	0.50 * V_{DDQ}	0.51 * V_{DDQ}	V
Termination Voltage[3]	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
Input High Voltage (DC)	V_{IH} (DC)	V_{REF} + 0.125	-	V_{DDQ} + 0.3	V
Input High Voltage (AC)	V_{IH} (AC)	V_{REF} + 0.200	-	-	V
Input Low Voltage (DC)	V_{IL} (DC)	-0.3	-	V_{REF} - 0.125	V
Input Low Voltage (AC)	V_{IL} (AC)	-	-	V_{REF} - 0.200	V

Note:
1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5xV_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF} (DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

CAPACITANCE

(V_{DD}=1.8V, V_{DDQ}=1.8V, TA=25°C)

Parameter	Symbol	Max.	Units
Input Capacitance (CKE, $\overline{CS}$)	C_{I1}	12	pF
Input Capacitance (Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}	12	pF
Input Capacitance (CK, $\overline{CK}$)	C_{CK}	11	pF
Input/Output Capacitance (DQ, DM, DQS, $\overline{DQS}$)	C_{IO}	10	pF

IDD SPECIFICATION PARAMETER

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions		Value	Units
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,190	mA
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		1,330	mA
IDD2P	**Precharge power-down current;** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		600	mA
IDD2Q	**Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		770	mA
IDD2N	**Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		770	mA
IDD3P	**Active power-down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	820	mA
		Slow PDN Exit MRS(12) = 1mA	660	
IDD3N	**Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		970	mA
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,460	mA
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		1,670	mA
IDD5	**Burst auto refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,900	mA
IDD6	**Self refresh current**; CK and CK\ at 0V; CKE <= 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING Normal Low Power		140	mA
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		2,780	mA

TIMING PARAMETER

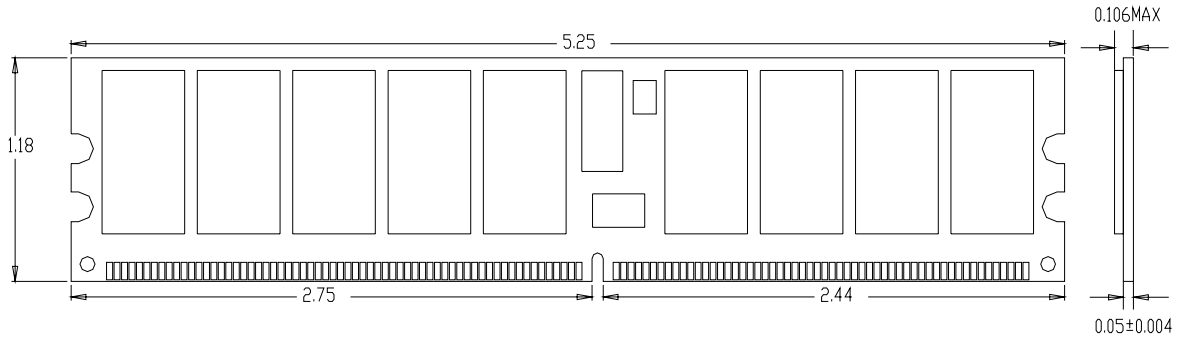
Parameter	Symbol	DDR2-667		Units
		min	Max	
Clock cycle time at CL=5.0	tCK	3	8	ns
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD	15	-	ns
Row precharge time	tRP	15	-	ns
Row cycle time	tRC	60	-	ns
Row active time	tRAS	45	70000	ns
DQ output access time from CK/ $\overline{CK}$	tAC	-450	450	ps
DQS output access time from CK/ $\overline{CK}$	tDQSCK	-400	400	ps
CK high-level width	tCH	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	tCK
CK half period	tHP	min(tCL, tCH)	-	ps
DQ and DM input hold time	tDH(base)	175	-	ps
DQ and DM input setup time	tDS(base)	100	-	ps
Control & Address input pulse width for each input	tIPW	0.6	-	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	-	tCK
Data-out high-impedance time from CK/ $\overline{CK}$	tHZ	-	tAC max	ps
DQS low-impedance time from CK/ $\overline{CK}$	tLZ(DQS)	tAC min	tAC max	ps
DQ low-impedance time from CK/ $\overline{CK}$	tLZ(DQ)	2* tACmin	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	ps
DQ hold skew factor	tQHS	-	340	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	0.25	tCK
DQS input high pulse width	tDQSH	0.35	-	tCK
DQS input low pulse width	tDQSL	0.35	-	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	tCK
Mode register set command cycle time	tMRD	2	-	tCK
Write post amble	tWPST	0.4	0.6	tCK
Write preamble	tWPRE	0.35	-	tCK
Address and control input hold time	tIH(base)	275	-	ps
Address and control input setup time	tIS(base)	200	-	ps
Read preamble	tRPRE	0.9	1.1	tCK
Read post amble	tRPST	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	-	ns
Active to active command period for 2KB page size products	tRRD	10	-	ns
Four Activate Window for 1KB page size products	tFAW	37.5	-	ns
Four Activate Window for 2KB page size products	tFAW	50	-	ns
CAS to CAS command delay	tCCD	2	-	tCK
Write recovery time	tWR	15	-	ns
Auto precharge write recovery + precharge time	tDAL	tWR+tRP		tCK
Internal write to read command delay	tWTR	7.5	-	ns
Internal read to precharge command delay	tRTP	7.5	-	ns
Exit self refresh to a non-read command	tXSNR	tRFC + 10	-	ns
Exit self refresh to a read command	tXSRD	200	-	tCK
Exit precharge power down to any nonread command	tXP	2	-	tCK
Exit active power down to read command	tXARD	2	-	tCK
Exit active power down to read command (slow exit, lower power)	tXARDS	7 – AL	-	tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3	-	tCK
ODT turn-on delay	tAOND	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max) +0.7	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+ 2	2tCK+tAC(max) +1	ns
ODT turn-off delay	tAOFD	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	ns
ODT to power down entry latency	tANPD	3	-	tCK
ODT power down exit latency	tAXPD	8	-	tCK
OCD drive mode output delay	tOIT	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	-	ns

PHYSICAL DIMENSIONS (UNITS IN INCHES)

(Drawing not to scale)

240-pin DIMM

Front



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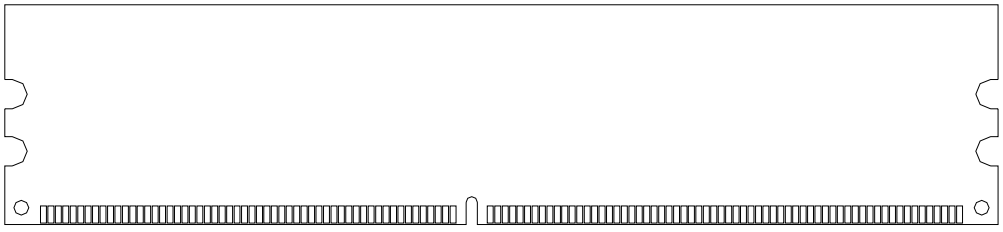

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