AW2013 3-channel LED Driver with I²C Compatible Interface

Feature

- 3-channel intelligent LED driver with constant current output
- Up to 15mA current output with 4-level adjustable for each LED
- Support both Direct PWM control mode and One Shot Programming mode
- Support 256 PWM steps
- Fast I²C interface with maximum operating frequency 400KHz
- Adaptive to 1.8V/2.8V/3V interface
- Configurable I²C address with default value 45h
- Interrupt pin INTN, active low
- LDO and OSC inside
- Power supply VCC，2.5V～3.3V
- ESD HBM 7kV
- Operation temperature -40℃~85℃
- Package 2mm×2mm DFN-10L

Applications

- Mobile phones, hand-hold devices
- LED in home Appliance

General Description

AW2013 is a product of 3-channel LED driver supporting auto breathing mode with I2C interface in AWINIC LED driver product line. It can drive 3 individual LEDs or one group of RGB.

AW2013 drives LEDs with common anode, constant current. The brightness can be modulated in PWM with 256 steps. The output current can be configured in 4 levels: 15mA、10mA、5mA、0mA(default)。

AW2013 supports fade-in and fade-out effect for brightness control. There are two modes: the Direct PWM Control mode and One Short Programming mode. In the one short programming mode, it's flexible to set the breathing speed, timing, brightness and repeat times.

Typical Application Circuit

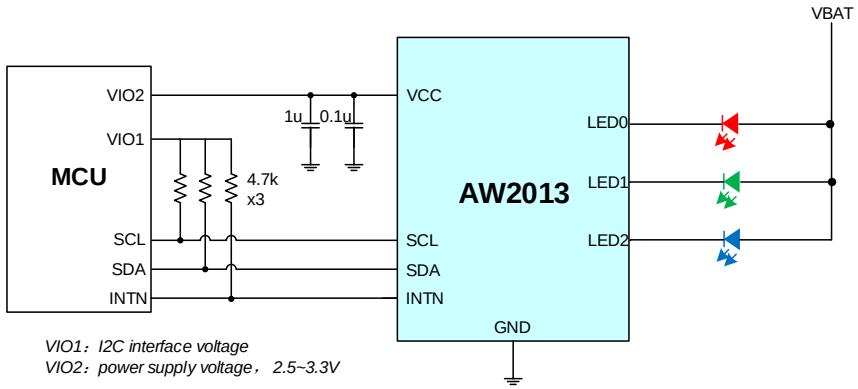


Figure 1 AW2013 Typical Application Circuit

1 Function Block Diagram

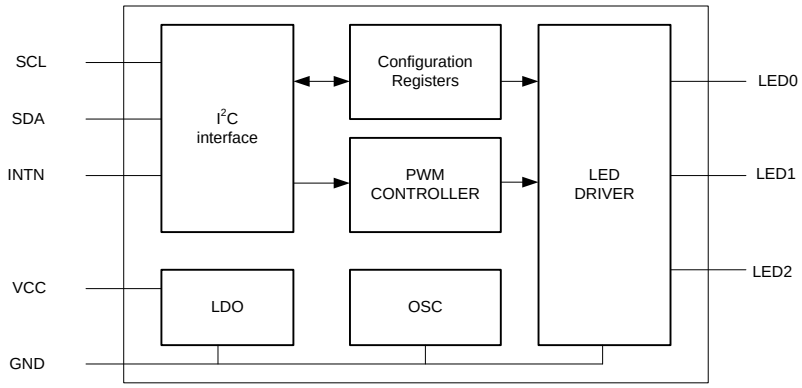


Figure 2 AW2013 block diagram

2 PIN information

AW2013 is available in DFN-10L(2mm*2mm)

2.1 Device PIN out

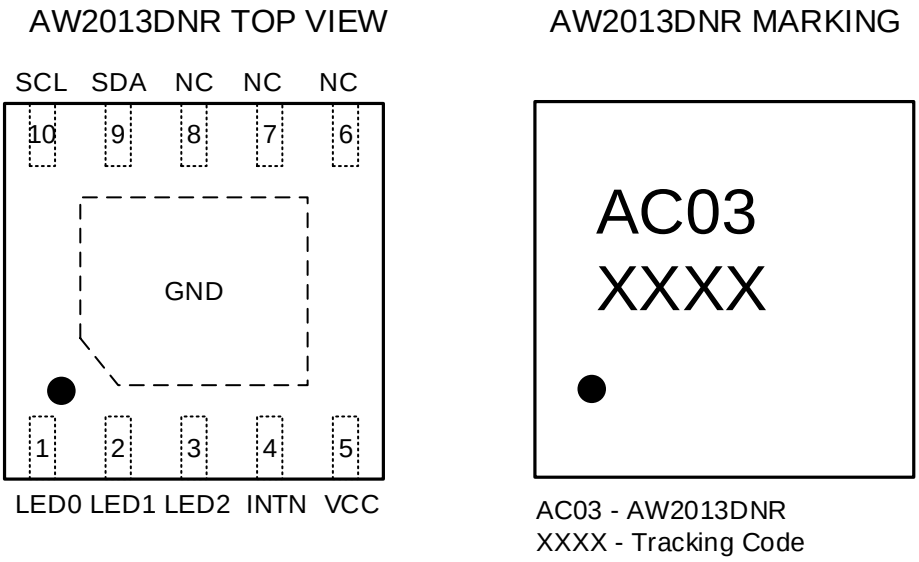


Figure 3 AW2013 Top View and Marking

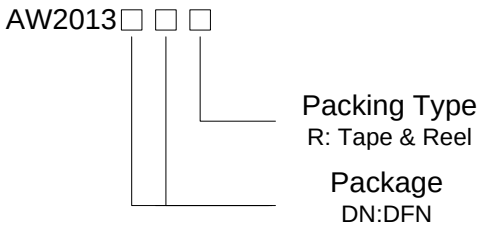
2.2 PIN description

INDEX	SYMBOL	DESCRIPTION
1	LED0	LED current source output, which can be connected to VBAT through LED
2	LED1	LED current source output, which can be connected to VBAT through LED
3	LED2	LED current source output, which can be connected to VBAT through LED
4	INTN	Interrupt PIN, open drain output, low active. Can be pull-up through outside resistor, floating is permitted when not used.

5	VCC	Power supply, 2.5-3.3V
6-8	NC	Not used, keep floating
9	SDA	DATA signal of I²C interface，1.8V/3.3V compatible.
10	SCL	Clock signal of I²C interface，1.8V/3.3V compatible.
Thermal PAD	GND	Thermal PAD, Connect to GND

3 Order Information

ORDER NUMBER	Temperature Range	Package	Marking	MSL Level	ROHS	Packing Type
AW2013DNR	-40℃～85℃	DFN2x2-10L	AC03	MSL3	Yes	3000units Tape&Reel



4 Absolute Maximum Ratings*(note 1)*

parameter	range
Power supply，V_{CC}	-0.3V ～ 3.6V
Voltage at input pin	-0.3V ～ V_{CC}+0.3V
GND terminal current	300mA
Operating temperature range	-40℃ to 85℃
Storage temperature range T_{STG}	-65℃ to 150℃
Package thermal resistance θ_{JA} （DFN-10）	45℃/W
Maximum junction temperature T_{JMAX}	160℃
Maximum lead temperature(soldering in 10s)	260℃
ESD HBM （Note 2）	±7KV
Latch-up Test standard：JEDEC STANDARD NO.78B DECEMBER 2008	+IT：450mA -IT：-450mA

Note 1：*Absolute maximum ratings indicate limits beyond which permanent damage to the component may occur. The above parameters are only extreme conditions not recommend conditions. The life and reliability of the component maybe affect after working in the extreme conditions for a long time.*

Note 2：*HBM test method: discharge the electric charge stored in a 100pF capacitor to the component pin through a 1.5KΩ resistor. Standard: MIL-STD-883G Method 3015.7*

5 Electrical Characteristics

Test conditions：T_A=-40℃～+85℃（unless otherwise specified）. Test condition for typical value: VCC=2.8V， T_A=25℃。

Symbol	Description	Test Condition	MIN	TYP	MAX	Unit

Symbol	Description	Test Condition	MIN	TYP	MAX	Unit
V_{CC}	Power Supply		2.5	2.8	3.3	V
I_{sleep}	Sleep power supply current	Immediately after power up or soft reset	-	90	-	uA
I_{cc}	Quiescent power supply current	Set register GCR=01h	-	450	-	uA
Output Current Set register GCR=01h，LEDE=07h，PWM0～2=FFh						
I_{out}	LED output current	LCFG0～2=03h（*Note1*）	12.5	15	19	mA
		LCFG0～2=02h（*Note1*）	8.5	10	12.5	
		LCFG0～2=01h（*Note1*）	4	5	6.5	
V_{drop}	Output Dropout Voltage	LCFG0～2=03h，I_{out}=15mA	-	225	-	mV
Logic Interface Electrical Characteristics						
V_{IH}	Input High Voltage	SCL，SDA pin	1.2	-		V
V_{IL}	Input Low Voltage	SCL，SDA pin	-	-	0.6	V
I_{IL}	Input Low Current	SCL，SDA pin	-	5		nA
I_{IH}	Input High Current	SCL，SDA pin	-	5		nA

Note1：Testing under PWM control mode, set register PWM0～2=FFh。

Logic Interface Switching Characteristics *(Note1)*

Symbol	Description	Con.	MIN	TYP	MAX	Unit
F_{SCL}	SCL clock frequency				400	kHz
t_{BUF}	Interval from a STOP to the next START condition		1.3			μS
$t_{HD,STA}$	Hold time (repeated) START condition		0.6			μS
t_{LOW}	SCL clock low period		1.3			μS
t_{HIGH}	SCLK clock high period		0.6			μS
$t_{SU,STA}$	Setup time for a START condition		1.3			μS
$t_{HD,DAT}$	Data hold time		0			μS
$t_{SU,DAT}$	Data setup time		0.1			μS
t_R	Rise time of SCL *(Note2)*				0.3	μS
t_F	Fall time of SCL *(Note2)*				0.3	μS
$t_{SU,STO}$	Setup time for STOP condition		0.6			μS
T_{DEG}	Input signal deglitch width	SCL		200		nS

Symbol	Description	Con.	MIN	TYP	MAX	Unit
		SDA		250		nS
Cb	Total capacitance of one bus line				400	pF

Note1：Designed to ensure

Note2：T_R，T_F is the time for Voltage from 0.3×Vcc to 0.7×Vcc.

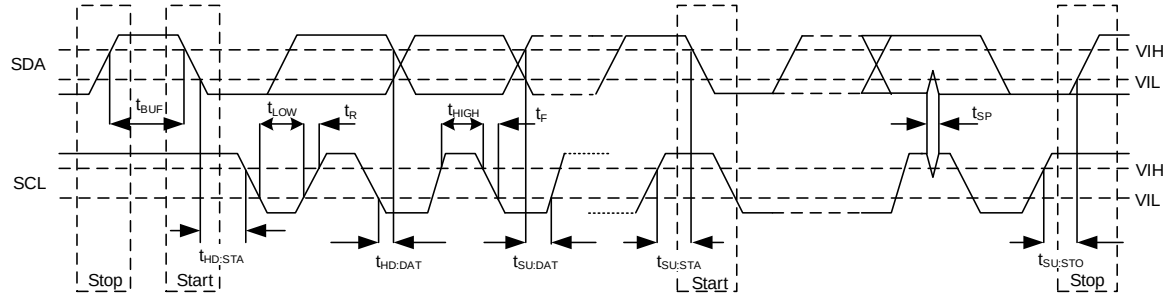


Figure 4 I2C interface timing diagram

6 I2C Interface

6.1 General

AW2103 uses a serial bus, which conforms to the I2C protocol to control the chip with two-wire: SCL and SDA. The maximum clock frequency supported is 400 KHz, which is compatible with I2C standard.

6.2 I2C Address

The default I2C device address (7-bit) of AW2013 is 45h, followed by the R/W bit(Read=1/Write=0)，composites an slave address byte：

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Device Address：45h							R/W

The device address of AW2013 can be modified by setting the inside configuration register IADR (address 77H).

IADR , Addr.=77h，Default value 45h							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ASEL	DA[6:0]						

When ASEL=0, I2C Device Address = 45h (default)

When ASEL=1, I2C Device Address =DA[6:0]。

Once the device address is changed, the master should use the new address to accessing AW2013.

The device address and register IADR will be reset to default value (45h) after power down or soft reset.

6.3 Accessing Operation

6.3.1 Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6,7)

i) Master generates STOP condition to indicate write cycle end

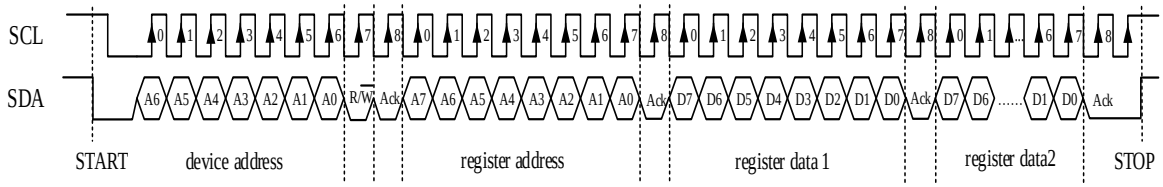


Figure 5 I2C write cycle, multiple registers are written

6.3.2 Read Cycle

In a read cycle, the following steps should be followed:

j) Master device generates START condition

k) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

l) Slave device sends acknowledge signal if the slave address is correct.

m) Master sends control register address (8-bit)

n) Slave sends acknowledge signal

o) Master generates STOP condition followed with START condition or REPEAT START condition

p) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

q) Slave device sends acknowledge signal if the slave address is correct.

r) Slave sends data byte from addressed register.

s) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

t) If the master device generates STOP condition, the read cycle is ended.

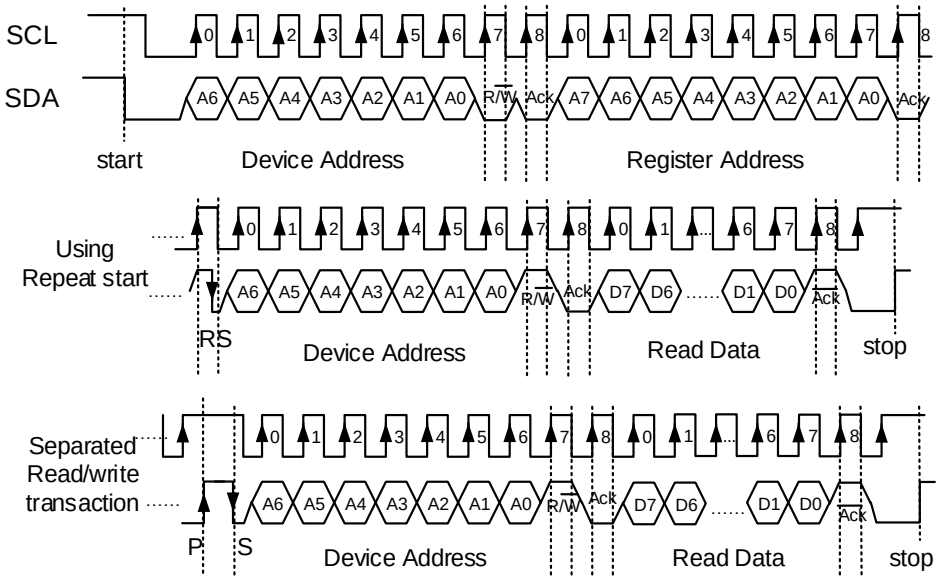


Figure 6 I2C Read Cycle

6.4 SDA,SCL

The two interface line SCL and SDA should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

The pull-up resistor can be selected in the range of 1k~10KΩ to make the rising time fit with the requirement of I2C compatible standard. The typical value is 4.7KΩ

AW2013 can support different high level (1.8V, 2.8V, 3V, 3.3V) of this two-wire interface. And deglitch circuit is also implemented inside to filter out the glitch in the SCL, SDA line.

6.5 Interrupt

INTN pin is open-drain output with active low. This signal can be active to inform the master that a programmed operation has been finished.

The highest 3-bit of GCR(address 01h) register is interrupt enable control bits. One bit for one channel independently.

If no interrupt generated, the INTN port will keep high-resistance output and the pin should be pulled-up by outside resistor connected with power supply; if there's interrupt generated, the INTN port will be driven low. Once an interrupt generated, the master device can read the ISR register to decide which kind of interrupt source and the ISR register will be cleared automatically after the read operation and the INTN pin will return back to high-resistance output.

7 Operating Mode

7.1 Power Up And Reset

After power-up, the LDO inside AW2013 starts to work and provides internal constant voltage power supply (1.8V). Once the internal power supply is stable, it will generate a reset signal to make AW2013 perform a power-up reset operation, which reset all of the control circuits and configurable registers to default state.

After power-up reset operation finished, the ISR.4(PUIS) will be set to “1”. The INTN port will be driven low to inform master AW2013 has finished the power-up operation and is ready to work. This bit can also be used to check whether there’s a power-down event after reading this register last time.

7.2 SLEEP Mode and RUN Mode

SLEEP mode: AW2013 will enter SLEEP mode after power-up, if no register configured.In this mode, internal OSC will be closed, LED0~2 will output high-resistance, power consumption is 90uA

RUN mode: Set GCR.0(LEDE) to “1”, AW2013 will enter RUN mode. OSC starts to work in 5us with the oscillation frequency at 16MHz. The power consumption in this mode is about 450uA

7.3 Soft Reset

AW2013 supports soft reset function. By writing 55h to the register RSTR(address 00h), the device will be soft reset, all of the control circuits and configurable registers are reset to default state.

8 LED Function And Configuration

8.1 General

AW2013 has a 3-channel independent LED controller, which can drive 3 individual LEDs or one group of RGB.

AW2013 drive LEDs with constant current, which has 4 level adjustable: 0mA, 5mA, 10mA, 15mA.

AW2013 support PWM duty cycle control in 256 steps to simplify brightness control.

8.2 LED Control

In AW2013, each channel can be configured independently. By setting “1” to the control bit LCTR.LEx (x=0~2) can enable the corresponding channel. LCTR.LEx are located in the lowest 3-bit of register LCTR (address 30h).

- LCTR.LEx = 0, LEDx channel is disabled
- LCTR.LEx = 1, LEDx channel is enabled

8.3 PWM Control Mode

AW2013 can work in PWM control mode by setting PWM mode control bit LCFGx.MD(x=0~2, address 31h~33h) to “0”.

In this mode, the brightness is controlled by register PWMx(x=0~2) directly. Different kind of brightness effect can be achieved by writing different value continuously to the register PWMx to modulate the brightness of the LEDs.

The value of PWMx can be set to 0~255. Different value is corresponding to different brightness. “0” is corresponding to dark, “255” is corresponding to maximum brightness.

AW2013 also support Fade-in/Fade-out effect by setting LCFGx.FI/LCFGx.FO respectively. If this kind of effect is enabled, AW2013 can automatically smooth the brightness change when the value set to PWMx is hopping.

The speed of Fade-in/out is decided by register LEDxT1/LEDxT3.

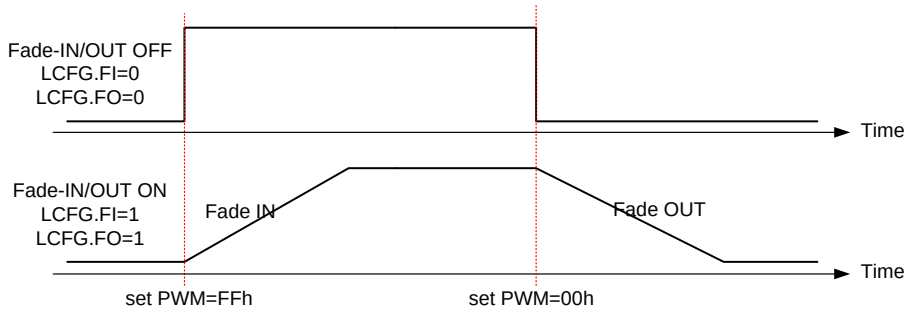


Figure 7 Fade-in/Fade-out in PWM Control Mode

8.4 One Short Programming Mode

AW2013 can work in One Short Programming mode by setting mode control bit LCFGx.MD(x=0~2, address 31h~33h) to “1”.

In this mode, AW2013 can modulate the brightness of LED according to the programmed timing in a breathing cycle. T0~T4 define the 4 key timing in a breathing cycle. T0 is a delay time for starting, T1~T4 composite a full cycle. Different RGB breathing effect with auto color changing can be achieved by setting different T0~T4 for the three channels.

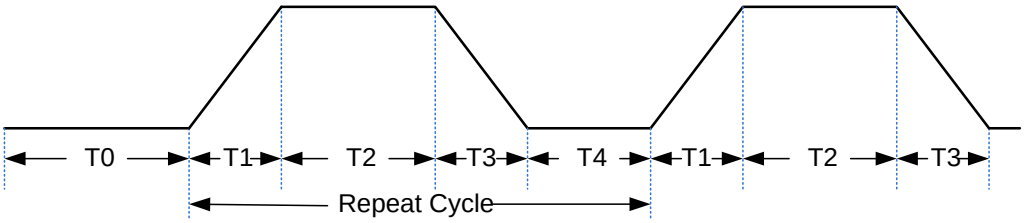


Figure 8 LED breath timing in one short programming mode

Repeat times of auto breathing can be configured by LEDxT2.REPEAT. The auto breathing will loop continuously and never stop, if the LEDxT2.REPEAT is set to “0”. Otherwise it will repeat LEDxT2.REPEAT times then stop.

After the breath effect finished, the interrupt status bit ISR.LISx will be set to “1” automatically. And this bit will be cleared after master read this register.

In this mode, each channel can be configured independently. The breath effect will start once LEDxT2 is written. If user wants to sync the three channel start at the same time, please follow the following steps:

a) Set LCTR to 00h
b) Set PWMx.MD to “0”
c) Configure T0~T4
d) Set PWMx.MD to “1”
e) Set LCTR to 07h

9 Registers

9.1 Register Function

Address	Name	Function	Default
00h	Soft Reset register, RSTR	Soft reset control	33h
01h	Global Control Register, GCR	Set Global control bits	00h
02h	Interrupt Status Register, ISR	Report interrupt status	00h
30h	LED Control Register, LCTR	Enable LED channels	00h
31h～33h	LED Mode Control Register, LCFG	Set working mode	00h
34～36h	PWM Setting Register, PWMx	Set brightness level	00h
37/3A/3Dh	LED Timing Control Register 0, LEDxT0	Set T1&T2 Timing	00h
38/3B/3Eh	LED Timing Control Register 1, LEDxT1	Set T3&T4 Timing	00h
39/3C/3Fh	LED Timing Control Register 2, LEDxT2	Set T0 and Repeat times	00h
77h	I2C address control register, IADR	Modify the device address for I2C bus	45h

9.2 Register Mapping

Addr	Name	W/R	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	RSTR	WR	0	0	1	0	0	0	1	1
01h	GCR	WR	LIE2	LIE1	LIE0	Reserved				ENABLE
02h	ISR	R	LIS2	LIS1	LIS0	PUIS	Reserved			
30h	LCTR	WR	Reserved					LE2	LE1	LE0
31h	LCFG0	WR	0	FO	FI	MD	0	0	IMAX	
32h	LCFG1	WR	0	FO	FI	MD	0	0	IMAX	
33h	LCFG2	WR	0	FO	FI	MD	0	0	IMAX	
34h	PWM0	WR	PWM							
35h	PWM1	WR	PWM							
36h	PWM2	WR	PWM							
37h	LED0T0	WR	0	T1			0	T2		
38h	LED0T1	WR	0	T3			0	T4		
39h	LED0T2	WR	T0				REPEAT			
3Ah	LED1T0	WR	0	T1			0	T2		
3Bh	LED1T1	WR	0	T3			0	T4		
3Ch	LED1T2	WR	T0				REPEAT			
3Dh	LED2T0	WR	0	T1			0	T2		
3Eh	LED2T1	WR	0	T3			0	T4		
3Fh	LED2T2	WR	T0				REPEAT			
77h	IADR	WR	ASEL	DA[6:0]						

9.3 Register Detail Description

9.3.1 Soft Reset register, RSTR

Address: 00h (Default value: 33h), RW

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0
Bit	Symbol	Description					
7:0	D[7:0]	Soft reset control register. Set this register to 55h, all of the circuits in AW2013 will be reset and the configurable registers will be reset to default value. This register can also be used for ID register when reading. The value is 33h when reading this register.					

9.3.2 Global Control Register, GCR

Address: 01h (Default value: 00h), RW							
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LIE2	LIE1	LIE0	Reserved				ENABLE
Bit	Symbol	Description					
7	LIE2	LED2 interrupt enable，enabled when set to “1”					
6	LIE1	LED1 interrupt enable，enabled when set to “1”					
5	LIE0	LED0 interrupt enable，enabled when set to “1”					
4-1	Reserved	Reserved, please set to “0”					
0	ENABLE	LED function enable. enabled when set to “1”					

9.3.3 Interrupt Status Register, ISR

Address: 02h (Default value: 00h), RC							
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LIS2	LIS1	LIS0	PUIS	Reserved			
Bit	Symbol	Description					
7	LIS2	LED2 interrupt indicator bit 0: no interrupt 1: there’s an interrupt request					
6	LIS1	LED1 interrupt indicator bit 0: no interrupt 1: there’s an interrupt request					
5	LIS0	LED0 interrupt indicator bit 0: no interrupt 1: there’s an interrupt request					
4	PUIS	Interrupt indicator for power up.					
3-0	Reserved	-					

9.3.4 LED Control Register, LCTR

Address: 30h (Default value: 00h), RW							
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					LE2	LE1	LE0
Bit	Symbol	Description					
7-3	Reserved	Reserved, please set to “0”					
2	LE2	LED2 enable bit 0： LED2 channel is disabled, the output LED2 shutdown. 1： LED2 channel is enabled					
1	LE1	LED1 enable bit 0： LED1 channel is disabled, the output LED1 shutdown. 1： LED1 channel is enabled					
0	LE0	LED0 enable bit 0： LED0 channel is disabled, the output LED0 shutdown. 1： LED0 channel is enabled					

9.3.5 LED Mode Control Register, LCFG0~2

Address: 31~33h (Default value: 00h), RW							
B0it7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

0	FO	FI	MD	0	0	IMAX
Bit	Symbol	Description				
6	FO	Fade out effect enable. If current brightness level is higher than the value set into PWMx, the controller will darken the LED smoothly when this bit is set to "1" This bit is only valid when LCFGx.MD=0				
5	FI	Fade in effect enable. If current brightness level is lower than the value set into PWMx, the controller will brighten the LED smoothly when this bit is set to "1" This bit is only valid when LCFGx.MD=0				
4	MD	Operating mode selection bit 0： PWM control mode 1： One short programming mode				
1-0	IMAX	Maximum current setting 00：0mA (default) 01：5mA 10：10mA 11：15mA				

9.3.6 PWM Setting Register, PWM0~2

Address: 34~36h (Default value: 00h), RW							
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM							
Bit	Symbol	Description					
7:0	PWM	Maximum brightness level setting. 0： dark 255：maximum brightness					

9.3.7 LED Timing Control Register0, LEDxT0

Address: 37h,3Ah,3Dh (Default value: 00h), RW							
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	T1			0	T2		
Bit	Symbol	Description					
6-4	T1	Set the T1 period in breath cycle. 8 levels can be selected. 000：0.13s 001：0.26s 010：0.52s 011：1.04s 100：2.08s 101：4.16s 110：8.32s 111：16.64s					
2-0	T2	Set the T2 period in breath cycle. 6 levels can be selected. 000：0.13s 001：0.26s 010：0.52s 011：1.04s 100：2.08s 101：4.16s					

9.3.8 LED Timing Control Register1, LEDxT1

Address: 38h,3Bh,3Eh (Default value: 00h), RW							
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	T3			0	T4		
Bit	Symbol	Description					
6-4	T3	Set the T3 period in breath cycle. 8 levels can be selected. 000：0.13s 001：0.26s 010：0.52s 011：1.04s 100：2.08s 101：4.16s 110：8.32s 111：16.64s					
2-0	T4	Set the T4 period in breath cycle. 8 levels can be selected.					

		000：0.13s 011：0.26s 010：0.52s 011：1.04s 100：2.08s 101：4.16s 110：8.32s 111：16.64s

9.3.9 LED Timing Control Register2, LEDxT2

Address: 39h,3Ch,3Fh (Default value: 00h), RW

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T0				REPEAT			

Bit	Symbol	Description
7-4	T0	Set the delay time for breath cycle start. 000：0s 001：0.13s 010：0.26s 011：0.52s 100：1.04s 101：2.08s 110：4.16s 111：8.32s 1000：16.64s
3-0	REPEAT	Set the repeat times 0000：loop continuously, never stop. 0001：repeat 1 time 0010：repeat 2 times …… 1111：repeat 15 times

9.3.10 I2C Address Control Register, IADR

Address: 77h (Default value: 45h), RW

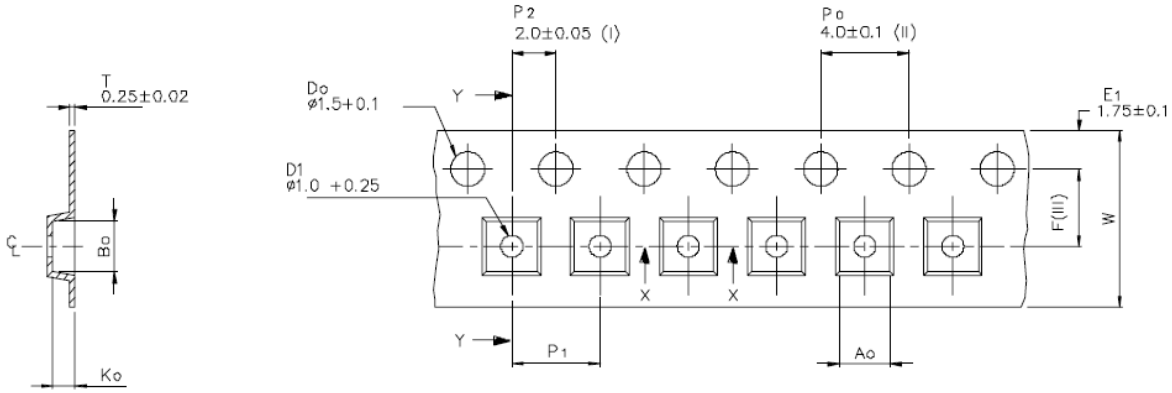
Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASEL	DA[6:0]						

Bit	Symbol	Description
7	ASEL	I2C address select control bit. 0：I2C address is 45h. 1：I2C address = DA[6:0]
6:0	DA[6:0]	Redefined I2C address, only valid when ASEL=1.

10 Package Information

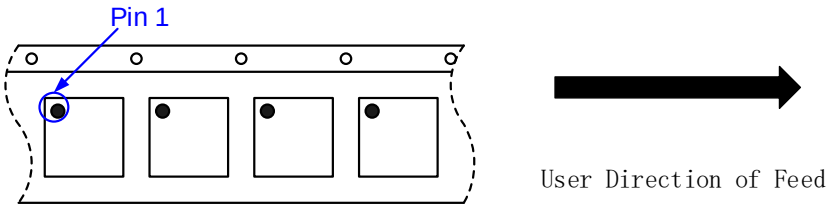
10.1 Tape And Reel

Carrier Tape

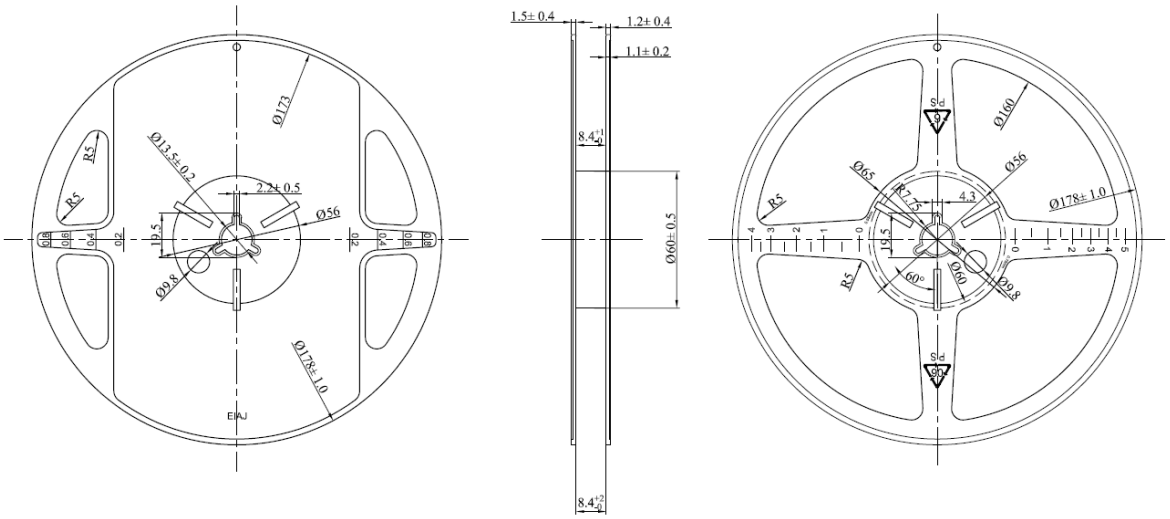


Ao	2.30 +/−0.05
Bo	2.30 +/−0.05
Ko	1.00 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +0.3/−0.1

Pin 1 direction

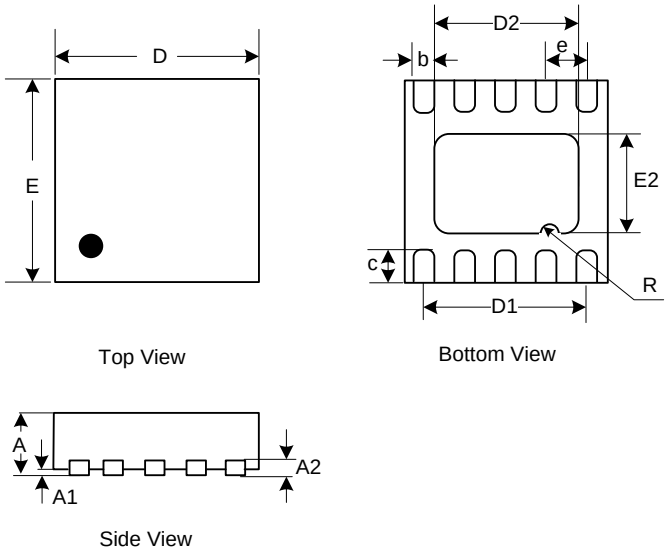


Reel



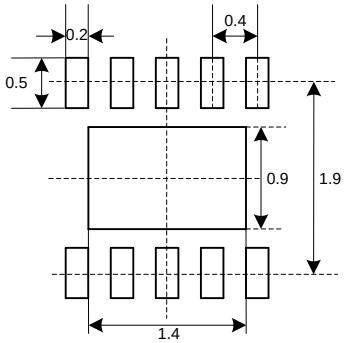
10.2 Package

DFN2x2-10



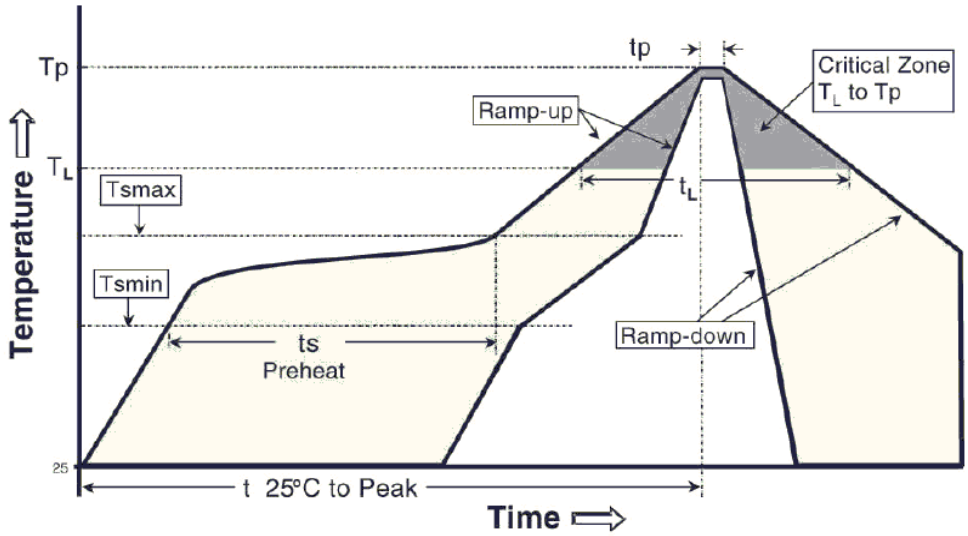
Unit:mm	DFN-10L		
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000		0.050
A2	0.152(Ref.)		
b	0.150	0.200	0.250
c	0.250	0.300	0.350
D	1.950	2.000	2.050
D2	1.350	1.400	1.450
D1	1.600 (Ref.)		
e	0.400 (BSC)		
E	1.950	2.000	2.050
E2	0.850	0.900	0.950
R		0.10	

10.3 Recommended Land Pattern



Recommended Land Pattern(Unit: mm)

10.4 Reflow Profile



Reflow profile

Figure 9 Classification Reflow Profile

Reflow condition	Sn-Pb eutectic assembly		Pb-Free assembly	
	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3 °C/second max.		3 °C/second max.	
Preheat - Temperature Min ($T_{s(min)}$) - Temperature Max ($T_{s(max)}$) - Time (min to max) (t_s)	100 °C 150 °C 60-120 seconds		150 °C 200 °C 60-180 seconds	
$T_{s(max)}$ to T_L - Ramp-up Rate			3 °C/second max.	
Time maintained above: - Temperature (T_L) - Time (t_L)	183 °C 60-150 seconds		217 °C 60-150 seconds	
Peak Temperature (T_p)	225 +0/-5 °C	240 +0/-5 °C	245 +0/-5 °C	250 +0/-5 °C
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.		6 °C/second max.	
Time 25 °C to Peak Temperature	6 minutes max.		8 minutes max.	

Parameters for classification reflow profile

Note: 1. All of the temperature parameters are measured from the top of package;

2、AW2013 is suitable for Pb-Free assembly.

11 Related Product Information

Name	Description	Feature
AW9120	20-channel LED driver with I2C compatible interface.	PWM modulation，Auto breathing effect.
AW9109	9-channel LED driver with I2C compatible interface.	PWM modulation，Auto breathing effect.
AW9106B	6-channel LED driver with I2C compatible interface.	Constant current driver, Auto breathing effect, GPIO expansion

12 Version History

Version	Date	Description
V1.0	2012/8/10	First Release
V1.1	2013/5/28	Change to new document template and add some detail functional description.
V1.2	2014/1/15	1. Fix the description of LCFGx 2. Add the operation description of LCTR.LEx=0
V1.3	2014/5/5	Add marking description
V1.4	2016/5/11	1. Add commended land pattern 2. Fix marking description
V1.5	2017/11/29	Update the ordering information Add the package information

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