AW32207 Switch-mode Single Cell Li-ion Battery Charger With Full USB Compliance and USB-OTG Support

Features

- High-Accuracy Voltage and Current Regulation
  - Charge Voltage Regulation Accuracy ±0.5%(25°C), ±1%(0°C to 85°C)
  - Charge Current Accuracy: ±5%
- Power Up System without Battery
- Programmable Charge Parameters through I²C™ compatible Interface(100kHz/400kHz):
  - -VIN DPM Threshold
  - -Fast-Charge Current
  - -Charge Regulation Voltage(3.5V to 4.5V)
  - -Smart Charge Termination Algorithm
- 2.0A Charge Current using 51mΩ Sensing Resistor
- Specific K-DPM™: VBUS Based Dynamic Power Management
- Up to 95% Charge Efficiency
- 20V Absolute Maximum VBUS Rating
- Trickle-CC-CV Three-stage Automatic Charging Process, Automatic Recharge
- Bad Adaptor Detection and Battery Removing Detection
- Strong Robust Protection: VBUS OVP, Minimum VBUS during Charging, Battery OVP, Reverse Leakage Protection, Thermal Shutdown
- Charge Status and Fault Indication
- 5.05V,1A Boost Mode Operation for USB OTG for 3.5V to 4.5V Battery Input
- FCQFN 2.0mm×2.0mm×0.55mm-20L Package

Applications

- Mobile and Smart Phones
- Digital Camera
- Gaming Device
- Other Handheld Devices

General Description

AW32207 is a high efficiency, large current，switch-mode Li-Ion battery charge management chip. The chip integrates 1.5 MHz synchronous Buck PWM controller, Boost PWM controller and power MOSFETs, effectively reducing the power loss.

The charge process of AW32207 includes: trickle, constant current (CC) and constant voltage (CV). The charge parameters and operating modes are programmable through I²C Interface. Also, the charge termination is determined by a programmable algorithm. The charge process runs automatically and recharging occurs when the battery voltage drops below V_{OREG}-V_{RCH}.

If the input source is removed, the IC enters a high-impedance mode, keeping ultra-low power loss from battery and preventing leakage from the battery to the input. Charge current is reduced when the temperature of die reaches 140°C, protecting the device and PCB from damage.

The IC can operate in boost mode to support USB OTG device on command from system. The boost regulator uses same external components with charge mode, and it supports up to 1A output current for OTG device. Meanwhile, the output voltage of boost regulator can be configured from 5.05V to 5.35V by the host.

Application Circuit

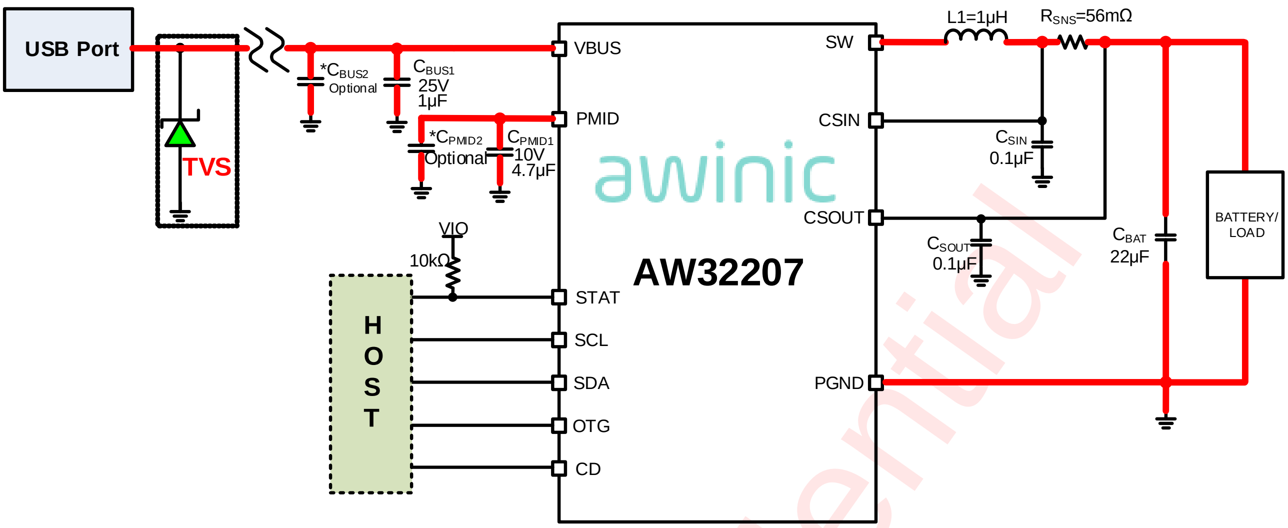

Figure 1 Typical Application Circuit of AW32207

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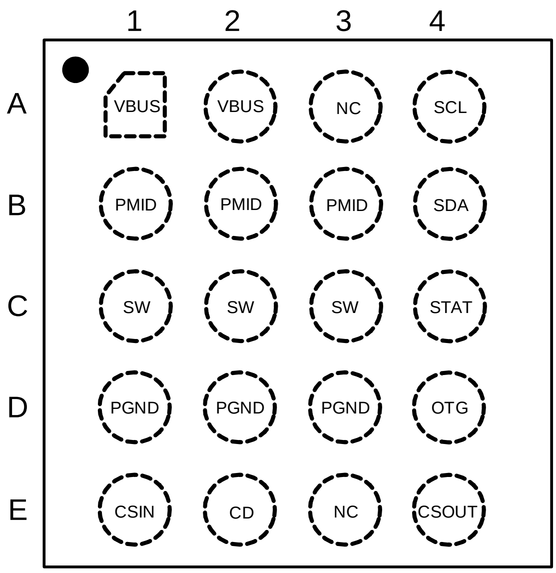
Pin Configuration and Top Mark

AW32207FCR PIN Configuration (Top View)



AW32207FCR Marking (Top View)

6I6Y – AW32207FCR

XXXX – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin No.	Pin Name	Description
A1, A2	VBUS	Charge input voltage and USB-OTG output voltage. Bypass with a 1μF capacitor to PGND.
A3	NC	No connection.
A4	SCL	I^2C Interface Serial Clock.
B1, B2, B3	PMID	Power input voltage. Bypass with a minimum of 4.7μF capacitor to PGND.
B4	SDA	I^2C Interface Serial Data.
C1, C2, C3	SW	Switch node. Connect to output inductor.
C4	STAT	Charge status and interrupt output pin. Open drain output indicating charge status. The charger pull the pin low when charging, and open drain for other conditions. During faults, a 128μs pulse interrupt signal is sent out.
D1, D2, D3	PGND	Power ground.
D4	OTG	On-The-Go. This pin sets the default charge current for charge mode. At POR while in default mode, the OTG pin is used as the input current limiting selection pin. When OTG=High, I_{BUS_LIMIT}<500mA and when OTG=Low, I_{BUS_LIMIT}<100mA. Also, the OTG pin enable the boost regulator in conjunction with OTG_EN and OTG_PL bits. The default value is pulled up to high level in the chip by a 0.3MΩ (typical) internal resistor.
E1	CSIN	Charge current-sense input. Connect to the sense resistor in series with the battery. Bypass this pin with a 0.1μF ceramic capacitor to PGND.
E2	CD	Charging disable. If this pin is set to high, fast charging is disabled, or if it is low, fast charging is enabled. The default value is pulled down to low level by a 1.2MΩ(typical) internal resistor.
E3	NC	No connection.
E4	CSOUT	Battery voltage and current sense input. Bypass it with a ceramic capacitor (minimum 0.1μF) to PGND.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32207FCR	-40°C～85°C	FCQFN 2×2-20L	6I6Y	MSL1	ROHS+HF	3000 units/ Tape and Reel

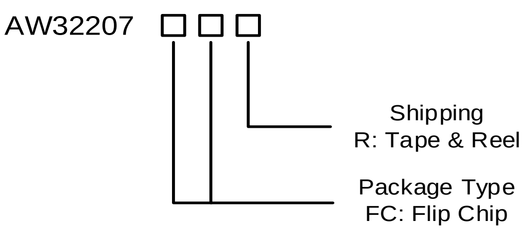


Figure 3 Package Information

Typical Application Circuits

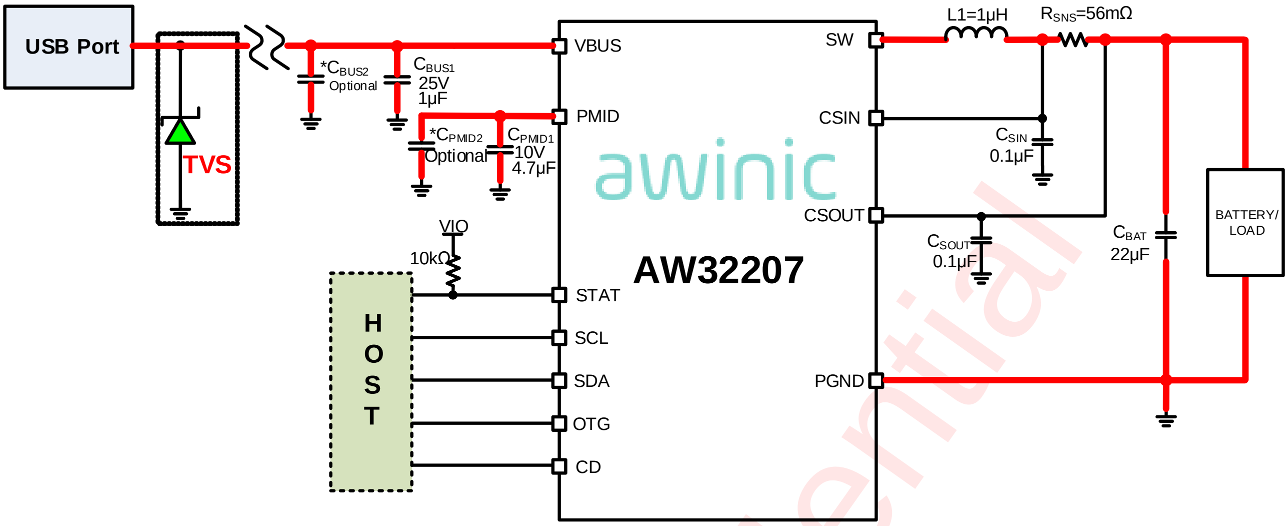


Figure 4 AW32207 Application Circuit

Notice for typical application circuits:

1：Please place C_{BUS1}, C_{PMID1}, C_{SIN}, C_{SOUT}, C_{BAT} to the chip and PGND as close as possible.

2：For the sake of driving capability, the power lines, output lines, and the connection lines of L1, R_{SNS}, and BATTERY should be as short and wide as possible. The power path is marked in red as shown in the Figure 4 above, please trace according to 2A power line alignment rules.

3：Large surge voltage at VBUS may damage the chip or VBUS capacitor. In order to avoid this risk, a TVS tube can be placed in parallel with the VBUS port of USB interface.

4: C_{BUS2} and C_{PMID2} are optional capacitors used for FCC test.

Absolute Maximum Ratings(NOTE1)

PARAMETERS		MIN	MAX	UNIT
Supply voltage range V_{BUS} (with respect to PGND)		-1.5	20	V
Input voltage range (with respect to PGND)	SCL, SDA, OTG, CD	-0.3	6	V
Output voltage range (with respect to PGND)	STAT	-0.3	6	V
	PMID, SW(NOTE 2)	-0.3	6	V
	BAT, CSIN	-0.3	6	V
Output sink current	STAT		10	mA
Output current(average)	SW		2	A
Operating free-air temperature range		-40	85	°C
Operating junction temperature T_J		-40	150	°C
Storage temperature T_{STG}		-65	150	°C
Lead temperature (Soldering 10 seconds)			260	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The chip integrates a 100mA pull-down current at PMID and SW pin, to protect these pins from being damaged by overvoltage.

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 3)	±2	kV
CDM(NOTE 4)	±1.5	kV
Latch-Up(NOTE 5)	+IT：200 -IT：-200	mA

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE4: Test method: ESDA/JEDEC JS-002-2018

NOTE5: Test method: JESD78E

Recommended Operating Conditions

PARAMETERS	DESCRIPTION	MIN	NORM	MAX	UNIT
V_{BUS}	Supply voltage	4		6(NOTE 6)	V
V_{BAT}	Battery voltage			4.50	V
V_{BUS_B}	Output voltage (Boost)			5.35	V
I_{VBUS_B}	Output current (Boost)			1	A
I_{BAT}	Fast charging current			1.82	A
T_A	Ambient temperature	-40		85	°C
L_1	Inductance		1		μH
R_{SNS}	Sense resistor		56		mΩ
C_{BUS1}	C_{BUS1} capacitance		1		μF
C_{PMID1}	C_{PMID1} capacitance		4.7		μF
C_{BAT}	C_{BAT} capacitance		22		μF
C_{SIN}	C_{SIN} capacitance		0.1		μF
C_{SOUT}	C_{SOUT} capacitance		0.1		μF

NOTE6: The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the PMID or SW pins. A tight layout minimizes switching noise.

Thermal Information

PARAMETERS	VALUE	UNIT
Junction-to-ambient thermal resistance θ_{JA}	51	°C /W

Electrical Characteristics

Circuit of Figure 4, V_{BUS}=5V, OPA_MODE=0, HZ_MODE=0, CD_PIN=0, T_J=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{VBUS}	VBUS supply current control	V_{BUS}>V_{INMIN}, V_{CSOUT}>V_{OREG}, PWM Switching		13		mA
		V_{BUS}>V_{INMIN}, V_{CSOUT}>V_{BAT_OVP}, PWM not switching		0.18		mA
		V_{BUS}=5V, CD=1		180		μA
		V_{BUS}=5V, HZ_MODE=1		160		μA
I_{LKG}	Leakage current from battery To VBUS pin	V_{CSOUT}=4.2V, V_{BUS}=0V			5	μA
	Battery discharge current in High Impedance mode	V_{BAT}=4.2V, High-Z mode, V_{BUS}=0V or unconnected, SCL, SDA, OTG=0V, 0°C < T_J < 85°C	10	16	30	μA
VBUS UVLO & VINMIN						
V_{UVLO}	UVLO exiting threshold voltage	V_{BUS} rising	3.4	3.6	3.8	V
	Hysteresis for UVLO	V_{BUS} falling	100	150	200	mV
	Deglitch time for V_{UVLO}	Exits UVLO		140		ms
V_{INMIN}	Input voltage lower limit for normal charging	V_{BUS} rising	3.8	4.0	4.2	V
	Hysteresis for V_{INMIN}	V_{BUS} falling	100	150	200	mV
I_{DET}	V_{BUS} validation detection current	V_{BUS} rising>4V	15	30	45	mA
T_{DET}	V_{BUS} validation time	V_{BUS} rising>4V		30		ms
SLEEP MODE						
V_{SLP}	Sleep-Mode entry threshold, V_{PMID}-V_{CSOUT}	3.8V<V_{CSOUT}, V_{BUS} falling	0	70	120	mV
V_{SLP_EXIT}	Sleep-Mode exit hysteresis, V_{PMID}-V_{CSOUT}	3.8V<V_{CSOUT}, V_{BUS} rising	80	200	280	mV
T_{SLP_EXIT}	Deglitch time for VBUS rising above V_{CSOUT} +$V_{SLP-EXIT}$	V_{BUS} rising		30		ms
CHARGE PROCESS						
V_{SHORT}	Trickle to fast charge threshold	V_{CSOUT} rising	2.0	2.1	2.2	V
	V_{SHORT} hysteresis	V_{CSOUT} falling		100		mV
V_{LOWV}	Weak battery voltage threshold	V_{CSOUT} rising		3.7		V
	Weak battery voltage accuracy		-5		5	%
	Hysteresis for V_{LOWV}	Battery voltage falling		100		mV
	Deglitch time			30		ms
V_{OREG}	Output regulation voltage programmable range	V_{BUS}=5V, TE=0, operating in voltage regulation, programmable	3.5		4.5	V
	Output regulation voltage accuracy	T_J=25°C	-0.5		0.5	%
		T_J=0°C~85°C	-1		1	%
V_{RCH}	Recharge threshold voltage	V_{OREG}=4.2V, below V_{OREG}	60	100	140	mV
	Recharge threshold voltage programmable range	V_{OREG}=4.2V, TE=1, charge done and V_{CSOUT} below V_{OREG}, programmable	50		200	mV

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Deglitch time for V_{RCH}	V_{CSOUT} falling after charge termination		130		ms
CHARGE CURRENT						
I_{CHG}	Output charge regulation current programmable range	$V_{SHORT} \leq V_{CSOUT} < V_{OREG}$, $R_{SENSE}=56m\Omega$	485		1821	mA
	Default charge current (OTG_PIN=1 after POR)	$V_{SHORT} \leq V_{CSOUT} < V_{OREG}$, $R_{SENSE}=56m\Omega$		485		mA
	Accuracy for charge current regulation	I_{CHG}=1820mA, $R_{SENSE}=56m\Omega$	-5		5	%
I_{PRE_CHG}	Trickle charge current	$V_{BUS}>V_{INMIN}$, $V_{CSOUT}<2.1V$	80	100	130	mA
CHARGE TERMINATION DETECTION						
I_{TERM}	Termination charge current threshold, programmable	$V_{CSOUT}>V_{OREG}-V_{RCH}$, $R_{SENSE}=56m\Omega$	60		485	mA
	Accuracy for charge termination detection	I_{TERM}=121mA	-15		15	%
T_{DET}	Termination detecting window programmable range	$I_{CHG}<I_{TERM}$	64		1024	ms
T_{TERM}	Termination deglitch time programmable range	$I_{CHG}<I_{TERM}$	8		256	ms
K_DPM™						
V_{K_DPM}	K_DPM™ clamps V_{BUS} programmable range		4.250		4.775	V
	Accuracy for K_DPM™ clamps V_{BUS}		-5		5	%
STAT						
$V_{OL(STAT)}$	Low-level output saturation voltage, STAT pin	I_O=10mA, sink current			0.3	V
I_{LKG_STAT}	High-level leakage current for STAT	STAT is in High-impedance status, V_{STAT}=5V			2	μA
CD, OTG PIN LOGIC LEVEL						
V_{IL}	Input low threshold level				0.45	V
V_{IH}	Input high threshold level		1.2			V
I²C BUS LOGIC LEVELS AND TIMING CHARACTERISITICS						
V_{OL}	Output low threshold level	I_O=10mA, sink current			0.3	V
V_{IL}	Input low threshold level	V_{pull_up}=1.8V, SDA and SCL			0.45	V
V_{IH}	Input high threshold level	V_{pull_up}=1.8V, SDA and SCL	1.2			V
I_{BIAS}	Input bias current	V_{pull_up}=1.8V, SDA and SCL			1	μA
PWM						
R_{OVP}	Internal OVP MOSFET on-resistance	I_{IN_LIMIT}=500mA, measured from VBUS to PMID		47		mΩ
R_{PMOS}	Internal top P-channel MOSFET on-resistance	I_{IN_LIMIT}=500mA, measured from PMID to SW		45		mΩ
R_{NMOS}	Internal bottom N-channel MOSFET on-resistance	I_{IN_LIMIT}=500mA, measured from SW to PGND		60		mΩ
f_{OSC}	Oscillator Frequency			1.5		MHz
	Frequency Accuracy		-10		+10	%
	Frequency Shift			+13		%
D_{MIN}	Minimum Duty Cycle		5			%

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
D_{MAX}	Maximum Duty Cycle				100	%
CHARGE PROCESS PROTECTION						
V_{OVP_VBUS}	Input VBUS OVP threshold voltage	V_{BUS} rising		6.4		V
	Accuracy for VBUS OVP threshold		-5		5	%
	V_{OVP_VBUS} hysteresis	V_{BUS} falling from above V_{OVP_VBUS}		180		mV
V_{OVP_BAT}	Output OVP threshold voltage	V_{CSOUT} threshold over V_{OREG} to turn off charger during charge		117.6		% V_{OREG}
	V_{OVP_BAT} hysteresis	Lower limit for V_{CSOUT} falling from above V_{OVP_BAT}		12.4		% V_{OREG}
I_{LIMIT}	Cycle-by-cycle current limit for charge	Charge mode operation		3.88		A
T_{CF}	Charge current reduction temperature	Junction temperature rising		140		°C
	Thermal hysteresis for T_{CF}	Junction temperature falling		30		°C
T_{OTP}	Overheating shutdown protection temperature	Junction temperature rising		160		°C
	Thermal hysteresis for T_{OTP}	Junction temperature falling		30		°C
BATTERY DETECTION						
I_{DBAT}	Battery detection current before charge done (sink current)	Begins after termination detected and V_{CSOUT}< V_{OREG}		-0.5		mA
T_{DBAT}	Battery detection time			262		ms
BOOST MODE						
V_{BUS_B}	Boost output voltage (to VBUS pin) programmable range	2.5V < V_{CSOUT} < 4.5 V	5.05		5.35	V
	Boost output voltage accuracy	3.5<V_{CSOUT}<4.5, I_{BO}=1A	-3		2	%
I_{BOTMAX}	Maximum output current for Boost	V_{BUS_B}=5.05V, 3.5V<V_{CSOUT}<4.5V			1000	mA
I_{LIMIT_B}	Cycle-by-cycle current limit for boost	V_{BUS_B} =5.05V, 3.5V<V_{CSOUT}<4.5V		2.65		A
V_{BUSOVP_B}	Overvoltage VBUS OVP threshold voltage for boost	V_{BUS} rising		6		V
	Accuracy for VBUS OVP Threshold		-5		5	%
	V_{BUSOVP_B} hysteresis	VBUS falling from above V_{BUSOVP_B}		200		mV
V_{UVLO_B}	Minimum battery voltage for boost	Before boost start		2.9		V
		Hysteresis		400		mV
R_{OUT_B}	Boost output resistance at High-Impedance mode (From VBUS to PGND)	CD=1 or HZ_MODE=1		304		kΩ

I²C INTERFACE TIMING

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock Frequency				400	kHz
$t_{DEGLITCH}$	Deglitch Time	SCL		200		ns
		SDA		250		ns
$t_{HD:STA}$	(Repeat-Start) Start Condition Hold Time		0.6			μs
t_{LOW}	Low Level Width of SCL		1.3			μs
t_{HIGH}	High Level Width of SCL		0.6			μs
$t_{SU:STA}$	(Repeat-Start) Start Condition Setup Time		0.6			μs
$t_{HD:DAT}$	Data Hold Time		0			μs
$t_{SU:DAT}$	Data Setup Time		0.1			μs
t_R	Rising Time of SDA And SCL				0.3	μs
t_F	Falling Time of SDA And SCL				0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
t_{BUF}	Time Between Start and Stop Condition		1.3			μs

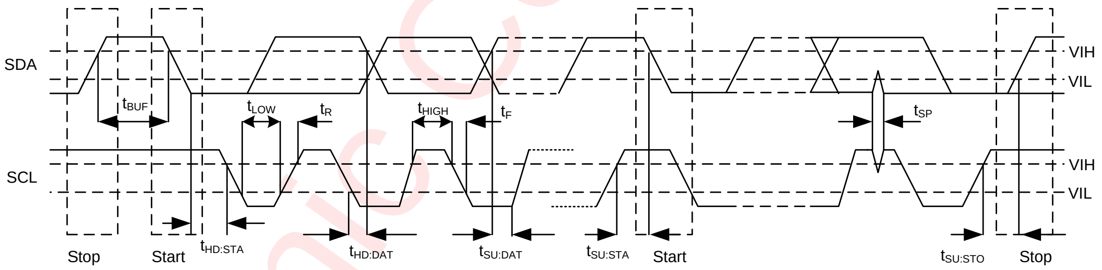


Figure 5 SCL and SDA timing relationships in the data transmission process

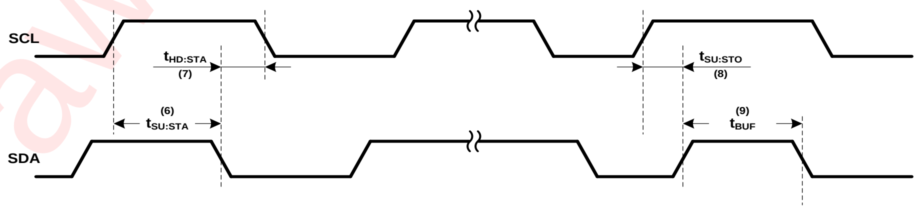


Figure 6 The timing relationship between START and STOP state

Typical Characteristics

VBUS=5V, T_A=25°C, Circuit of Figure 4 unless other noted.

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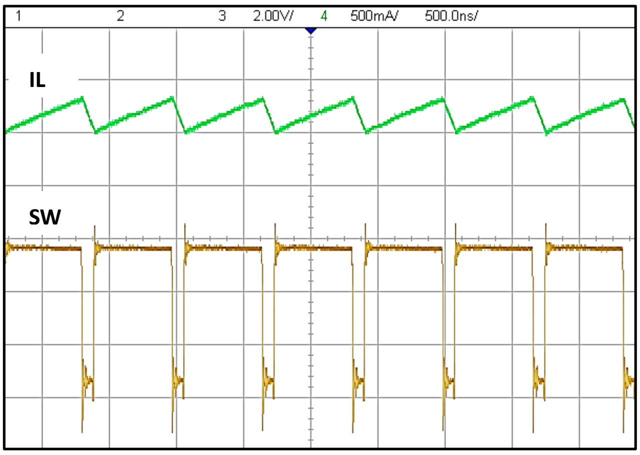
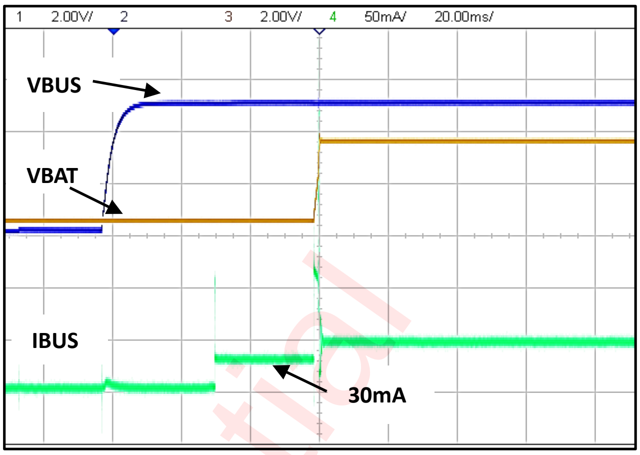


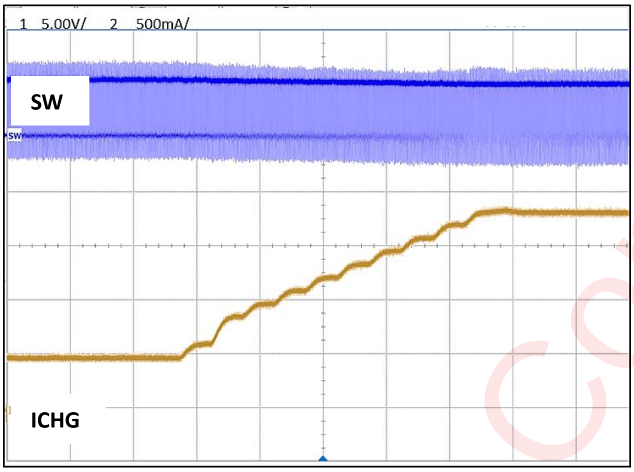
V_{BAT}=3.6V, I_{CHG}=1.82A, V_{OREG}=4.36V

Figure 7 PWM charging waveform



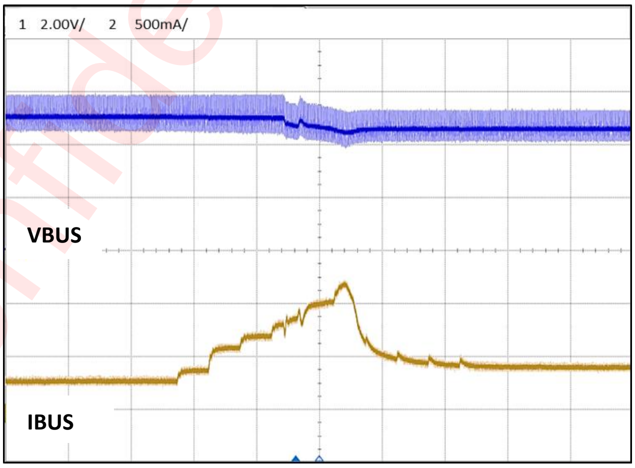
No battery, OTG=1

Figure 8 VBUS power up



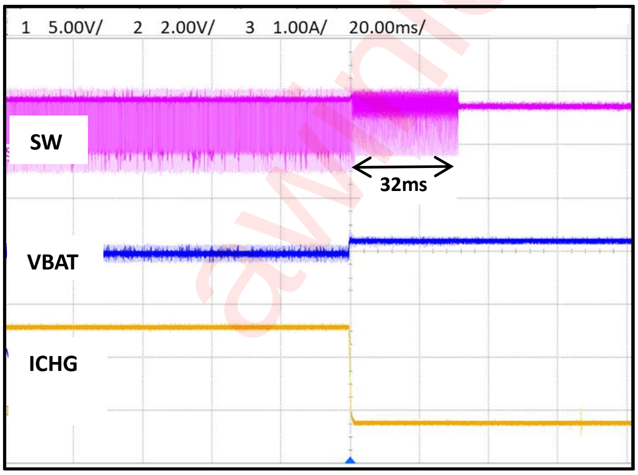
V_{BAT}=3.6V, I_{CHG} ramp up from 0.485A to 1.82A

Figure 9 Charge current ramp up



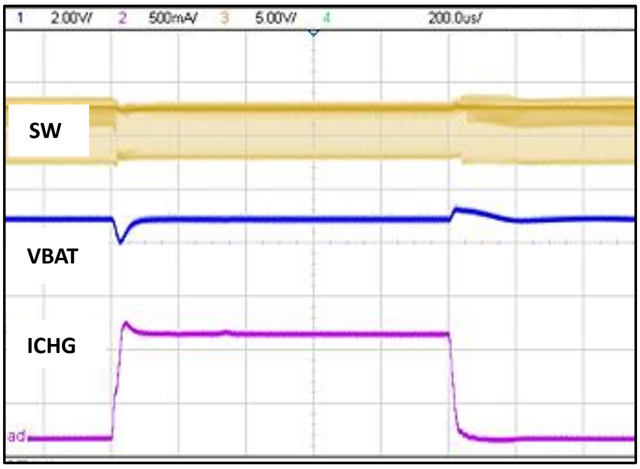
VBUS=5V at 500mA, V_{BAT}=3.5V, I_{CHG}=1.82A, V_{DPM}=4.55V,

Figure 10 VIN based DPM



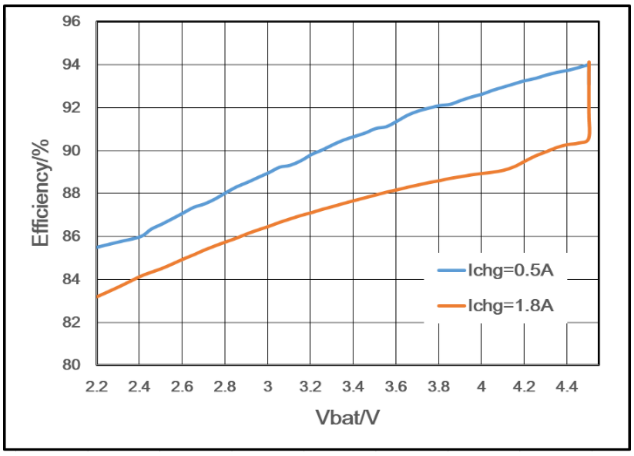
TE=1, TE_P=0, TE_NUM=8, TE_DEG=32ms

Figure 11 Charge termination detection



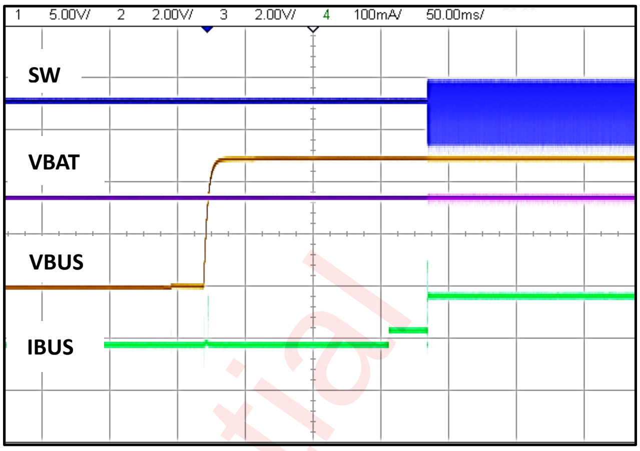
V_{OREG}=4.36V, I_{CHG}=1.82A, V_{BAT}=4.2V, I_{LOAD}=0 to 1A

Figure 12 Load transient in download mode



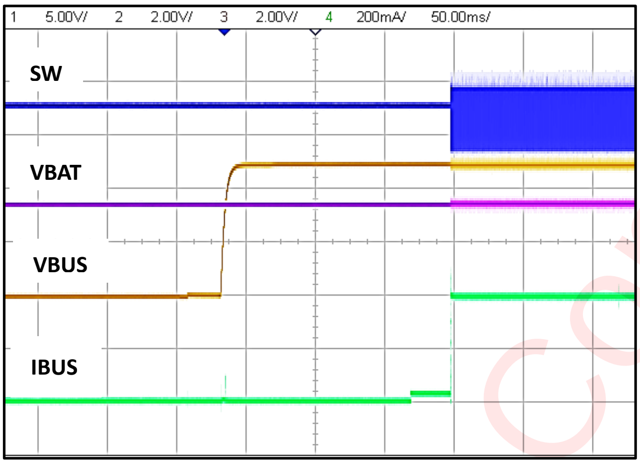
V_{BUS}=5V, the DCR of Inductor is 23mΩ

Figure 13 Charge efficiency vs. VBAT



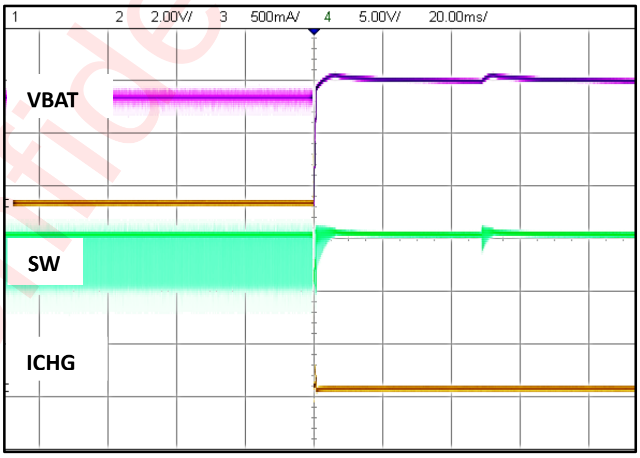
V_{BAT}=3.4V, OTG=0

Figure 14 Charge startup at VBUS plug-in



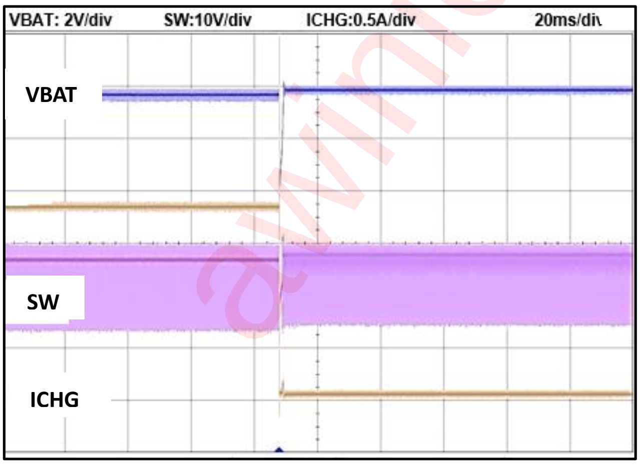
V_{BAT}=3.4V, OTG=1

Figure 15 Charge startup at VBUS plug-in



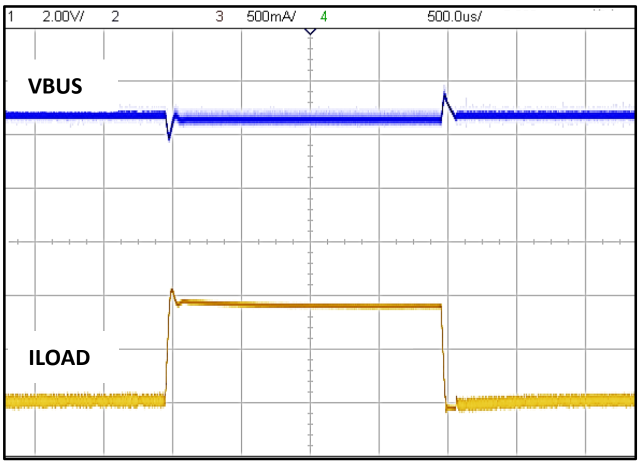
V_{BAT}=3.9V, I_{CHG}=1.82A, TE=1

Figure 16 Battery removal during charging



V_{BAT}=3.9V, I_{CHG}=1.82A, TE=0

Figure 17 Battery removal during charging



I_{LOAD}= 5mA to 1A and to 5mA

Figure 18 Load transient for boost mode

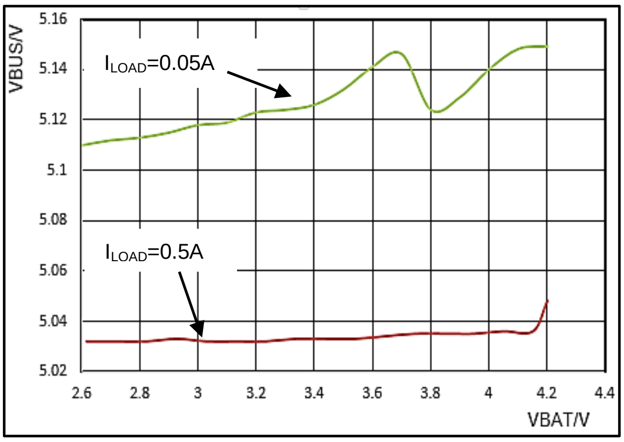


Figure 19 Line regulation for boost mode

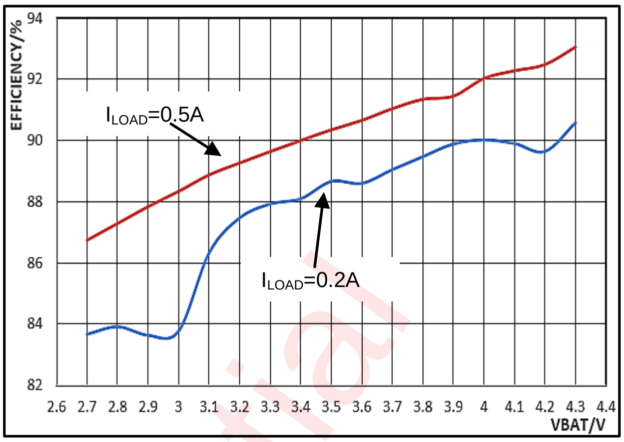


Figure 20 Efficiency for boost mode

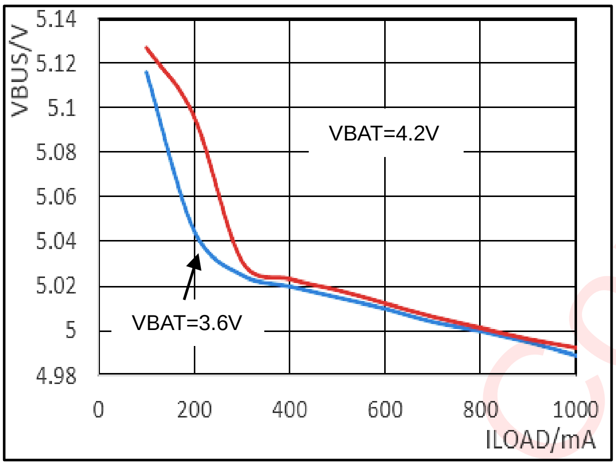
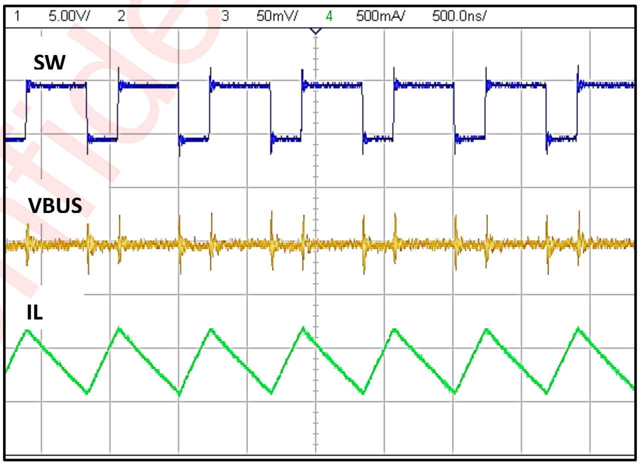
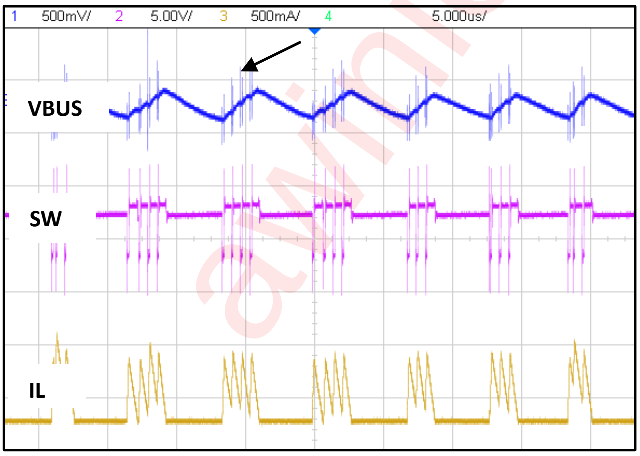


Figure 21 Load regulation for boost mode



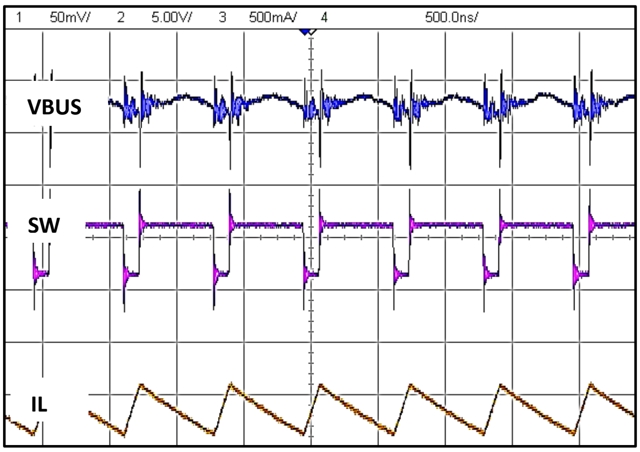
V_{BAT}=3.8V, I_{LOAD}=1A

Figure 22 Boost PWM waveform



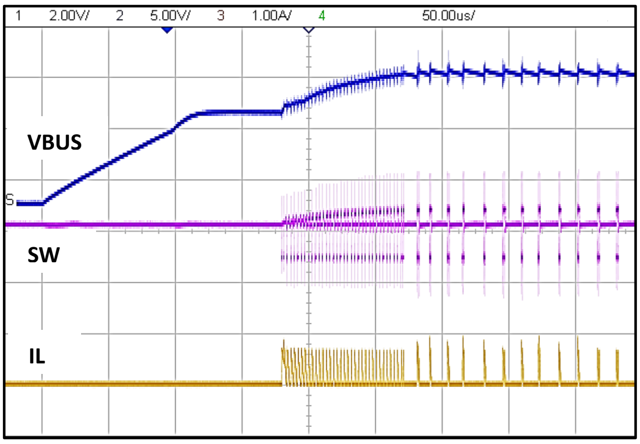
V_{BAT}=4.2V, I_{LOAD}=0.1A

Figure 23 Boost BURST mode waveform



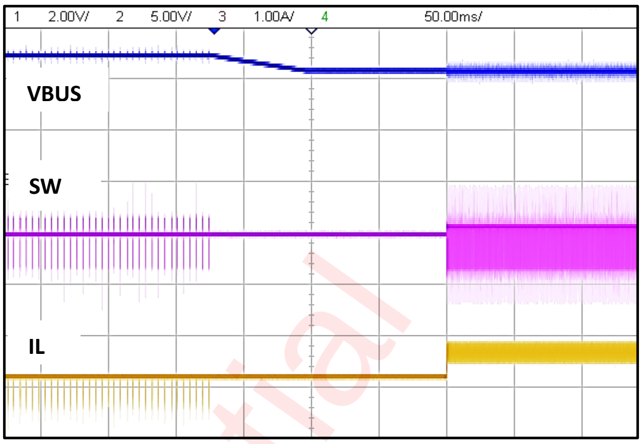
V_{BAT}=4.2V, I_{LOAD}=0.1A, force PWM operation

Figure 24 Boost FPWM waveform at light load



Boost start up with V_{BAT}=3.6V, I_{LOAD}=20mA, C_{BUS1}=10μF

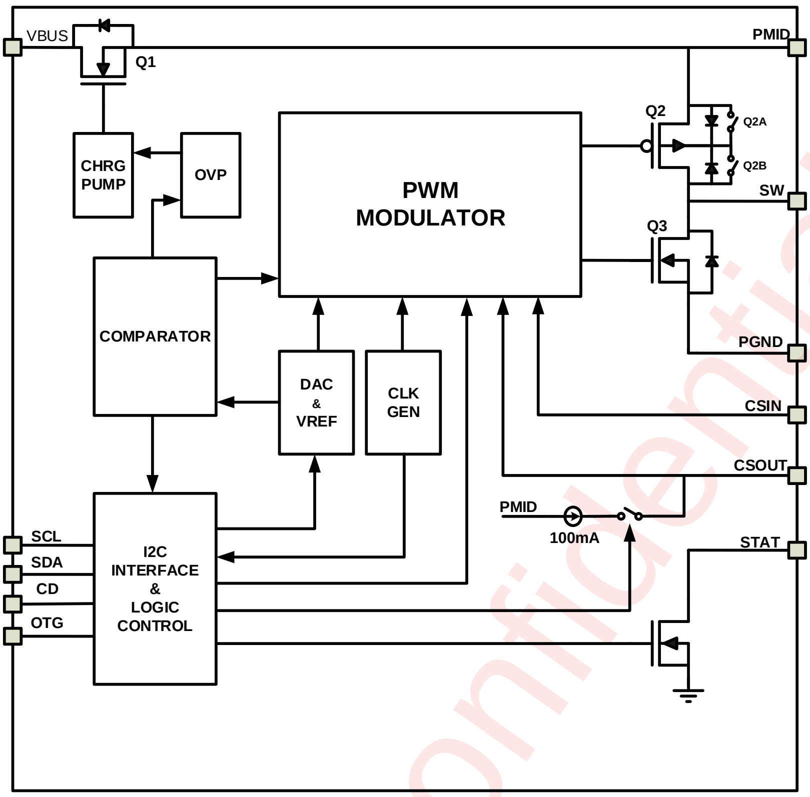
Figure 25 Boost startup



VBUS=4.5V(CHG)/5.05V(BST), VBAT=3.5V

Figure 26 Boost to charge mode transition

Functional Block Diagram



PMID	Q2A	Q2B
$>V_{BAT}$	ON	OFF
$<V_{BAT}$	OFF	ON

Figure 27 The AW32207 Function Block

Detailed Functional Description

AW32207 is a highly efficient, highly integrated synchronous switch charger. It has a wide range of output regulation voltage and can provide maximum 2-A current for single-cell lithium ion or lithium polymer battery. Furthermore, AW32207 also supports boost mode for USB OTG applications.

The AW32207 has three operation mode:

• Charge mode: charges a single-cell battery with default or host configured value.

• Boost mode: boosts the battery voltage to 5.05V(default value) on VBUS pin for OTG applications.

• High impedance mode: stops charging or boosting and operates in a low power cost mode.

The IC starts in charge mode, which is the default mode and using each register's default value, also, it can switch smoothly among the different modes through I^{2}C communication with the host.

Battery Charge Profile

The AW32207 Provides three main charging phases: pre-charge，fast-charge and constant-voltage charge (see the Figure 28). If the charging parameters is not configured via I^{2}C, the charger works under the default configuration.

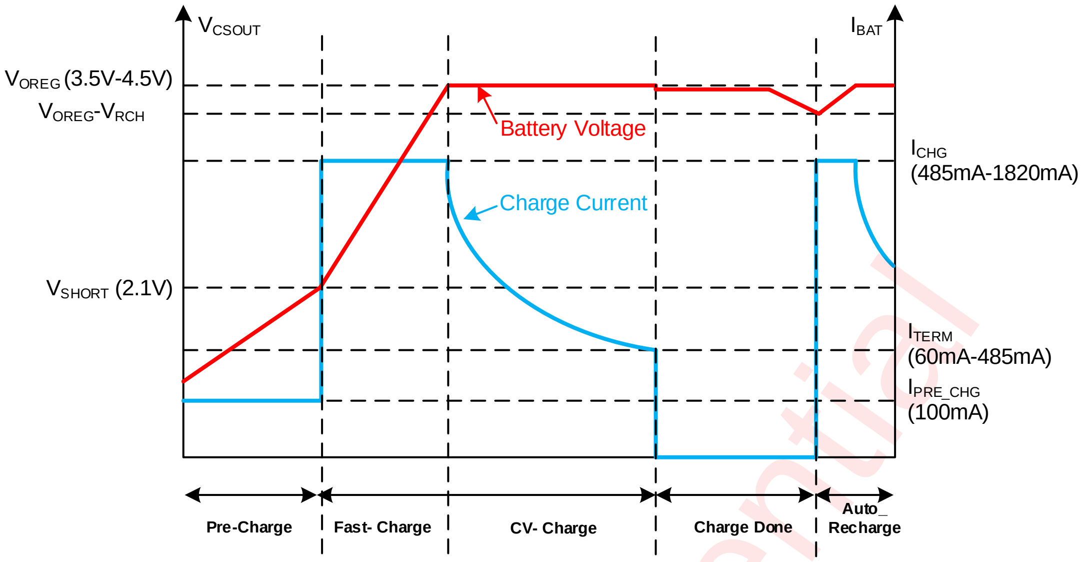


Figure 28 The AW32207 Function Block

- Pre-charge: In the pre-charge process, the IC can safely pre-charge the deeply depleted battery with small current until the battery voltage rise to the pre-charge threshold (V_{SHORT}), in which the IC enter the fast-charge process.
- Fast charge: When V_{BAT} exceeds V_{SHORT}, the IC enters the fast charge process. The REG04H[6:3] can be set to change the fast-charge current.
- Constant-voltage charge: The charge mode changes from CC to CV, when the V_{BAT} rises to the battery-full voltage (V_{OREG}) set via REG02H[7:2]. At the same time, the charge current starts decreasing in CV charge process.

Due to multiple loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation, the actual charge current may be less than the setting value.

When the charge current is smaller than termination current threshold I_{TERM} in CV process and the CTA is satisfied, the charge cycle will be completed and the charge status is updated to charge done. The register REG04H[2:0] can set the termination charge current threshold I_{TERM}. The termination function can be disabled via TE=0 (REG01H[3] = 0). The termination function is show as table 2.

Table 2 Termination Function Selection Table

TE	After Termination Condition is Meet	
	Operation	**Charge Status**
0	Keep CV Charge	Charge
1	Charge done	Charge done

A new charge cycle starts when any of the following conditions are valid:

- Auto-recharge kicks in.
- Battery charging is enabled via the I^2C.
- The input power is recycled .

Under the following condition:

- No any charge fault was reported.

Operational Chart Flow

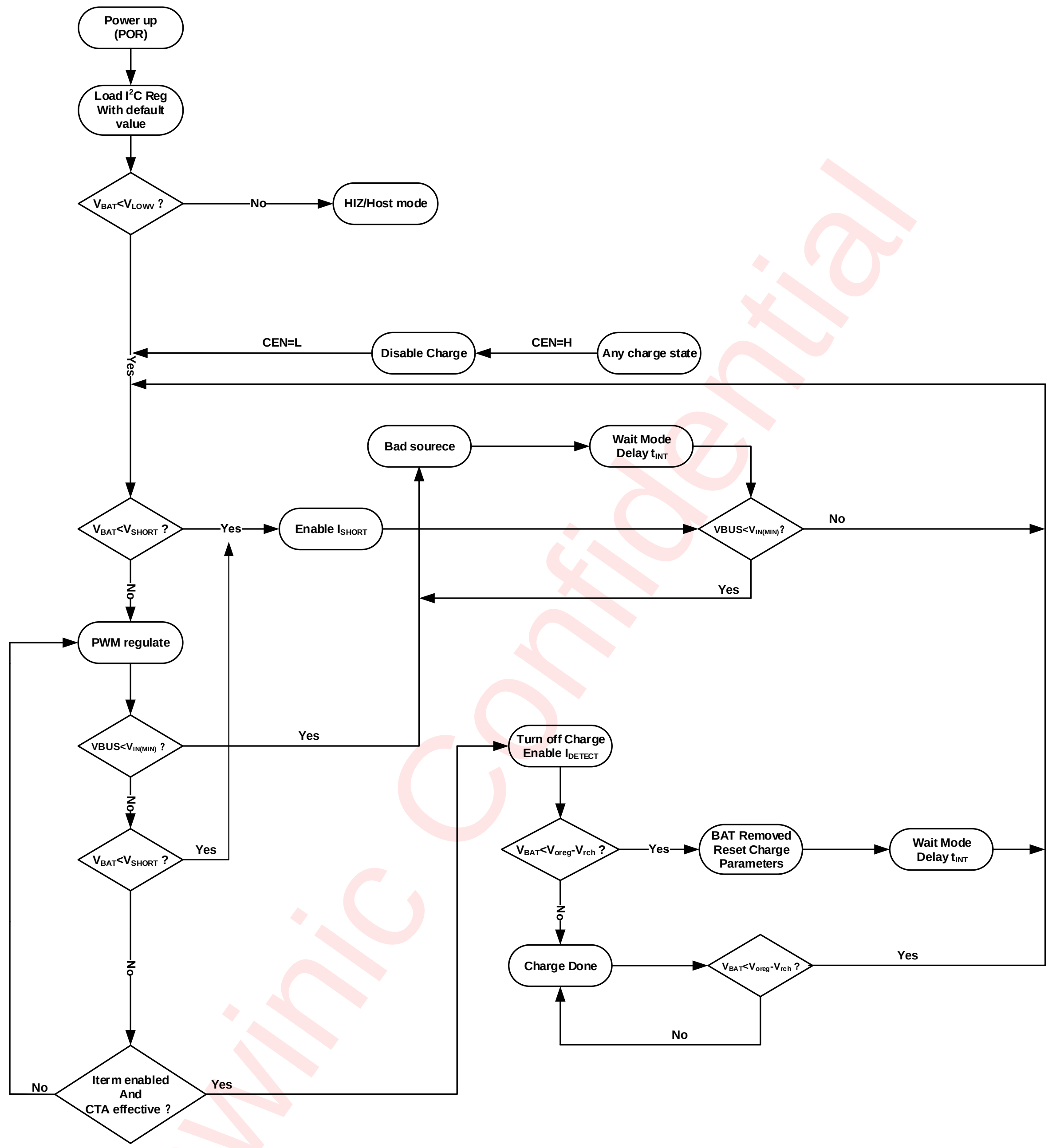


Figure 29 Charge Flow Chart of AW32207

The charge flow chart of AW32207 is showed as above. The IC loads registers value after power-on-reset(POR), then detects the VBAT voltage. If $V_{BAT}>V_{LOWV}$, the IC enters HZ MODE; otherwise, it operates in the charge mode. At the beginning of charge process, when battery voltage is lower than V_{SHORT}, the charger outputs a short-circuit current, I_{PRE_CHG}, to pre-charge the battery. When the battery voltage reaches V_{SHORT}, the charge current increases to I_{CHG}, which is the fast charge current and can be set by the host. Once the battery voltage is near or equal to the regulation voltage, V_{OREG}, the IC enters voltage regulation phase. In this phase, the voltage of battery is stable but the charge current is decreasing. The default regulation voltage is 3.54V, meanwhile, it can be programmed from 3.5V to 4.5V through I²C interface. During the charge process, the IC monitors the charge current if termination function is enabled (REG01H[3]=1), once the Charge

Termination Algorithm(CTA™) is meet, the IC turns off the PWM charge process and discharge the battery with a small current, I_{DET}, for a period of t_{DET} (262ms typical). Then the IC will check the battery voltage, if it is still above the recharge threshold after t_{DET}, the battery charging is complete, the status bit and pin are updated to indicate the charging process has completed. This strategy is used to ensure that termination do not occur when the battery is removed. If a charge process has completed, the new charge cycle will restart when the battery voltage falls below the V_{OREG}-V_{RCH} threshold.

Meanwhile, all the parameters of CTA are programmable, and setting the charge termination bit (REG01H[3]) to 0 can disable the charging termination detection, please refer to I²C register section for more details.

VBUS Protection

The chip sets OVP, SLEEP MODE, K-DPM™, VINMIN protection mechanisms at the VBUS input port.

VBUS OVP

AW32207 integrates input overvoltage protection to prevent the device and other downstream components from damage of the high input voltage (Voltage from VBUS to GND). If the VBUS voltage exceeds V_{OVP_VBUS} threshold(6.4V typical)， the chip will stop charging and send out a fault pulse from STAT pin. When V_{BUS} drops lower than the input overvoltage exit threshold (6.4V-0.18V typical), the charge process will continue.

Bad Adaptor Detection

This detection makes sure that the adaptor has enough abilities to charge the battery. In this detection process, when VBUS rises above V_{INMIN} (4.0V typical), the IC applies a current sink to VBUS for 30ms and then detects the voltage of VBUS. If the V_{BUS} is still higher than V_{INMIN}, the adaptor is good and the charge process begins. Otherwise, this detection does not pass and the charge process is suspended. This detection repeats every t_{INT}, until a good adaptor is detected.

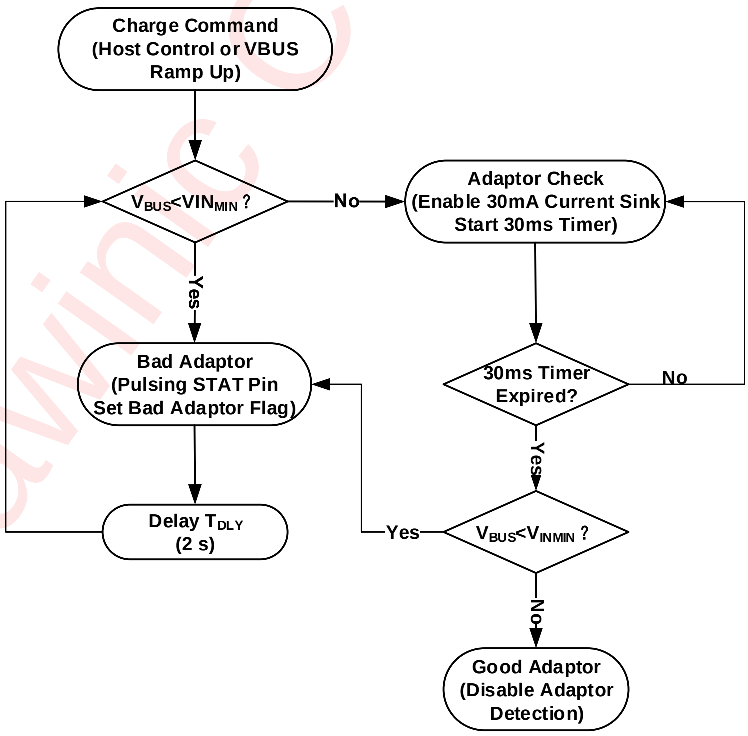


Figure 30 Bad Adaptor Detection Scheme Flow Chart

Sleep Mode

When V_{BUS} is lower than V_{CSOUT}+V_{SLP} (lasts for 1 ms), and V_{BUS} is higher than V_{INMIN}, the IC enters sleep mode. During sleep mode, PWM switching is turned off to prevent the battery from drain into VBUS.

VBUS Based Dynamic Power Management——K-DPM™

The K-DPM™ allows AW32207 to adaptively match USB or small power adapter. During the charging process, if the input power source is unable to provide the charging current set by R_{SNS}, the VBUS voltage will decrease. Once the VBUS drops below 4.55V(typ.), the K-DPM™ loop begins to reduce charge current, preventing any further drop of VBUS, and finally balance will be achieved between them. The K-DPM™ gives the IC ability to charge battery with different adapters.

Battery Protection

Safety Voltage and Safety Current Limit

The REG06H register is a safe output voltage and output current configuration register that needs to be set up first after power-up to prevent damage to the battery caused by excessive charger output voltage or output current. To prevent the I²C from tampering with the security register settings, the security register is locked once the other registers are read or written. Only hard reset (internal POR reset --- power-on reset) can reset the safety register.

Battery OVP

Overvoltage protection is integrated in the chip to protect the device against damage if the voltage at CSOUT pin goes too high. The IC will turn off the PWM converter if an overvoltage condition is detected, when the voltage of CSOUT is higher than V_{OVP_BAT} which is equal to 117.6%*V_{OREG}, and STAT pin would generate a 128μs pulse and then behave as a high impedance (open-drain). Once V_{CSOUT} is lower than the battery overvoltage exit threshold, charge process resumes.

Battery Short Protection

During the normal charging process, when the battery voltage drops to the short-circuit threshold, V_{SHORT}(2.1V typical), the charger operates in linear charge mode with a lower charge current of I_{PRE_CHG}.

Battery Detection

Once the termination bit (TE) is set 1, AW32207 can detect if the battery is absence or not for applications with removable battery packs. During normal charge process, when the voltage at the CSOUT pin is above the battery recharge threshold, V_{OREG} - V_{RCH}, and the CTA is meet, the IC turns off the PWM charge and enables a discharge current I_{DBAT} (-0.5mA, typ.) for a period of T_{DBAT}, (262 ms typ.). If the battery voltage is still above the recharge threshold after T_{DBAT}, the battery is present. On the other hand, the battery is absent and the IC:

• Sets the register to their default values.

• Sets the FAULT bits (REG00H[2:0]) to 111.

• Restarts charge process with default values after t_{INT} (2s typ.).

Thermal Regulation and Protection

To avoid overheating of the chip at the charge process, the IC detects the junction temperature (T_J) of the die. When T_J reaches the thermal regulation threshold T_{CF}(140°C), I_{CHG} configuration code would reduce to "0000"(REG04H[6:3]=0000) gradually. In any state, if T_J exceeds T_{OTP}(160°C), the IC suspends charging. And charging resumes when T_J falls below T_{OTP} by approximately 30°C.

Charge Termination Algorithm(CTA)

To end the charging process reasonably, the IC applies the unique Charge Termination Algorithm(CTA), which could adjust the termination strategies by I²C interface flexibly. If the termination is enabled, once the charge current is below the termination charge current threshold (I_{TERM}), the termination detecting window timer will be enabled. During the termination window, if the time of I_{CHG}<I_{TERM} is longer than configured valid I_{TERM} deglitch time, the IC turns off the PWM charge and enables a discharge current (I_{DBAT}) for a period of T_{DBAT}, then checks the battery voltage. If the battery voltage is still above the recharge threshold after T_{DBAT}, the battery charging is complete. The termination current level, the detecting window periods, the valid I_{TERM} periods and the deglitch time of each period can be programmed by the Recharge/Charge Termination Algorithm Configure Register (REG07H).

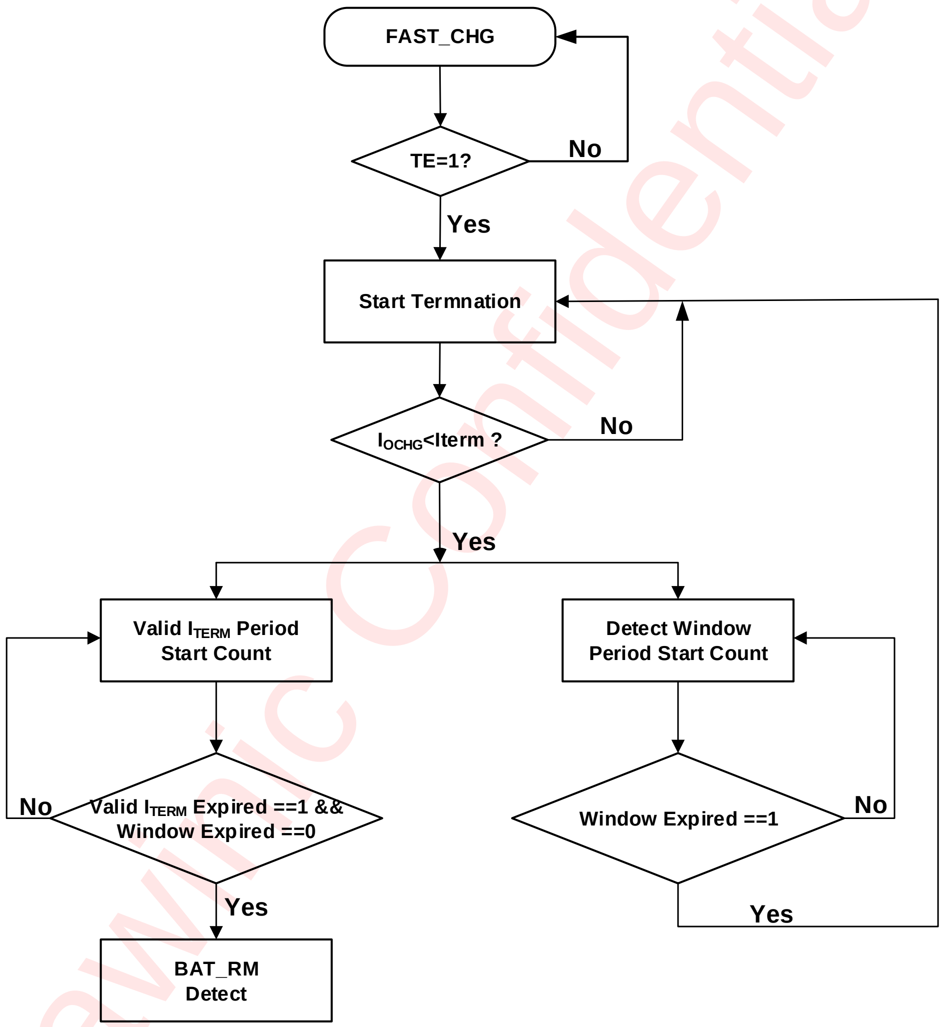


Figure 31 Charge Termination Algorithm Scheme Flow Chart

STAT Pin Output

The STAT pin is used to indicate operation conditions of the IC and provides a fault indicator for interrupt systems. The status of STAT pin at different operation conditions is summarized in Table 3.

Table 3 STAT Pin Summary

EN_STAT (REG00H[6])	CHARGE STATE	STAT
1	Charge in progress and EN_STAT=1	Low
X	Other normal conditions	Open-drain
X	Charge mode faults: Sleep mode, VBUS or battery overvoltage, poor input source, VBUS UVLO, no battery, thermal shutdown	128μs pulse, then open-drain
X	Boost mode faults: Over load, VBUS overvoltage, low battery voltage, thermal shutdown	128μs pulse, then open-drain
0	X	Open-drain

Charge Mode Control Bits/Pin

CEN Bit

The CEN bit(REG01H[2]) in the control register is used to disable or enable the charge process. Writing “0” to this bit enables the charge and writing “1” to this bit disables the charge.

RESET Bit

The RESET bit(REG04H[7]) in the control register resets all the charge parameters. Writing ‘1” to the RESET bit will reset all the charge parameters to default values except the safety limit register, and it is not recommended to set the RESET bit when the IC operates in charging or boosting process. Once writing ‘1” to the RESET bit via I^2C, it needs to wait 32ms at least before next I^2C command can be accepted.

OPA_Mode Bit

The OPA_MODE bit(REG01H[0]) is the operation mode control bit. When OPA_MODE=1 and HZ_MODE=0, the IC operates in boost mode. Other conditions can be referred in Table 3 for details.

CD Pin (Charge Disable)

The CD pin controls the charging process. When the CD pin is low, fast charge is enabled. When the CD pin is high, fast charge is disabled.

Table 4 Operation Mode Summary

CD	OPA_MODE	HZ_MODE	OPERATION MODE
0	0	0	Charge mode (VBUS > UVLO); High impedance (VBUS < UVLO)
1	0	X	High impedance mode
X	1	0	Boost(No faults); Any fault go to charge configure mode
X	X	1	High impedance mode

BOOST Mode Operation

When the IC operates in boost mode, it delivers the power to VBUS pin from the battery and boosts the battery voltage to V_{BUS_B} (about 5.05V). Boost mode can be configured as showed as Table 4 and Table 5.

PWM Controller in Boost Mode

Similar to charge mode operation, the IC integrates an 1.5 MHz frequency peak current mode controller to regulate output voltage at VBUS pin (V_{BUS_B}) in boost mode. The feedback loop is internally compensated for a wide load range and battery voltage range.

Boost Start Up

When the boost is enabled, if V_{BAT}>V_{UVLO_B}, the regulator first attempts to bring V_{PMID} within 300mV of V_{BAT} using an internal 150mA current source from VBAT (linear startup). If the voltage of PMID pin has reached V_{CSOUT}-300mV within 3ms, the IC enters the boost soft-startup operation process. If V_{PMID} has not achieved V_{CSOUT}-300mV after 3ms, a FAULT state is indicated. And the process of boost startup is showed as below:

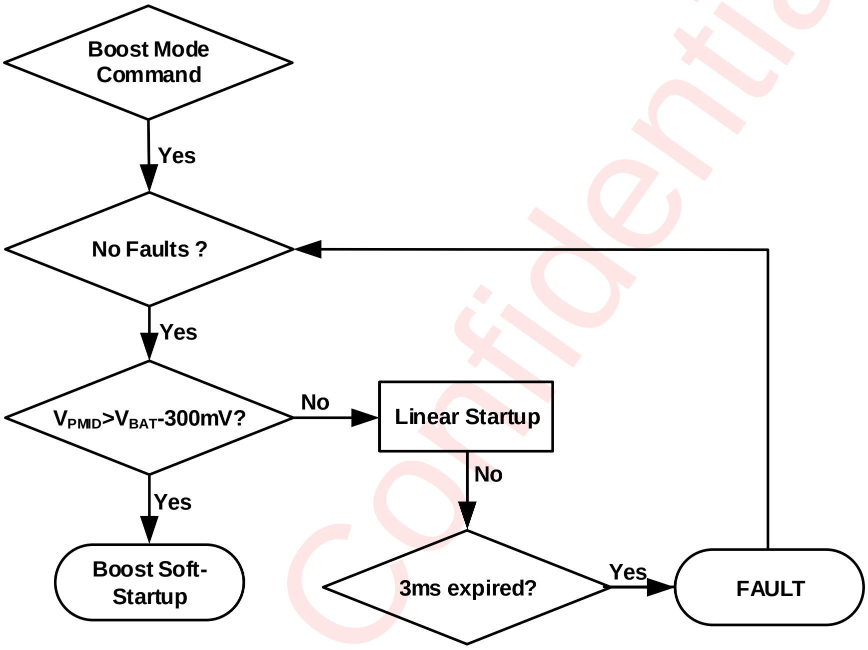


Figure 32 Boost Mode Start Scheme Flow Chart

Burst Mode at Light Load

In boost mode, under light load conditions, the IC operates in burst mode to reduce the power loss and improve the converter's efficiency. During boosting, the PWM converter is turned off once the inductor current is less than I_{BURST_IN}; and the PWM is turned back on when the voltage at PMID pin drops to about 101% of the rated output voltage. If the inductor current is continuously reduced, the IC will operate in Power Save Mode(PS Mode) when the inductor current is less than I_{PS_IN}. A pre-set circuit is used to make the smooth transition between PWM, Burst and PS mode.

Force PWM at Light Load

To reduce the ripple voltage under light load, AW32207 integrates Force PWM mode in boost mode, which could effectively decrease the output ripple voltage in VBUS pin. And this function can be enabled or disabled by register REG0AH[3] (default value is disabled).

Protection in Boost Mode

If a boost fault occurs:

• The STAT pin pulses. During normal boosting operation, the STAT pin behaves as a high impedance (open-drain) output. Under fault conditions, a 128μs pulse is sent out to notify the host.

• OPA_MODE bit is reset. If the IC operates in boost mode with OPA_MODE=1(not in force OTG mode), it will enter charge mode because the OPA_MODE is reset to 0.

• The fault bits (REG09H[2:0]) are set to indicate the fault type as register table.

Output Overvoltage Protection

The IC provides a built-in overvoltage protection to protect the device and other components against damage if the voltage (Voltage from VBUS to GND) is too high in boost mode-- exceeding 6.0V typical.

Output Overload Protection

The IC provides a built-in over-load protection to avoid the device damage when VBUS is over loaded. Once VBUS fails to achieve the voltage required to advance to the next stage during soft-start or sustained (>20µs) current limit during boost mode, the IC will enter overload protection mode.

Thermal Protection

To prevent overheating of the chip during the boost mode, the IC monitors the junction temperature (T_J) of the die. If T_J exceeds T_{OTP}(160°C), the IC suspends boosting, and the thermal hysteresis is about 30°C.

Battery UVLO Protection

During boosting, when the battery voltage is below the battery under voltage threshold (V_{UVLO_B}), the IC turns off the PWM converter.

Restart After Boost Faults

If boost is enabled with the OPA_MODE bit, boost mode can only be restarted through subsequent I^2C commands since OPA_MODE is reset on boost faults. When OTG_PL=1/0, the OTG pin ACTIVE state is 1/0. If OTG_EN=1 and OTG pin is still ACTIVE, the boost restarts after all faults are cleared. All the methods that can enable OTG mode are showed as Table 5.

Table 5 Enabling Boost

OTG_EN	OTG_PIN	HZ_MODE	OPA_MODE	BOOST
0	X	0	1	Enable
1	ACTIVE	X	X	Enable
1	INACTIVE	0	1	Enable

High Impedance (HZ) Mode

In this mode, the charger stops charging and enters a low quiescent current state to conserve power. The charger enters HZ mode if

• The voltage on CD pin is logic high;

• The HZ-MODE control bit is set to “1” and OTG pin is not in active status;

• V_{BUS} > V_{UVLO} and a battery with V_{BAT} > V_{LOWV} is inserted after POR;

• VBUS falls below UVLO.

In order to exit HZ mode, the CD pin must be low, VBUS must be higher than UVLO and the HOST must write a "0" to the HZ-MODE control bit.

General I²C Operation

The AW32207 is compatible with I²C interface. The SCL line is an input and the SDA line is a bi-directional open-drain output.

Device Address

AW32207 7-bit slave address (A7~A1) is 1101010 binary(0x6AH). After the START condition, the I²C master sends the 7-bit chip address followed by an eighth (A0) read or write bit (R/W). R/W= 0 indicates a WRITE function and R/W = 1 indicates a READ function.

Table 6 Device Address

A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	1	0	R/W

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

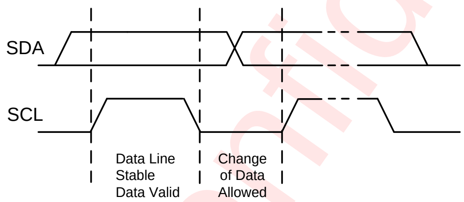


Figure 33 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

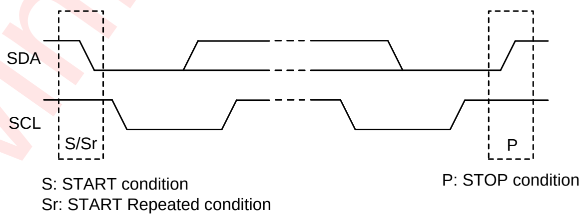


Figure 34 Start and Stop Conditions

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

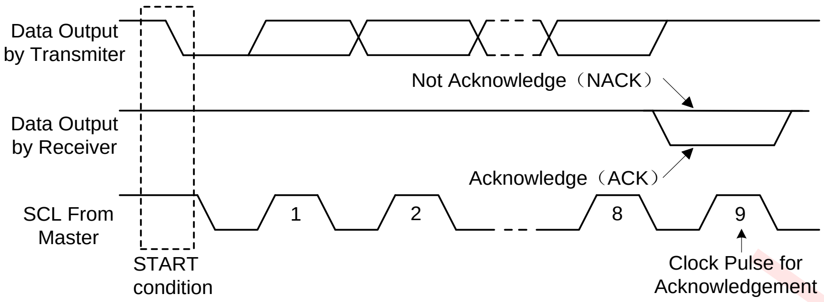


Figure 35 Acknowledgement Diagram

Write Process

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat steps f and g)

i) Master generates STOP condition to indicate write cycle end

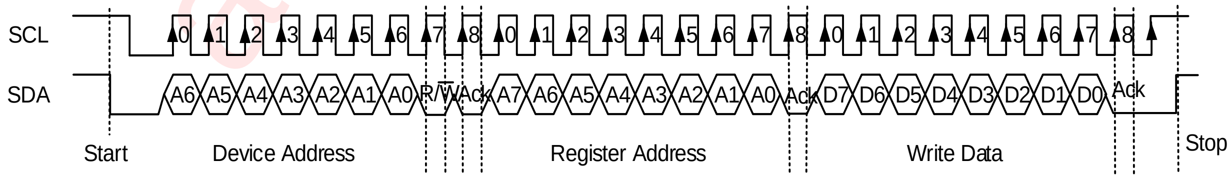


Figure 36 I²C Write Timing

Read Process

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

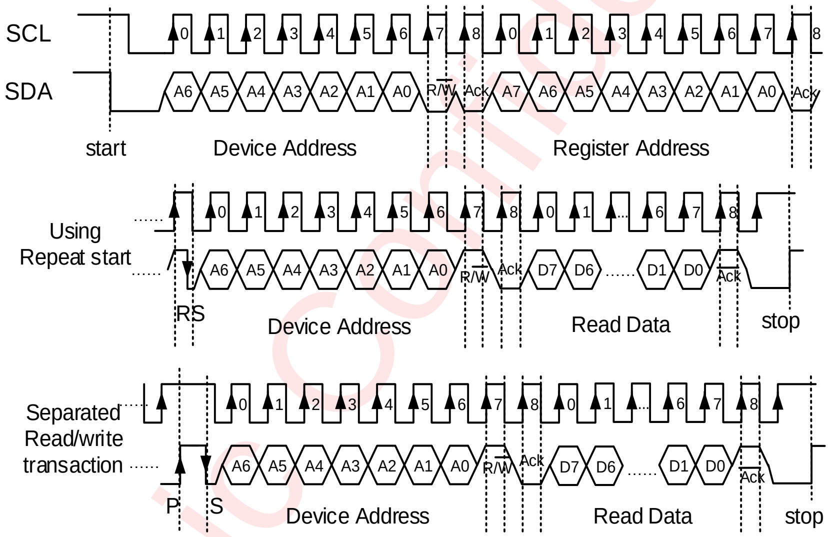


Figure 37 I²C Read Timing

Register List

Status/Control Register

Address: 00H, Reset State: x1xx 0xxx.

BIT Name	W/R	BIT	Function
OTG	R	B7	Read: OTG pin status, 0-OTG pin at Low level; 1-OTG pin at High level
EN_STAT	W/R	B6	0-Disable STAT pin function; 1-Enable STAT pin function (**default**)
STAT	R	B5-B4	HEX State HEX State 00 Ready; 02 Charge done; 01 Charge in progress; 03 Fault
BOOST	R	B3	1-Boost mode; 0-Not in boost mode (**default**)
CHG_FAULT	R	B2-B0	Charge mode: HEX State HEX State 00 Normal; 04 Output OVP; 01 VBUS OVP; 05 Thermal shutdown; 02 Sleep mode; 06 NA; 03 Bad Adaptor or $V_{BUS}<V_{UVLO}$; 07 No battery.

Control Register

Address: 01H, Reset State:0011 0000.

BIT Name	W/R	BIT	Function
NA	NA	B7-B6	NA
NA	NA	B5-B4	NA
TE	W/R	B3	1-Enable charge current termination; 0-Disable charge current termination (**default**)
CEN	W/R	B2	1-Charger is disabled; 0-Charger is enabled (**default**)
HZ_MODE	W/R	B1	1-High impedance mode; 0-Not high impedance mode (**default**)
OPA_MODE	W/R	B0	1-Boost mode; 0-Charger mode (**default**)

Control/Battery Voltage Register

Address: 02H, Reset State:0000 1010

BIT Name	W/R	BIT	Function
VOREG	W/R	B7-B2	Battery voltage charging control: HEX VOREG HEX VOREG HEX VOREG HEX VOREG 00H 3.50V 0FH 3.80V 1EH 4.10V 2DH 4.40V 01H 3.52V 10H 3.82V 1FH 4.12V 2EH 4.42V **02H 3.54V(default)** 11H 3.84V 20H 4.14V 2FH 4.44V 03H 3.56V 12H 3.86V 21H 4.16V 30H 4.46V 04H 3.58V 13H 3.88V 22H 4.18V 31H 4.48V 05H 3.60V 14H 3.90V 23H 4.20V 32H 4.50V 06H 3.62V 15H 3.92V 24H 4.22V 33H-3FH 4.50V 07H 3.64V 16H 3.94V 25H 4.24V 08H 3.66V 17H 3.96V 26H 4.26V 09H 3.68V 18H 3.98V 27H 4.28V 0AH 3.70V 19H 4.00V 28H 4.30V 0BH 3.72V 1AH 4.02V 29H 4.32V 0CH 3.74V 1BH 4.04V 2AH 4.34V 0DH 3.76V 1CH 4.06V 2BH 4.36V 0EH 3.78V 1DH 4.08V 2CH 4.38V
OTG_PL	W/R	B1	1-OTG Boost Enable with High level **(default)**; 0-OTG Boost Enable with Low level; not applicable to OTG pin control of current limit at POR in default mode.
OTG_EN	W/R	B0	Enable OTG Pin in HOST mode; 0-Disable OTG pin in HOST mode **(default)**, not applicable to OTG pin control of current limit at POR in default mode.

Vender/Part/Revision Register

Address: 03H, Reset State:0100 0011.

BIT Name	W/R	BIT	Function
Vender	R	B7-B5	Vender code:010
PN	R	B4-B3	6AH:00-AW32207
Revision	R	B2-B0	011: Revision 1.0 **(default)**; 001: Revision 1.1; 100-111: Future Revisions

Battery Termination/Fast Charge Current Register

Address: 04H, Reset State:0000 0001.

BIT Name	W/R	BIT	Function
RESET	W/R	B7	Write: 1-Charger in reset mode; 0-No effect, Read: always get "0", After the software reset command is input through I^2C, it needs to wait at least 32ms before any other I^2C command can be accepted.
ICHG	W/R	B6-B3	HEX I_{CHG}(mA)(68mΩ) I_{CHG} (mA)(56mΩ) I_{CHG} (mA)(51mΩ) 00 400 **485(default)** 533 01 500 607 666 02 700 850 933 03 800 971 1066 04 900 1092 1200 05 1000 1214 1333 06 1100 1336 1466 07 1200 1457 1600 08 1300 1578 1733 09 1400 1699 1866 0A 1500 1821 2000 0B 1500 1821 2000 0C 1500 1821 2000 0D 1500 1821 2000 0E 1500 1821 2000 0F 1500 1821 2000
ITERM_CFG	W/R	B2-B0	HEX ITERM(mA)68mΩ ITERM(mA)56mΩ ITERM(mA)51mΩ 00 50 60 66 01 100 **121(default)** 133 02 150 181 200 03 200 242 266 04 250 303 333 05 300 364 400 06 350 425 466 07 400 485 533

Special Charger Voltage/Enable Pin Status Register

Address: 05H, Reset State:0010 0100.

BIT Name	W/R	BIT	Function
NA	NA	B7-B5	NA
DPM_STATUS	R	B4	0 – DPM mode is not active (**default**) 1 – DPM mode is active
CD_STATUS	R	B3	0 – CD pin at LOW level (**default**) 1 – CD pin at HIGH level
VSP	W/R	B2-B0	VBUS DPM regulation voltage： HEX VSP(V) HEX VSP(V) 00 4.250 01 4.325

			02 4.400 03 4.475 **04** **4.550(default)** 05 4.625 06 4.700 07 4.775

Safety Limit Register

Address: 06H, Reset State:0100 0000.

BIT Name	W/R	BIT	Function
ISAFE	W/R	B7-B4	Maximum charge current: HEX I_{CHG_MAX}(mA)(68mΩ) I_{CHG_MAX}(mA)(56mΩ) I_{CHG_MAX}(mA)(51mΩ) 00 400 485 533 01 500 607 666 02 700 850 933 03 800 971 1066 04 900 **1092(default)** 1200 05 1000 1214 1333 06 1100 1336 1466 07 1200 1457 1600 08 1300 1578 1733 09 1400 1699 1866 0A 1500 1821 2000 0B 1500 1821 2000 0C 1500 1821 2000 0D 1500 1821 2000 0E 1500 1821 2000 0F 1500 1821 2000
VSAFE	W/R	B3-B0	Maximum charge voltage: HEX V_{OREG_MAX}(V) HEX V_{OREG_MAX}(V) **00** **4.20(default)** 08 4.36 01 4.22 09 4.38 02 4.24 0A 4.40 03 4.26 0B 4.42 04 4.28 0C 4.44 05 4.30 0D 4.46 06 4.32 0E 4.48 07 4.34 0F 4.50

Recharge/Charge Termination Algorithm Configure Register

Address: 07H, Reset State:0001 0001.

BIT Name	W/R	BIT	Function
TE_P	W/R	B7	0-The algorithm counting 8 period (**default**); 1- The algorithm counting 16 period
TE_NUM	W/R	B6-B5	The number of period which ICHG<ITERM during counting period: 00-1(**default**); 01-2; 10-4; 11-8
TE_DEG_TM	W/R	B4-B3	Deglitch time of each period: HEX Deglitch time (ms) HEX Deglitch time (ms) 00 8 02 32 01 16(**default**) 03 64
NA	NA	B2	NA
VRCH	W/R	B1-B0	Recharge threshold is V_{OREG}-V_{RCH}, HEX V_{RCH} (mV) HEX V_{RCH} (mV) 00 50 02 150 01 100(**default**) 03 200

AWINIC Vendor Register

Address: 08H, Reset State:1111 1111.

BIT Name	W/R	BIT	Function
VENDOR	R	B7-B0	AWINIC Vendor Number

Boost Faults State Register

Address: 09H, Reset State:0000 0000.

BIT Name	W/R	BIT	Function
NA	NA	B7-B3	NA
BST_FAULT	R	B2-B0	Boost mode: 000-Normal **(default)**; 001-VBUS OVP; 010-Over load; 011-Battery voltage is too low; 100-NA; 101-Thermal shutdown; 110-NA; 111-NA

Boost Output/Control Driver Configure Register

Address: 0AH, Reset State:0000 0000.

BIT Name	W/R	BIT	Function
PWM_FRQ	W/R	B7	PWM frequency shift enable: 0-1.5MHz buck/boost operation **(default)**; 1-1.7MHz buck/boost operation
SLOW_SW	W/R	B6-B5	Reduce slew rate of power train driver HEX slew rate HEX slew rate 00 default driver **(default)** 02 slower driver 01 slow driver 03 slowest driver
FIX_DEADT	W/R	B4	0: Multiple stage power train driver **(default)**; 1: Fix dead-time power train driver
FPWM	W/R	B3	1: Force PWM modulation in boost mode; 0: Disable force PWM modulation **(default)**
NA	NA	B2	NA
BSTOUT_CFG	W/R	B1-B0	OTG output configure voltage HEX BSTOUT (V) HEX BSTOUT (V) 00 5.05**(default)** 02 5.25 01 5.15 03 5.35

Application Information

INDUCTOR SELECTION GUIDELINE

The selection of inductance depends mainly on the inductor current ripple size requirement. Here is an example to illustrate the computational process of inductance selection.

Refer to the equation of BUCK inductor ripple current,

$$\Delta I_L = \frac{VBAT \bullet (VBUS - VBAT)}{VBUS \bullet f_{sw} \bullet L}$$

the worst case is when battery voltage is equal to half of the input voltage, so the worst case occurs at VBUS= 5.0V, VBAT=2.5V. If the ripple current peak-to-peak is expected to below 800mA, we have

$$L = \frac{VBAT \bullet (VBUS - VBAT)}{VBUS \bullet f_{SW} \bullet \Delta I_L}$$
$$= \frac{2.5 \bullet (5.0 - 2.5)}{5.0 \times (1.5 \times 10^6) \times 0.8}$$
$$= 1.04(\mu H)$$

Select 2.5mm×2.0mm 1.0μH, surface mount multi-layer inductor.

CAPACITORS SELECTION

VBUS INPUT CAPACITOR C_{BUS1}

AW32207 advises to use a 1μF ceramic capacitor at VBUS pin as shown in Figure 4.

PMID OUTPUT CAPACITOR C_{PMID1}

AW32207 advises to use a 4.7μF ceramic capacitor at PMID pin as shown in Figure 4, to reduce the voltage ripple of PMID Pin, a ceramic capacitor with the capacitance between 2.2μF and 22μF is acceptable.

BAT OUTPUT CAPACITOR C_{BAT}

The IC provides internal loop compensation. With the internal loop compensation, the recommended value for C_{OUT} is 22μF in Figure 4, to reduce the output voltage ripple, a ceramic capacitor with the capacitance between 20μF and 100μF is acceptable. The C_{SIN} and C_{SOUT} Pin should bypass with 0.1μF ceramic capacitor to PGND.

R_{SNS} SELECTION

R_{SNS} selection mainly depends on its resistance and power rating. For example, choose a 56mΩ resistor, setting the constant current to 1.82A. The power dissipation across the resistor can be calculated according to $P=I^2R$, which is 0.185W, that means you must select the resistor whose rated power is greater than 0.185W. AW32207's fast charge current and termination current can be set via R_{SNS} as following equation:

$$I_{CHG} = \frac{\Delta V_{RSNS}}{R_{SNS}} = \frac{V_{CSIN} - V_{CSOUT}}{R_{SNS}}$$
$$\approx \frac{54.4mV \times I_{CHG}[6] + 27.2mV \times I_{CHG}[5] + 13.6mV \times I_{CHG}[4] + 6.8mV \times (I_{CHG}[3] + 3 + A)}{R_{SNS}}$$

When ICHG[6:3]>01H, A=1, otherwise, A=0.

$$I_{TERM} = \frac{\Delta V_{RSNS}}{R_{SNS}} = \frac{V_{CSIN} - V_{CSOUT}}{R_{SNS}}$$
$$\approx \frac{13.6mV \times I_{TERM\_CFG}[2] + 6.8mV \times I_{TERM\_CFG}[1] + 3.4mV \times (I_{TERM\_CFG}[0] + 1)}{R_{SNS}}$$

The Key BOM of Figure 4

Qty	Ref	Value	Description	Package	Manufacture
1	C_{BUS1}	1μF	Ceramic Capacitor; 25V	0603	Any
1	C_{BUS2}	Optional	Ceramic Capacitor; 25V	0603	Any
1	C_{PMID1}	4.7μF	Ceramic Capacitor; 16V	0603	Any
1	C_{PMID2}	Optional	Ceramic Capacitor; 16V	0603	Any
1	L_1	1μH	Inductor	2520	Any
1	R_{SNS}	56mΩ	Sense Resistor	0805	Any
1	C_{SIN}	0.1μF	Ceramic Capacitor; 16V	0603	Any
1	C_{SOUT}	0.1μF	Ceramic Capacitor; 16V	0603	Any
1	C_{BAT}	22μF	Ceramic Capacitor; 16V	0603	Any

PCB LAYOUT CONSIDERATION

AW32207 is a switch charger chip, to obtain the optimal performance, it is important to pay special attention to the PCB layout. The following provides some guidelines:

• Place 4.7μF input capacitor as close as possible to the PMID pin and the PGND pin to make high frequency current loop area as small as possible. Place 1μF input capacitor as close as possible to the VBUS pin and the PGND pin to make high frequency current loop area as small as possible.

• The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The PGND pins should be connected to the ground plane to return current through the internal low-side FET. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high frequency oscillation problems, proper layout to minimize high frequency current path loop is critical. **The power path shown in red as the Figure 4 must be widen. Please trace according to 2A rule.**

• The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the R_{SNS} back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path).

• Place all decoupling capacitors close to their respective IC pins and close to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.

• The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small signal components). A star ground design approach is typically used to keep circuit block currents isolated(high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.

• A surge voltage would arise when charger is hot-plugged into a USB interface. The over-shoot may damage the VBUS capacitor or chip. To avoid this risk, a TVS tube is recommended to add to the USB power output port.

• There will be strong switch-signal on the inductor while the charger is operating, to avoid interference, place the IC far from FM, RF and PA models.

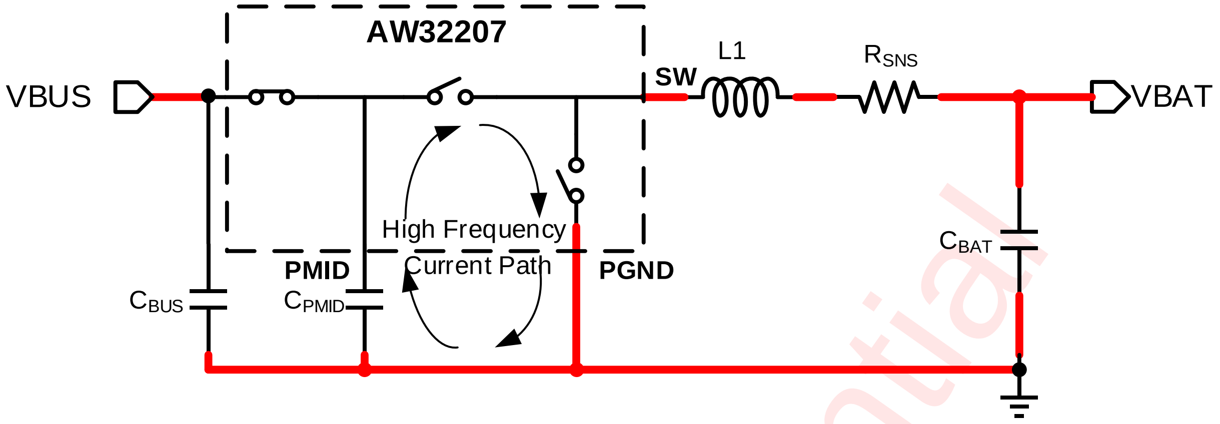


Figure 38 High Frequency Current Path

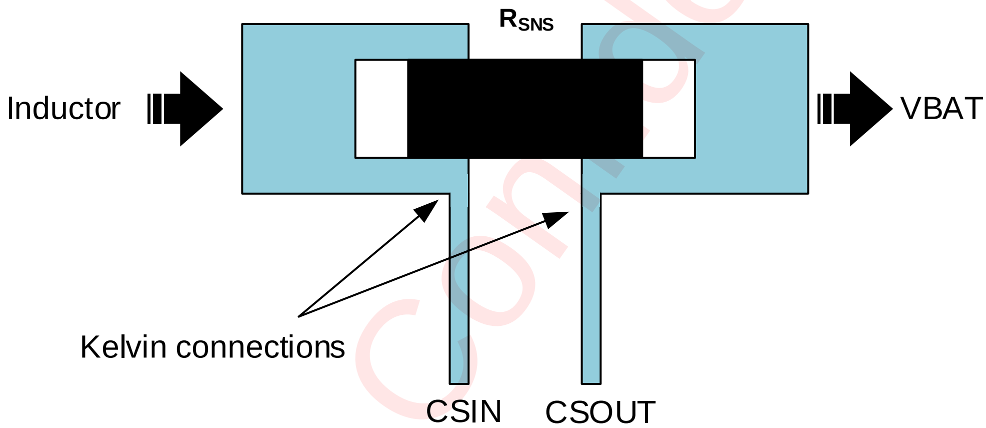


Figure 39 Sense Resistor PCB Layout

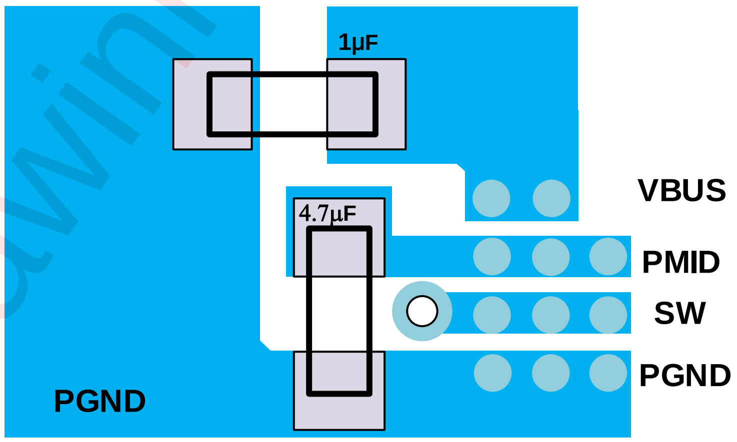
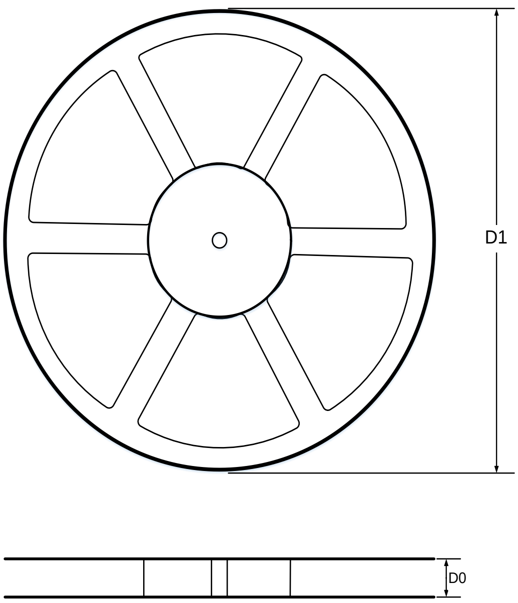


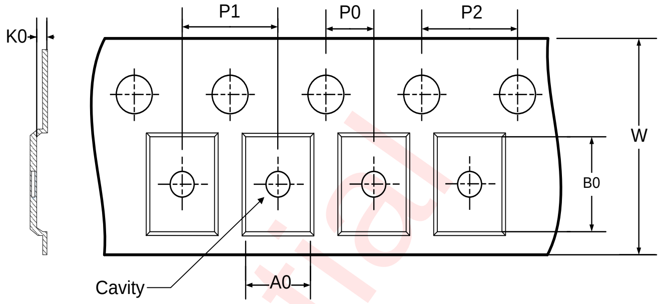
Figure 40 Sense Resistor PCB Layout

Tape and Reel Information

REEL DIMENSIONS

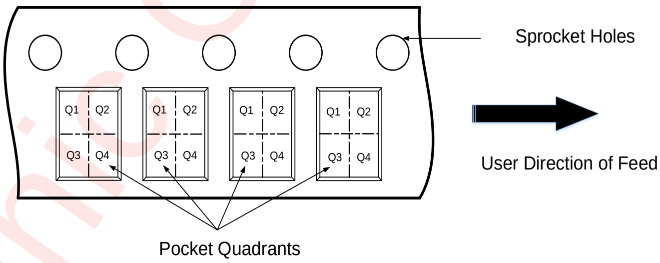


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

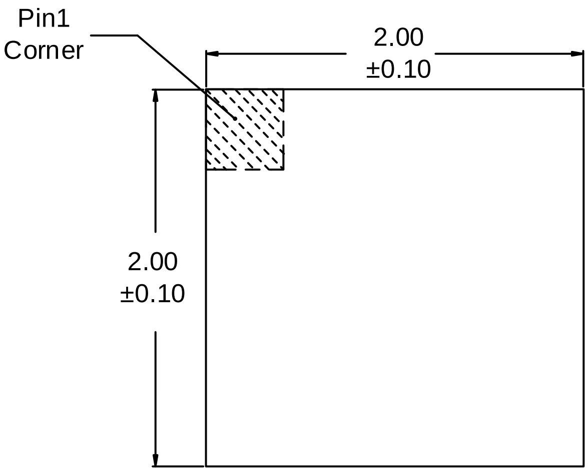
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



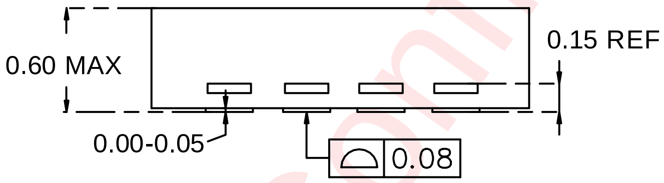
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.25	2.25	0.75	2	4	4	8	Q1

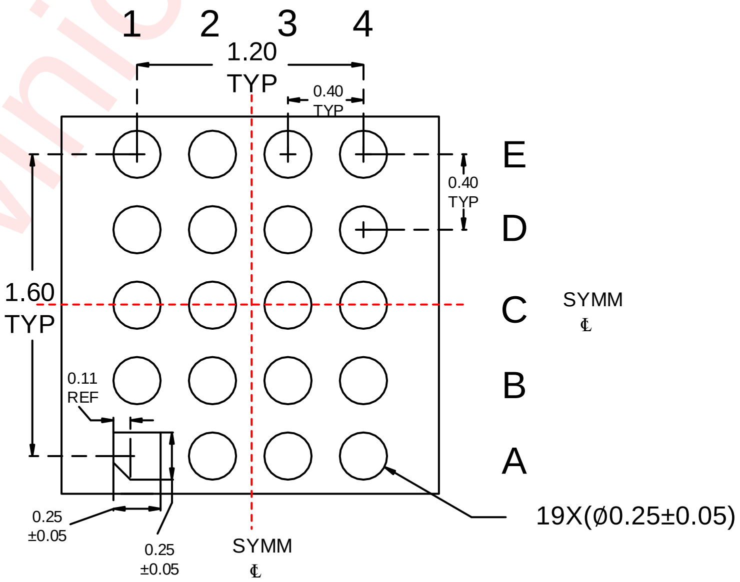
Package Description(POD)



Top View



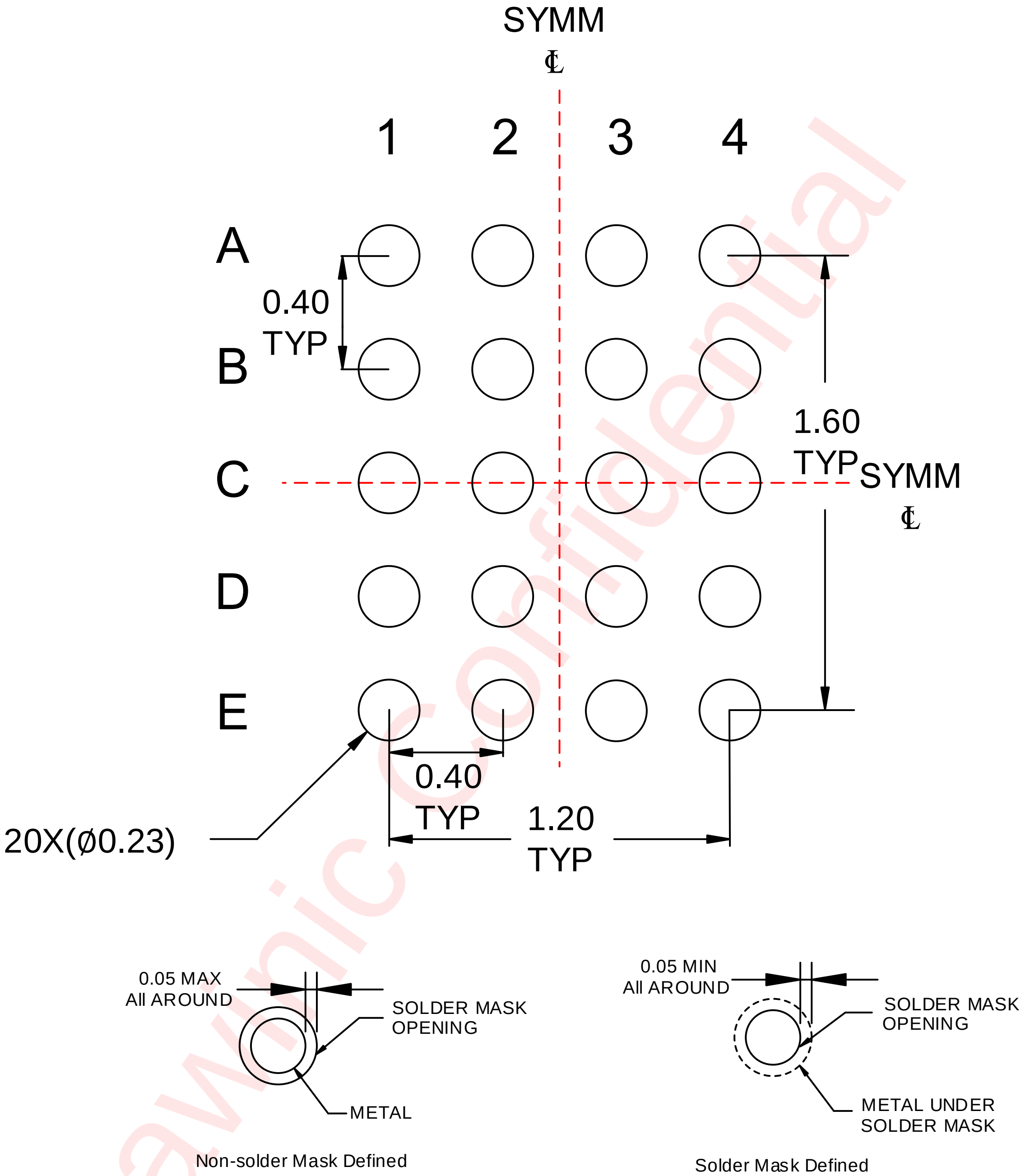
Side View



Bottom View

Unit: mm

Land Pattern Data



Unit: mm

Revision History

Vision	Date	Change Record
V1.0	Oct. 2018	Official Released
V1.1	Oct. 2018	Update the EC Table
V1.2	Nov. 2018	Update the application circuit
V1.3	Mar. 2019	Update the function description
V1.4	Sept. 2019	Update the function description
V1.5	May. 2020	Update the EC Table, the function description and some syntax errors
V1.6	Oct. 2021	1. Changed the REG04H[7] RESET function description "it needs to wait at least 2ms" to "it needs to wait at least 32ms"; 2.Added "*Safety Voltage and Safety Current Limit*"; 3.Updated "R_{SNS} SELECTION" description; 4.Refreshed some parameters in EC table; 5.Fixed the Figure 28 error. 6.Update the Package Description(POD) and Land Pattern Data.

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