Over-Voltage Protection Load Switch

FEATURES

- Highly reliable1.2mm × 1.2mm FCQFN-9 package
- Integrated low R_{dson} nFET switch: typical 30mΩ
- 5A continuous current capability
- Default Over-Voltage Protection (OVP) threshold
  - AW33901: 5.95V
  - AW33902: 6.2V
  - AW33905: 6.8V
  - AW33909: 9.98V
  - AW33910: 10.5V
- OVP threshold adjustable range: 4V to 20V
- Input maximum voltage rating: $32V_{DC}$
- Fast turn-off response: typical 50ns
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)

APPLICATIONS

- Smartphones
- Tablets
- Charging Ports

GENERAL DESCRIPTION

The AW339XX features an ultra-low 30mΩ (typ.) R_{dson} nFET load switch. When input voltage exceeds the OVP threshold, the switch is turned off very fast to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to $32V_{DC}$.

The default OVP threshold is 5.95V (AW33901), 6.2V (AW33902), 6.8V (AW33905), 9.98V (AW33909) and 10.5V (AW33910). The OVP threshold can be adjusted from 4V to 20V through external OVLO pin.

The device features an open-drain output $\overline{ACOK}$, when $V_{IN\_UVLO}<V_{IN}<V_{IN\_OVLO}$ and the switch is on, $\overline{ACOK}$ will be driven low to indicate a good power input, otherwise it is in high impedance mode (HiZ).

The device features over-temperature protection that prevents itself from thermal damaging.

The AW339XX is available in a RoHS compliant 1.2mm × 1.2mm FCQFN-9 package.

TYPICAL APPLICATION CIRCUIT

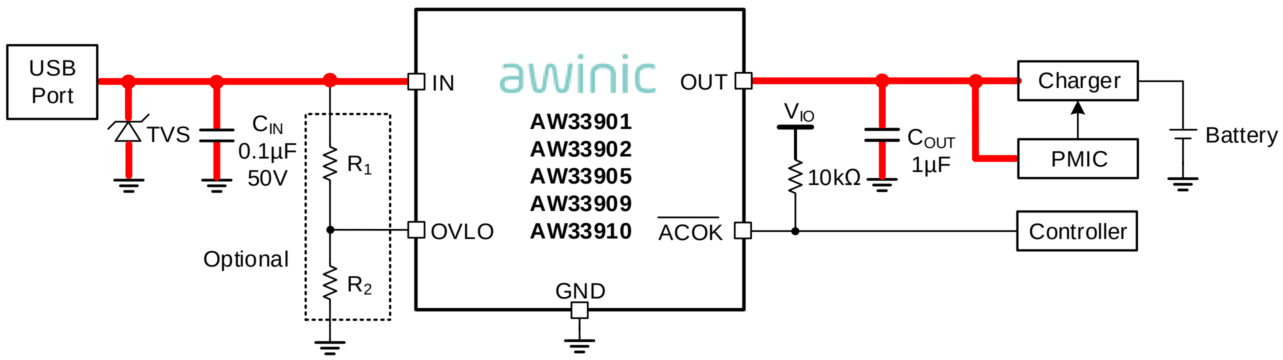


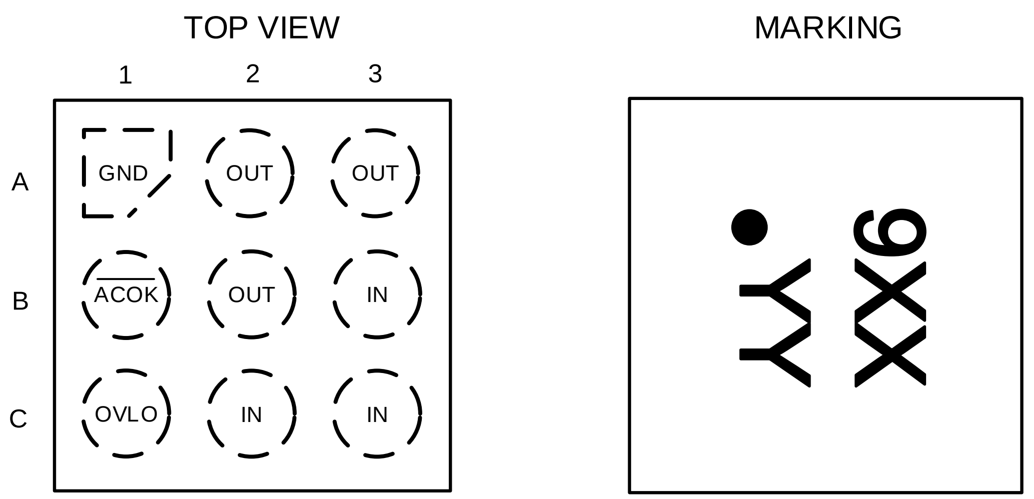
Figure 1 AW339XX typical application circuit

Note: when using default OVP threshold, R_1 and R_2 are not required, and connect OVLO pin to ground.

DEVICE COMPARISON TABLE

Device	V_{IN_OVLO}(V)				V_{IN_OVLO} Hysteresis(mV)
	Condition	Min.	Typ.	Max.	
AW33901	V_{IN} rising	5.83	5.95	6.07	130
AW33902	V_{IN} rising	6.08	6.20	6.32	130
AW33905	V_{IN} rising	6.66	6.80	6.94	140
AW33909	V_{IN} rising	9.78	9.98	10.18	210
AW33910	V_{IN} rising	10.29	10.50	10.71	210

PIN CONFIGURATION AND TOP MARK



9XX – AW33901/AW33902/AW33905/
AW33909/AW33910
YY – Production tracking code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

Pin	Name	Description
B3,C2,C3	IN	Switch input and device power supply
A1	GND	Device ground
C1	OVLO	OVP threshold adjustment pin
A2,A3,B2	OUT	Switch output
B1	$\overline{\text{ACOK}}$	Power good flag, active-low, open-drain

FUNCTIONAL BLOCK DIAGRAM

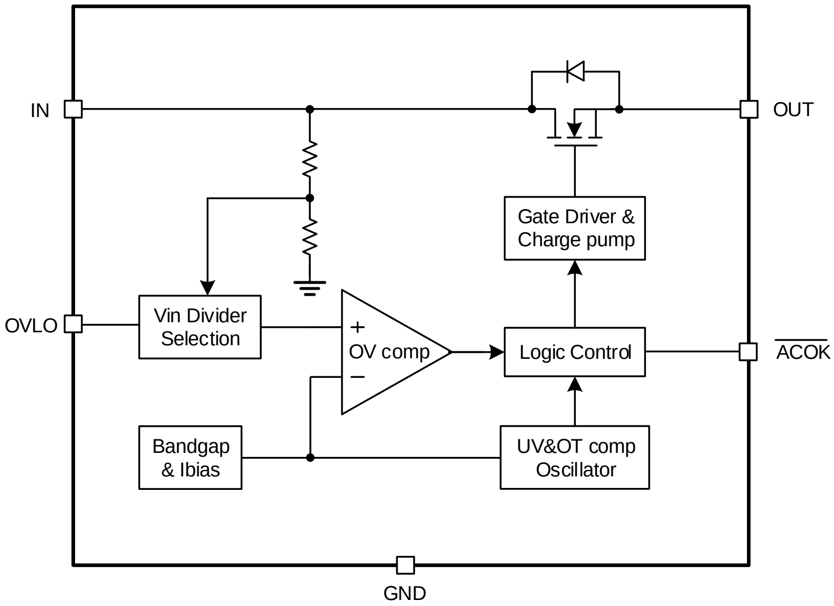


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

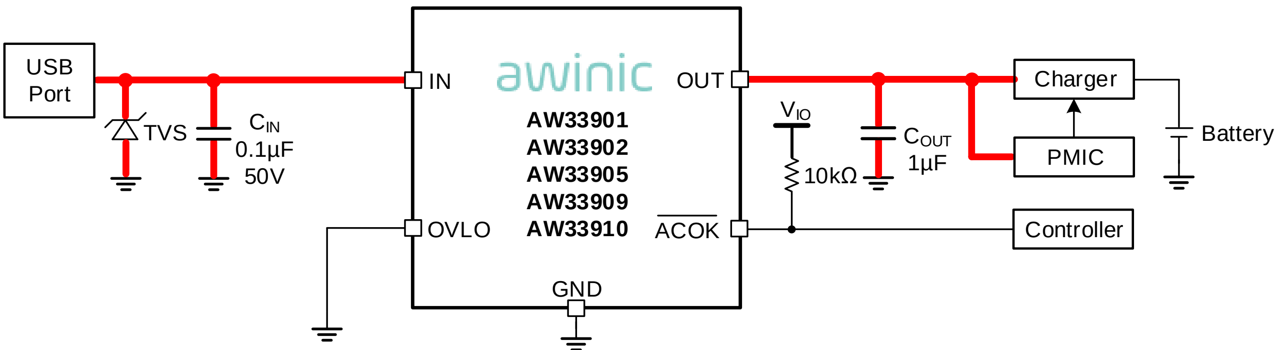


Figure 4 AW339XX typical application circuit(using default OVP threshold)

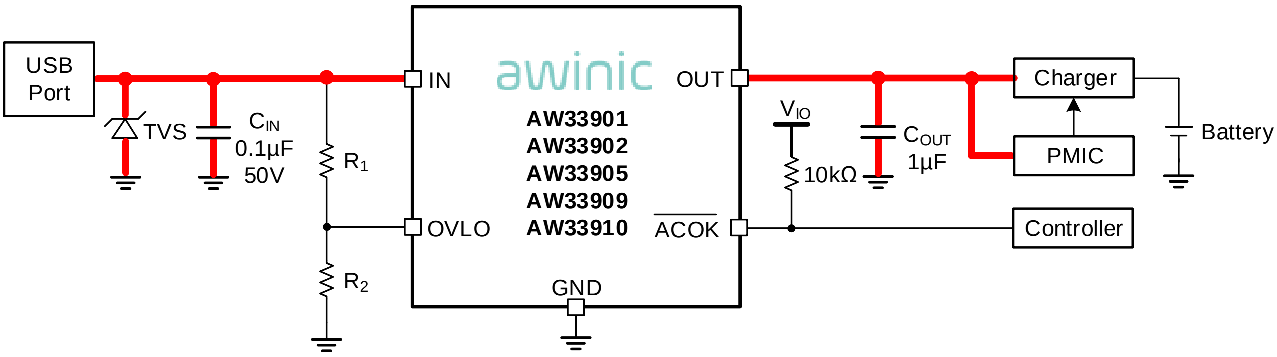


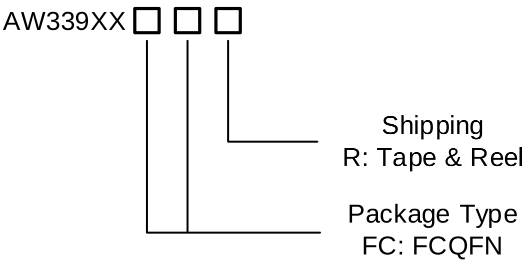
Figure 5 AW339XX typical application circuit(using external OVP threshold)

Notice for Typical Application Circuits:

1. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. OVLO pin cannot be left floating.
2. If R_1 and R_2 are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
3. C_{IN} = 0.1μF is recommended for typical application, larger C_{IN} is also acceptable. The rated voltage of C_{IN} should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW339XX is used, the rated voltage of C_{IN} should be 50V.
4. C_{OUT} = 1μF is recommended for typical application, larger C_{OUT} is also acceptable. The rated voltage of C_{OUT} should be larger than the OVP threshold. For example, if the OVP threshold is 6.8V, the rated voltage of C_{OUT} should be 10V or higher.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW33901FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	901	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33902FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	902	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33905FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	905	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33909FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	909	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33910FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	910	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel



ABSOLUTE MAXIMUM RATINGS(NOTE1)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IN}	Input DC voltage		-0.3	32	V
V_{IN_PUL}	Input peak pulse voltage	20μs pulse width, repeat 100 times		40	V
V_{OUT}	Output voltage		-0.3	See(NOTE 2)	V
$V_{\overline{ACOK}}$	$\overline{\text{ACOK}}$ voltage		-0.3	7	V
V_{OVLO}	OVLO voltage		-0.3	7	V
I_{SW}	Continuous current of switch IN-OUT(NOTE 3)	Continuous current on IN and OUT pin		5	A
I_{PEAK}	Peak current	Peak input and output current on IN and OUT pin(10ms)		8	A
I_{DIODE}	Continuous diode current	Continuous forward current through the nFET body diode		1.5	A
T_A	Ambient temperature		-40	85	°C
T_J	Junction temperature		-40	150	°C
T_{STG}	Storage temperature		-65	150	°C
T_{LEAD}	Soldering temperature	At leads, 10 seconds		260	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: 29V or V_{IN}+0.3V, whichever is smaller.

NOTE3: Limited by thermal design.

THERMAL INFORMATION

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Thermal resistance from junction to ambient (NOTE 1)	In free air	70	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

ESD AND LATCH-UP RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{ESD}	Human Body Model	All pins, per MIL-STD-883J Method 3015.9	±6.5	kV
	Charged Device Model	All pins, per ESDA/JEDEC JS-002-2014	±2	kV
	Machine Model	All pins, per JESD22-A115C	±450	V
$I_{Latch-up}$	Latch-up	All pins, per JESD78D, I Trigger	±800	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input DC voltage	3		30	V
C_{IN}	Input capacitance		0.1		μF
C_{OUT}	Output load capacitance		1	100	μF

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 0.1μF, I_{IN}≤ 5A and T_A = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
R_{dson}	Switch on resistance	V_{IN} = 5V, I_{OUT} = 1A, T_A = 25°C		30	41	mΩ
I_Q	Input quiescent current	V_{IN} = 5V, V_{OVLO}=0V,I_{OUT} = 0A		80	150	μA
I_{IN_OVLO}	Input current at over-voltage condition	V_{IN} = 5V, V_{OVLO}=3V,V_{OUT} = 0V		78	150	μA
V_{OVLO_TH}	OVLO set threshold		1.16	1.20	1.24	V
V_{OVLO_RNG}	OVP threshold adjustable range		4		20	V
V_{OVLO_SEL}	External OVLO select threshold	OVLO rising	0.19	0.26	0.33	V
		Hysteresis		0.06		V
I_{OVLO}	OVLO pin leakage current	V_{OVLO}=V_{OVLO_TH}	-0.2		0.2	μA
Protection						
V_{IN_OVLO}	OVP trip level	AW33901 V_{IN} rising	5.83	5.95	6.07	V
		AW33901 Hysteresis		0.13		
		AW33902 V_{IN} rising	6.08	6.20	6.32	
		AW33902 Hysteresis		0.13		
		AW33905 V_{IN} rising	6.66	6.80	6.94	
		AW33905 Hysteresis		0.14		
		AW33909 V_{IN} rising	9.78	9.98	10.18	
		AW33909 Hysteresis		0.21		
		AW33910 V_{IN} rising	10.29	10.50	10.71	
		AW33910 Hysteresis		0.21		
V_{IN_UVLO}	UVLO trip level	V_{IN} rising		2.9	3.0	V
		Hysteresis		0.1		

ELECTRICAL CHARACTERISTICS(CONTINUED)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 0.1μF, I_{IN}≤ 5A and T_A = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Protection(continued)						
T_{SDN}	Shutdown temperature			150		°C
T_{SDN_HYS}	Shutdown temperature hysteresis			20		°C
R_{DCHG}	Output discharge resistance	V_{OUT}=7V,V_{OVLO}=3V		50		Ω
Digital Logical Interface						
V_{OL}	$\overline{ACOK}$ output low voltage	I_{SINK}=1mA			0.4	V
$I_{LEAK\_\overline{ACOK}}$	$\overline{ACOK}$ leakage current	V_{IO}=5V, $\overline{ACOK}$ de-asserted	-0.5		0.5	μA
Timing Characteristics (Figure 6)						
t_{DEB}	Debounce time	From V_{IN} > V_{IN_UVLO} to 10% V_{OUT}		15		ms
t_{START}	Start-up time	From V_{IN} > V_{IN_UVLO} to $\overline{ACOK}$ low		30		ms
t_{ON}	Switch turn-on time	R_L = 100Ω, C_L = 22μF, V_{OUT} from 10% V_{IN} to 90% V_{IN}		2		ms
t_{OFF}	Switch turn-off time	C_L = 0μF, R_L = 100Ω, V_{IN} > V_{IN_OVLO} to V_{OUT} stop rising, V_{IN} rise at 10V/μs		50		ns

TIMING DIAGRAM

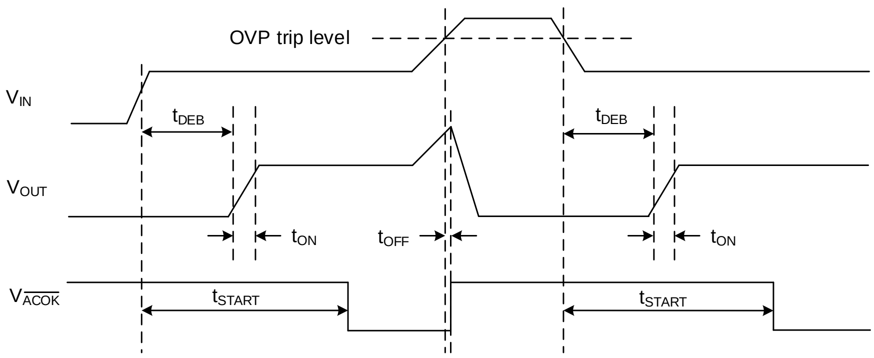


Figure 6 Timing diagram

TYPICAL CHARACTERISTICS

Table 1 Table of Figures

V_{IN} = 5V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25°C unless otherwise specified.

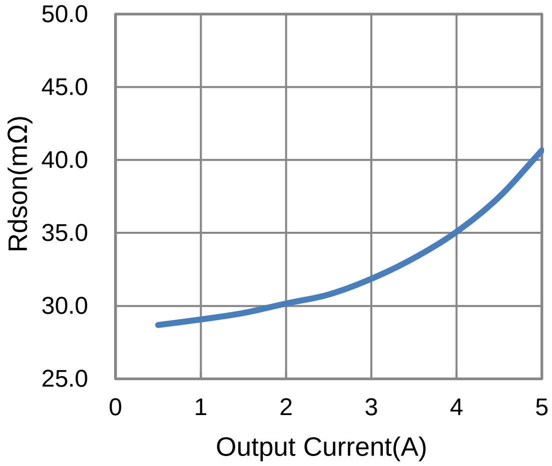


Figure 7 R_{dson} vs. Output Current

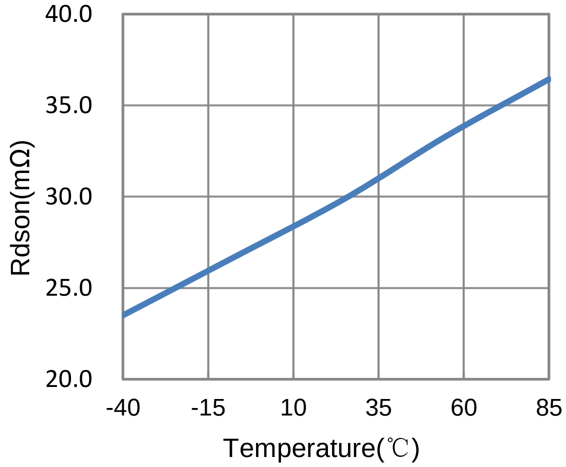


Figure 8 R_{dson} vs. Temp. (I_{OUT} = 1A)

TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25°C unless otherwise specified.

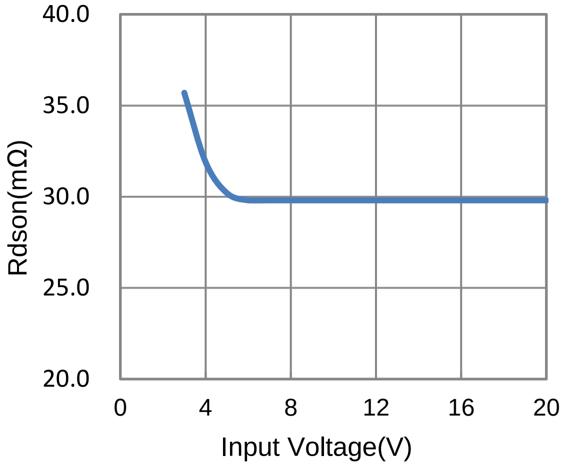


Figure 9 R_{dson} vs. Input Voltage (I_{OUT} = 1A)

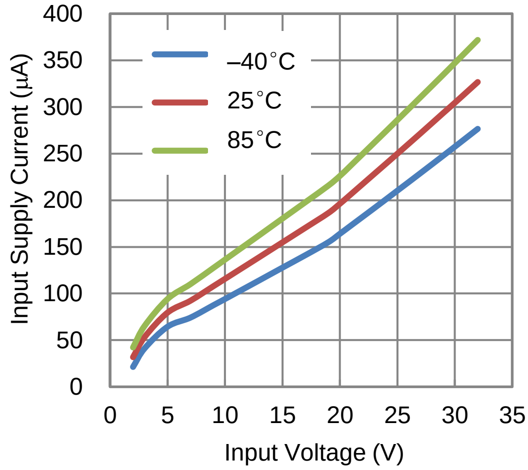


Figure 10 Input Supply Current vs. Supply Voltage

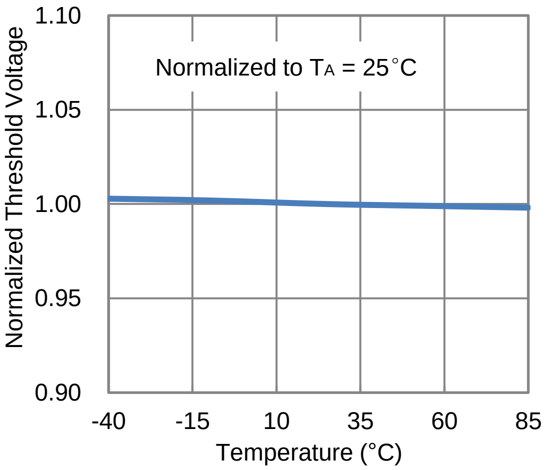


Figure 11 Normalized Internal OVP Threshold

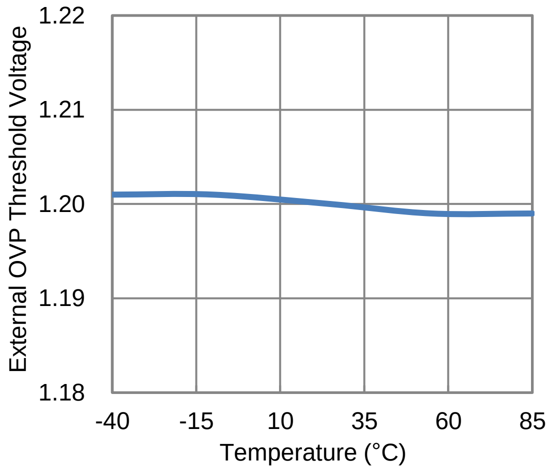


Figure 12 External OVP Threshold

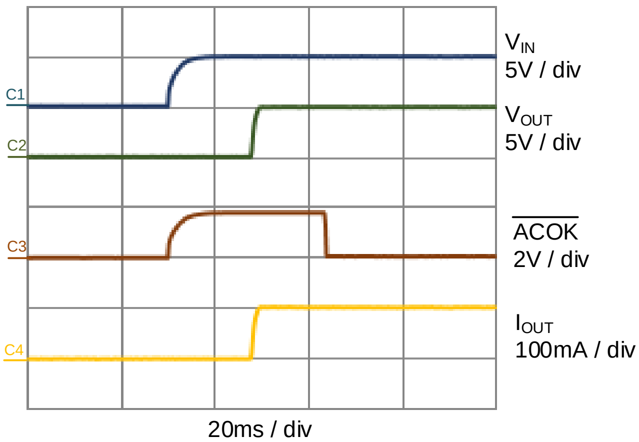


Figure 13 Power-up (C_{OUT} = 1μF, 100mA load).

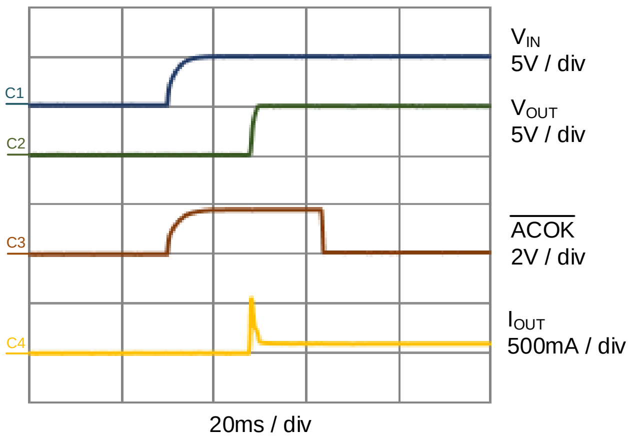


Figure 14 Power-up (C_{OUT} = 100μF, 100mA load)

TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25°C unless otherwise specified.

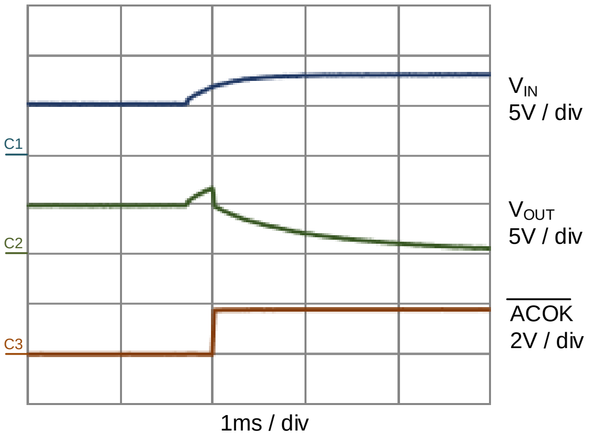


Figure 15 OVP Response (AW33905)

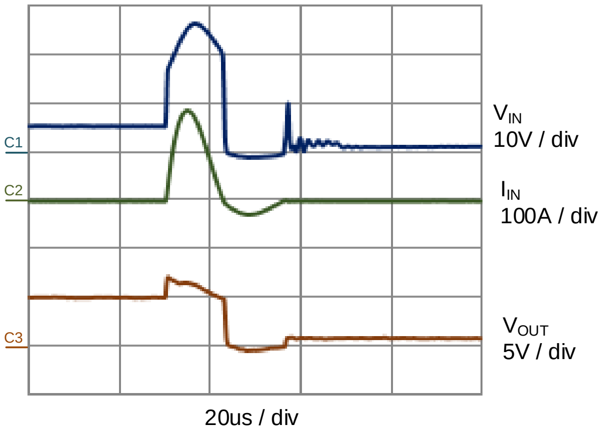


Figure 16 400V Surge Response (AW33905 with 12V TVS)

DETAILED FUNCTIONAL DESCRIPTION

Device Operation

If the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. $\overline{\text{ACOK}}$ will be driven low about 30ms after V_{IN} valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 50ns. If input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

The adjustment range is 4V to 20V. When the OVLO pin voltage V_{OVLO} exceeds V_{OVLO_SEL} (0.26V typical), V_{OVLO} is compared with the reference voltage V_{OVLO_TH} (1.2V typical) to judge whether input supply is over-voltage. It is recommended that the total resistance of R1 and R2 is less than 100kΩ.For example, if we select R_1 = 51kΩ and R_2 = 12.4kΩ, then the new OVP threshold calculated from the above formula is 6.14V.

$\overline{\text{ACOK}}$ Output

The device features an open-drain output $\overline{\text{ACOK}}$, it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and $V_{IN\_UVLO}<V_{IN}<V_{IN\_OVLO}$, $\overline{\text{ACOK}}$ will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, the switch will be turned off and $\overline{\text{ACOK}}$ will be pulled high. If this function is not needed, $\overline{\text{ACOK}}$ pin can be floating or grounded.

USB On-The-Go (OTG) Operation

If V_{IN} = 0V and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When $V_{IN} > V_{IN\_UVLO}$, internal charge pump begins to open the load switch after debounce time (15ms typical). After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

PCB LAYOUT CONSIDERATION

To make fully use of the performance of AW339XX, the guidelines below should be followed.

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW339XX) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW339XX) and close to OUT pin.

2. IN pin routing passes through the external TVS firstly, and then connect AW339XX.

3. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

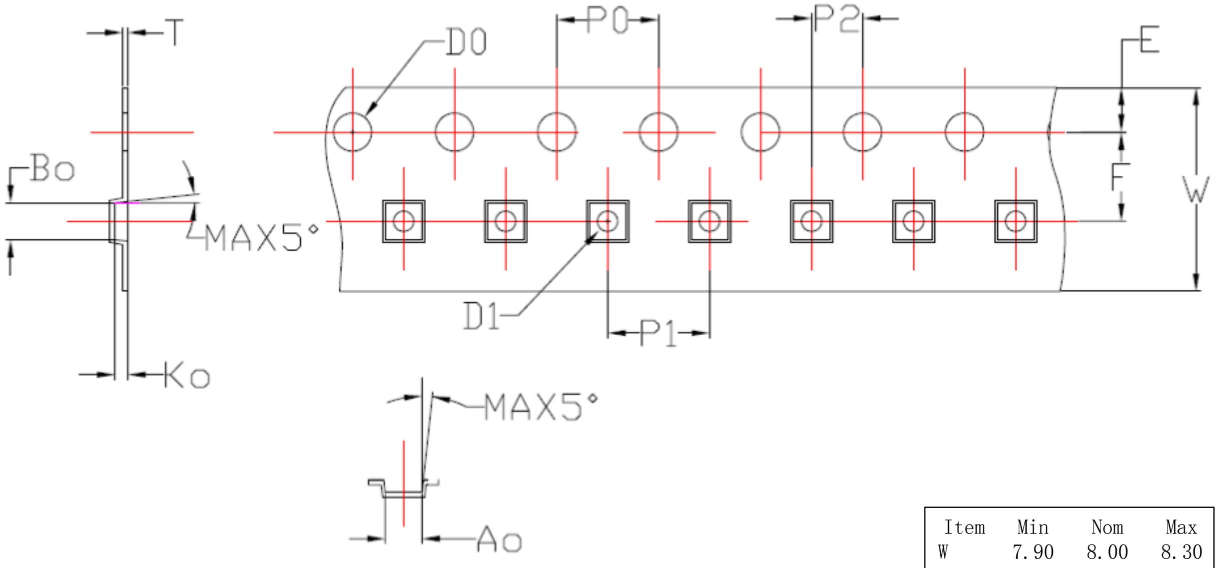
4. If R_1 and R_2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.

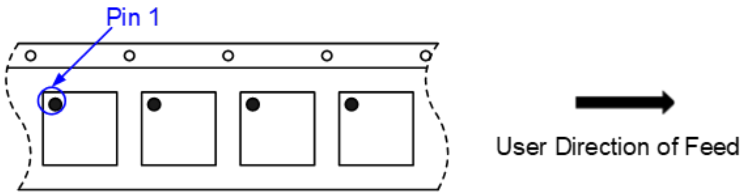
5. The power trace from USB connector to AW339XX may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.

6. Use rounded corners on the power trace from USB connector to AW339XX to decrease EMI coupling.

TAPE AND REEL INFORMATION

CARRIER TAPE

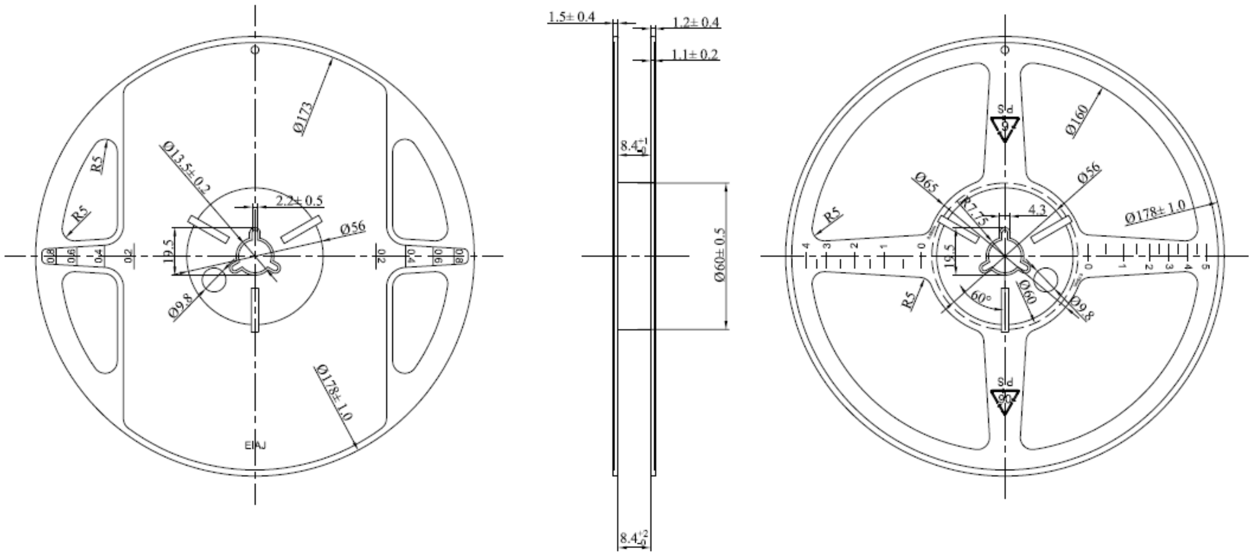




Item	Min	Nom	Max
W	7.90	8.00	8.30
A0	1.33	1.38	1.43
B0	1.33	1.38	1.43
K0	0.70	0.75	0.80
P	3.90	4.00	4.10
E	1.65	1.75	1.85
F	3.45	3.50	3.55
D0	1.50	1.50	1.60
D1	0.75	0.80	0.85
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
T	0.22	0.25	0.28

NOTE:
1. Unit: mm;
2. Material: ABS;
3. Carrier camber not exceed 1mm in 250mm;
4. 10 sprocket hole pitch cumulative tolerance ±0.2mm;
5. All tape and sprocket hole dimensioning are as per EIA-481 unless otherwise stated;
6. A0 and B0 measured on a place in the middle of the comer RADⅡ.

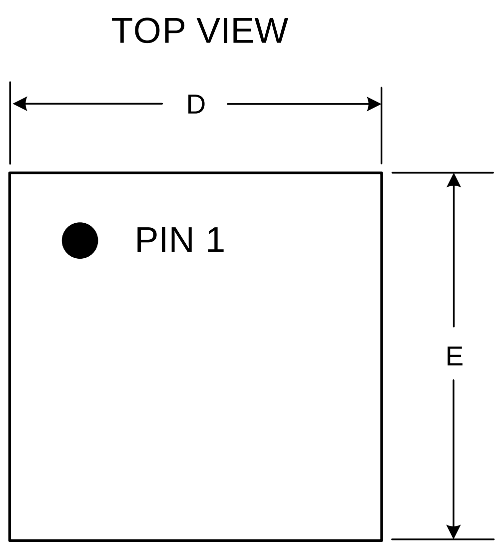
REEL

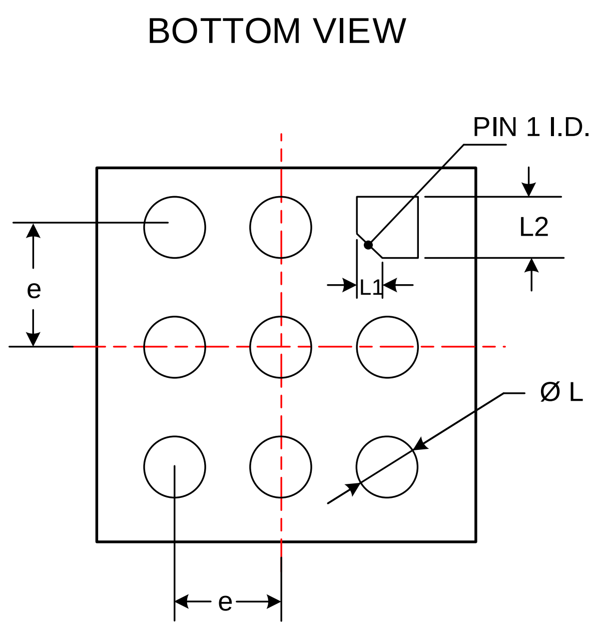


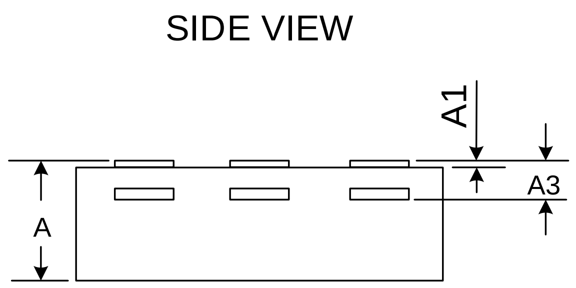
NOTE:

1. Units: mm;
2. Material: polystyrene;
3. Planeness: max 3mm;
4. Surface resistance: 10^5 to 10^{11} ohms/sq;
5. All outstanding tolerance: ±0.25mm.

PACKAGE DESCRIPTION



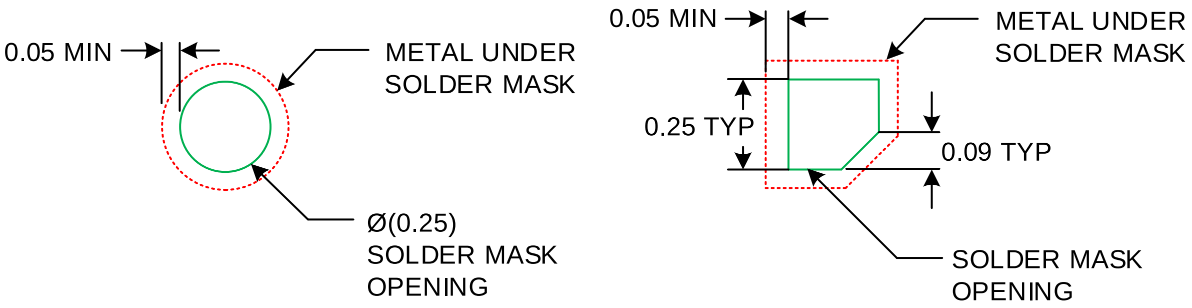




SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF.	
D	1.10	1.20	1.30
E	1.10	1.20	1.30
e		0.400REF.	
L	0.18	0.25	0.30
L1		0.090REF.	
L2		0.250REF.	

Unit: mm

SOLDER MASK DETAILS



SOLDER MASK DETAILS

NOT TO SCALE

NOTE:

Unit: mm.

REFLOW

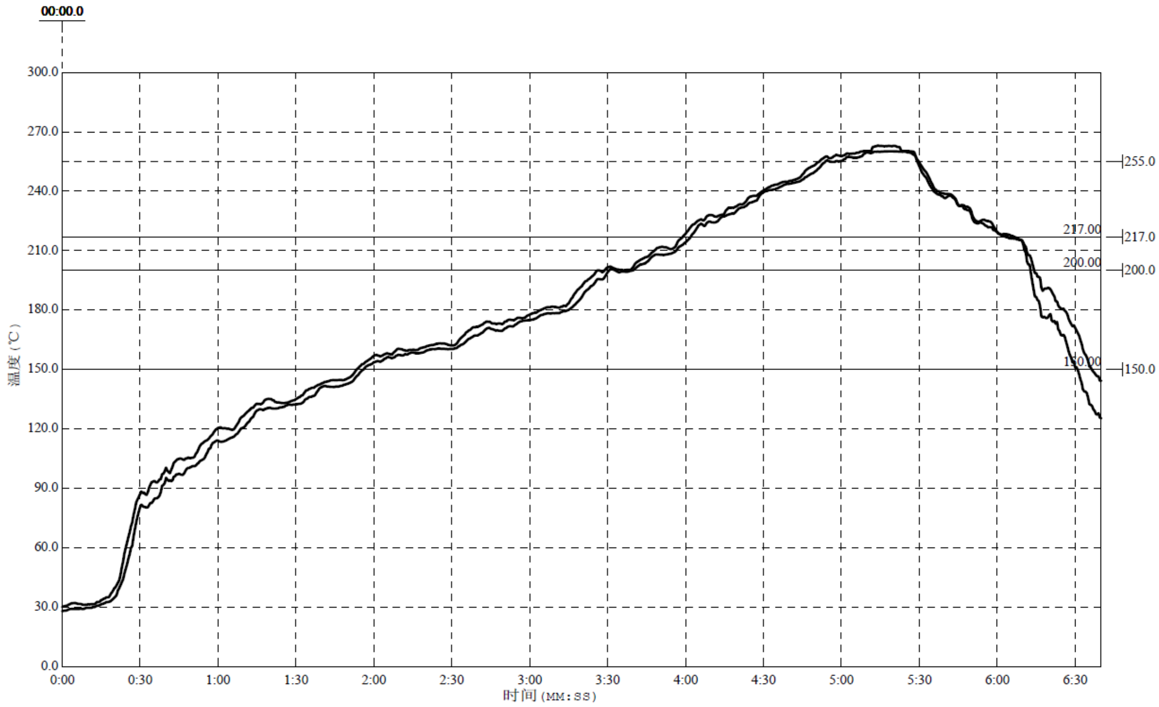


Figure 17 Package Reflow Oven Thermal Profile

Table 1 Package Reflow Standard

Reflow Note	Spec
Average ramp-up rate (217°C to Peak)	Max. 3°C /sec
Time of Preheat temp.(from 150°C to 200°C)	60-120 sec
Time to be maintained above 217°C	60-150 sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40 sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW339XX adopted the Pb-Free assembly.

REVISION HISTORY

Vision	Date	Change Record
V0.9	November 2017	Datasheet V0.9 Released.
V1.0	December,2017	1. Added AW33901 part number. 2. Added Typical Characteristics. 3. Added Tape and Reel information. 4. Added Solder Mask Details.
V1.1	February,2018	1. Modified Reel information. 2. Modified POD information. 3. Modified Solder Mask Details.
V1.2	September, 2018	Storage Temperature Modified

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