

Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

FEATURES

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- low noise figure(NF)=0.85dB@1.575GHz; NF =0.79dB@1.227GHz;NF=0.80dB@1.176GHz;
- High power gain=18.2dB@1.575GHz;power gain=18.9dB@1.227GHz;power gain=18.7dB @1.176 GHz;
- High linearity IIP3oob=+6.5dBm;
- High input 1dB-compression point=-7.6dBm;
- Requires only one input matching inductor;
- RF output internally matched to 50 ohm;
- Supply voltage: 1.5V to 3.6V;
- Operating frequencies: GPS L1、 L2/L5 band;
- DFN 1.5mmX1.0mmX0.55mm-6L package;
- 3KV HBM ESD protection (including RFIN and RFOUT pin);

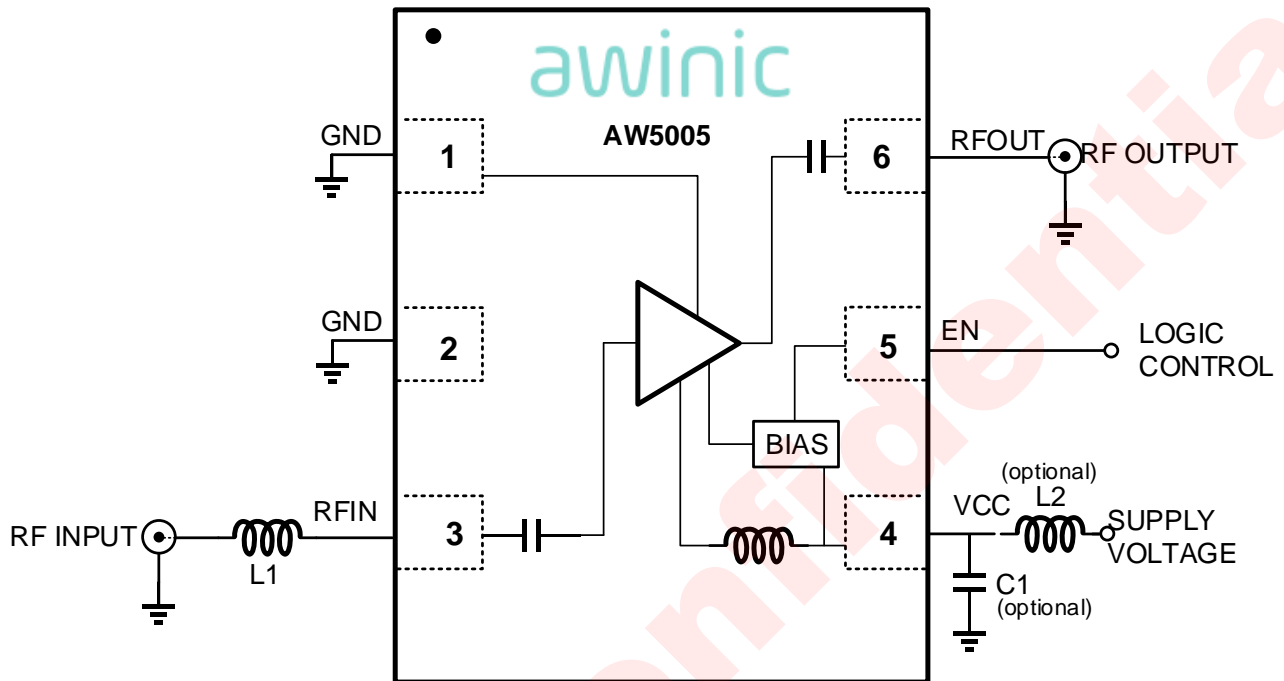
APPLICATIONS

- Smart phones, feature phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

GENERAL DESCRIPTION

- The AW5005 is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW5005 can be close to the antenna, requires only one external input matching inductor, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW5005 with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.6V. All these features make AW5005 an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.
- The AW5005 is available in a small lead-free, RoHS-Compliant, DFN 1.5mm X 1.0mm X 0.55mm -6L package.

TYPICAL APPLICATION CIRCUIT



C1, L2 Closed to LNA

Figure 1 Typical Application Circuit of AW5005 for GNSS L1、L2/L5

All trademarks are the property of their respective owners.

PIN CONFIGURATION AND TOP MARK

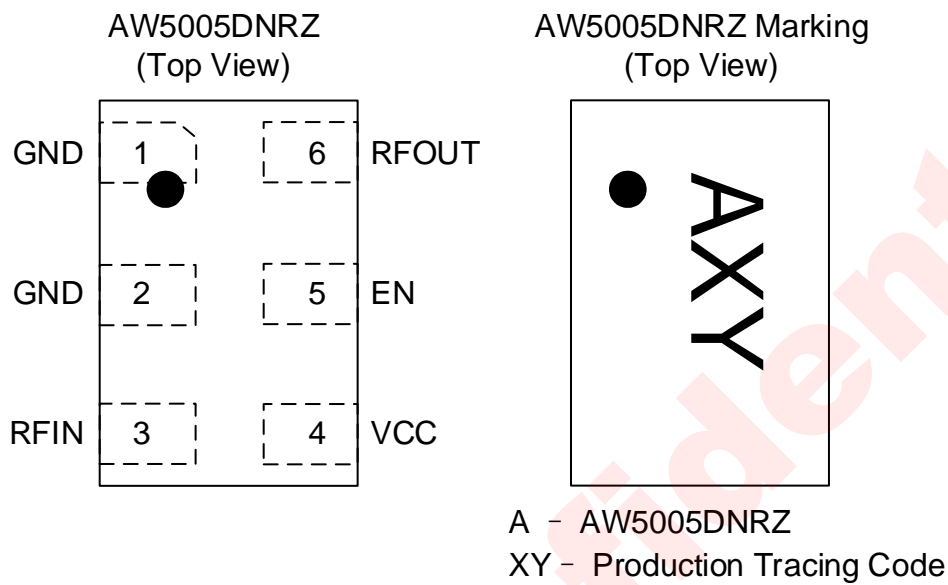
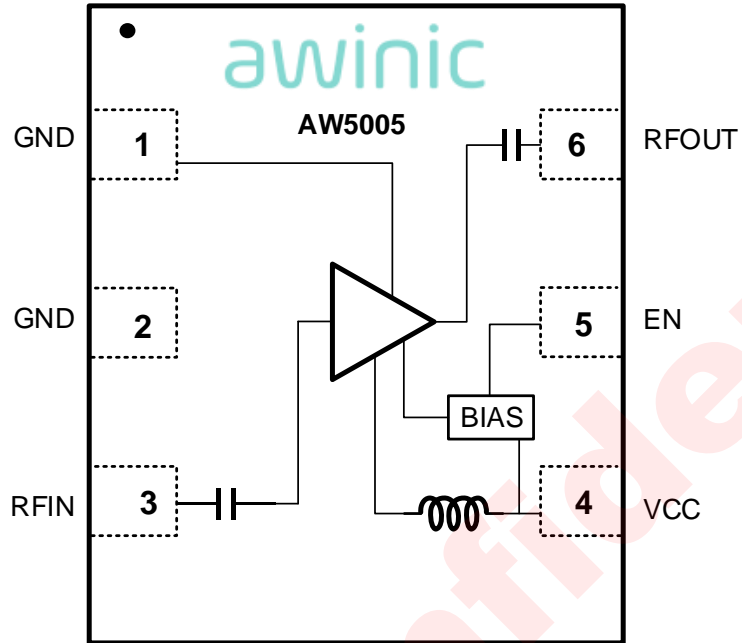


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

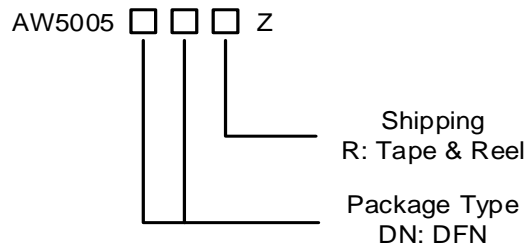
No.	NAME	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	RFIN	LNA input
4	VCC	DC Supply
5	EN	Logic control
6	RFOUT	LNA output

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW5005DNRZ	-40°C ~ 85°C	DFN 1.5mmX1.0mm-6L	A	MSL3	ROHS+HF	3000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS^[1]

PARAMETERS	Symbol	Values			
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V _{CC}	-0.3	-	5	V
Voltage at pin EN [2]	V _{EN}	-0.3	-	5	V
Current into pin VCC	I _{CC}	-	-	30	mA
RF input power [3]	P _{IN}	-	-	10	dBm
Package thermal resistance	θ _{JA}	-	148.2	-	°C/W
Junction temperature	T _J	-	-	150	°C
Storage temperature range	T _{STG}	-65	-	150	°C
Ambient temperature range	T _{amb}	-40	-	85	°C
Solder temperature(10s)		-	260	-	°C
ESD range					
HBM [4]			±3000		V
CDM			±1000		V
Latch-up					
Standard: JEDEC STANDARD NO.78E SEPTEMBER 2016			+IT: +400 -IT: -400		mA

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2: Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 5.0V in order to avoid excess current.

Note3: The RF input and RF output are AC coupled through internal DC blocking capacitor.

Note4: HBM standard: MIL-STD-883J Method 3015.9.

ELECTRICAL CHARACTERISTICS

(AW5005 EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1550MHz to 1615MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1575.42MHz, input matched to 50Ω using a 9.1nH inductor, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.6	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		8.0	13.0	mA
V _{EN}	Digital Input-Logic High		0.80			V
V _{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		16.0	18.2	18.5	dB
RL _{in}	Input Return Loss			5.6		dB
RL _{out}	Output Return Loss			10		dB
ISL	Reverse Isolation		25.0	28.5		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer		0.85		dB
K _f	Stability factor	f=20MHz...10GHz	1			
NF _j	Noise Figure with jammer	P _{jam} =-20dBm; f _{jam} =850MHz		0.72	1.10	dB
		P _{jam} =-20dBm; f _{jam} =1850MHz		1.14	1.50	dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-9.0	-7.6		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-20dBm;	+4.0	+6.1		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm;	+4.5	+6.5		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-20dBm	-2.0	-1.2		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-30dBm	-2.0	-1.2		dBm
H2-input referred	LTE band-13 2 nd Harmonic	f=787.76MHz; Pin=-25dBm;		-74.4	-70.0	dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		fH2=1575.52MHz				
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	2.5	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	2.0	μs

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1}-IM3)+Pi_{f1}$.

Note4: $IIP2=Po_{f2}+Pi_{f2}-IM2$.

(AW5005 EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1550MHz to 1615MHz; Typical values are at VCC=1.8V and TA=+25°C, f=1575.42MHz, input matched to 50Ω using a 9.1nH inductor, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.6	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		6.0	15.0	mA
V _{EN}	Digital Input-Logic High		0.80			V
V _{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		16.0	17.5	18.0	dB
RL _{in}	Input Return Loss			5.3		dB
RL _{out}	Output Return Loss			10		dB
ISL	Reverse Isolation		25.0	28.0		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer		0.83		dB
K _f	Stability factor	f=20MHz...10GHz	1			
NF _j	Noise Figure with jammer	P _{jam} =-20dBm; f _{jam} =850MHz		0.76	1.10	dB
		P _{jam} =-20dBm; f _{jam} =1850MHz		1.18	1.50	dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-14.0	-12.5		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-20dBm;	-1.0	0.7		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm;	0	2.5		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-20dBm	-3.0	-1.9		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-30dBm	-3.0	-1.7		dBm
H2-input referred	LTE band-13 2 nd Harmonic	f=787.76MHz; Pin=-25dBm; fH2=1575.52MHz		-72.6	-70.0	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	2.5	μs

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	2.0	μs

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1}-IM3)+Pi_{f1}$.

Note4: $IIP2=Po_{f2}+Pi_{f2}-IM2$.

(AW5005 EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1227.60±1.023MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1227.60MHz, input matched to 50Ω using a 15nH inductor, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.6	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		8	13.0	mA
V _{EN}	Digital Input-Logic High		0.80			V
V _{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		16.0	18.9	18.5	dB
RL _{in}	Input Return Loss			5.5		dB
RL _{out}	Output Return Loss			12.3		dB
ISL	Reverse Isolation		25.0	26.2		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer		0.79		dB
K _f	Stability factor	f=20MHz...10GHz	1			
NF _j	Noise Figure with jammer	P _{jam} =-20dBm; f _{jam} =850MHz		0.72	1.10	dB
		P _{jam} =-20dBm; f _{jam} =1850MHz		1.14	1.50	dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-9.0	-7.6		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-20dBm;	+4.0	+6.1		dBm
IIP3 _{oob}	Out-of-band input	f1=1712.7MHz ^[3] ; f2=1850MHz;	+4.5	+6.5		dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	3 rd -order intercept point	Pin=-30dBm;				
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-20dBm	-2.0	-1.2		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-30dBm	-2.0	-1.2		dBm
H2-input referred	LTE band-13 2 nd Harmonic	f=787.76MHz; Pin=-25dBm; fH2=1575.52MHz		-74.4	-70.0	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	2.5	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	2.0	μs

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1-IM3})+Pi_{f1}$.

Note4: $IIP2=Po_{f2}+Pi_{f2}-IM2$.

(AW5005 EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1227.60±1.023MHz; Typical values are at VCC=1.8V and TA=+25°C, f=1227.60MHz, input matched to 50Ω using a 15nH inductor, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.6	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		6.0	13.0	mA
V _{EN}	Digital Input-Logic High		0.80			V
V _{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		16.0	18.2	18.5	dB
RL _{in}	Input Return Loss			5.4		dB
RL _{out}	Output Return Loss			12.4		dB
ISL	Reverse Isolation		25.0	25.6		dB
NF	Noise Figure ^[2]	Zs=50 ohm; No jammer		0.83		dB
Kf	Stability factor	f=20MHz...10GHz	1			

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
NF _j	Noise Figure with jammer	P _{jam} =-20dBm; f _{jam} =850MHz		0.72	1.10	dB
		P _{jam} =-20dBm; f _{jam} = 1850MHz		1.14	1.50	dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-9.0	-7.6		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-20dBm;	+4.0	+6.1		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm;	+4.5	+6.5		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-20dBm	-2.0	-1.2		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-30dBm	-2.0	-1.2		dBm
H2-input referred	LTE band-13 2 nd Harmonic	f=787.76MHz; Pin=-25dBm; fH2=1575.52MHz		-74.4	-70.0	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	2.5	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	2.0	μs

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1-IM3})+Pi_{f1}$.

Note4: $IIP2=Po_{f2}+Pi_{f2}-IM2$.

(AW5005 EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1176.45±1.023MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1176.45MHz, input matched to 50Ω using a 15nH inductor, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.6	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		8.0	13.0	mA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{EN}	Digital Input-Logic High		0.80			V
V_{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
G_p	Power Gain		16.0	18.7	18.9	dB
RL_{in}	Input Return Loss			4.9		dB
RL_{out}	Output Return Loss		12.0	14.3		dB
ISL	Reverse Isolation		25.0	26.0		dB
NF	Noise Figure ^[2]	Zs=50 ohm; No jammer		0.80		dB
Kf	Stability factor	f=20MHz...10GHz	1			
NF _j	Noise Figure with jammer	Pjam=-20dBm; fjam=850MHz		0.72	1.10	dB
		Pjam=-20dBm; fjam=1850MHz		1.14	1.50	dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-9.0	-7.6		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-20dBm;	+4.0	+6.1		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm;	+4.5	+6.5		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-20dBm	-2.0	-1.2		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-30dBm	-2.0	-1.2		dBm
H2-input referred	LTE band-13 2 nd Harmonic	f=787.76MHz; Pin=-25dBm; fH2=1575.52MHz		-74.4	-70.0	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	2.5	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	2.0	μs

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1}-IM3)+Pi_{f1}$.

Note4: $IIP2=Po_{f2}+Pi_{f2}-IM2$.

(AW5005 EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1176.45±1.023MHz; Typical values are at VCC=1.8V and TA=+25°C, f=1176.45MHz, input matched to 50Ω using a 15nH inductor, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V _{CC}	Supply Voltage		1.5	-	3.6	V
I _{SD}	Shut-Down Current	EN=Low			1	μA
I _{CC}	Supply Current	EN=High		6.0	13.0	mA
V _{EN}	Digital Input-Logic High		0.80			V
V _{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
G _p	Power Gain		16.0	18.0	18.7	dB
RL _{in}	Input Return Loss			5.2		dB
RL _{out}	Output Return Loss		12.0	14.2		dB
ISL	Reverse Isolation		25.0	25.4		dB
NF	Noise Figure ^[2]	Z _s =50 ohm; No jammer		0.84		dB
K _f	Stability factor	f=20MHz...10GHz	1			
NF _j	Noise Figure with jammer	P _{jam} =-20dBm; f _{jam} =850MHz		0.72	1.10	dB
		P _{jam} =-20dBm; f _{jam} =1850MHz		1.14	1.50	dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-9.0	-7.6		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-20dBm;	+4.0	+6.1		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point	f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm;	+4.5	+6.5		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-20dBm	-2.0	-1.2		dBm
IIP2 _{oob}	Out-of-band input 2 nd -order intercept point	f1=824.6MHz ^[4] ; f2=2400MHz; Pin=-30dBm	-2.0	-1.2		dBm
H2-input referred	LTE band-13 2 nd Harmonic	f=787.76MHz; Pin=-25dBm; fH2=1575.52MHz		-74.4	-70.0	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2.2	2.5	μs

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1.7	2.0	μs

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1}-IM3)+Pi_{f1}$.

Note4: $IIP2=Po_{f2}+Pi_{f2}-IM2$.

APPLICATION BOARD

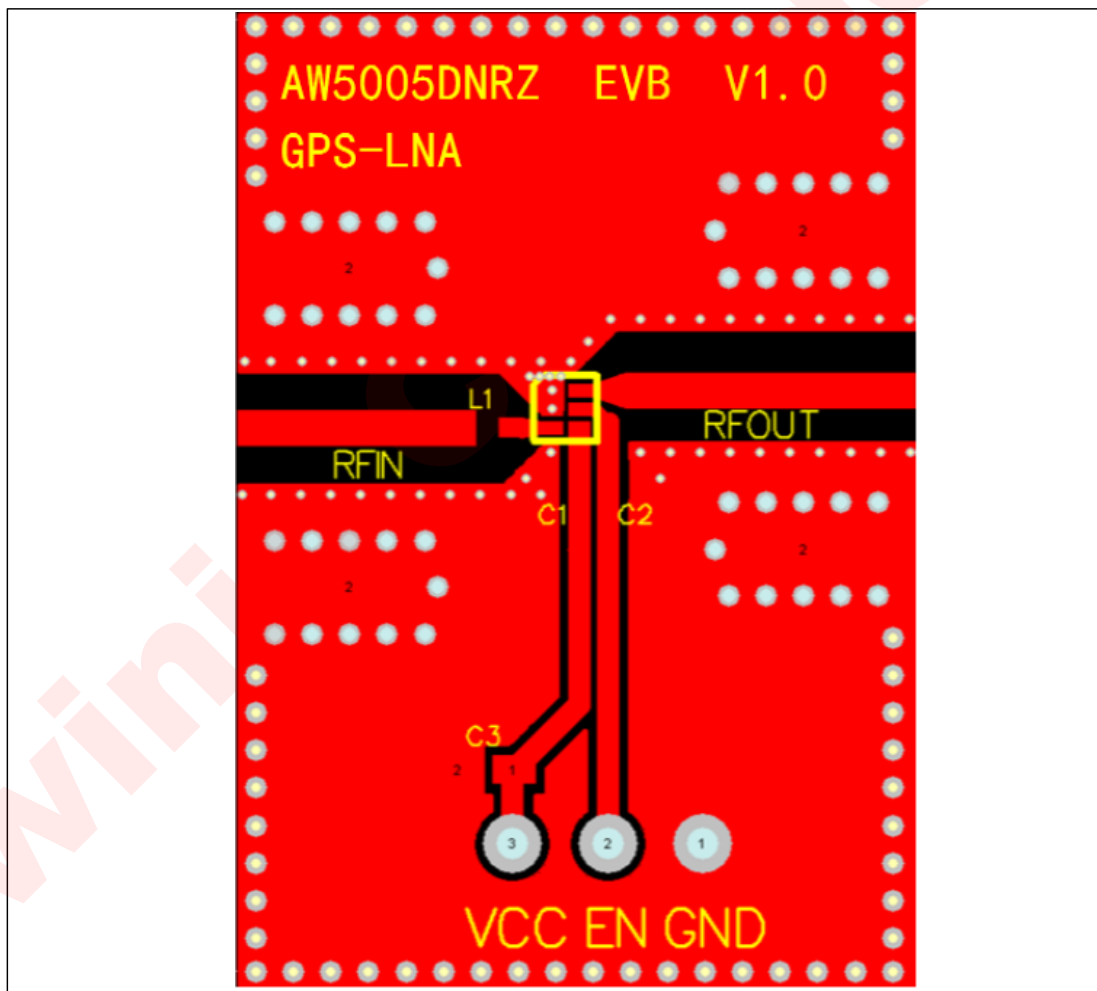


Figure 3. Drawing of Application Board

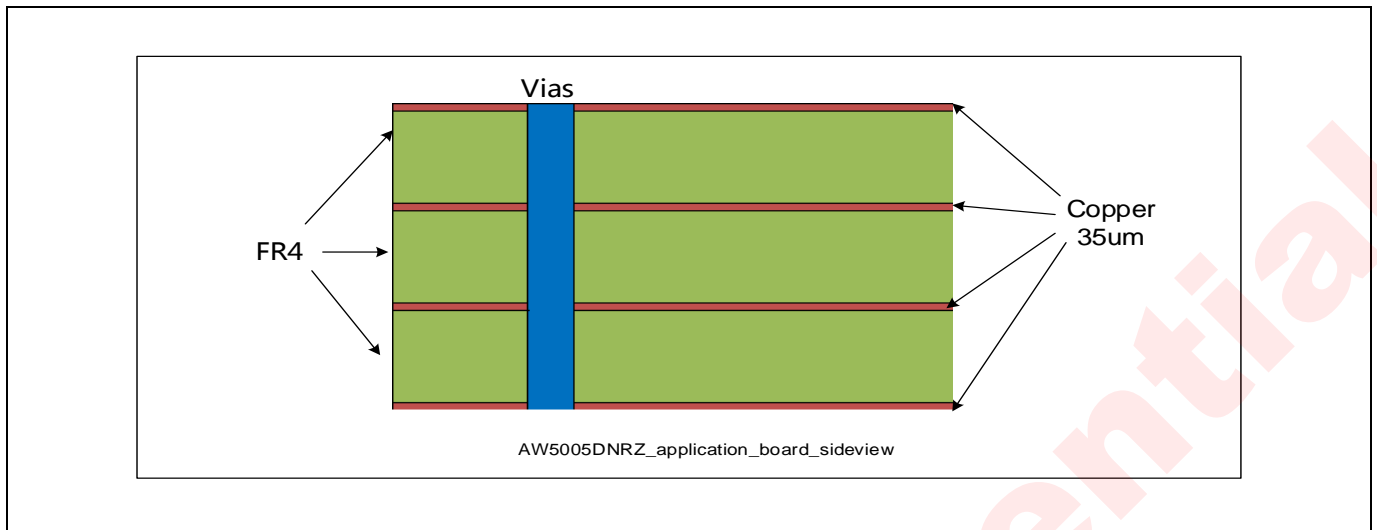
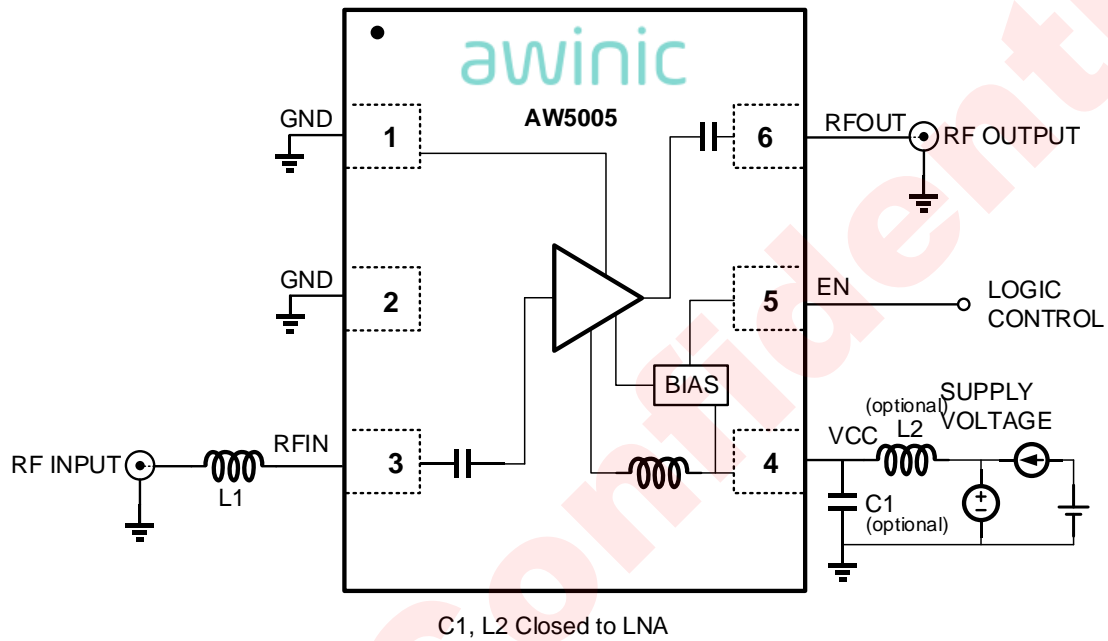


Figure 4. Application Board Cross-Section

TEST CIRCUITS

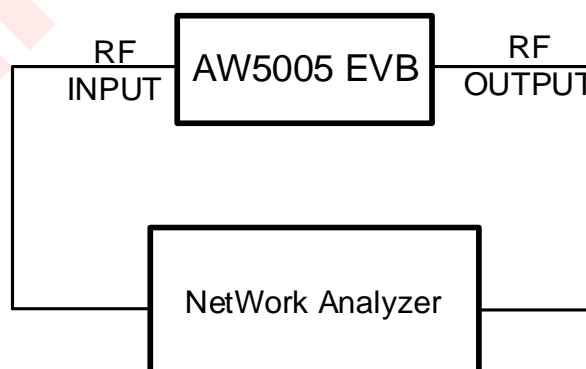
DC Characteristics

The following is the test bench for power supply, pin voltage, supply current, standby current



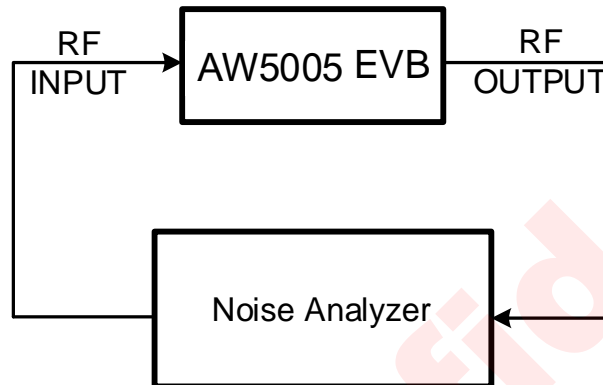
S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.



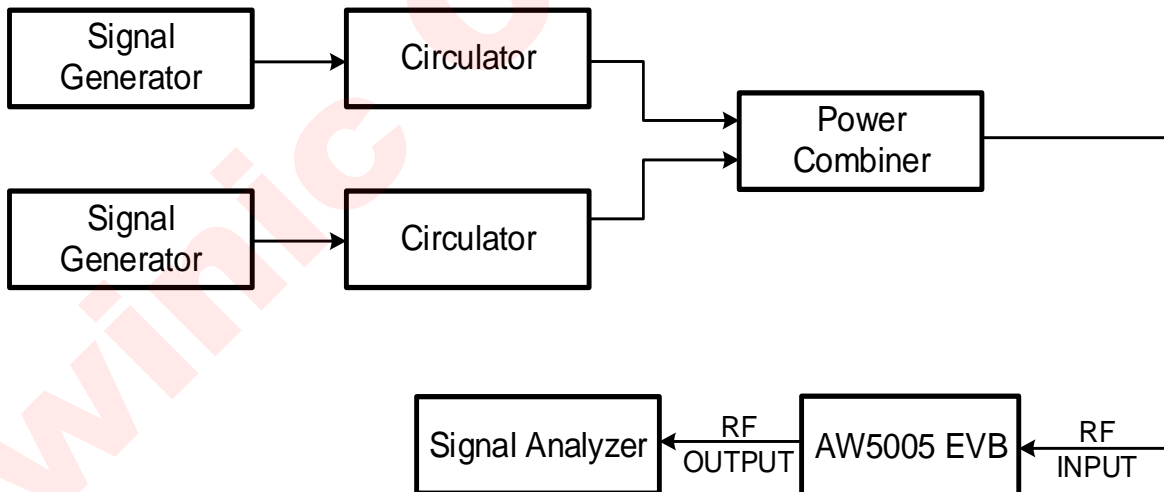
Noise Figure

The following is the test bench for noise figure, power gain.



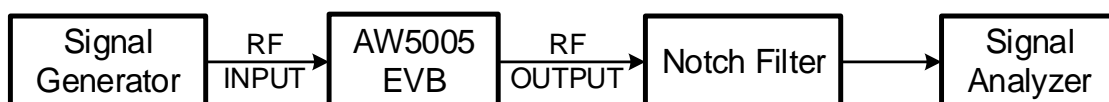
Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.



Harmonic distortion

The following is the test bench for second-order harmonic distortion.



RECOMMENDED COMPONENTS LIST

Table1 lists the recommended inductor types and values; Table 2 lists the recommended capacitor types and values.

Table1: list of inductor for GNSS L1

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	9.1	25	250	Murata	0402
L1	SDWL1005C	9.1	24	250	Sunlord	0402
L2	LQW15A	100	20	150	Murata	0402

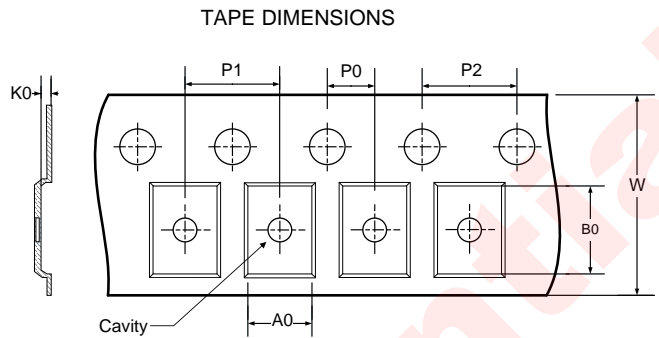
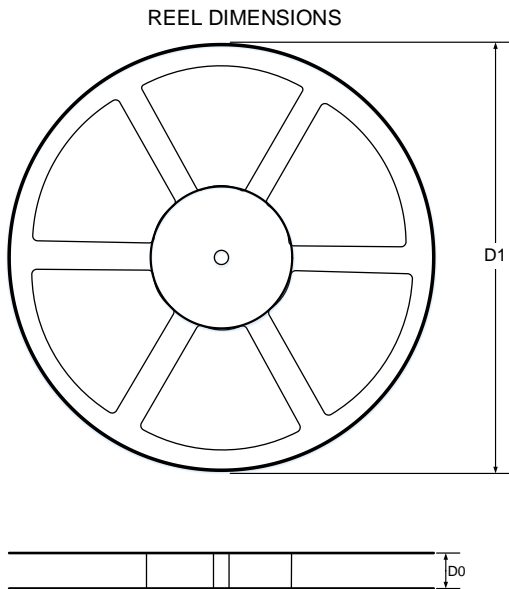
Table2: list of capacitor

Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
	Units	pF	V		
C1	GRM155	1000	50	Murata	0402

PCB LAYOUT CONSIDERATION

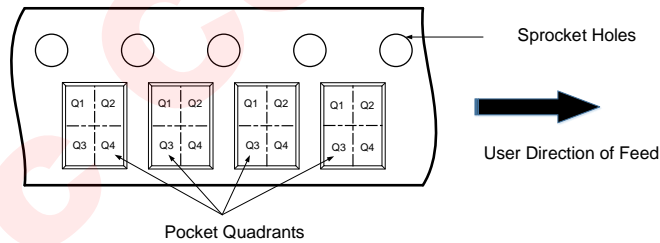
1. The AW5005 requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the capacitor we can get better performance like a little higher gain etc. The value is optimized for the best gain, noise figure, return loss performance. Typical value of inductor is 9.1nH, capacitor is 1nF. For schematics see Figure1.
2. The output of AW5005 is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.
3. The AW5005 should be placed close to the GPS antenna with the input-matching inductor. Use 50 ohm micro strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor should be located close to the device. For long VCC lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

TAPE AND REEL INFORMATION



- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width

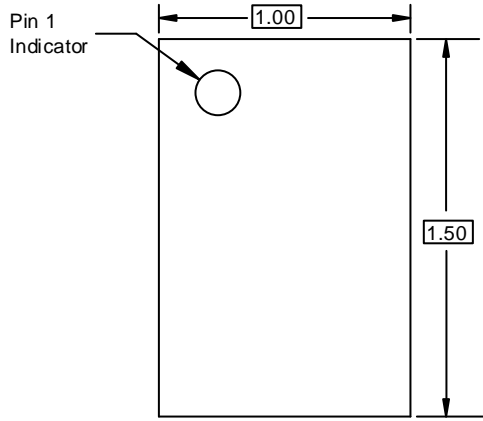
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



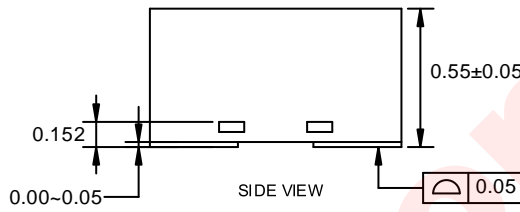
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.12	1.72	0.7	2	4	4	8	Q1

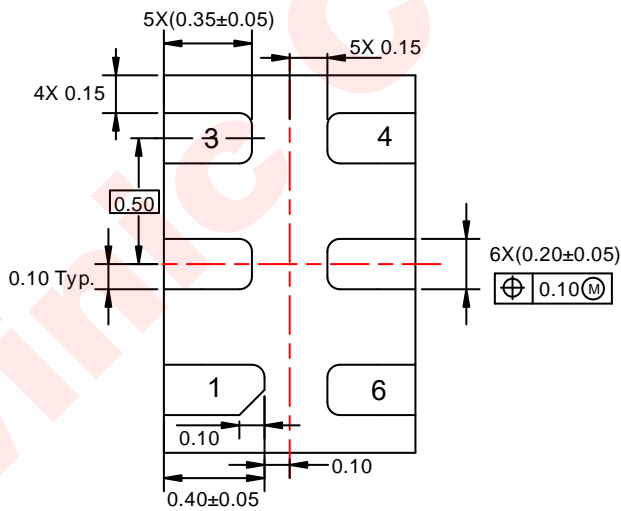
PACKAGE DESCRIPTION



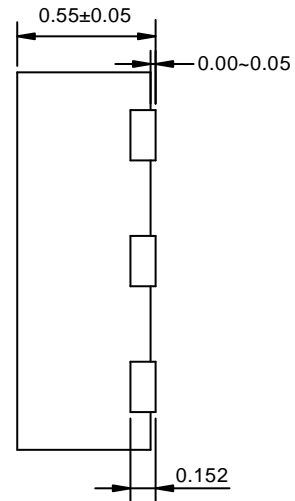
TOP VIEW



SIDE VIEW



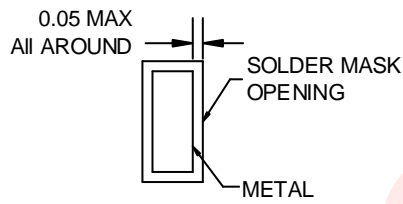
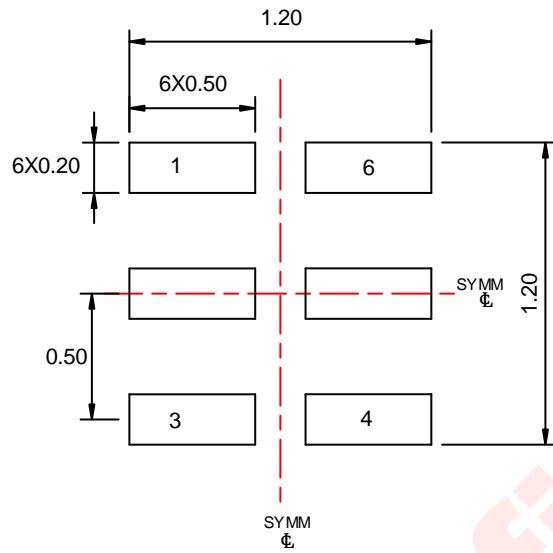
BOTTOM VIEW



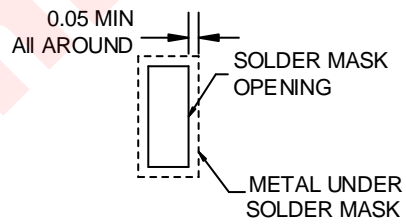
SIDE VIEW

Unit: mm

LAND PATTERN DATA



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Document ID	Release date	Change Record
AW5005_V1.4	2019-5	<ul style="list-style-type: none">● Updated S11 AND S22 OF L1 BAND
AW5005_V1.3	2019-5	<ul style="list-style-type: none">● Updated SP AND NF OF L1/L2/L5 BAND
AW5005_V1.2	2019-5	<ul style="list-style-type: none">● Updated S21 OF L1 BAND● Added S21 AND NF OF L2/L5 BAND
AW5005_V1.1	2019-2	<ul style="list-style-type: none">● Updated TAPE AND REEL INFORMATION● Updated PACKAGE DESCRIPTION● Updated LAND PATTERN DATA● Updated the Awinic logo
AW5005_V1.0	2016-12	Officially Released

DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Operational Amplifiers - Op Amps](#) category:

Click to view products by [Awinic](#) manufacturer:

Other Similar products are found below :

[OPA2991IDSGR](#) [OPA607IDCKT](#) [007614D](#) [633773R](#) [635798C](#) [635801A](#) [702115D](#) [709228FB](#) [741528D](#) [NCV33072ADR2G](#)
[SC2902DTBR2G](#) [SC2903DR2G](#) [SC2903VDR2G](#) [LM258AYDT](#) [LM358SNG](#) [430227FB](#) [430228DB](#) [460932C](#) [AZV831KTR-G1](#) [409256CB](#)
[430232AB](#) [LM2904DR2GH](#) [LM358YDT](#) [LT1678IS8](#) [042225DB](#) [058184EB](#) [070530X](#) [SC224DR2G](#) [SC239DR2G](#) [SC2902DG](#)
[SCYA5230DR2G](#) [714228XB](#) [714846BB](#) [873836HB](#) [MIC918YC5-TR](#) [TS912BIYDT](#) [NCS2004MUTAG](#) [NCV33202DMR2G](#)
[M38510/13101BPA](#) [NTE925](#) [SC2904DR2G](#) [SC358DR2G](#) [LM358EDR2G](#) [AZV358MTR-G1](#) [AP4310AUMTR-AG1](#) [HA1630D02MMEL-E](#)
[NJM358CG-TE2](#) [HA1630S01LPEL-E](#) [LM324AWPT](#) [HA1630Q06TELL-E](#)