

AW5017:内置可调谐电容的 FM 低噪声放大器

特性

- 无需耳机及拉杆天线,通过复用 GSM 天线实现 FM 信号接收
- 内置一线可编程逻辑单元的可调谐电容阵列,有效提升短天线在不同工作频段的天线效率
- 极低的噪声系数:1.2dB
- 标准 CMOS 工艺
- 1.8V 工作电压下高达 20dB 的增益
- 高线性度
- EN 管脚支持一线可编程逻辑的 4bit 可调谐电容
- 工作电压: 1.5V~3.6V
- 关机电流<0.1μA
- 纤小的 1.5x1.0x0.55 mm³ DFN-6L 封装

描述

AW5017 是一款低噪声放大器,无需耳机和拉杆天线,通过复用 GSM 天线实现 FM 信号接收。

AW5017 内置 EN 管脚控制的一线可编程逻辑单元,可控制 16 个台阶的可调谐电容阵列,有效提升短天线增益

AW5017 具有低噪声,高增益,高线性度的特性,典型值噪声系数 1.2dB,增益 21dB。

AW5017 的电源电压和使能 EN 电压范围在 1.5V 到 3.6V,典型值为 1.8/2.8V。

AW5017 将 RF 射频开关集成在内部芯片,在关断的条件下可以实现高阻抗,关机电流小于 0.1μA。

AW5017 采用纤小的 1.5mmx1.0mmx0.55mm DFN-6L 封装,额定的工作温度范围为-40℃至 85℃。

应用

- 功能和智能手机
- 便携式音频设备

引脚分布及标记图

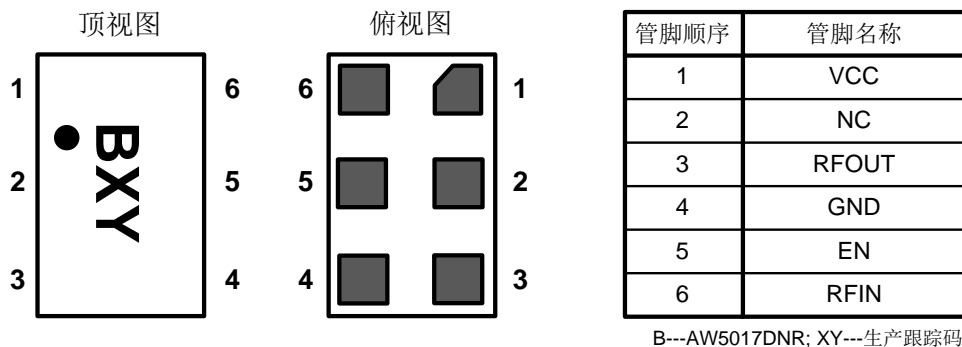


图1 AW5017 引脚分布图

FM Low-Noise-Amplifier with Embedded Tunable Capacitor

FEATURES

- Without any earphone or telescopic antenna, receive FM-radio signal through re-using GSM antenna
- Internal tunable capacitor-array using One-Line-Logic unit
- Ultra-low noise-figure: 1.2dB
- Standard CMOS process technology
- High power gain of 20dB under 1.8V supply
- High linearity
- EN supports 4-bit programmable One-Line-Logic
- Supply voltage: 1.5V~3.6V
- Shut-down current: <0.1μA
- Slim 1.5x1.0x0.55 mm³ DFN-6L package

GENERAL DESCRIPTION

AW5017 is a Low-Noise-Amplifier (LNA), without earphone or telescopic antenna, re-using GSM antenna to receive FM-radio signal.

AW5017 is characterized with low noise, high gain and high linearity. Typical noise figure is 1.2dB and power gain is 21dB.

AW5017 is powered by 2.6V~3.6V supply with typical 2.8V. EN supports 2.8V/1.8V GPIO input.

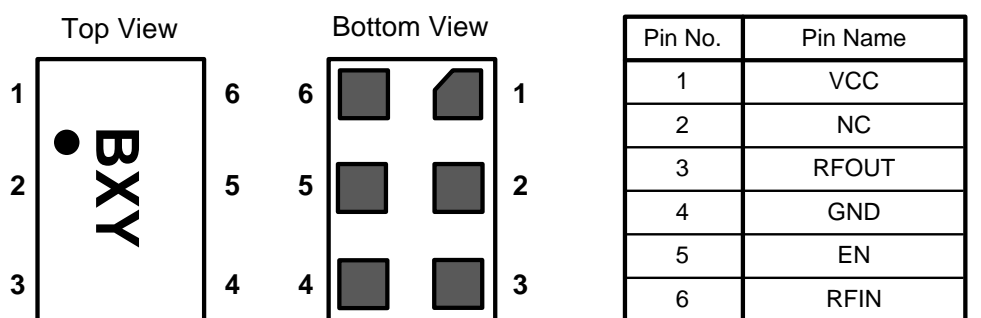
AW5017 integrates RF radio switch inside, implementing high impedance under shut-down condition. Shut-down current is less than 0.1μA.

AW5017 is available in slim 1.5mmx1.0mmx0.55mm DFN-6L package. The specified operating free- air temperature ranges from -40°C to 85°C.

APPLICATIONS

- Feature of Smart mobile phone
- Mobile audio device

PIN CONFIGURATION AND TOP MARK



B---AW5017DNR; XY---Manufacture Code

Figure 1 AW5017 pin configuration and top mark

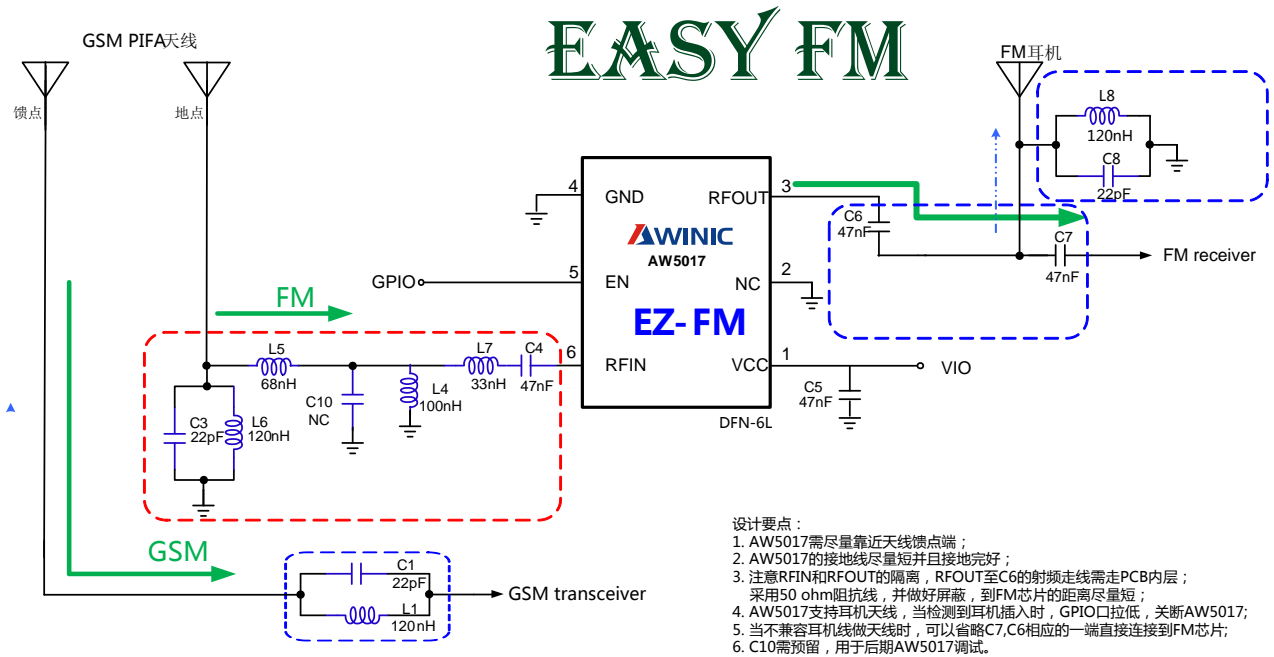
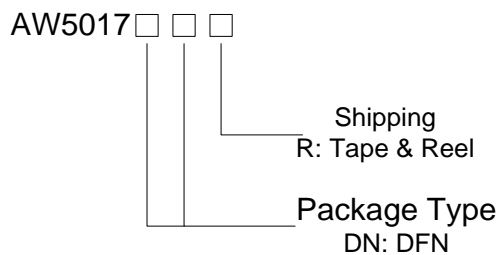


Figure 2 AW5017 typical application circuit

ORDERING INFORMATION

Table 1 ORDERING INFORMATION

Part Number	Temperature	Package	RoHS	Marking	Delivery Form
AW5017DNR	-40°C ~ 85°C	1.5mm×1.0mm×0.55mm DFN-6L	Yes	B	3000 units/ Tape and Reel



PIN DEFINITION

Table 2 PIN DEFINITION AND THEIR FUNCTION DESCRIPTION

No.	NAME	DESCRIPTION
1	VCC	Supply connection.
2	NC	Not connected. Prefer ground.
3	RFOUT	RF output.
4	GND	Ground.
5	EN	EN (high level) supports 1.8V/2.8V IO with internal 150Kohm pull-down resistor.
6	RFIN	RF input.

ABSOLUTE MAXIMUM RATINGS (NOTE1)

Table 3 ABSOLUTE MAXIMUM RATINGS

PARAMETERS	RANGE
Supply Voltage VCC	-0.3 V to 4.2 V
EN pin voltage	-0.3 V to 4.2 V
Supply maximum current ICC	30 mA
RFIN input power Pin	20 dBm
Junction-to-ambient thermal resistance θ_{JA}	625 °C/W
Maximum Junction temperature T _{JMAX}	125 °C
Storage temperature T _{STG}	-65 °C to 150 °C
Operating free-air temperature range	-40 °C to 85 °C
Lead Temperature (Soldering 10 Seconds)	260 °C
ESD^(NOTE 2)	
PINs HBM (human body model)	RFIN/RFOUT PINs: ±3500 V Other PINs: ±5000 V
Latch-up	
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008	+IT: +300 mA -IT: -300 mA

ELECTRICAL CHARACTERISTICS

Table 4 INFORMATION OF ELECTRICAL CHARACTERISTICS UNDER 1.8V SUPPLY

Test condition: TA=25 °C, VCC=1.8 V, EN=1.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
ISD	Shut-down Current	EN=0V		0.1	1	μA
IQ	Static Current	EN=1.8V		6.8		mA
NF	Noise Figure	Input/Output 50ohm		1.4		dB
S11	Input Return Loss	Input/Output 50ohm		-3.8		dB
S12	Reverse Isolation	Input/Output 50ohm		-39.0		dB
S21	Power Gain	Input/Output 50ohm		21.0		dB
S22	Output Return Loss	Input/Output 50ohm		-20.5		dB
Kf	Stability Factor	Input/Output 50ohm		>1		
IIP3	Input 3rd-order intercept point	(NOTE 3)		-12		dBm
IB P-1dB	In-Band 1dB-compression point	Input/Output 50ohm		-23		dBm
OOB P-1dB	Output-Of-Band 1dB- compression point	(NOTE 4)		-6		dBm

Table 5 INFORMATION OF ELECTRICAL CHARACTERISTICS UNDER 2.8V SUPPLY

Test condition: TA=25 °C, VCC=2.8 V, EN=2.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
ISD	Shut-down Current	EN=0V		0.1	1	μA
IQ	Static Current	EN=2.8V		9.2		mA
NF	Noise Figure	Input/Output 50ohm		1.2		dB
S11	Input Return Loss	Input/Output 50ohm		-3.9		dB
S12	Reverse Isolation	Input/Output 50ohm		-37.3		dB
S21	Power Gain	Input/Output 50ohm		21.0		dB
S22	Output Return Loss	Input/Output 50ohm		-18.0		dB
Kf	Stability Factor	Input/Output 50ohm		>1		
IIP3	Input 3rd-order intercept point	(NOTE 3)		-9		dBm
IB P-1dB	In-Band 1dB-compression point	Input/Output 50ohm		-21		dBm
OOB P-1dB	Output-Of-Band 1dB- compression point	(NOTE 4)		-2		dBm

Table 6 ELECTRICAL CHARACTERISTICS OF TUNABLE CAPACITOR

Test condition: TA=25 °C, VCC=1.5~3.6V, EN=VCC, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

	PARAMETER	MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	1.5	2.8	3.6	V
T _H	EN High Level Duration Time	0.4		50	μs
T _L	EN Low Level Duration Time	0.4		50	μs
T _{LATCH}	EN State Latch Time ^(NOTE 5)	150		500	μs
T _{OFF}	EN Off Delay Time ^(NOTE 6)	150		500	μs
n	Tunable Stage Number		16		
C _{min}	Minimum Tunable Capacitor		15		pF
C _{max}	Maximum Tunable Capacitor		45		pF
C _{step}	Minimum Stage		2		pF

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7

NOTE3: Measure IIP3 parameter through two tones of -40dBm/tone with the frequency of 97M and 98MHz

NOTE4: Input/Output are both 50-ohm; Input signal is composed of in-band 90-MHz signal and out-of-band 900MHz signal. Signal of 90-MHz is fixed to -40-dBm; signal of 900MHz varies and power level is measured when power gain of 90MHz signal drops 1dB.

NOTE5: Latch mechanism is already designed inside. When pulse width of high-level is wider than state latch time, chip will keep latch state inside unchanged and won't accept any new pulses, until off state.

NOTE6: Latch mechanism is already designed inside. When EN is changed from high-level to low-level, state inside will be changed to off after off delay time.

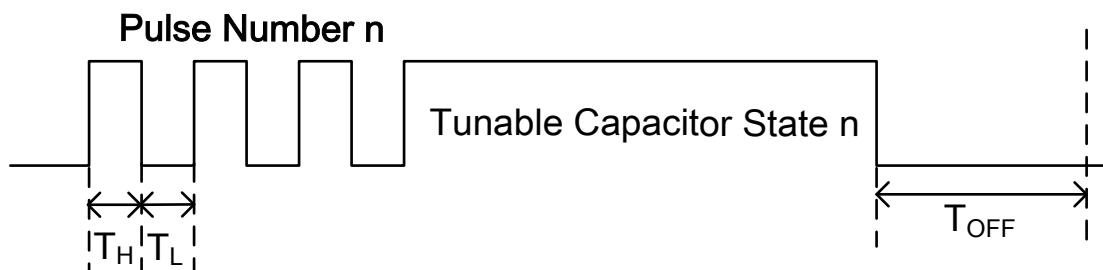


Figure 3 One-Line-Logic Timing Diagram

TYPICAL CHARACTERISTICS

Test condition: TA=25 °C, VCC=1.8 V, EN=1.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

Table 7 TABLE OF FIGURES

INDEX		FIGURE No.
S parameter	S11/S21/S12/S22	FIGURE 4/5/6/7
Noise Figure	NF	FIGURE 8
Stability Factor	K_f	FIGURE 9
P1dB Compression Point	P1dB(In-band/Out-of-Band)	FIGURE 10
Noise Figure	C_{in}	FIGURE 11

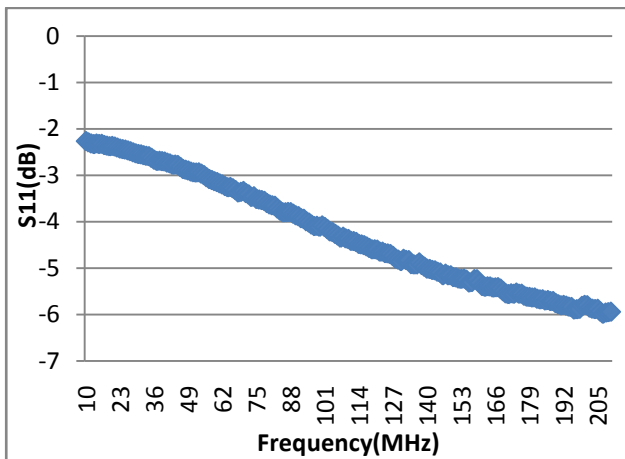


Figure 4 Input Return Loss(S11)

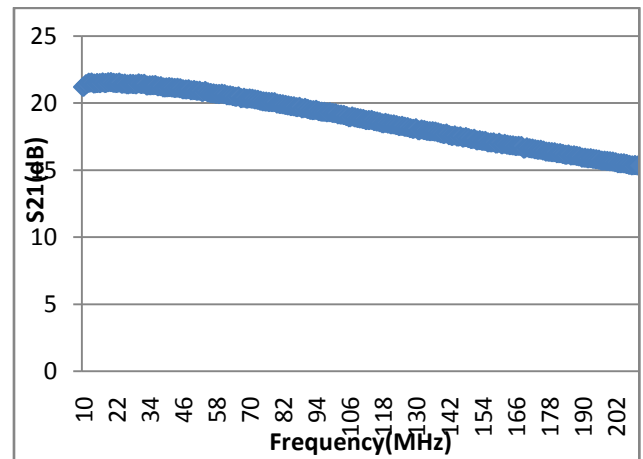


Figure 5 Power Gain(S21)

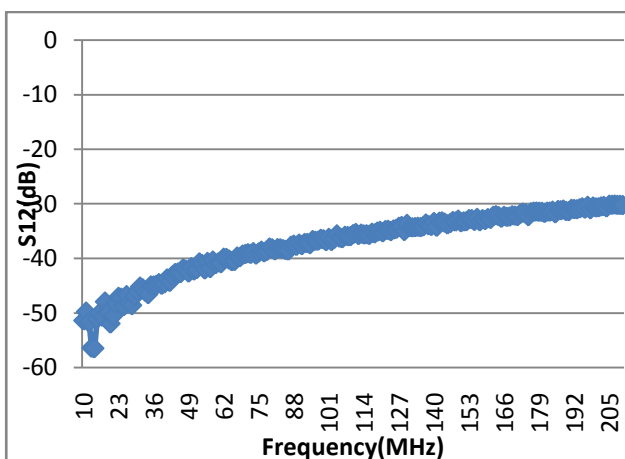


Figure 6 Reverse Isolation(S12)

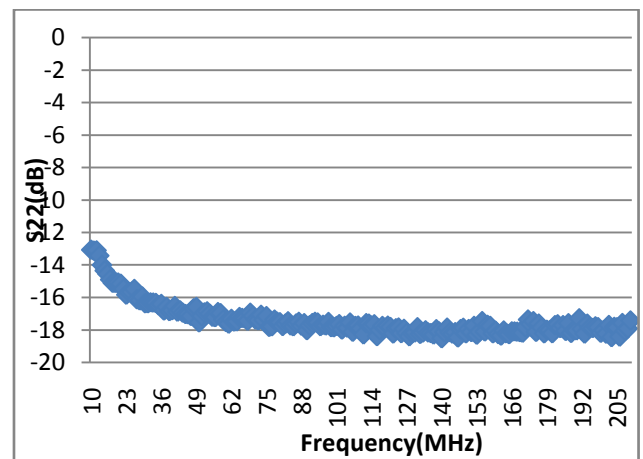


Figure 7 Output Return Loss(S22)

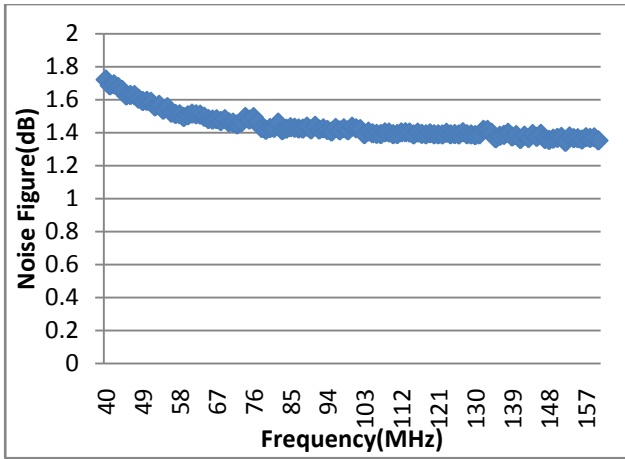


Figure 8 Noise Figure(NF)

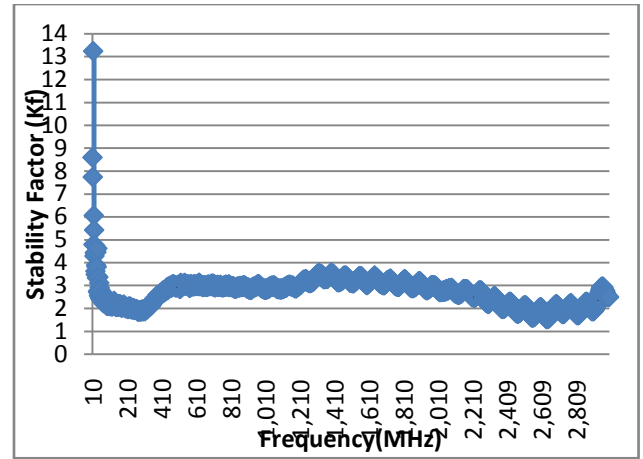


Figure 9 Stability Factor(Kf)

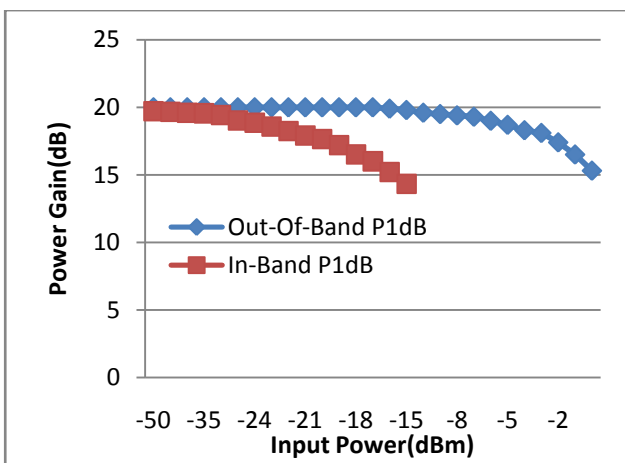


Figure 10 P1dB(In-Band/Out-Of-Band)

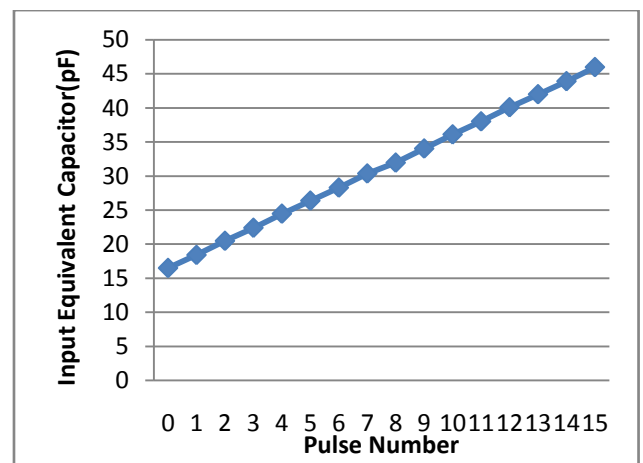


Figure 11 Tunable Capacitor(C_{in})

Test condition: TA=25 °C, VCC=2.8 V, EN=2.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

Table 8 TABLE OF FIGURES

INDEX		FIGURE No.
S parameter	S11/S21/S12/S22	FIGURE 12/13/14/15
Noise Figure	NF	FIGURE 16
Stability Factor	K _f	FIGURE 17
P1dB Compression Point	P1dB(In-band/Out-of-Band)	FIGURE 18
Noise Figure	C _{in}	FIGURE 19

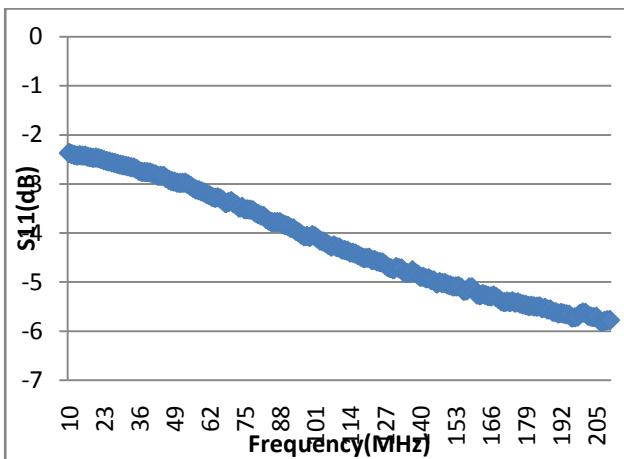


Figure 12 Input Return Loss(S11)

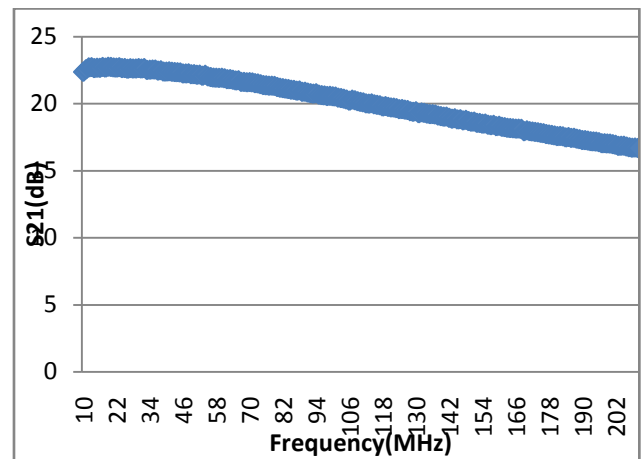


Figure 13 Power Gain(S21)

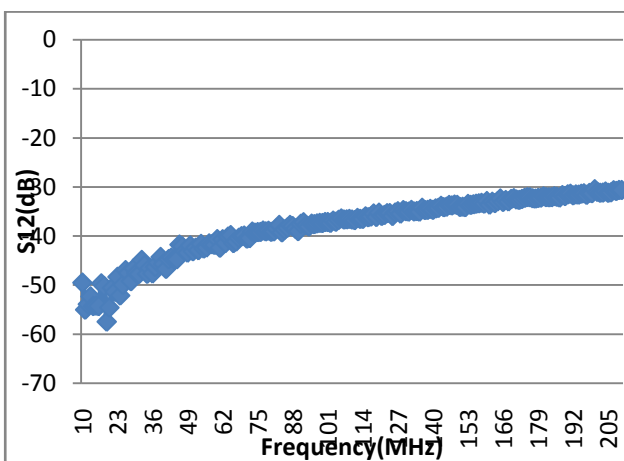


Figure 14 Reverse Isolation(S12)

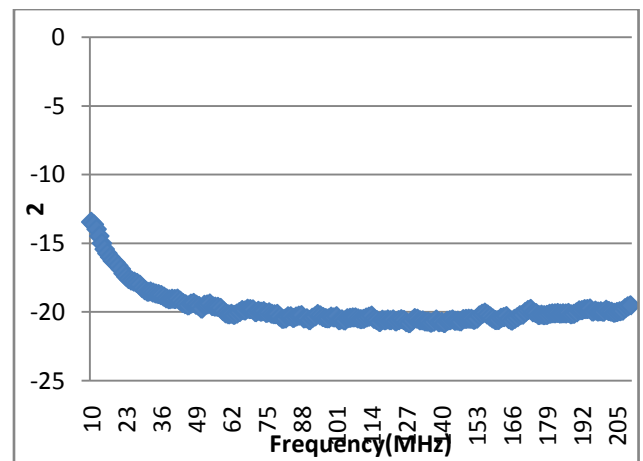


Figure 15 Output Return Loss(S22)

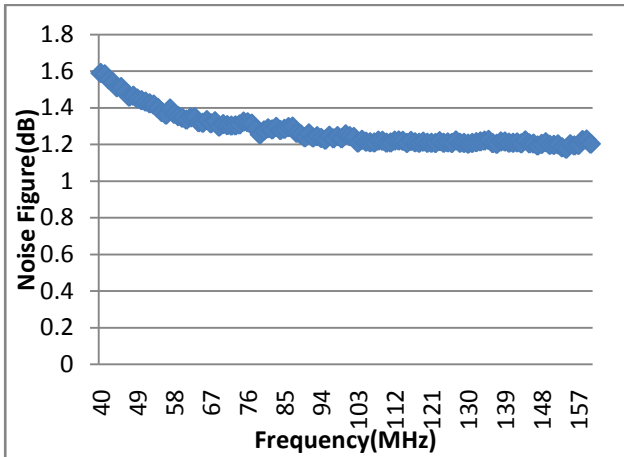


Figure 16 Noise Figure(NF)

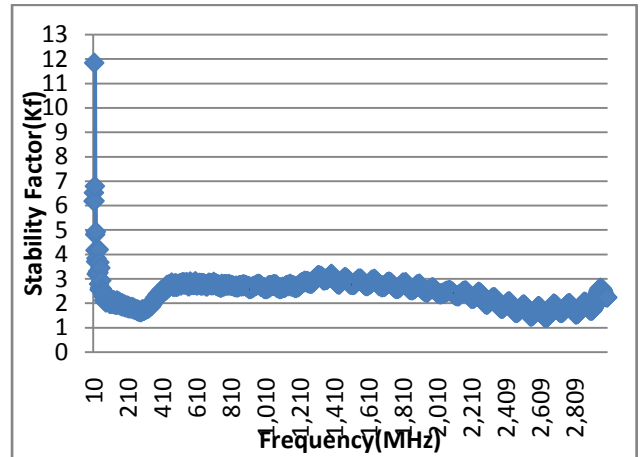


Figure 17 Stability Factor(K_f)

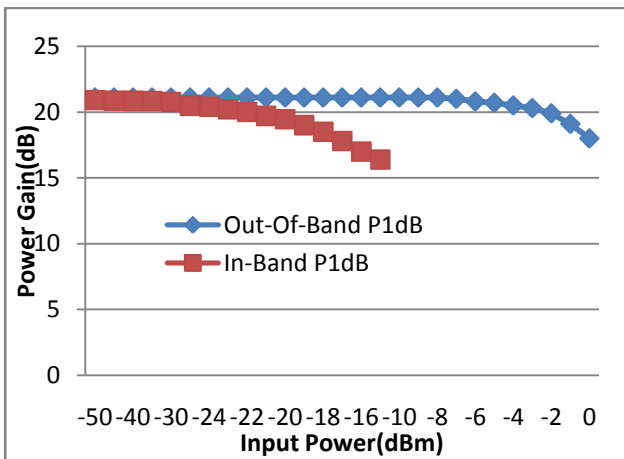


Figure 18 P1dB(In-Band/Out-Of-Band)

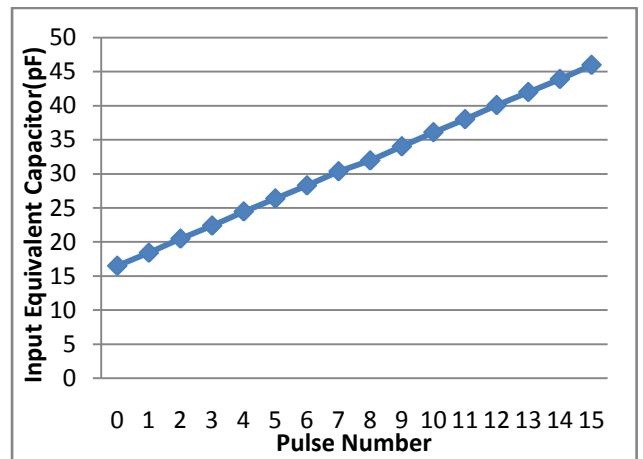


Figure 19 Tunable Capacitor(C_{in})

FUNCTIONAL BLOCK DIAGRAM

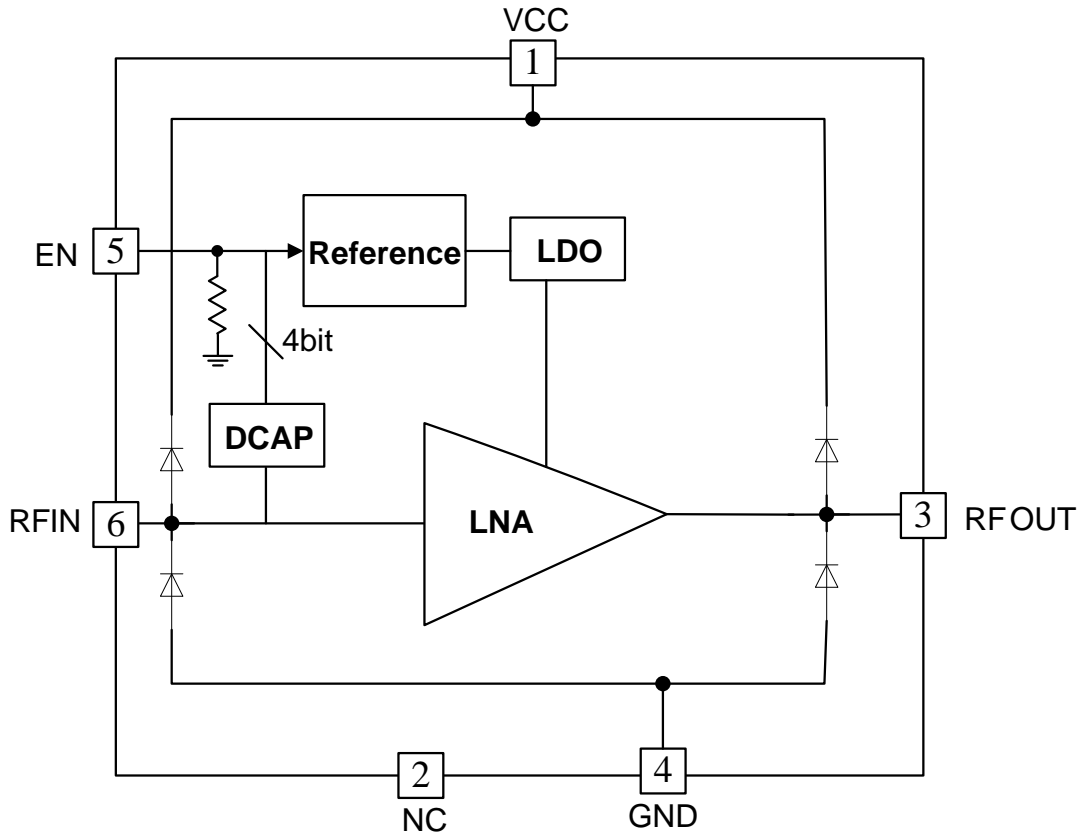


Figure 20 AW5017 FUNCTION BLOCK DIAGRAM

MEASUREMENT DIAGRAM

Test DC Characteristics (Current&Power)

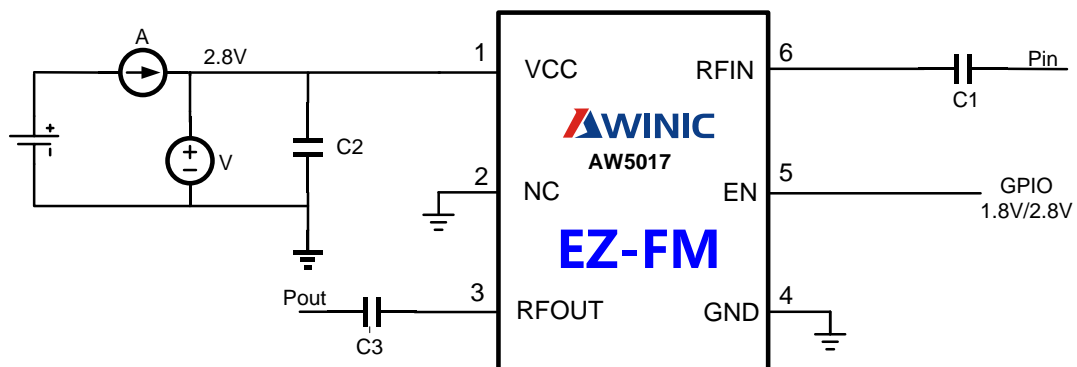


Figure 21 AW5017 DC Test diagram

Test S-parameter

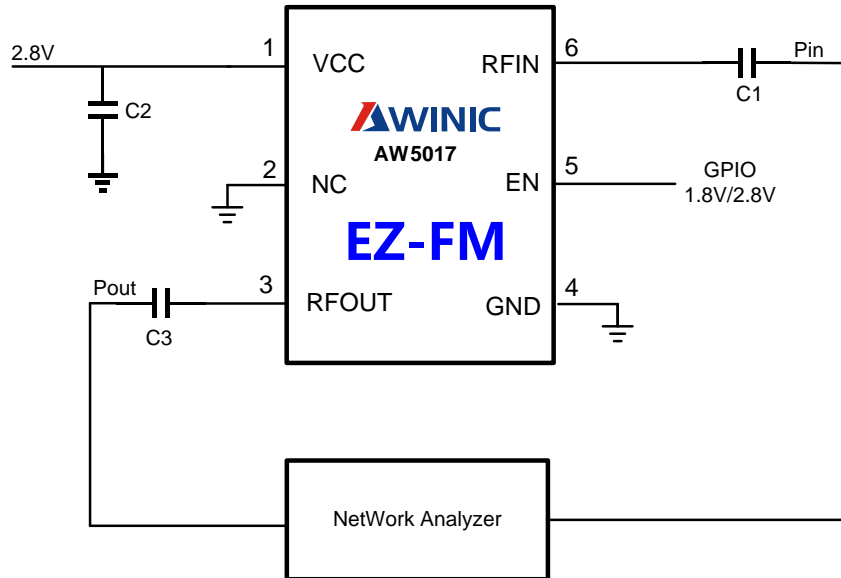


Figure 22 AW5017 S-parameter measurement Diagram

Test Noise-Figure

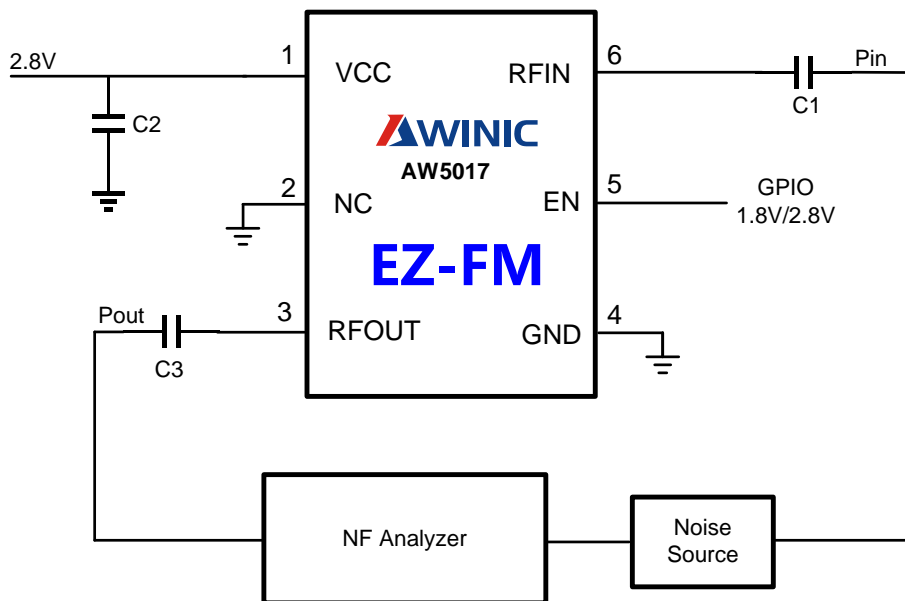


Figure 23 AW5017 Noise Figure Measurement Diagram

Test IIP3

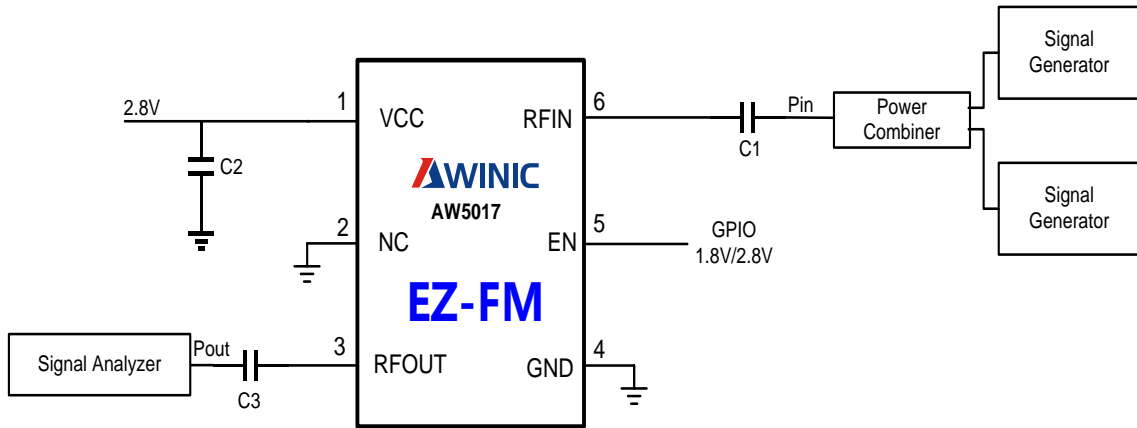


Figure 24 AW5017 IIP3 Measurement Diagram

Test Tunable Capacitor

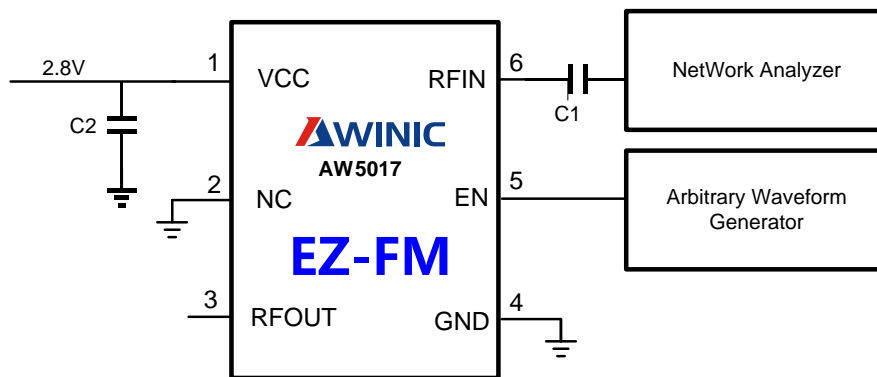


Figure 25 AW5017 Tunable Capacitor Measurement Diagram

APPLICATION INFORMATION

Choice of components

Take Figure 2 for example:

Filter block near PIFA antenna is composed of L6 and C3. These two components can be removed for Dipole antenna. Typical value of L6 is 68 nH and of C3 is 39 pF.

Filter block of FM signal is composed of C1 and L1. GSM signal could go through and FM signal will be blocked. GSM antenna π -type matching circuit is composed of C2, L3 and L4, adjustable based on GSM antenna characteristics. Typically C1 is 39 pF and L1 is 68 nH.

Matching circuit of FM signal path is composed of C4, L4, L5 and L7. FM signal could go through and GSM signal will be blocked. Typically L4 is 100 nH, L5 is 68 nH and L7 is 33 nH.

C5 is supply filtering capacitor. C6 is DC-blocking capacitor. Both are 47 nF typically.

Only when supporting earphone antenna application, C7 is added with the value of 47 nF.

Table 9 shows recommended inductor type and values. Table 10 shows recommended capacitor type and values.

Table 9 CHOICE OF INDUCTOR

PART No.	TYP.	Q(min)	Frequency	MFR	SIZE
LQG15HS33NJ02	33nH	8	100MHz	Murata	0402
LQG15HS68NJ02	68nH	8	100MHz		0402
LQG15HSR12J02	120nH	8	100MHz		0402
LQG15HSR10J02	100nH	8	100MHz		0402
SDCL1005C33NJTDF	33nH	8	100MHz	Sunlord	0402
SDCL1005C68NJTDF	68nH	8	100MHz		0402
SDCL1005CR12JTDF	120nH	8	100MHz		0402
SDCL1005CR10JTDF	100nH	8	100MHz		0402

Table 10 CHOICE OF INDUCTOR

PART No.	TYP.	Voltage	MFR	SIZE
GRM1555C1H220JA01	22pF	25V	Murata	0402
GRM1555C1H390JA01	39pF	25V		0402
GRM155R71C473KA01	47nF	16V		0402

EN Control

AW5017 supports earphone. When baseband detects earphone inserting, GPIO will pull down, cutting off AW5017 to avoid unnecessary power consumption.

When One-Line-Logic is enabled to change the capacitance of tunable capacitor to improve the voltage gain at the input port, based equivalent diagram is shown as figure 26.

In operation frequency band of FM, short antenna can be approximated to series of open induced voltage and equivalent inductor. Therefore, through tuning capacitance value in input port, the voltage gain can be achieved in specified frequency. Meanwhile the receiver performance will be improved.

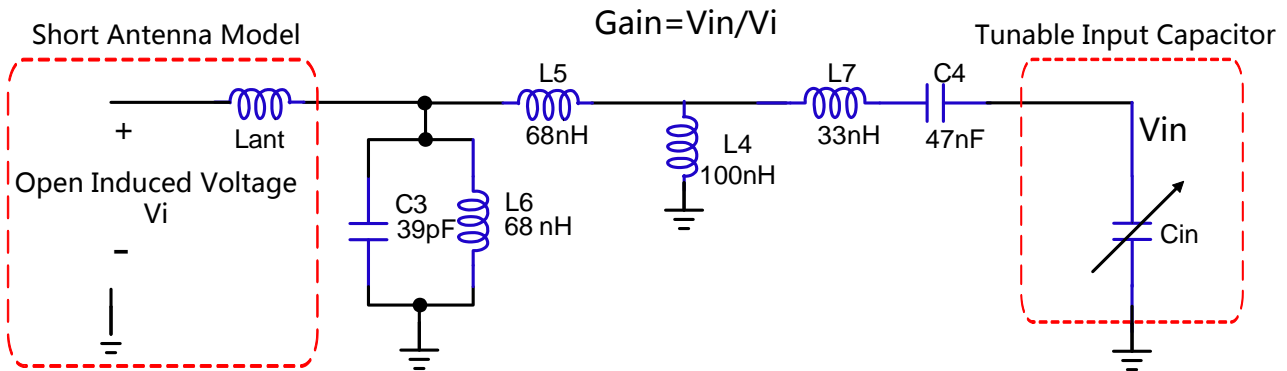


Figure 26 AW5017 Frequency Tuning Equivalent Schematic

In schematic, the value of tunable capacitor will be derived as following. f_{boost} is FM operation frequency, L_{eqq} is equivalent inductance of input port towards antenna side, which depends on the type and size of short antenna, C_{in} is tunable capacitance of input port.

$$f_{boost} = \frac{1}{2 * \pi * \sqrt{L_{eqq} * C_{in}}} \text{ (Hz)}$$

Figure 27 shows an example of voltage gain influenced by tunable capacitor. Blue and red curves are voltage gain (equal to input voltage / open induced voltage) with maximum and minimum tunable capacitor, respectively. The equivalent inductance of short antenna is 150nH.

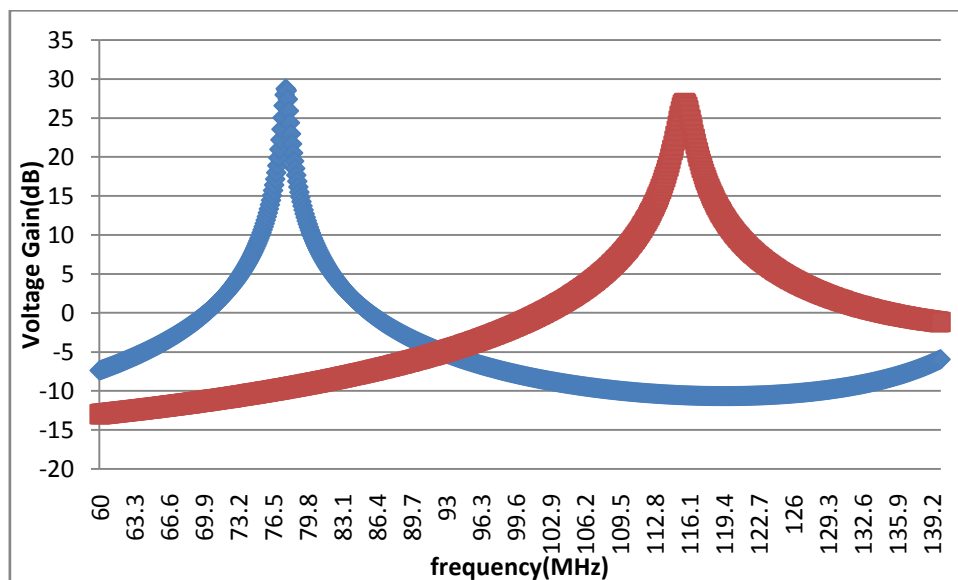
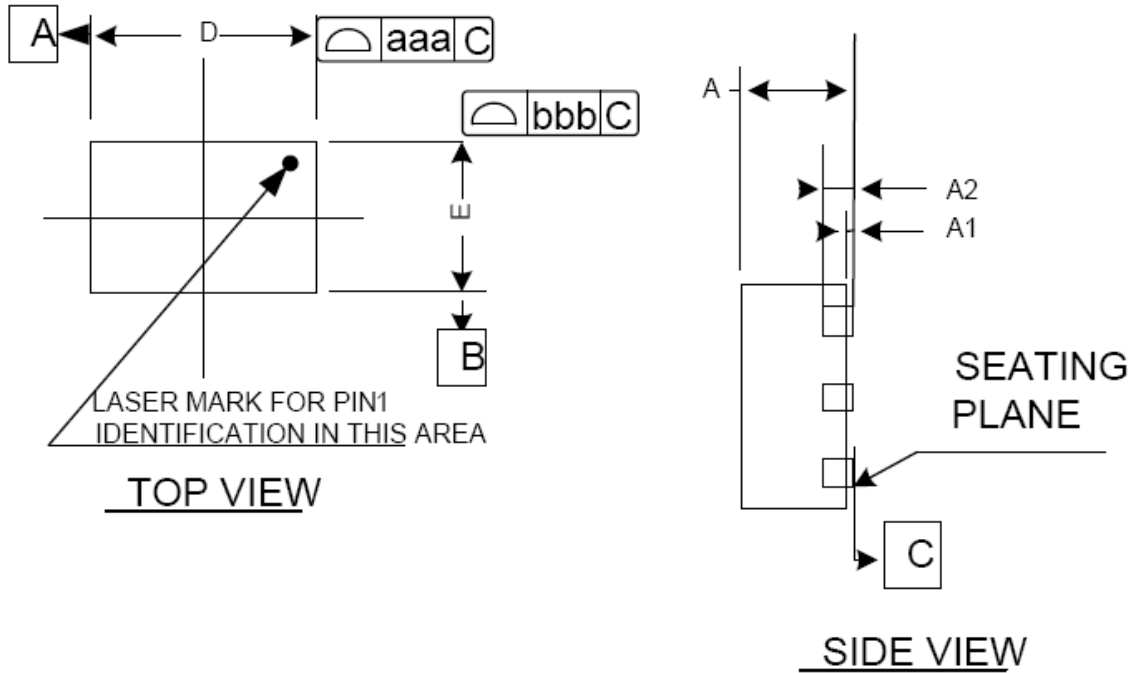


Figure 27 Voltage Gain with Different Tunable Capacitor

PACKAGE DESCRIPTION



* CONTROLLING DIEMENSIONMM

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.02	0.022	0.024
A1	---	---	0.05	---	---	0.002
A2	0.152REF			0.006REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.50 ^{bsc}			0.060 ^{bsc}		
E	1.00 ^{bsc}			0.040 ^{bsc}		
E2	1.000REF			0.040REF		
L	0.30	0.35	0.40	0.012	0.014	0.016
L2	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 ^{bsc}			0.020 ^{bsc}		
TOLERANCES OF FORM AND POSITION						
aaa	0.05			0.002		
bbb	0.05			0.002		

Figure 28 Package outline

TAPE&REEL DESCRIPTION

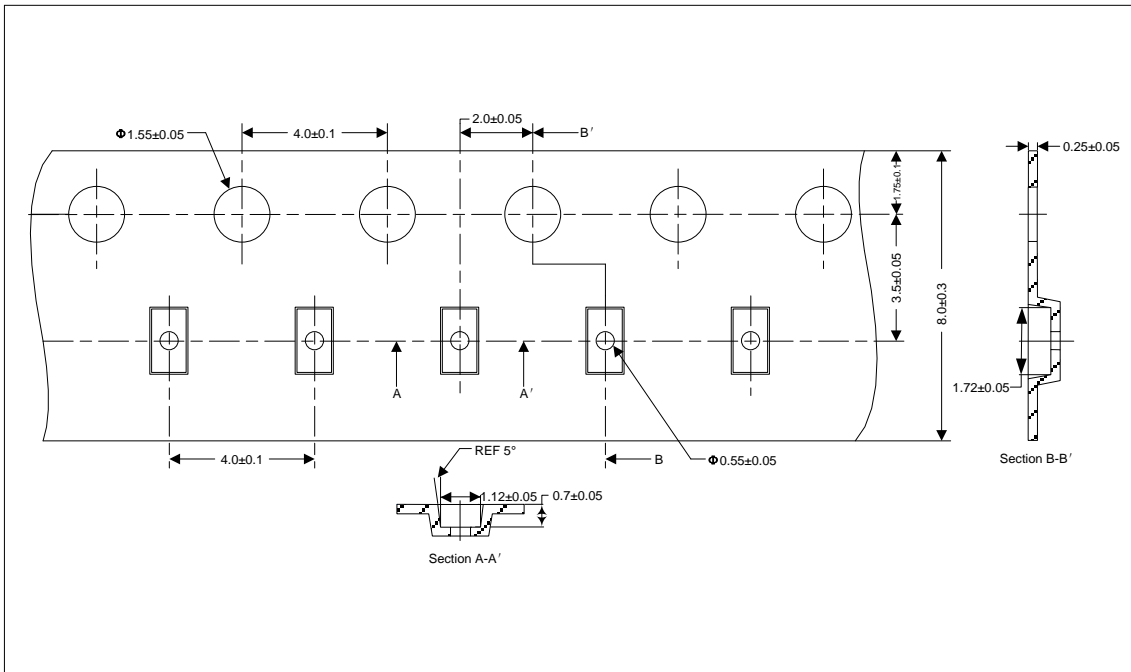


Figure 29. Tape and Reel

REVISION HISTORY

Table 11. Revision history

Document ID	Release date	Change notice	Supersedes
AW5017_V1.2	2016-01	Added Tape & Reel Description and corrected the marking location of Pin1	AW5017_V1.1
AW5017_V1.1	2015-12	Modified Marking A into B	AW5017_V1.0
AW5017_V1.0	2015-11	Added matching capacitor C10	AW5017_V0.9
AW5017_V0.9	2014-12	Preliminary data sheet	-

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