

BDS/GPS/GNSS INTEGRATED FRONT-END MODULE WITH LOW NOISE AMPLIFIER AND FILTER

FEATURES

- Low Noise Figure: 1.7dB;
- High power gain: 17dB typical @ 1.575 GHz
- Low current consumption: 6.9mA
- RF input/output impedance 50ohm
- Supply voltage: 1.5V-3.6V
- Operation frequency range: 1550MHz-1615MHz
- Small DFN (6-pin, 1.5mm x 1.0 mm) package
- 3kV HBM ESD protection (including RFIN and RFOUT pin)
- High Out-Of-Band jammer rejection at Cellular/PCS/WLAN bands
- Fully-integrated module without any component at input/output side

APPLICATIONS

- Small phones, Feature Phones;
- Tablet PCs;
- Personal Navigation Devices;
- Complete GPS/BDS chipset modules;
- Theft protection(laptop, ATM)
- Smart watch and other mobile devices

TYPICAL APPLICATION CIRCUIT

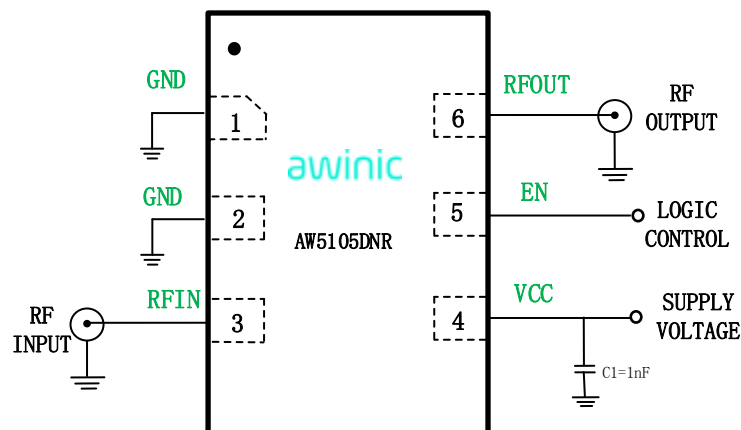


Figure 1 Typical Application Circuit of AW5105

GENERAL DESCRIPTION

The AW5105 is a Front-End Module (FEM) with a fully integrated Low-Noise Amplifier and Pre-Filter for BDS/GPS/GNSS. The AW5105 requires no external capacitor/inductor, reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The AW5105 achieves low noise figure, high gain, excellent linearity and high Out-Of-Band rejection. All these feature make AW5105 an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against out-of-band jammer signals with high linearity, and reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.

The AW5105 is provided in a compact 1.5mm x 1.0mm, 6-pin DFN package.

PIN CONFIGURATION AND TOP MARK

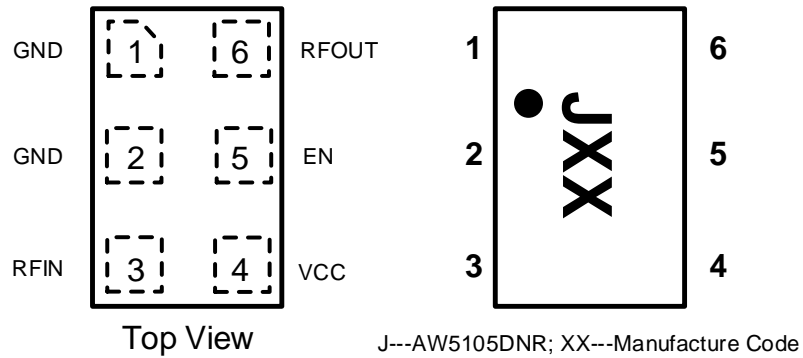


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	GND
2	GND	GND
3	RFIN	RF INPUT
4	VCC	DC power supply
5	EN	Logic Control
6	RFOUT	RF OUTPUT

FUNCTIONAL BLOCK DIAGRAM

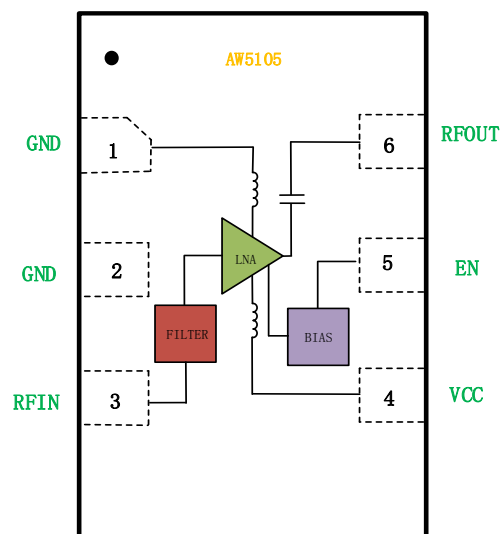
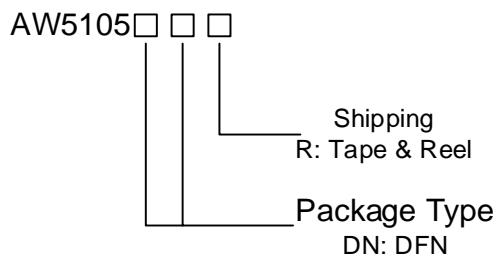


Figure 3 FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW5105DNR	-40°C~85°C	1.5mm x 1.0mm x 0.55mm DFN-6L	JXX	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS^(NOTE1)

PARAMETERS	RANGE
Supply Voltage VCC	-0.3 V to 4.2 V
EN pin voltage	-0.3 V to 4.2 V
Supply maximum current ICC	30 mA
RFIN input power Pin	20 dBm
Maximum Junction temperature T _{JMAX}	125 °C
Storage temperature T _{STG}	-65 °C to 150 °C
Operating free-air temperature range	-40 °C to 85 °C
Lead Temperature (Soldering 10 Seconds)	260 °C
ESD ^(NOTE 2)	
HBM	±3kV
CDM	±1kV

ELECTRICAL CHARACTERISTICS

TA=25 °C, VCC=1.8 V, EN=1.8 V, Rs=Ro=50 ohm, frequency=1575.42 MHz for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
VCC	Supply Voltage		1.5	1.8	3.6	V
ISD	Shut-down Current	EN=Low		0.1	1	μA
IQ	Static Current	EN=2.8V		6.7		mA
VEN	Digital Input Logic High		1			V
VEN	Digital Input Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
GP	Power Gain			16.5		dB
NF	Noise Figure	Input/Output 50ohm		1.7		dB
S11	Input Return Loss	Input/Output 50ohm		-5		dB
S22	Output Return Loss	Input/Output 50ohm		-15		dB
Kf	Stability Factor	Input/Output 50ohm	1.0			
IB P-1dB	In-Band 1dB-compression point	Input/Output 50ohm		-9.2		dBm
IIP3 OOB	Out of band input 3 rd order intercept point	f1=1712.7MHz f2=1850MHz Pin=-20dBm		-0.8		dBm
IIP3 OOB	Out of band input 3 rd order intercept point	f1=1712.7MHz f2=1850MHz Pin=-30dBm		-0.5		dBm
IIP2	Out of band input 2 nd order intercept point			6.2		dBm
FREQUENCY RESPONSE CHARACTERISTICS						
PG ripple	Power Gain Ripple	f=1.57542GHz ± 0.1MHz		0.1		dB
ATT	Attenuation	f=DC~1GHz	20	25		dBc
ATT	Attenuation	f=2.4~3GHz	10	15		dBc

TA=25 °C, VCC=2.8 V, EN=2.8 V, Rs=Ro=50 ohm, frequency=1575.42MHz for typical values (unless otherwise noted).

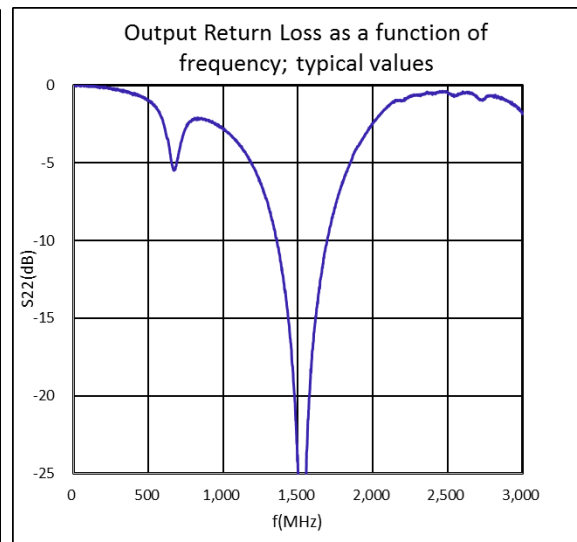
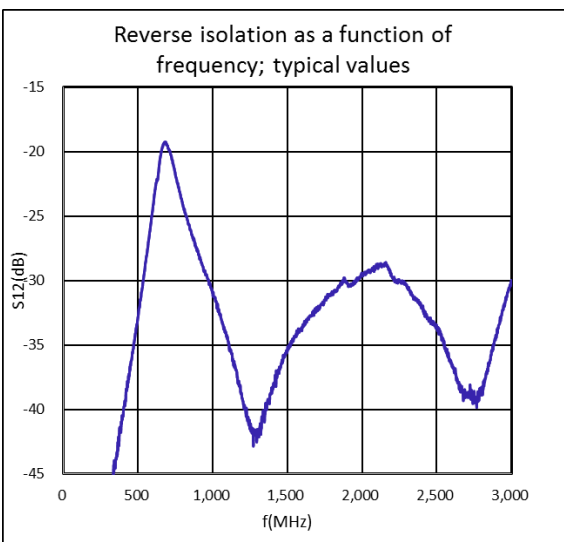
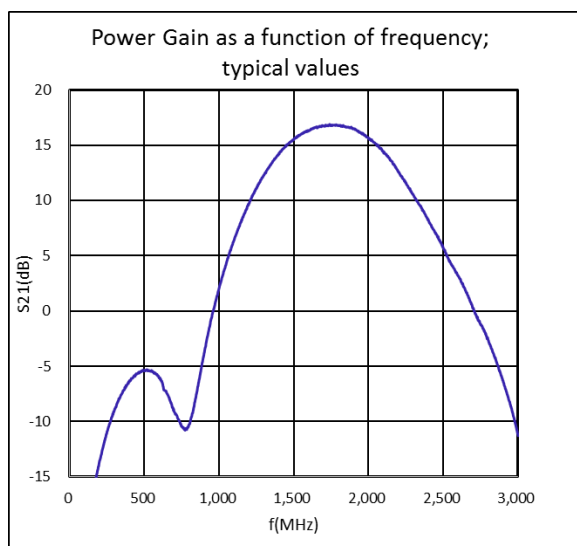
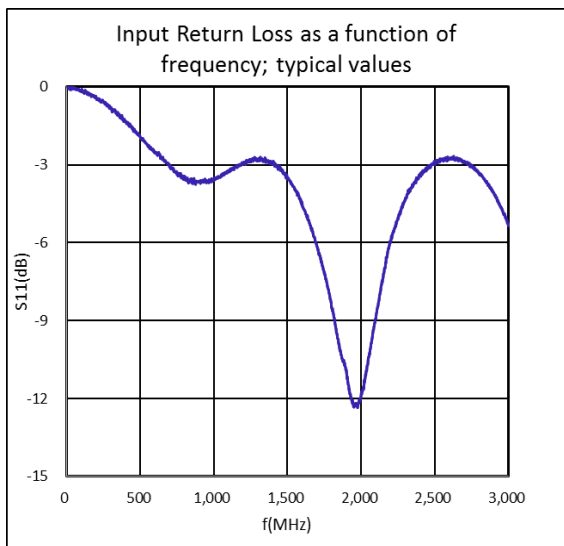
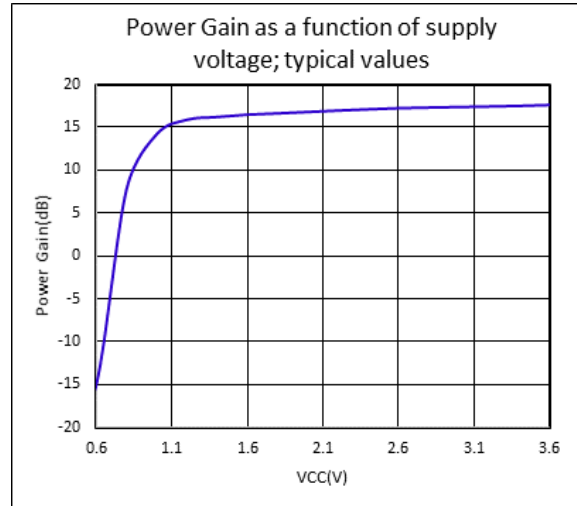
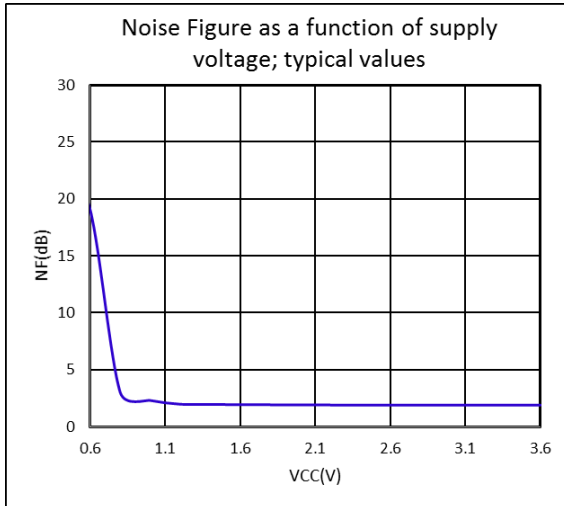
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
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VCC	Supply Voltage		1.5	2.8	3.6	V
ISD	Shut-down Current	EN=Low		0.1	1	μA
IQ	Static Current	EN=2.8V		8.8		mA
VEN	Digital Input Logic High		1			V
VEN	Digital Input Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
GP	Power Gain			17		dB
NF	Noise Figure	Input/Output 50ohm		1.7		dB
S11	Input Return Loss	Input/Output 50ohm		-5		dB
S22	Output Return Loss	Input/Output 50ohm		-15		dB
Kf	Stability Factor	Input/Output 50ohm	1.0			
IB P-1dB	In-Band 1dB-compression point	Input/Output 50ohm		-7		dBm
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IIP3 OOB	Out of band input 3 rd order intercept point	f1=1712.7MHz f2=1850MHz Pin=-30dBm		0.7		dBm
IIP2	Out of band input 2 nd order intercept point			8.5		dBm
FREQUENCY RESPONSE CHARACTERISTICS						
PG ripple	Power Gain Ripple	f=1.57542GHz±0.1MHz		0.1		dB
ATT	Attenuation	f=DC~1GHz	20	25		dBc
ATT	Attenuation	f=2.4~3GHz	10	15		dBc

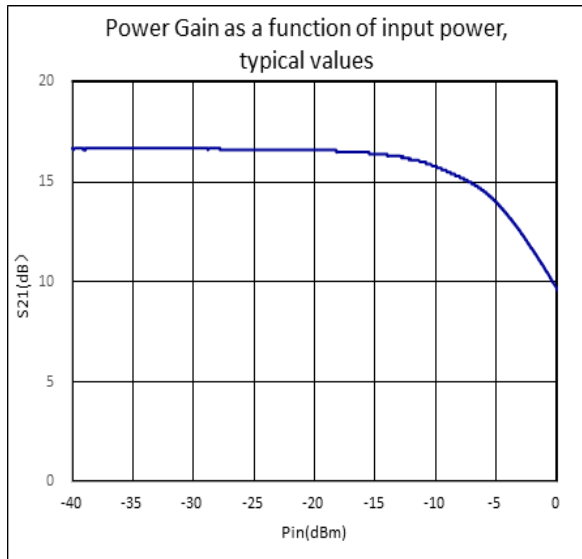
NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7

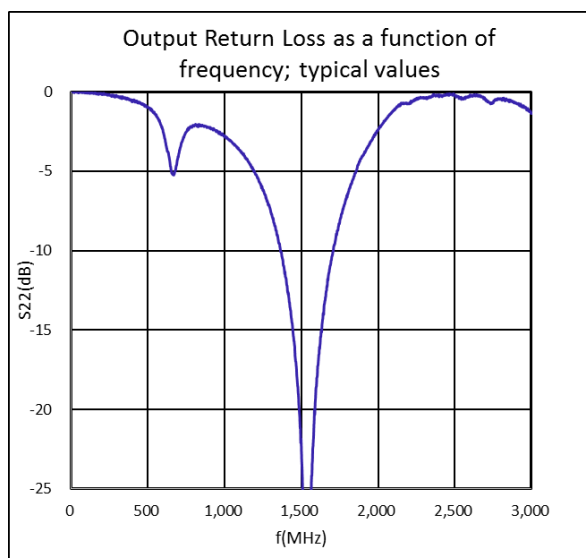
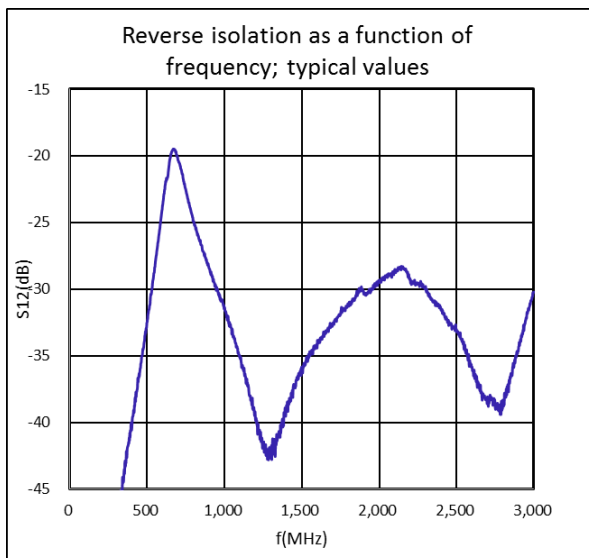
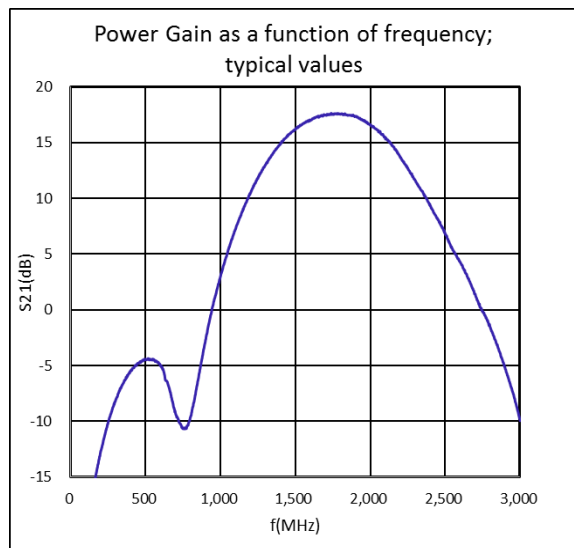
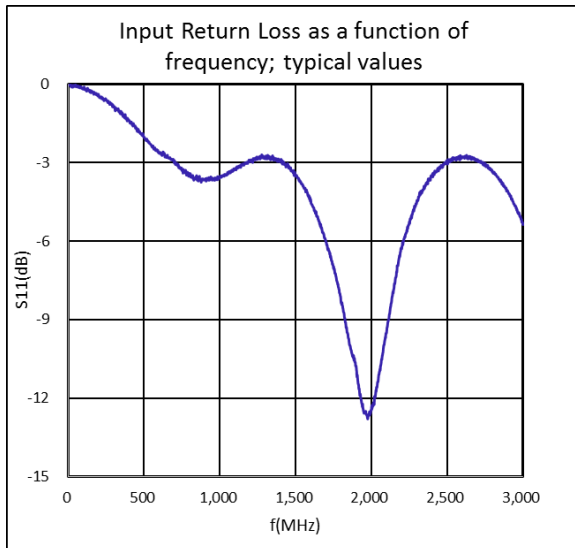
TYPICAL CHARACTERISTICS

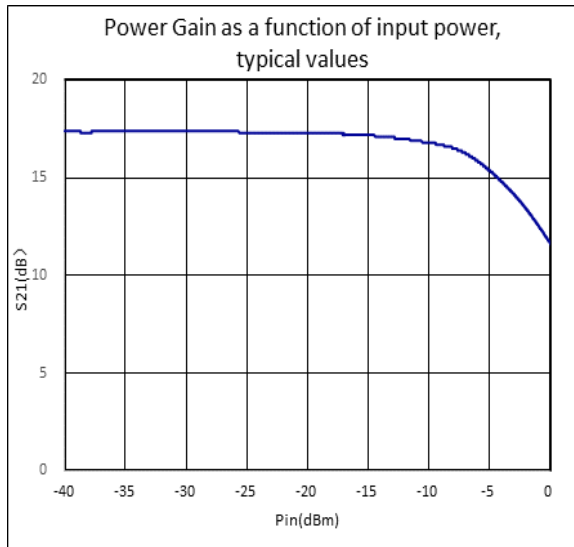
TA=25 °C, VCC=1.8 V, EN=1.8 V, Rs=Ro=50 ohm, for typical values (unless otherwise noted).





TA=25 °C, VCC=2.8 V, EN=2.8 V, Rs=Ro=50 ohm, for typical values (unless otherwise noted).





AW5105 APPLICATION BOARD

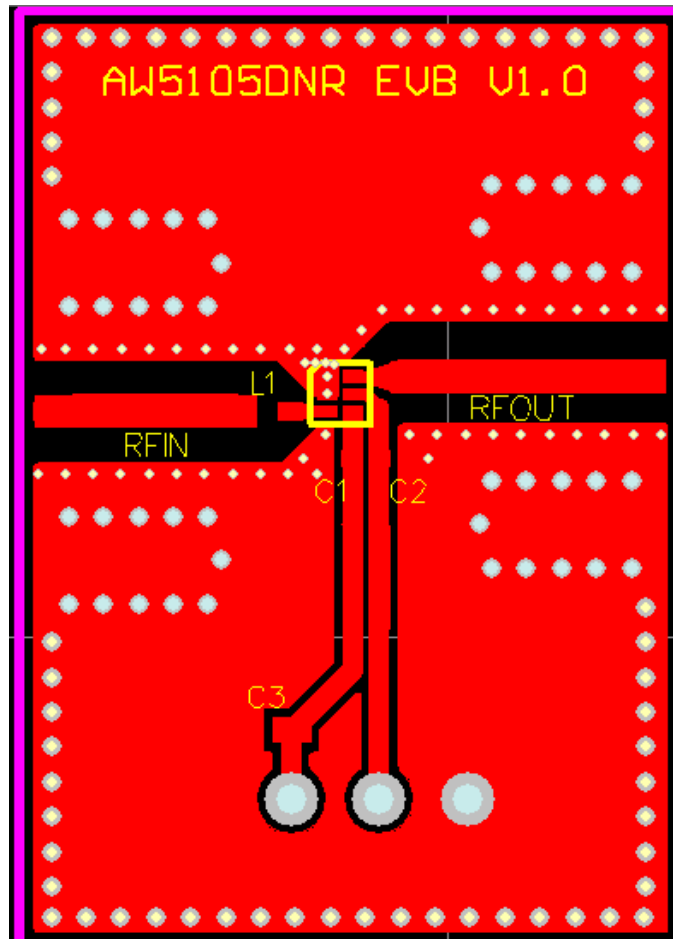


Figure 4 Drawing of Application Board

TEST CIRCUITS

Test DC Characteristics (Current&Power)

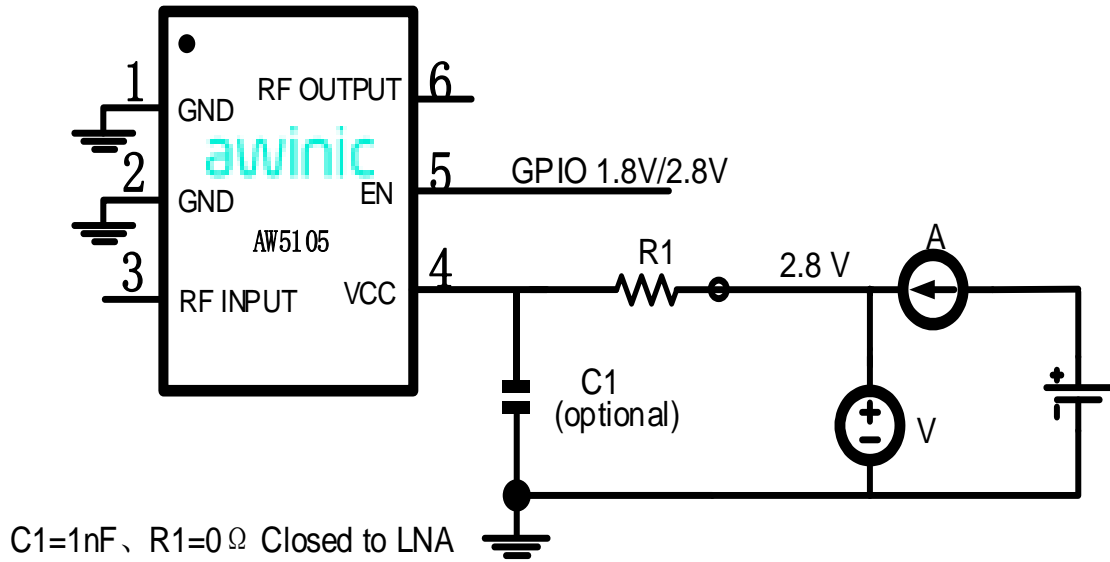


Figure5 Circuit for DC test

Test S-parameter

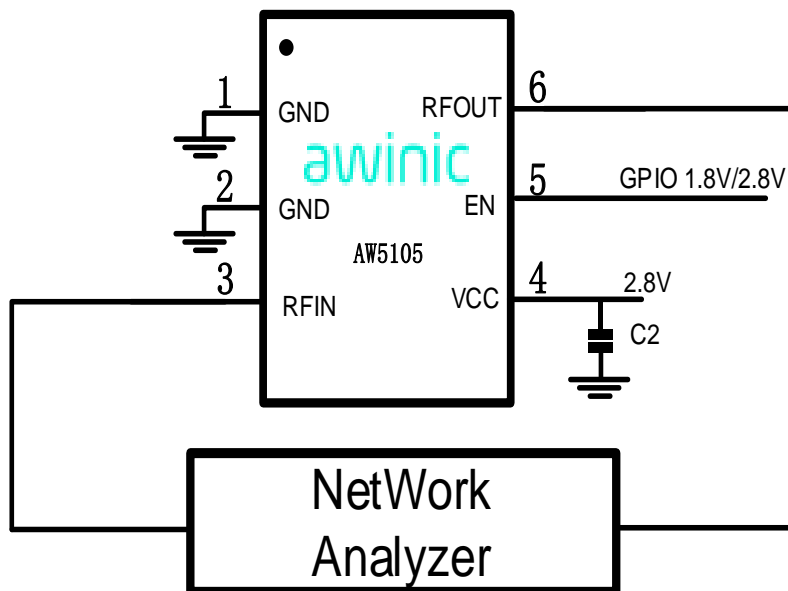


Figure6 Circuit for S Parameter test

Test Noise-Figure

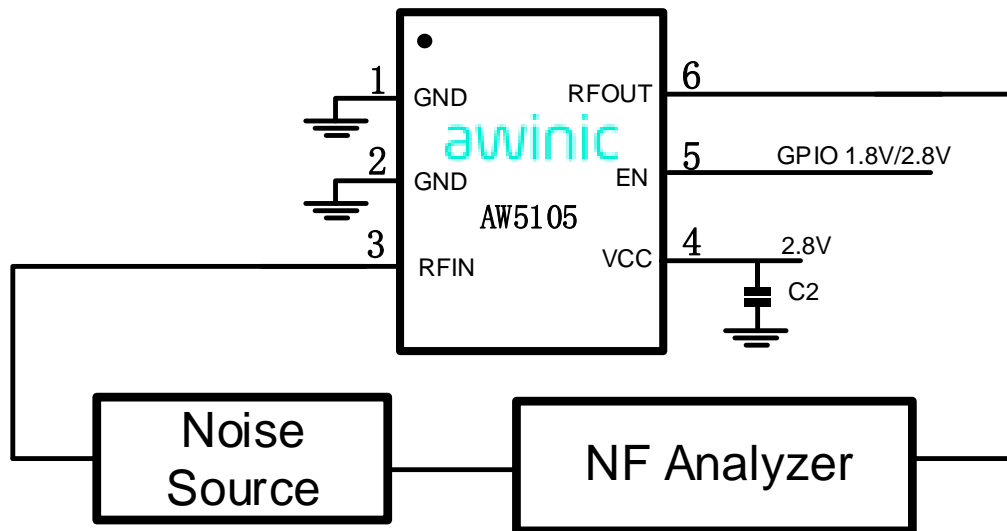


Figure7 Circuit for Noise Figure test

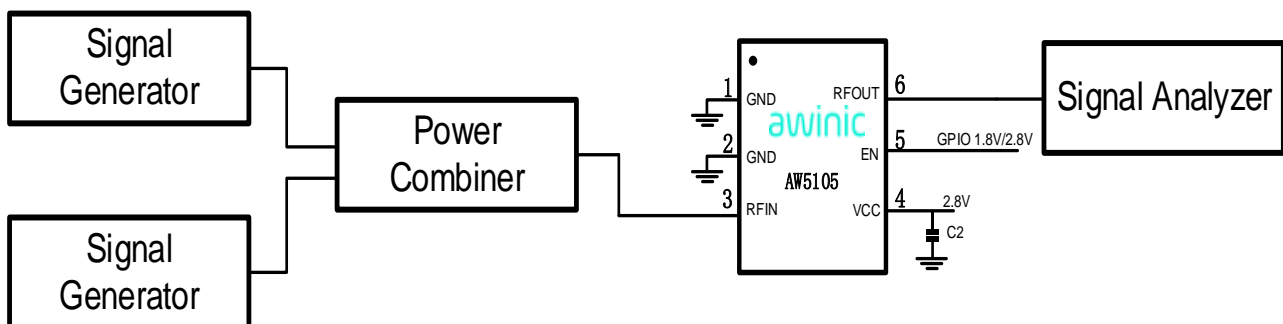
Test IIP3

Figure8 Circuit for intermodulation distortion test

APPLICATION INFORMATIONS

Choice of components

Take Figure 1 for example:

The AW5105 includes an internal switch to turn off the entire chip: apply logic high to EN to turn on, and a logic low to shut down.

The output of AW5105 is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.

The AW5105 should be placed close to the GPS antenna. Use 50-ohm microstrip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor should be located close to the device. For long Vcc lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

CHOICE OF CAPACITOR

Part Number	Capacitance	Rated Voltage	Supplier	Size
Units	pF	V		
GRM155	1000	50	Murata	0402

PACKAGE INFORMATION

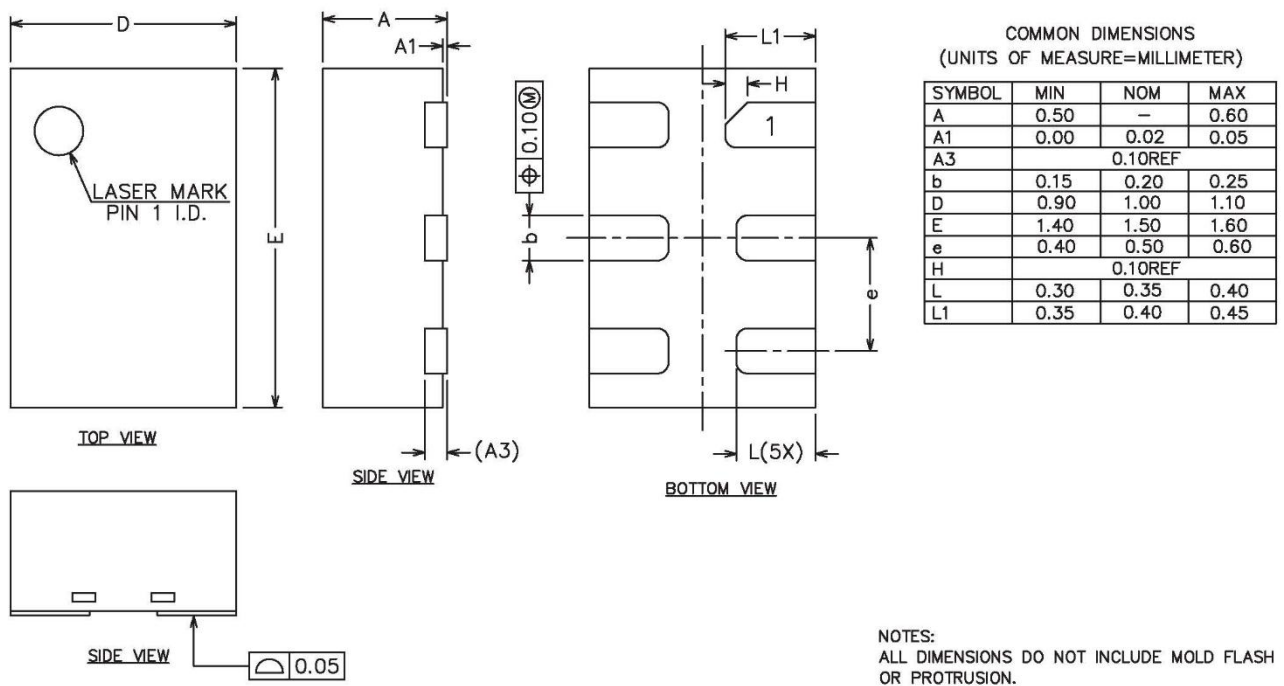
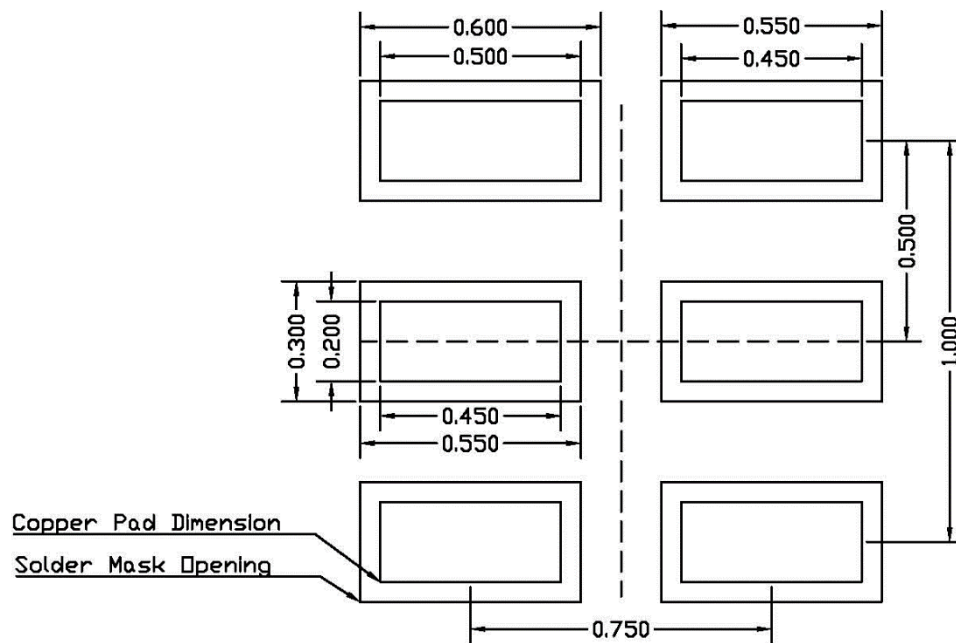


Figure 9 Package outline

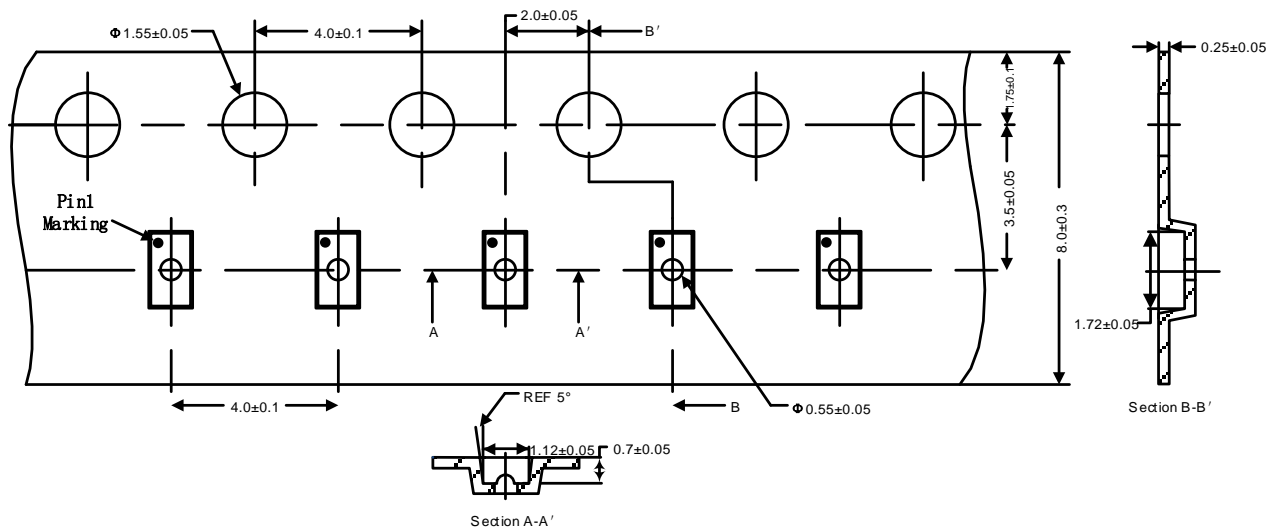
LAND PATTERN



Dimension are all In millimeters

Figure 10 Land Pattern

TAPE REEL DESCRIPTION



Notes:

1. 10 procket hole pitch cumulative tolerance ± 0.2
2. The meander of the tape is assumed with 1mm or less every 100mm between 250mm
3. MATERIAL: CONDUCTIVE POLYSTYRENE
4. ALL DIMS IN MM
5. There must not be foreign body adhesion and the state of the surface must be excellent
6. 17" PAPER-Reel, 125000 pockets (500m)
7. Surface resistance 1×10^{11} (max) OHMS/SQ

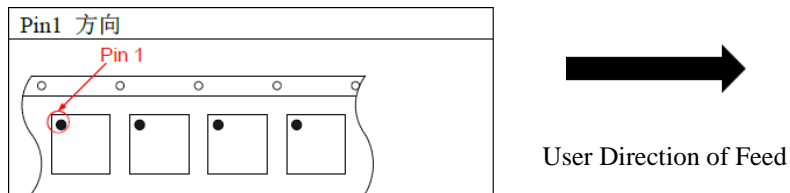


Figure 11 Tape Description

REEL DESCRIPTION

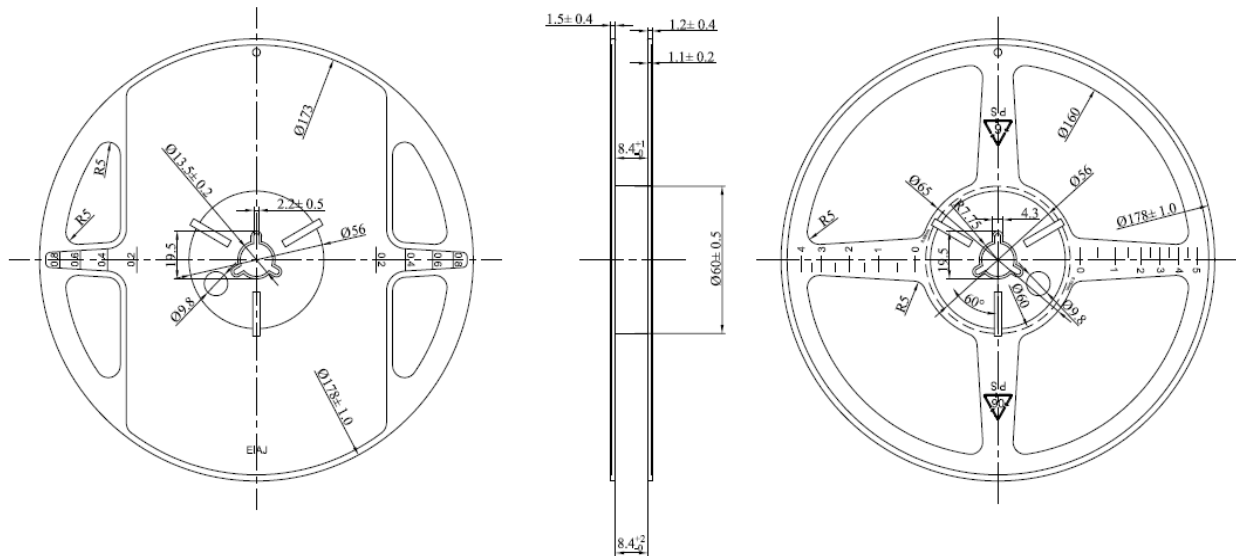


Figure 12 Reel Description

Note:

1. Material: polystyrene (black)
2. Planeness: max 3mm
3. Surface resistance: within 10E5~10E11 OHMS/SQ
4. All outstanding tolerance: $\pm 0.25\text{mm}$.
5. Dimensions are all in millimeters

REFLOW

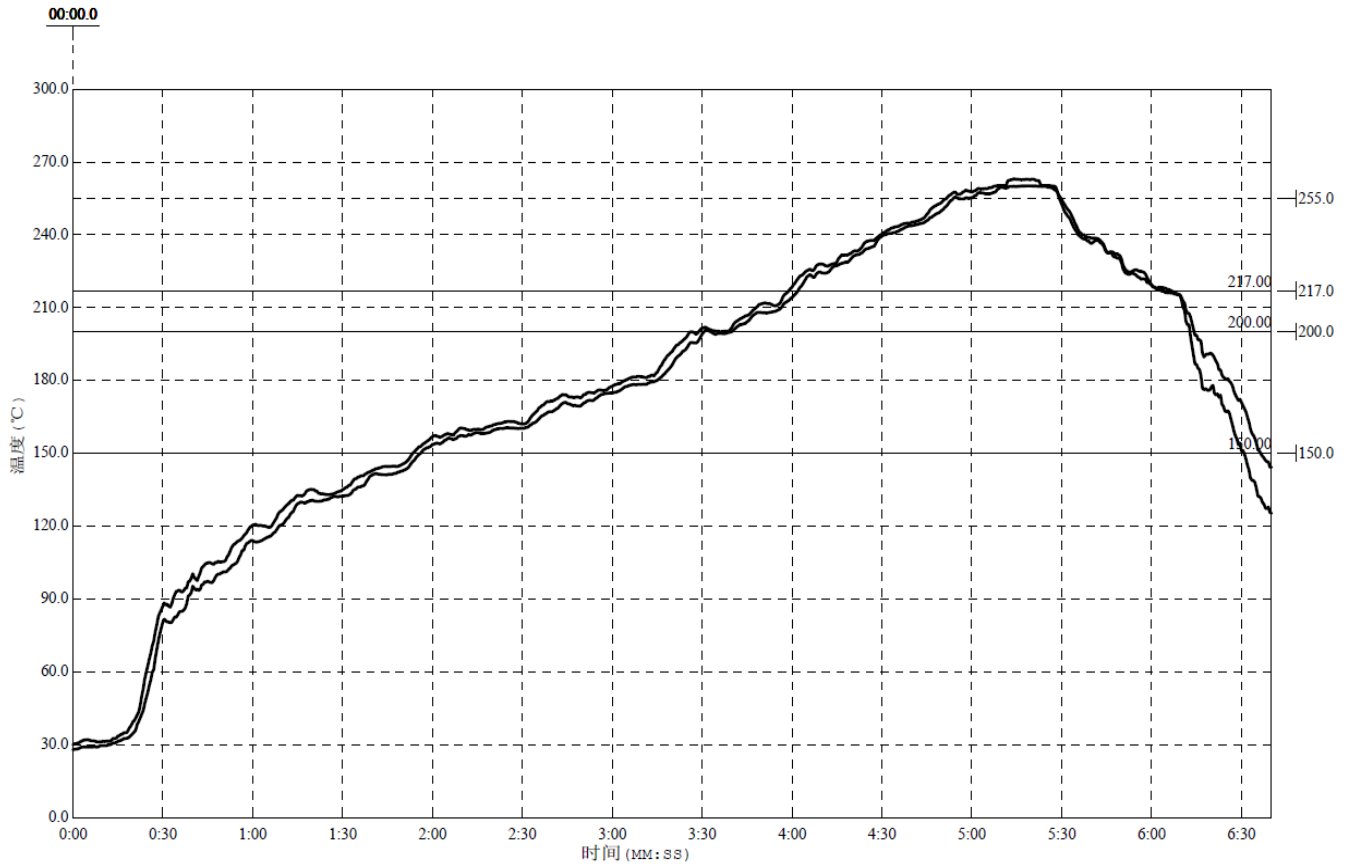


Figure 13 Package Reflow Oven Thermal Profile

Reflow Note	Spec
Average ramp-up rate (217°C to Peak)	Max. 3°C/sec
Time of Preheat temp.(from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec.
Ramp-down rate	Max. 6°C/sec
Time from 25°C to peak temp	Max. 8min.

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW5105DNR adopted the Pb-Free assembly.

REVISION HISTORY

Revision history

Document ID	Release date	Change notice	Supersedes
AW5105_V1.0	2018-01	Officially Released	--
AW5105_V1.1	2018-03	Update marking in diagram	--

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[AW5105DNR](#) [AW5005DNRZ](#) [AW8090ACOR](#) [AW36404DNR](#) [AW5008L1FDR](#) [AW87318CSR](#) [AW3206DNR](#) [AW9201QNR](#)
[AW36518FCR](#) [AW8110CSR](#) [AW8145CSR](#) [AW3643CSR](#) [AW5007ASTR](#) [AW8155FCR](#) [AW9962EDNR](#)