AW8623 Low Power F0 Detect and Tracking LRA/ERM Haptic Driver

FEATURES

- 1MHz I²C Bus Control (Address 0x5A)
- F0 detect option
- F0 tracking option
- Automatic Overdrive and Braking
- Resistance-Based LRA Diagnostics
- Drive signal monitor for LRA protect
- Drive Compensation Over Battery Discharge
- Integrated 8-KByte Internal Waveform Memory
- Up to 4-KByte configurable FIFO Interface
- Three playback mode:

  Real time playback, memory playback and hardware trigger playback
- Support automatically switch to standby mode
- Standby current：8μA
- Shutdown current：0.5μA
- 3V to 5.5V Supply Voltage Range
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection
- DFN 3X3-10L package

APPLICATIONS

- Tablets
- Wearable Devices

DESCRIPTION

AW8623 is a single chip, low cost H-bridge haptic driver IC that integrates configurable automatic overdrive and brake function, up to 8KB waveform memory, and supports real time playback, memory playback and hardware trigger playback with fast startup time. All these make it an ideal candidate for haptic driver.

The internal F0 detect function can trace the actual F0 frequency after LRA delivered to customs or after LRA mounted in the mobile, which can keep a strong vibration under all circumstances.

The software configurable automatic overdrive and brake process incorporating with the internal waveform memory and a variety of playback modes makes the control of complex haptic effects economical, simple and flexible.

AW8623 supplies Short Circuit Protection, Over-Temperature Protection and Under-Voltage Protection for robust operation.

AW8623 features configurable automatically switch to standby mode to help reduce power consumption. The RSTN pin provides further power saving by fully shut down the whole device. The dedicated interrupt output pin can detect real time FIFO status and the error status of the chip.

The AW8623 is available in DFN 3X3-10L package.

TYPICAL APPLICATION CIRCUIT

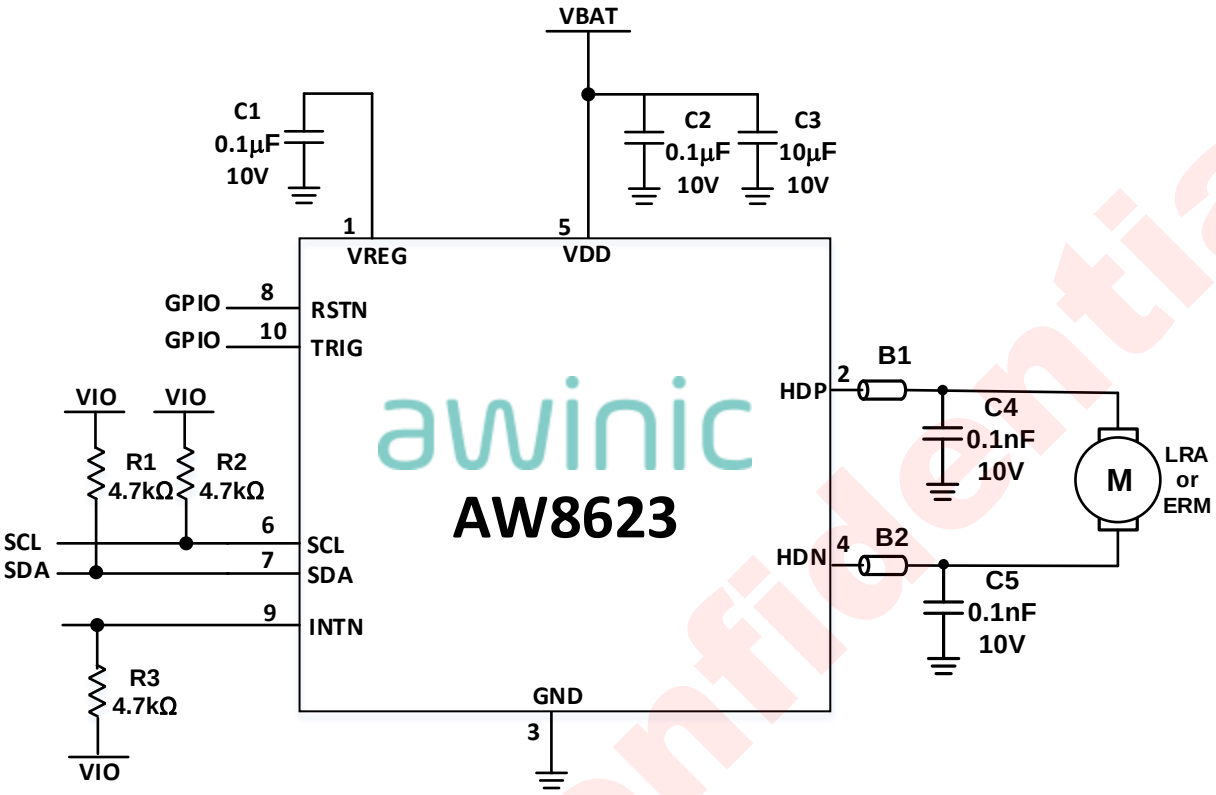

Figure 1 Typical Application Circuit of AW8623

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Notice for Typical Application Circuits:

1. Please place C_1, C_2, C_3 as close to the chip as possible. The capacitors should be placed in the same layer with the AW8623 chip.

2. For the sake of driving capability, the power lines (especially the one to Pin 5) and output lines should be short and wide as possible.

PIN CONFIGURATION AND TOP MARK

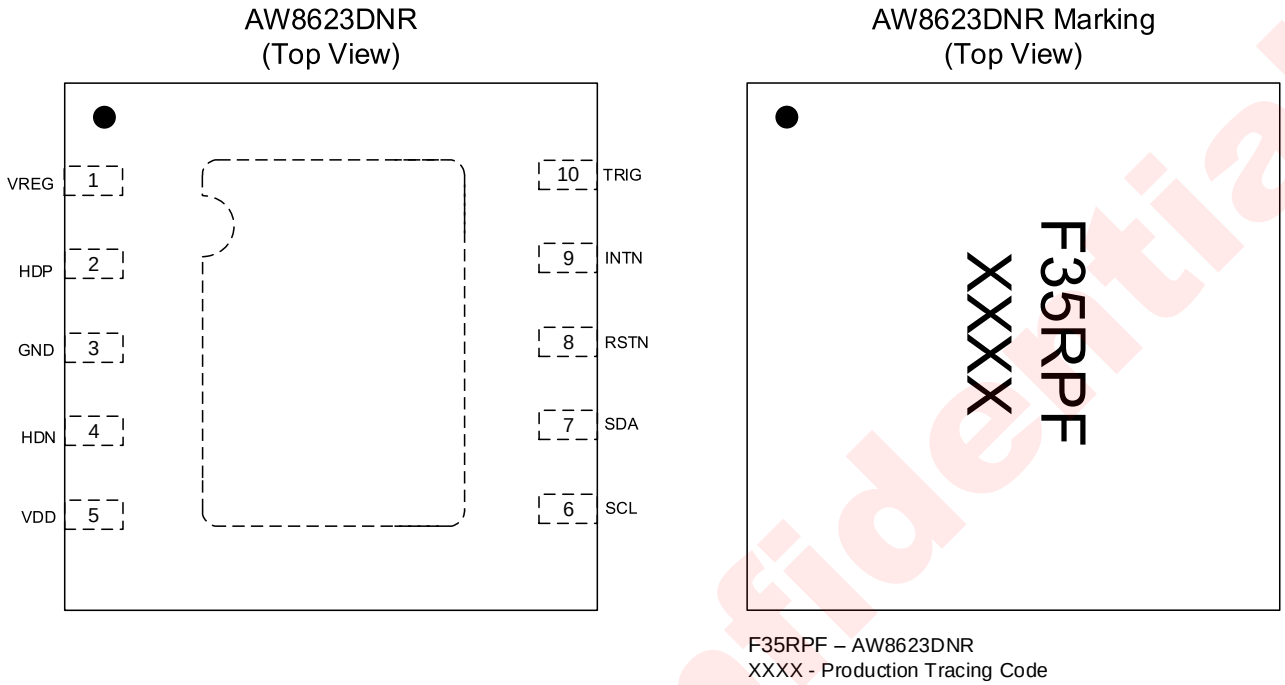


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

NAME	No.	DESCRIPTION
VREG	1	1.8V regulator output
HDP	2	Positive haptic driver differential output
GND	3	Supply ground
HDN	4	Negative haptic driver differential output
VDD	5	Chip power supply
SCL	6	I2C bus clock input
SDA	7	I2C bus data input/output
RSTN	8	Active low hardware reset, when low, shutdown chip
INTN	9	output interrupt, open drain
TRIG	10	Input trigger, internal pull down

FUNCTIONAL BLOCK DIAGRAM

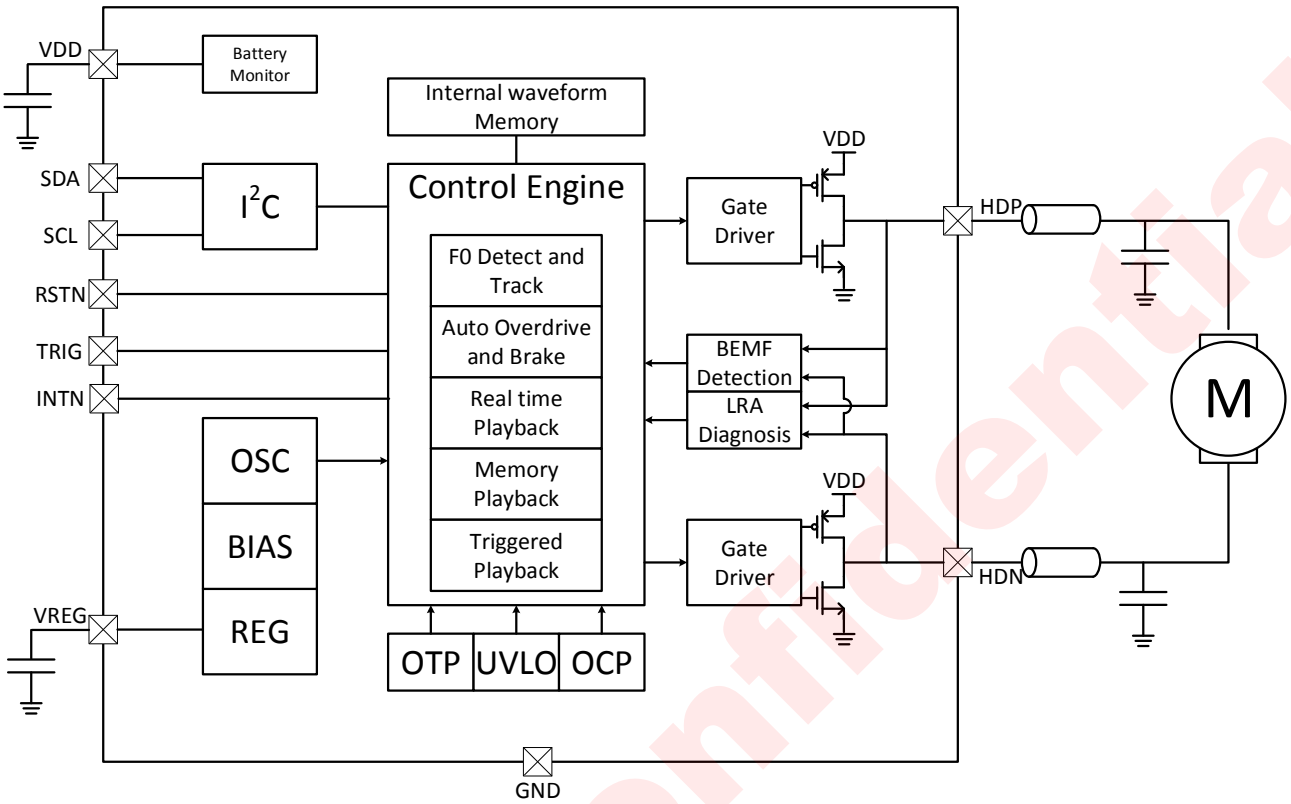
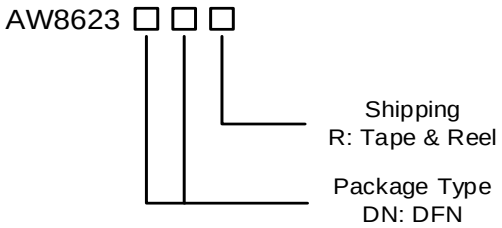


Figure 3 FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environment Information	Delivery Form
AW8623DNR	-40°C ~ 85°C	DFN 3X3-10L	F35RPF	MSL3	ROHS+HF	6000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS(NOTE1)

Parameter	Range
Battery Supply Voltage VDD	-0.3V to 6.0V
HDP, HDN	-0.3V to VDD+0.3V
Minimum load resistance R_L	5Ω
Package Thermal Resistance θ_{JA}	60°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (NOTE 2 3)	
HBM（Human Body Model）	±2000V
CDM(Charge Device Model)	±1500V
Latch-up	
Test Condition: JEDEC STANDARD NO.78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 2：The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001.

NOTE 3：Charge Device Model test method: JESD22-C101.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition: TA=25°C，VDD=3.6V，RL=8Ω+100μH

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
VDD	Battery supply voltage	On pin VDD	3		5.5	V
VREG	Voltage at VREG pin			1.8		V
V_{IL}	Logic input low level	RSTN/TRIG/SCLK			0.5	V
V_{IH}	Logic input high level	RSTN/TRIG/SCLK	1.3			V
V_{OL}	Logic output low level	INTN/SDA I_{OUT}=4mA			0.4	V
V_{OH}	Logic output high level	INTN/SDA I_{OUT}=-4mA	1.3			V
V_{OS}	Output offset voltage	I^2C signal input 0	-30	0	30	mV
I_{SD}	Shutdown current	VDD=4.2V, RSTN =0V		0.5	1	μA
I_{STBY}	Standby current	VDD=3.6V RSTN=SCL=SDA=1.8V		10		μA
I_Q	Quiescent current	VDD=3.6V		1		mA
UVP	Under-voltage protection voltage			2.7		V
	Under-voltage protection hysteresis voltage			100		mV
T_{SD}	Over temperature protection threshold			160		°C
T_{SDR}	Over temperature protection recovery threshold			130		°C
T_{START}	Waveform startup time	From trigger to output signal		0.4		ms
HDRIVER						
R_{dson}	Drain-Source on-state resistance	Include NMOS and PMOS		400		mΩ
R_{ocp}	Load impedance threshold for over current protection	VDD=3.6V		2		Ω
$F_{o(PWM)}$	PWM Output Frequency	VDD=3V to 5.5V	-2.5%	24	+2.5%	kHz
V_{peak}	Output voltage	RL=8Ω+100μH, VDD=4.2V		3.6		V
	Output voltage	RL=16Ω+100μH, VDD=4.2V		3.8		V

I²C INTERFACE TIMING

Parameter			Super-fast mode			UNIT
No.	Symbol	Name	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			1000	kHz
2	t_{LOW}	SCL Low level Duration	0.5			μs
3	t_{HIGH}	SCL High level Duration	0.3			μs
4	t_{RISE}	SCL, SDA rise time			0.1	μs
5	t_{FALL}	SCL, SDA fall time			0.1	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.3			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.3			μs
9	t_{BUF}	the Bus idle time START state to STOP state	0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

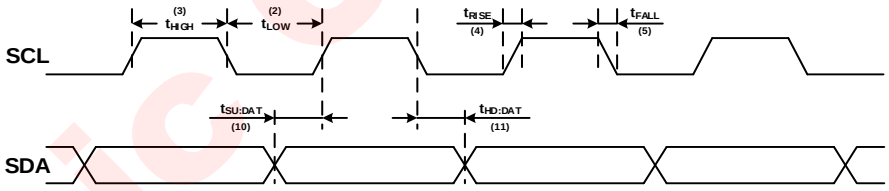


Figure 4 SCL and SDA timing relationships in the data transmission process

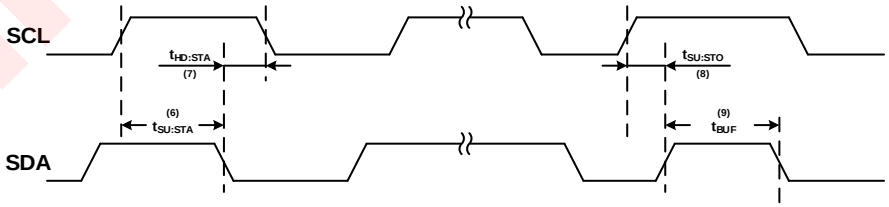


Figure 5 The timing relationship between START and STOP state

MEASUREMENT SETUP

AW8623 features switching digital output, as shown in Figure 6. Need to connect a low pass filter to HDP/HDN output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

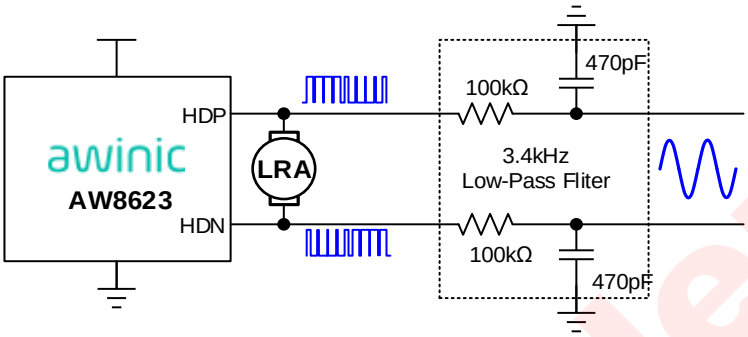
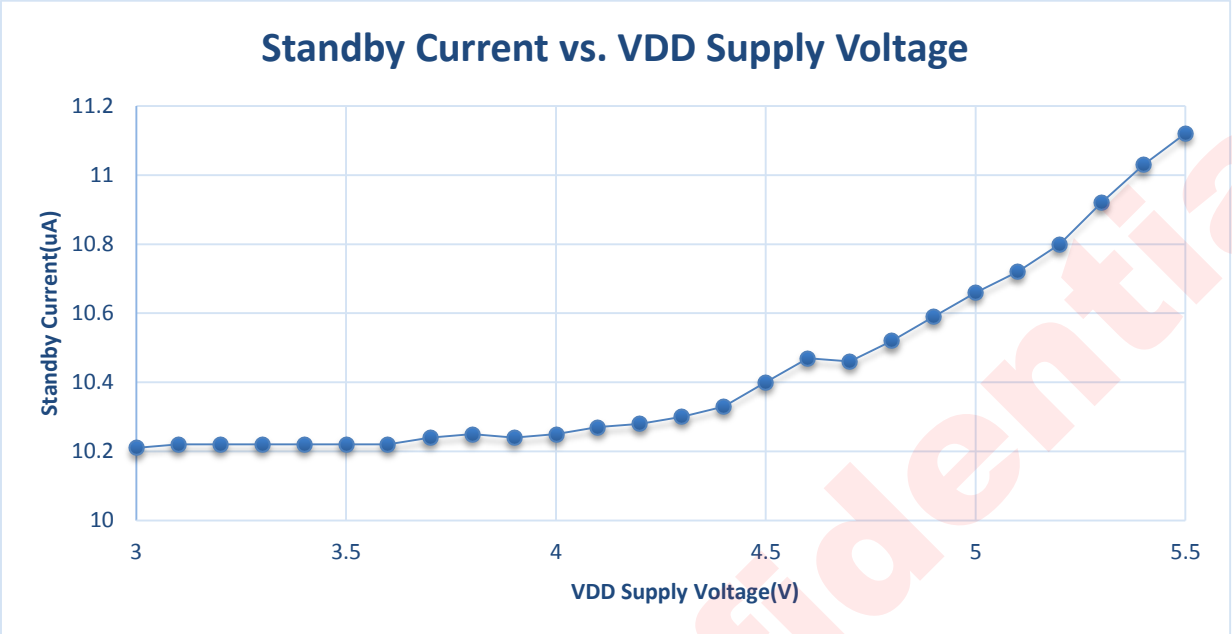


Figure 6 AW8623 test setup

TYPICAL CHARACTERISTICS



DETAILED FUNCTIONAL DESCRIPTION

SUPPORT FOR ERM AND LRA

The AW8623 device supports both ERM and LRA. The SEL_LRA_ERM bit must be set to select the type of actuator. The default actuator type is LRA.

POWER ON RESET

The device provides a power-on reset feature that is controlled by DVDD OK. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers. When the VDD power on, the DVDD voltage raises and produces the OK indication, the reset is over.

The interrupt bit SYSINT.UVLI will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected power-on event has taken place.

OPERATION MODE

The device supports three operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	VDD = 0V or RSTN = 0V	Power supply is not ready or RSTN is tie to low. Whole chip shutdown including I²C interface.
Standby	VDD > 2.7V and RSTN = 1 and STANDBY = 1	Power supply is ready and RSTN is tie to high. Most parts of the device are power down for low power consumption except I²C interface and LDO.

Active	STANDBY = 0	Driver is ready for operating

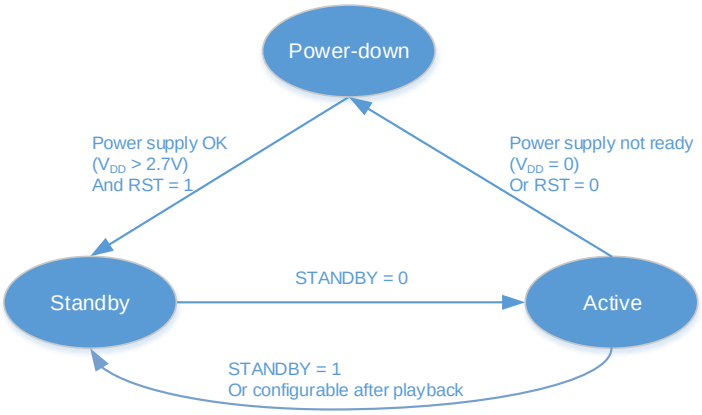


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when the supply voltage is not ready or RSTN pin is set to low.

In this mode, all circuits inside this device will be shut down. I^2C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when the supply voltages are OK and RSTN pin is set to high.

STANDBY MODE

The device switches to standby mode when the power supply voltages are OK and RSTN pin set to high. In this mode I^2C interface is accessible, other modules except LDO module are still powered down. Customer can set device to this mode when the device is no needed to work by setting STANDBY to high. Also in this mode, customer can initialize waveform library in SRAM. Device can be switched to this mode after haptic waveform playback finished.

ACTIVE MODE

The device is fully operational in this mode. H-bridge driver will start to work. Customer can set STANDBY = 0 to make device in this mode.

POWER UP AND PLAYBACK SEQUENCE

This device power up sequence is illustrated in the following figure:

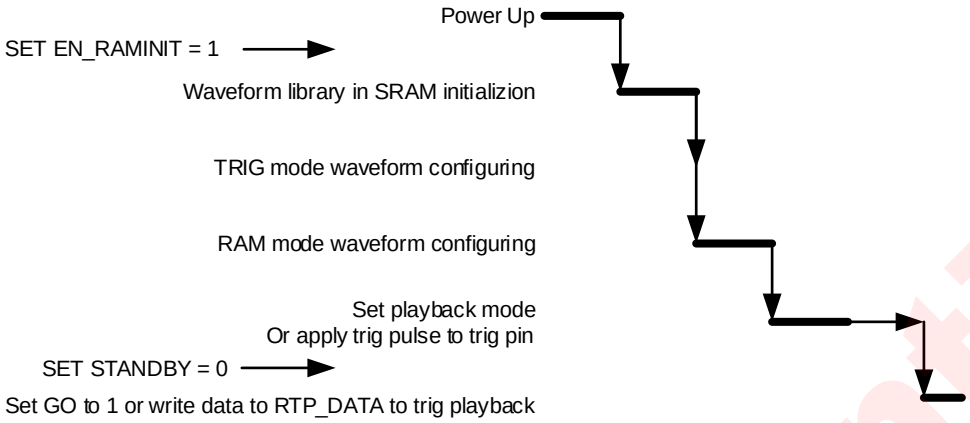


Figure 8 Power up and playback sequence

Detail description for each step is listed in the following table.

Table 2 Detail Description of Power up and playback sequence

Index	description	Mode
1	Wait for VDD supply power up and RSTN to 1	Power-Down
2.1	Waveform library initialization in SRAM	Standby
2.2	Trig mode waveform configuring	Standby
2.3	RAM mode waveform configuring	Standby
2.4	Set playback mode or apply trig pulse signal to trig pins	Standby or Active
3	Set GO to 1 or additionally write data to RTP_DATA to trig playback	Active

SOFTWARE RESET

Writing 0xAA to register CHIPID(0x00) via I2C interface will reset the device internal circuits and all configuration registers.

BATTERY VOLTAGE DETECT

Software can send command to detect the battery voltage. The register VBATDET[7:0] reports this information.

CONSTANT VIBRATION STRENGTH

The device features power-supply feedback. If the supply voltage discharge over time, the vibration strength remains the same as long as enough supply voltage is available to sustain the required output voltage. It is especially useful for ring application.

LRA RESONANT FREQUENCY DETECT

The resonant frequency detect function can be controlled by software. When LRA is driven under the non-resonant frequency, there will be a dramatically reduction in vibration strength and efficiency. With the resonant frequency detect function, the driver can provide stronger and more consistent vibration across LRA and consume lower power consumption meanwhile.

LRA RESISTANCE DETECT

Software can send command to detect the LRA's resistance. The register RLDET[7:0] reports this information. Based on this information host can diagnose the LRA's status. When RLDET[7:0] is less than low threshold, the LRA is short and if RLDET[7:0] is larger than high threshold, the LRA is open.

FLEXIBLE HAPTIC DATA PLAYBACK

The device offers multiple ways to playback haptic effects data. The PLAY_MODE bits select RAM mode, RTP mode or CONT mode. Additional flexibility is provided by the external TRIG pin, which can override PLAY_MODE bit to playback haptic effects data as configuration.

The device contains 8 kB of integrated SRAM to store customer haptic waveforms' data. The whole SRAM is separated to RAM waveform library and RTP FIFO region by base address. And RAM waveform library is

including waveform library version, waveform header and waveform data.

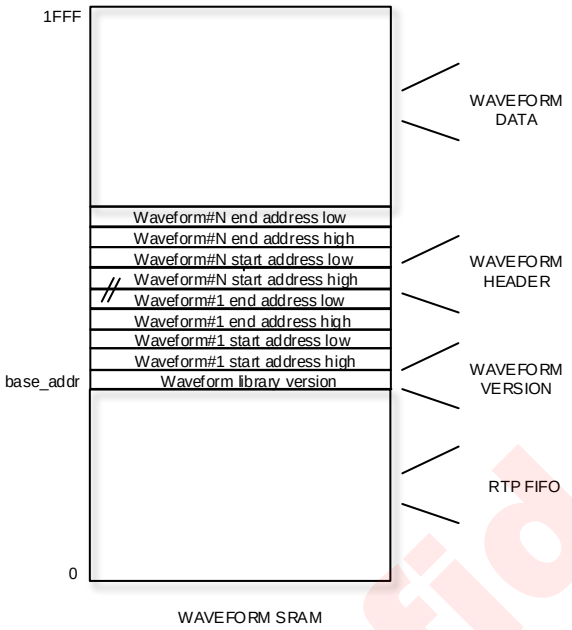


Figure 9 Data structure in SRAM

RAM mode and TRIG mode playback the waveforms in RAM waveform library and RTP mode playback the waveform data written in RTP FIFO, CONT mode playback non-filtered or filtered square wave with rated drive voltage .

RAM WAVEFORM LIBRARY DATA STRUCTURE

A RAM waveform library consists of a waveform version byte, a waveform header section, and the waveform data content. The waveform header defines the data boundaries for each waveform ID in the data field, and the waveform data contains a signed data format (2's complement) to specify the magnitude of the drive.

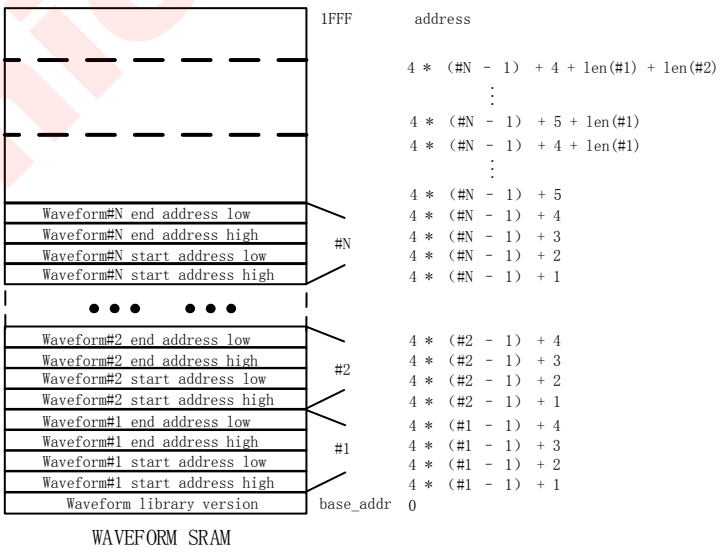


Figure 10 Waveform library data structure

Waveform version:

One byte located on SRAM base address, setting to different value to identify different version of RAM waveform library.

Waveform header:

The waveform header block consist of N-boundary definition blocks of 4 bytes each. N is the number of waveforms stored in the SRAM (N cannot exceed 127). Each of the boundary definition blocks contain the start address (2 bytes) and end address (2 bytes). So the total length of waveform header block are N*4 bytes.

The start address contains the location in the memory where the waveform data associated with this waveform begins.

The end address contains the location in the memory where the waveform data associated with this waveform ends.

The waveform ID is determined after base address is defined. Four bytes begins with the address next to base address are the first waveform ID's header, and next four bytes are the second waveform ID's header, and so on.

Waveform data:

The waveform data contains a signed data format (2's complement) to specify the magnitude of the drive. The begin address and end address is specified in waveform ID's header.

Waveform library initialization steps:

- Prepare waveform library data including: waveform library version, waveform header fields for waveform in library and waveform data of each waveform;
- Set register 0x04 to 0x61 to let the device in standby mode and enable SRAM initial;
- Set register 0x40, 0x41 to base address;
- Write waveform library data into register 0x42 continually until all the waveform library data written;

RAM MODE HAPTIC DATA PLAYBACK

To playback haptic data with RAM mode, the waveform ID must first be configured into the waveform playback queue and then the waveform can be played by writing GO bit register.

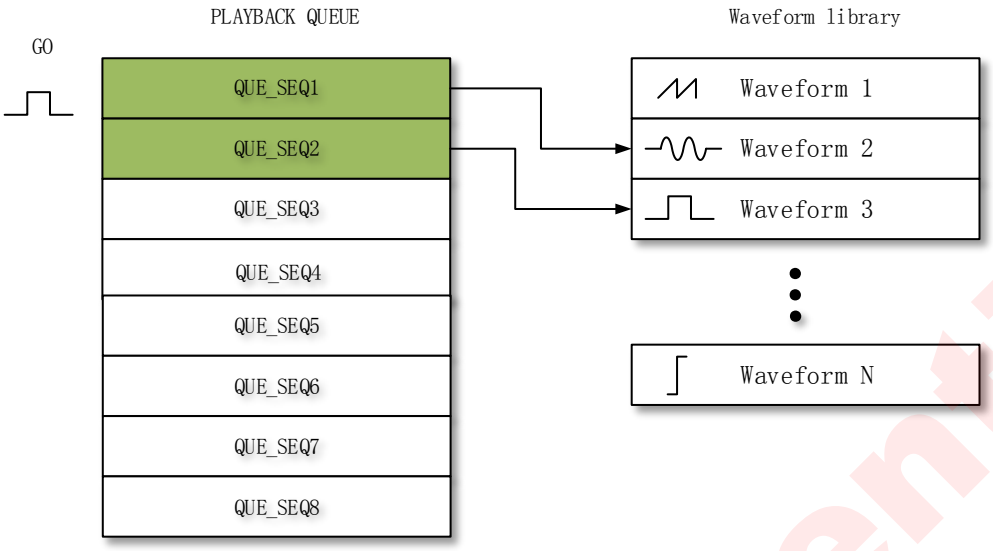


Figure 11 RAM mode playback

The waveform playback queue defines waveform IDs in waveform library for playback. Eight QUE_SEQx registers queue up to eight library waveforms for sequential playback. A waveform ID is an integer value referring to the index of a waveform in the waveform library. Playback begins at QUE_SEQ1 when the user triggers the waveform playback queue. When playback of that waveform ends, the waveform queue plays the next waveform ID held in QUE_SEQ2 (if non-zero). The waveform queue continues in this way until the queue reaches an ID value of zero or until all eight IDs are played whichever comes first.

The waveform ID is a 7-bit number. The MSB of each ID register can be used to implement a delay between queue waveforms. When the MSB is high, bits 6-0 indicate the length of the wait time. The wait time for that step then becomes QUE_SEQ[6:0] × wait_time unit. Wait_time unit can be configuration of 20us, 160us, 1280us or 10ms.

The device allows for looping of individual waveforms by using the SEQx_LOOP registers.When used, the state machine will loop the particular waveform the number of times specified in the associated SEQx_LOOP register before moving to the next waveform. The waveform-looping feature is useful for long, custom haptic playbacks, such as a haptic ringtone.

RAM mode playback steps:

- Waveform library must be initialized before playback;
- Set PLAY_MODE bit to 0 in register 0x04;
- Set playback queue registers (0x07 ~ 0x13) as desired;
- Set brake enable in register 0x39 when using;
- Set enable of BRAKE0/ BRAKE1/ BRAKE2, number and amplitude of brake pulses in register 0x32~0x35 when using;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically;

RTP MODE HAPTIC DATA PLAYBACK

The real-time playback mode is a simple, single 8-bit register interface that holds an amplitude value. When real-time playback is enabled, begin to enters a register value to RTP_DATA over the I²C will trigger the playback, the value is played until the data sending finished or removes the device from RTP mode.

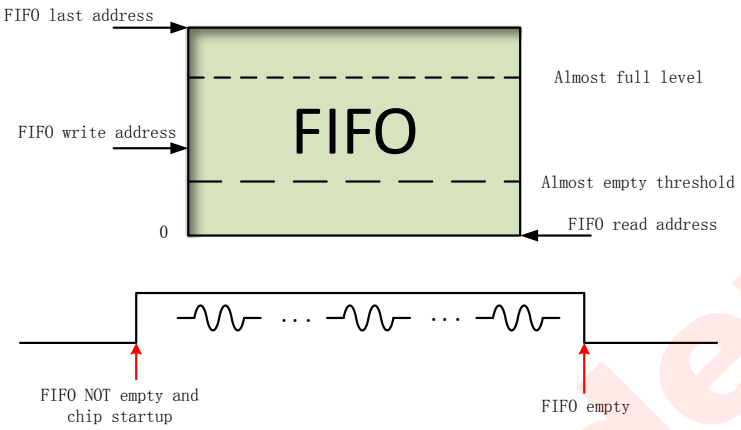


Figure 12 RTP mode playback

RTP mode playback steps:

- Prepare RTP data before playback;
- Set PLAY_MODE bit to 1 in register 0x04;
- Set brake enable in register 0x39 when using;
- Set enable of BRAKE0/ BRAKE1/ BRAKE2, number and amplitude of brake pulses in register 0x32~0x35 when using;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- Write RTP data continually to register 0x06 to playback RTP waveform;
- HOST need monitor the full and empty status for RTP FIFO;

TRIG MODE HAPTIC DATA PLAYBACK

The device has an external trigger pin TRIG. It can serve as a dedicated hardware pin for quickly trigger haptic data playback. Only support edge trigger. The pin can be configured single edge trigger or double edge trigger. Positive pulse and negative pulse can be supported by configuration.

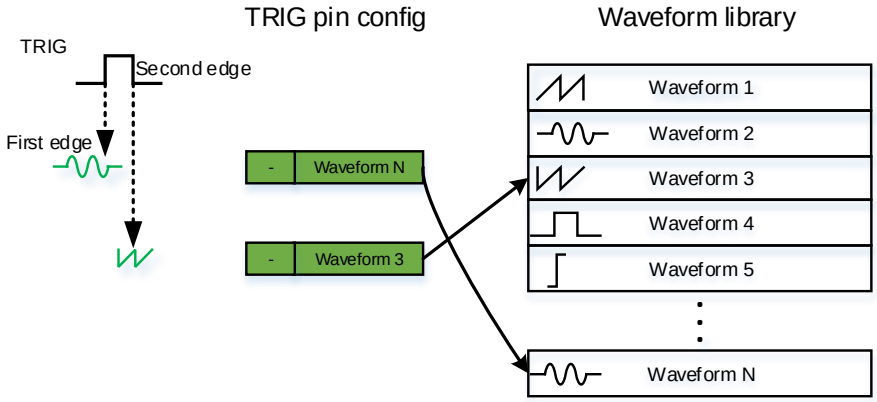


Figure 13 TRIG mode playback

Register 0x14 configure the waveform ID for the first edge of TRIG pin and register 0x17 configure the waveform ID for the second edge of TRIG pin if double edge selected by configuring register 0x1B bit 0;

Register 0x1B bit 1 should set to 1 when the trigger signal sent from host is negative pulse.

TRIG mode playback steps:

- Waveform library must be initialized before playback;
- Set trigger playback registers (0x14, 0x17, 0x1B) as desired;
- Set brake enable in register 0x39 when using;
- Set enable of BRAKE0/ BRAKE1/ BRAKE2, number and amplitude of brake pulses in register 0x32~0x35 when using;
- Send trigger pulse in TRIG pin to playback waveform.

CONT MODE HAPTIC DATA PLAYBACK

The CONT mode mainly performs two functions: power-on f0 detection, real-time resonance-frequency tracking. The power-on f0 detection can be launched when the chip is powered on or a LRA motor's resonant frequency need to be measured. The f0 can be acquired through register 0x68 and register 0x69.The real-time resonance-frequency tracking function tracks the resonant frequency of a LRA in real time by constantly monitoring the BEMF of the actuator. It provides stronger and more consistent vibrations and lower power consumption. If the resonant frequency shifts for any reason, the function tracks the frequency from cycle to cycle. In addition, a loop-open play mode can be launched for maximum flexibility.

Power-on f0 detection mode playback steps:

- Set PLAY_MODE bit to 0x2 in register 0x04 to enable CONT mode ;
- Set EN_F0_DET bit to 0x1 in register 0x48 to enable power-on f0 detection;
- Set RC filter function in register 0x2B when using;
- Set power-on f0 detection playback registers (0x48, 0x72, 0x73, 0x7D~0x7F) as desired;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically;

- F0 of the LRA motor can be acquired in register 0x68, 0x69.

Real-time resonance-frequency tracking mode playback steps:

- Set PLAY_MODE bit to 0x2 in register 0x04 to enable CONT mode;
- Set EN_F0_DET bit to 0x0 and EN_CLOSE bit to 0x1 to enable real-time resonance-frequency tracking;
- Set Td in register 0x4B, 0x4C;
- Set RC filter function in register 0x2B when using;
- Set ZC threshold in register 0x72、0x73;
- Set real-time resonance-frequency tracking playback registers (0x48, 0x78~0x7C,) as desired;
- Set brake enable in register 0x39 when using;
- Set enable of BRAKE0/ BRAKE1/ BRAKE2, number and amplitude of brake pulses in register 0x32~0x35 when using;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically.

Loop-open play mode playback steps:

- Set PLAY_MODE bit to 0x2 in register 0x04 to enable CONT mode;
- Set EN_F0_DET bit to 0x0 and EN_CLOSE bit to 0x0 to enable loop open play mode;
- Set RC filter function in register 0x2B when using;
- Set loop open playback registers (0x48, 0x79, 0x7B) as desired;
- Set brake enable in register 0x39 when using;
- Set enable of BRAKE0/ BRAKE1/ BRAKE2, number and amplitude of brake pulses in register 0x32~0x35 when using;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically;

AUTO-BRAKING OPTION

AW8623 features an automatic braking option to reduce the brake time of the actuator for a better tactile feedback. It can automatically decide the brake direction, calculate the brake cycle by constantly monitoring BEMF of the actuator. The automatic braking feature can be enabled or disabled by using the EN_BRAKE_CONT bit in CONT playback mode.

To achieve a better braking effect, the braking process is divided into three stages: BRAKE0, BRAKE1 and BRAKE2. In these stages, the brake enable, the number of brake pulses and the amplitude can be set respectively by using the special register. In addition, a stop brake threshold is set by using the THRS_BRAKE_END bit. If the BEMF of the actuator at a pre-set monitoring position is less than the stop brake threshold, the automatic braking stop immediately.

PROTECTION MECHANISMS

OVER TEMPERATURE PROTECTION (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

OVER CURRENT (SHORT) PROTECTION (OCP)

The short circuit protection function is triggered when HDP/HDN is short too VDD/GND or HDP is short to HDN, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

VDD UNDER VOLTAGE LOCK OUT PROTECTION (UVLO)

The device has a battery monitor that monitors the VDD level to ensure that is above threshold 2.8V, In the event of a VDD droop, the device immediately power down the H-bridge driver and latches the UVLO flag.

DRIVE DATA ERROR PROTECTION (DDEP)

When haptic data sent to drive LRA is error such as: a DC data or almost DC data, it will cause the LRA heat to break. The device configurable immediately power down and H-bridge driver and latched the DDEP flag.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz and super-fast mode at 1000kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 2.2kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address is 0x5A and can't be set.

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

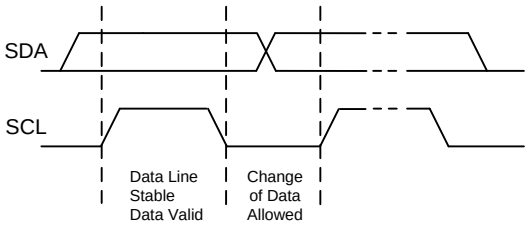


Figure 14 Data Validation Diagram

GENERAL I²C OPERATION

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

START state: The SCL maintain a high level, SDA from high to low level

STOP state: The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 15.

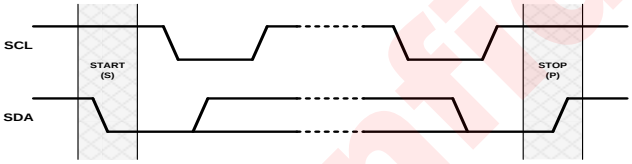


Figure 15 START and STOP state generation process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 16. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 17. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

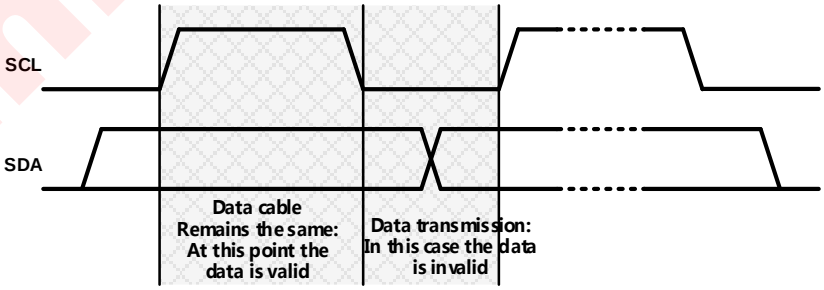


Figure 16 The data transfer rules on the I²C bus

The whole process of actual data transmission is shown in Figure 17. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The

master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

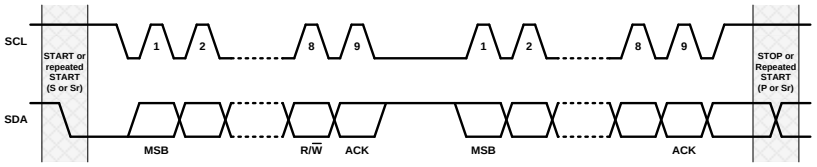


Figure 17 Data transmission on the I²C bus

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 18:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the device.

The master device generates the STOP state to end the data transmission.

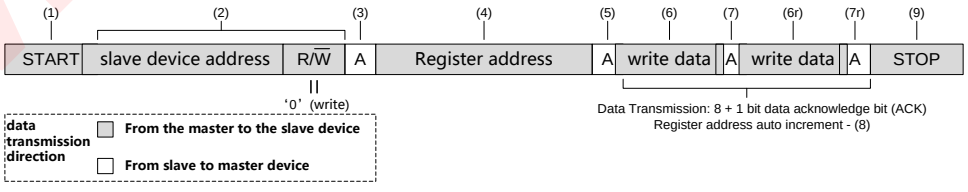


Figure 18 Writing process (data transmission direction remains the same)

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW8623 as the slave device, the transmission process carried out by following steps listed in Figure 19:

Master device asserts a start condition;

Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the register address to make sure where the first data byte will read;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

Master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

The device automatically increment register address once after sent each acknowledge bit (ACK),

The master device generates the STOP state to end the data transmission.

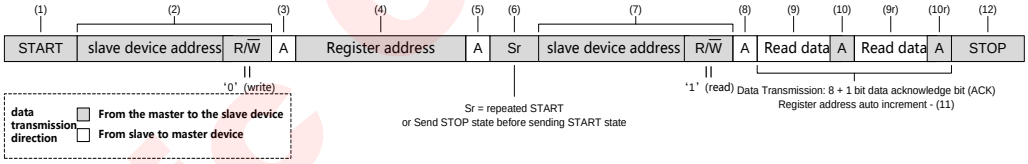


Figure 19 Reading process (data transmission direction remains the same)

REGISTER CONFIGURATION

REGISTER LIST

ADDR	NAME	7	6	5	4	3	2	1	0	Default
0x00	ID	CHIPID								0x23
0x01	SYSST	Reserved	OVS	UVLS	FF_AES	FF_AFS	OCDS	OTS	DONES	0x10
0x02	SYSINT	Reserved	OVI	UVLI	FF_AEI	FF_AFI	OCDI	OTI	DONEI	0x10
0x03	SYSINTM	Reserved	OVM	UVLM	FF_AEM	FF_AFM	OCDM	OTM	DONEM	0x7F
0x04	SYSCTRL	WAVDAT_MODE		EN_RAMINIT	Reserved	PLAY_MODE		Reserved	STANDBY	0x41
0x05	GO	Reserved							GO	0x00
0x06	RTPDATA	RTP_DATA								0x00
0x07	WAVSEQ1	WAIT1	WAV_FRM_SEQ1							0x01
0x08	WAVSEQ2	WAIT2	WAV_FRM_SEQ2							0x00
0x09	WAVSEQ3	WAIT3	WAV_FRM_SEQ3							0x00
0x0A	WAVSEQ4	WAIT4	WAV_FRM_SEQ4							0x00
0x0B	WAVSEQ5	WAIT5	WAV_FRM_SEQ5							0x00
0x0C	WAVSEQ6	WAIT6	WAV_FRM_SEQ6							0x00
0x0D	WAVSEQ7	WAIT7	WAV_FRM_SEQ7							0x00
0x0E	WAVSEQ8	WAIT8	WAV_FRM_SEQ8							0x00
0x0F	WAVLOOP1	SEQ1_LOOP				SEQ2_LOOP				0x00
0x10	WAVLOOP2	SEQ3_LOOP				SEQ4_LOOP				0x00
0x11	WAVLOOP3	SEQ5_LOOP				SEQ6_LOOP				0x00
0x12	WAVLOOP4	SEQ7_LOOP				SEQ8_LOOP				0x00
0x13	MAINLOOP	Reserved				MAINLOOP				0x00
0x14	TRG1SEQP	Reserved	TRG1_FRM_SEQ_P							0x01
0x17	TRG1SEQN	Reserved	TRG1_FRM_SEQ_N							0x01
0x1B	TRGCFG1	Reserved						TRG1_POLAR	TRG1_EDGE	0x00
0x1C	TRGCFG2	Reserved							TRG1_EN	0x40
0x20	DBGCTRL	Reserved				INTMODE		WAITSLOT		0x03
0x21	BASE_ADDRH	Reserved			BASE_ADDRH					0x08
0x22	BASE_ADDRL	BASE_ADDRL								0x00
0x23	FIFO_AEH	Reserved				FIFO_AEH				0x02
0x24	FIFO_AEL	FIFO_AEL								0x00
0x25	FIFO_AFH	Reserved				FIFO_AFH				0x06
0x26	FIFO_AFL	FIFO_AFL								0x00
0x2B	DATCTRL	Reserved		EN_LPF	Reserved			EN_FIR	Reserved	0x60
0x2D	PWMPRC	PRC_EN	PRCTIME							0xA0
0x2E	PWMDBG	Reserved	PWMCLK_MODE		PD_HWM	Reserved			PWM_OE	0xC1
0x30	DBGSTAT	LDO_OK	Reserved		VBGOK	Reserved	FF_ERROR	FF_FULL	FF_EMPTY	0x01
0x31	WAVECTRL	NUM_OV_DRIVER				Reserved			SEL_LRA_ERM	0x31
0x32	BRAKE0_CTRL	Reserved	BRAKE0_LEVEL							0x7F
0x33	BRAKE1_CTRL	EN_BRAKE1	BRAKE1_LEVEL							0x9F
0x34	BRAKE2_CTRL	EN_BRAKE2	BRAKE2_LEVEL							0x87
0x35	BRAKE_NUM	BRAKE2_P_NUM		BRAKE1_P_NUM			BRAKE0_P_NUM			0x5B
0x38	ANACTRL	Reserved		LRA_TRIM_SRC	OSC_TRIM_SRC	Reserved				0x09
0x39	SW_BRAKE	Reserved	SEL_PERIOD_BRAKE		Reserved	EN_BRAKE_CONT	EN_BRAKE_RAM	Reserved		0x08

0x3B	DATDBG	GAIN					0x80
0x3E	PRLVL	PR_EN	PRLVL				0x3F
0x3F	PRTIME	PRTIME					0x12
0x40	RAMADDRH	Reserved	RAMADDRH				0x00
0x41	RAMADDRL	RAMADDRL					0x00
0x42	RAMDATA	RAMDATA					0x00
0x44	BRA_MAX_NUM	BRAKE_MAX_NUM					0x12
0x48	CONT_CTRL	Reserved	CONT_MODE	EN_CLOSE	EN_F0_DET	Reserved	0x98
0x49	F_PRE_H	F_PRE_H					0x07
0x4A	F_PRE_L	F_PRE_L					0x25
0x4B	TD_H	TD_BRAKE	TD_H				0xB0
0x4C	TD_L	TD_L					0x5D
0x4F	THRS_BRA_END	Reserved	THRS_BRAKE_END				0x04
0x5B	TRIM_LRA	Reserved	TRIM_LRA				0x00
0x5F	DETCTRL	Reserved	RL_OS	PRCT_MODE	Reserved	VBAT_GO	DIAG_GO	0x00
0x60	RLDET	RL					0x00
0x61	OSDET	OS					0x80
0x62	VBATDET	VBAT					0x00
0x66	ADCTEST	Reserved	VBAT_MODE	Reserved			0x00
0x68	F_LRA_F0_H	F_LRA_F0_H					0x00
0x69	F_LRA_F0_L	F_LRA_F0_L					0x00
0x6A	F_LRA_CONT_H	F_LRA_CONT_H					0x00
0x6B	F_LRA_CONT_L	F_LRA_CONT_L					0x00
0x72	ZC_THRSH_H	ZC_THRSH_H					0x0F
0x73	ZC_THRSH_L	ZC_THRSH_L					0xF1
0x79	DRV_TIME	DRV_TIME					0x3F
0x7A	TIME_NZC	TIME_NZC					0x1F
0x7B	DRV_LVL	DRV_LEVEL					0x50
0x7C	DRV_LVL_OV	DRV_LEVEL_OV					0x7F
0x7D	NUM_F0_1	NUM_F0_PRE	Reserved				0x59
0x7E	NUM_F0_2	NUM_F0_REPEAT					0x05
0x7F	NUM_F0_3	NUM_F0_TRACE					0x0F

REGISTER DETAILED DESCRIPTION

ID：Chip ID Register(Address 0x00) Default: 0x23

Bit	Symbol	R/W	Description	Default
7:0	CHIPID	RO	Chip ID (23) will be returned after read. All configuration registers will be reset to default value after 0xaa is written	0x23

SYSST：System status Register(Address 0x01) Default: 0x10

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Reserved	0
6	OVS	RO	Wave data overflow or DPWM DC error	0

5	UVLS	RO	Under voltage lock out signal，0：VDD>UVLO_THRES，1：VDD<UVLO_THRES	0
4	FF_AES	RO	1：RTP FIFO almost empty	1
3	FF_AFS	RO	1：RTP FIFO almost full	0
2	OCDS	RO	1：Over Current status	0
1	OTS	RO	1：Over Temperature status	0
0	DONES	RO	1：The indication of playback done	0

SYSINT：System Interrupt Register(Address 0x02) Default: 0x10

Bit	Symbol	R/W	Description	Default
7	Reserved	RC	Reserved	0
6	OVI	RC	Interrupt for OVS	0
5	UVLI	RC	Interrupt for UVLS	0
4	FF_AEI	RC	Interrupt for FF_AES	1
3	FF_AFI	RC	Interrupt for FF_AFS	0
2	OCDI	RC	Interrupt for OCDS	0
1	OTI	RC	Interrupt for OTS	0
0	DONEI	RC	Interrupt for DONES	0

SYSINTM：System Interrupt Mask Register(Address 0x03) Default: 0x7F

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6	OVM	RW	Interrupt mask for OVI	1
5	UVLM	RW	Interrupt mask for UVLI	1
4	FF_AEM	RW	Interrupt mask for FF_AEI	1
3	FF_AFM	RW	Interrupt mask for FF_AFI	1
2	OCDM	RW	Interrupt mask for OCDI	1
1	OTM	RW	Interrupt mask for OTI	1
0	DONEM	RW	Interrupt mask for DONEI	1

SYSCTRL：System control Register(Address 0x04) Default: 0x41

Bit	Symbol	R/W	Description	Default
7:6	WAVDAT_MODE	RW	Waveform data upsample rate selection: 1: 1x upsample rate 0: 2x upsample rate others: 4x upsample rate	1
5	EN_RAMINIT	RW	Enable SRAM initialization for effects After power up, system should initial SRAM for preload effects, to do so, this bit must be set to 1	0
4	Reserved	RW	Reserved	0

3:2	PLAY_MODE	RW	Waveform play mode for GO trig 0: RAM mode 1: RTP mode 2: CONT mode	0
1	Reserved	RW	Reserved	0
0	STANDBY	RW	Chip enable/disable control 0: set chip into active mode 1: set chip into standby mode	1

GO：Process control Register(Address 0x05) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Reserved	0
0	GO	RWC	RAM/RTP/CONT mode playback trig bit When set to 1, chip will playback waveforms from SRAM as configuration, after playback finished , it will be cleared internally During playback, if it is set to 0, playback will stop	0

RTPDATA：RTP mode data Register(Address 0x06) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	RTP_DATA	RW	RTP mode , data write entry, when data written into this register, the data will be written into RTP FIFO	0

WAVSEQ1：First Waveform Register(Address 0x07) Default: 0x01

Bit	Symbol	R/W	Description	Default
7	WAIT1	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ1	RW	Wait time or wave sequence number	0x01

WAVSEQ2：Second Waveform Register(Address 0x08) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT2	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ2	RW	Wait time or wave sequence number	0x00

WAVSEQ3：Third waveform Register(Address 0x09) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT3	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ3	RW	Wait time or wave sequence number	0x00

WAVSEQ4：Fourth waveform Register(Address 0x0A) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT4	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ4	RW	Wait time or wave sequence number	0x00

WAVSEQ5：Fifth Waveform Register(Address 0x0B) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT5	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ5	RW	Wait time or wave sequence number	0x00

WAVSEQ6：Sixth Waveform Register(Address 0x0C) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT6	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ6	RW	Wait time or wave sequence number	0x00

WAVSEQ7：Seventh waveform Register(Address 0x0D) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT7	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ7	RW	Wait time or wave sequence number	0x00

WAVSEQ8：Eighth waveform Register(Address 0x0E) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	WAIT8	RW	When set to 1 , WAV_FRM_SEQ means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ8	RW	Wait time or wave sequence number	0x00

WAVLOOP1：Waveform loop control Register(Address 0x0F) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:4	SEQ1_LOOP	RW	Control the loop number of the first sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ2_LOOP	RW	Control the loop number of the second sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

WAVLOOP2：Waveform loop control Register(Address 0x10) Default: 0x00

Bit	Symbol	R/W	Description	Default

7:4	SEQ3_LOOP	RW	Control the loop number of the third sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ4_LOOP	RW	Control the loop number of the fourth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

WAVLOOP3：Waveform loop control Register(Address 0x11) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:4	SEQ5_LOOP	RW	Control the loop number of the fifth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ6_LOOP	RW	Control the loop number of the sixth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

WAVLOOP4：Waveform loop control Register(Address 0x12) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:4	SEQ7_LOOP	RW	Control the loop number of the seventh sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ8_LOOP	RW	Control the loop number of the eighth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

MAINLOOP：The main loop control Register(Address 0x13) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	0x0
3:0	MAINLOOP	RW	Control the main loop number 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

TRG1SEQP：TRIG1 First Edge waveform Register(Address 0x14) Default: 0x01

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6:0	TRG1_FRM_SEQ_P	RW	Wave sequence number trigged by first edge of trig1 pulse	0x01

TRG1SEQN：TRIG1 Second Edge waveform Register(Address 0x17) Default: 0x01

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0

6:0	TRG1_FRM_SEQ_N	RW	Wave sequence number trigged by second edge of trig1 pulse	0x01

TRGCFG1：Trig pins config Register(Address 0x1B) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Reserved	0x00
1	TRG1_POLAR	RW	TRIG1 pin active polarity, when host supply positive pulse, this bit set to 0, else set to 1	0
0	TRG1_EDGE	RW	TRIG1 pin trigging edge config, set to 1 , only first edge can trig playback, else both edge can trig playback	0

TRGCFG2：Trig pins config Register(Address 0x1C) Default: 0x40

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Reserved	0x00
0	TRG1_EN	RW	TRIG1 pin trigging enable	0

DBGCTRL：Debug control Register(Address 0x20) Default: 0x03

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	0x0
3:2	INTMODE	RW	Interrupt mode x0: interrupt level mode; x1: interrupt edge mode; 0x: interrupt posedge mode; 1x: interrupt both edge mode;	0x0
1:0	WAITSLOT	RW	Unit of wait time 00: 20μs 01: 160μs 10: 1280μs 11: 10ms	0x3

BASE_ADDRH：High five bits of Wave SRAM Register(Address 0x21) Default: 0x08

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Reserved	0x0
4:0	BASE_ADDRH	RW	High five bits of start Address 0xof wave SRAM	0x08

BASE_ADDRL：Low eight bits of Wave SRAM Register(Address 0x22) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	BASE_ADDRL	RW	Low eight bits of start Address 0xof wave SRAM	0x00

FIFO_AEH：High four bits of FIFO AE Register(Address 0x23) Default: 0x02

Bit	Symbol	R/W	Description	Default

7:4	Reserved	RW	Reserved	0x0
3:0	FIFO_AEH	RW	High four bits of RTP FIFO almost empty threshold	0x2

FIFO_AEL：Low eight bits of FIFO AE Register(Address 0x24) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AEL	RW	Low eight bits of RTP FIFO almost empty threshold	0x00

FIFO_AFH：High four bits of FIFO AF Register(Address 0x25) Default: 0x06

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	0x0
3:0	FIFO_AFH	RW	High four bits of RTP FIFO almost full threshold	0x6

FIFO_AFL：Low eight bits of FIFO AF Register(Address 0x26) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AFL	RW	Low eight bits of RTP FIFO almost full threshold	0x00

DATCTRL: Global control data register(Address 0x2B) Default: 0x60

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Reserved	0x1
5	EN_LPF	RW	Set enable of RC filter	1
4:2	Reserved	RW	Reserved	0x0
1	EN_FIR	RW	Set enable of FIR filter	0
0	Reserved	RW	Reserved	0

PWMPRC: PWM output protect configuration register(Address 0x2D) Default: 0xA0

Bit	Symbol	R/W	Description	Default
7	PRC_EN	RW	Set enable of output signal protection mode of pwm	1
6:0	PRCTIME	RW	Set protection time of output signal protection mode of pwm	0x20

PWMDBG: PWM debug register(Address 0x2E) Default: 0xC1

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	1
6:5	PWMCLK_MODE	RW	PWM data sample rate mode: 0x: 48kB 10: 24kB 11: 12kB	0x2
4	PD_HWM	RW	Shutdown half wave modulate	0
3:1	Reserved	RW	Reserved	0x0
0	PWMOE	RW	PWM output enable	1

DBGSTAT: Debug status register(Address 0x30) Default: 0x01

Bit	Symbol	R/W	Description	Default
7	LDO_OK	RO	LDO OK indication	1
6:5	Reserved	RO	Reserved	0x0
4	VBGOK	RO	VBG OK indication	0
3	Reserved	RO	Reserved	0
2	FF_ERROR	RO	RTP FIFO error status	0
1	FF_FULL	RO	RTP FIFO full status	0
0	FF_EMPTY	RO	RTP FIFO empty status	1

WAVECTRL: Wave ctrl register(Address 31h) Default: 0x31

Bit	Symbol	R/W	Description	Default
7:4	NUM_OV_DRIVER	RW	Control the number of overdrive pulses in LOOP_OPEN state or LOOP_CLOSE state in LRA mode. 0000: no overdrive pulse 0001~1111: play n overdrive pulses	0x3
3:1	Reserved	RW	Reserved	0x0
0	SEL_LRA_ERM	RW	Set the type of motor to drive 0: ERM 1: LRA	1

BRAKE0_CTRL: Brake0 ctrl register(Address 32h) Default: 0x7F

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6:0	BRAKE0_LEVEL	RW	Set the voltage amplitude of brake0 waveform. This value is positive, ranging from 0 to 127.	0x7F

BRAKE1_CTRL: Brake1 ctrl register(Address 33h) Default: 0x9F

Bit	Symbol	R/W	Description	Default
7	EN_BRAKE1	RW	Set enable of the brake1 waveform. 1:enable 0:disable	1
6:0	BRAKE1_LEVEL	RW	Set the voltage amplitude of brake1 waveform. This value is positive, ranging from 0 to 127.	0x1F

BRAKE2_CTRL: Brake2 ctrl register(Address 34h) Default: 0x8F

Bit	Symbol	R/W	Description	Default
7	EN_BRAKE2	RW	Set enable of the brake2 waveform. 1:enable 0:disable	1
6:0	BRAKE2_LEVEL	RW	Set the voltage amplitude of brake2 waveform. This value is positive, ranging from 0 to 127.	0x0F

BRAKE_NUM: brake number ctrl register(Address 0x35) Default: 0x5B

Bit	Symbol	R/W	Description	Default

7:6	BRAKE2_P_NUM	RW	Set the number of brake2 pulses 00: one brake2 pulse 01: two brake2 pulses 10: three brake2 pulses 11: four brake2 pulses	0x1
5:3	BRAKE1_P_NUM	RW	Set the number of brake1 pulses 000: one brake1 pulse 001: two brake1 pulses ------ 110: seven brake1 pulses 111: eight brake1 pulses	0x3
2:0	BRAKE0_P_NUM	RW	Set the number of brake0 pulses 000: one brake0 pulse 001: two brake0 pulses ------ 110: seven brake0 pulses 111: eight brake0 pulses	0x3

ANACTRL: Analog control register(Address 0x38) Default: 0x09

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Reserved	0x0
5	LRA_TRIM_SRC	RW	LRA trim source select 0: efuse 1: register	0
4	OSC_TRIM_SRC	RW	OSC trim source select 0: efuse 1: register	0
3:0	Reserved	RW	Reserved	0x9

SW_BRAKE: Brake switch register(Address 0x39) Default: 0x08

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6:5	SEL_PERIOD_BRAKE	RW	Select the period of braking pulse 00: Real time measured braking cycles 01: pre_set cycles 10: Real time measured braking cycles 11:the measured period of f0 after power on	0x0
4	Reserved	RW	Reserved	0
3	EN_BRAKE_CONT	RW	Set enable of braking in CONT mode 0: disable 1: enable	1
2	EN_BRAKE_RAM	RW	Set enable of braking in RAM mode 0: disable 1: enable	0
1:0	Reserved	RW	Reserved	0x0

DATDBG: DATA GAIN register(Address 0x3B) Default: 0x80

Bit	Symbol	R/W	Description	Default
7:0	GAIN	RW	Gain setting for waveform data, it is a global setting for all waveform data.	0x80

HDRVDBG: Hdriver debug register(Address 0x3D) Default: 0x01

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Reserved	0x0
1:0	HDRV_DT	RW	Hdriver dead time select 00: 12ns 01: 20ns(default) 10: 27ns 11: 36ns	0x1

PRLVL: Waveform protect level configuration(Address 0x3F) Default: 0xBF

Bit	Symbol	R/W	Description	Default
7	PR_EN	RW	Set enable of input signal protection mode of pwm	1
6:0	PRLVL	RW	Set protection voltage of input signal protection mode of pwm	0x3F

PRTIME: Waveform protect period configuration(Address 0x3F) Default: 0x12

Bit	Symbol	R/W	Description	Default
7:0	PRTIME	RW	Set protection time of input signal protection mode of pwm	0x12

RAMADDRH: SRAM Address 0xhigh register(Address 0x40) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Reserved	0x0
4:0	RAMADDRH	RW	High five bits of SRAM Address	0x0

RAMADDRL: SRAM Address 0xlow register(Address 0x41) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	RAMADDRL	RW	Low eight bits of SRAM Address	0x00

RAMDATA: SRAM data register(Address 0x42) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	RAMDATA	RW	SRAM data entry	0x00

TM: BIST/SCAN mode control register(Address 0x43) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	TM	WO	Write 2C to set to SCAN mode; Write B4 to set to BIST mode;	0x00

BRA_MAX_NUM: Max braking number register(Address 0x44) Default: 0x12

Bit	Symbol	R/W	Description	Default
7:0	BRAKE_MAX_NUM	RW	Set the max braking number in the brake mode When set to 0,no braking pulse. When set to 0x12,eighteen braking pulse.	0x12

CONT_CTRL：CONT mode control Register(Address 0x48) Default: 0x98

Bit	Symbol	R/W	Description	Default

7:5	Reserved	RW	Reserved	0x4
4	CONT_MODE	RW	Playback time control 1:control by register iRtime 0:control by go_signal	1
3	EN_CLOSE	RW	Loop_close play mode enable 1:loop_close play mode 0:loop_open play mode	1
2	EN_F0_DET	RW	F0 detection mode enable 1:enable 0:disable	0
1:0	Reserved	RW	Reserved	0x0

F_PRE_H: High 8 bits pre setting f0 value(Address 0x49) Default: 0x07

Bit	Symbol	R/W	Description	Default
7:0	F_PRE_H	RW	High eight bits of default f0 value of LRA.. F_PRE = {F_PRE_H,F_PRE_L} x 2.6μs	0x07

F_PRE_L: Low 8 bits pre setting f0 value(Address 0x4A) Default: 0x25

Bit	Symbol	R/W	Description	Default
7:0	F_PRE_L	RW	Low eight bits of default f0 value of LRA.. F_PRE = {F_PRE_H,F_PRE_L} x 2.6μs	0x25

TD_H: High 4 bits of delay time setting(Address 0x4B) Default: 0xB0

Bit	Symbol	R/W	Description	Default
7:4	TD_BRAKE	RW	Set the time delay of brake Time delay of BRAKE = TD_BRAKE x 41.6μs.	0xB
3:0	TD_H	RW	High four bits of time delay TD = {TD_H,TD_L} x 2.6μs	0x0

TD_L: Low 8 bits of delay time setting(Address 0x4C) Default: 0x5D

Bit	Symbol	R/W	Description	Default
7:0	TD_L	RW	Low eight bits of time delay TD = {TD_H,TD_L} x 2.6μs	0x5D

THRS_BRA_END: Stop brake threshold register(Address 0x4F) Default: 0x04

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6:0	THRS_BRAKE_END	RW	Set stop braking threshold	0x04

EF_TRIM_LRA: EFUSE TRIM LRA register(Address 0x5B) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Reserved	0x0

5:0	TRIM_LRA	RW	Register LRA trim setting Trimming OSC frequency adaptive for LRA resonant frequency deviation with efuse 0000: LRA(1+0%)(LRA real resonant frequency) 0001~1111: LRA(1+n*0.25%), n is a complement.	0

DETCTRL: Detection control register(Address 0x5F) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6	RL_OS	RW	Set diagnostic mode 1: RL detection of actuator 0: OS detection of ADC	0
5	PRCT_MODE	RW	Set protect mode 0: valid 1: invalid	0
4:2	Reserved	RW	Reserved	0x0
1	VBAT_GO	RW	Set the enabled of VBAT mode	0
0	DIAG_GO	RW	Set the enabled of DIAG mode	0

RLDET: Detected RL of LRA register(Address 0x60) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	RL	RO	Measured resistance value of LRA in DIAG mode	0x00

OSDET: Detected offset of LRA register(Address 0x61) Default: 0x80

Bit	Symbol	R/W	Description	Default
7:0	OS	RO	Measured OS value in OS mode	0x80

VBATDET: Detected VBAT register(Address 0x62) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	VBAT	RO	Measured VBAT value in VBAT mode	0x00

ADCTEST: ADC test register(Address 0x66) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	0
6	VBAT_MODE	RW	VBAT adjust mode, 0: software adjust mode, 1: hardware adjust mode	0
5:0	Reserved	RW	Reserved	0x0

F_LRA_F0_H: High 8 bits detected f0 value(Address 0x68) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_F0_H	RO	High eight bits of the measure value of f0 in the f0 detection mode F_LRA_F0 = {F_LRA_F0_H,F_LRA_F0_L} x 2.6μs	0x00

F_LRA_F0_L: Low 8 bits detected f0 value(Address 0x69) Default: 0x00

Bit	Symbol	R/W	Description	Default

7:0	F_LRA_F0_L	RO	Low eight bits of the measure value of f0 in the f0 detection mode F_LRA_F0 = {F_LRA_F0_H,F_LRA_F0_L} x 2.6μs	0x00

F_LRA_CONT_H: High 8 bits CONT_ENG gotten f0 value(Address 0x6A) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_CONT_H	RO	High eight bits of the measure value of f0 in the continuous detection mode F_LRA_CONT = {F_LRA_CONT_H,F_LRA_CONT_L} x 2.6μs	0x00

F_LRA_CONT_L: Low 8 bits CONT_ENG gotten f0 value(Address 0x6B) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_CONT_L	RO	Low eight bits of the measure value of f0 in the continuous detection mode F_LRA_CONT = {F_LRA_CONT_H,F_LRA_CONT_L} x 2.6μs	0x00

ZC_THRSH_H: Zero cross threshold high 8 bits configuration register(Address 0x72) Default: 0x0F

Bit	Symbol	R/W	Description	Default
7:0	ZC_THRSH_H	RW	Zero-cross detection positive threshold of BEMF	0x0F

ZC_THRSH_L: Zero cross threshold low 8 bits configuration register(Address 0x73) Default: 0xF1

Bit	Symbol	R/W	Description	Default
7:0	ZC_THRSH_L	RW	Zero-cross detection negative threshold of BEMF	0xF1

DRV_TIME: Drive time setting register(Address 0x79) Default: 0x3F

Bit	Symbol	R/W	Description	Default
7:0	DRV_TIME	RW	Set play time of the LOOP_OPEN state or the LOOP_CLOSE state play time = DRV_TIME x 5333.3μs	0x3F

TIME_NZC: Non zero cross time setting register(Address 0x7A) Default: 0x1F

Bit	Symbol	R/W	Description	Default
7:0	TIME_NZC	RW	Set the time threshold of non-zero-cross time threshold = TIME_NZC x 166.67μs	0x1F

DRV_LVL: Drive level setting register(Address 0x7B) Default: 0x50

Bit	Symbol	R/W	Description	Default
7:0	DRV_LVL	RW	Set the level of drive waveform in normal driving	0x50

DRV_LVL_OV: Drive level for overdrive setting register(Address 0x7C) Default: 0x7F

Bit	Symbol	R/W	Description	Default
7:0	DRV_LVL_OV	RW	Set the level of drive waveform in overdrive	0x7F

NUM_F0_1: Number configuration for F0 trace register 1 (Address 0x7D) Default: 0x59

Bit	Symbol	R/W	Description	Default
7:4	NUM_F0_PRE	RW	Drive waveform play times in the first period in the f0 detection	0x5
3:0	Reserved	RW	Reserved	0x9

NUM_F0_2: Number configuration for F0 trace register 2 (Address 0x7E) Default: 0x05

Bit	Symbol	R/W	Description	Default
7:0	NUM_F0_REPEAT	RW	The repeat times in the f0 detection	0x05

NUM_F0_3: Number configuration for F0 trace register 3 (Address 0x7F) Default: 0x0F

Bit	Symbol	R/W	Description	Default
7:0	NUM_F0_TRACE	RW	Drive waveform play times in the second period and later in the f0 detection	0x0F

APPLICATION INFORMATION

CAPACITORS SELECTION

Supply Decoupling Capacitor（C_S）

The device requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

Output beads, capacitors

The AW8623 passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from driver to load, placed as close as possible to the output pin.

The device output is a square wave signal, which causing switch current at the output capacitor, increasing static power consumption, and therefore output capacitor should not be too large, 0.1nF ceramic capacitors is recommended.

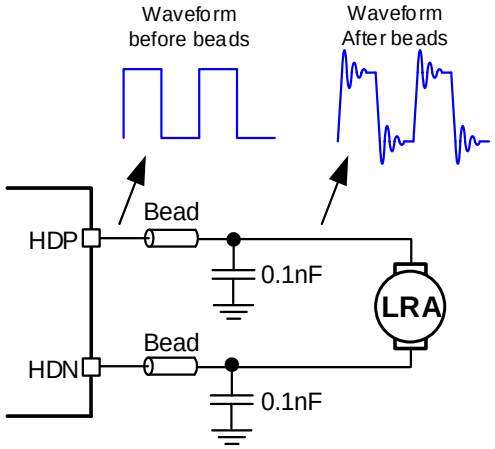


Figure 20 Ferrite Chip Bead and capacitor

The device output is a square wave signal. The voltage across the capacitor will be much larger than the VDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 10V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 10V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 10V capacitor, but quiescent current will increase.

PCB LAYOUT CONSIDERATION

EXTERNAL COMPONENTS PLACEMENT

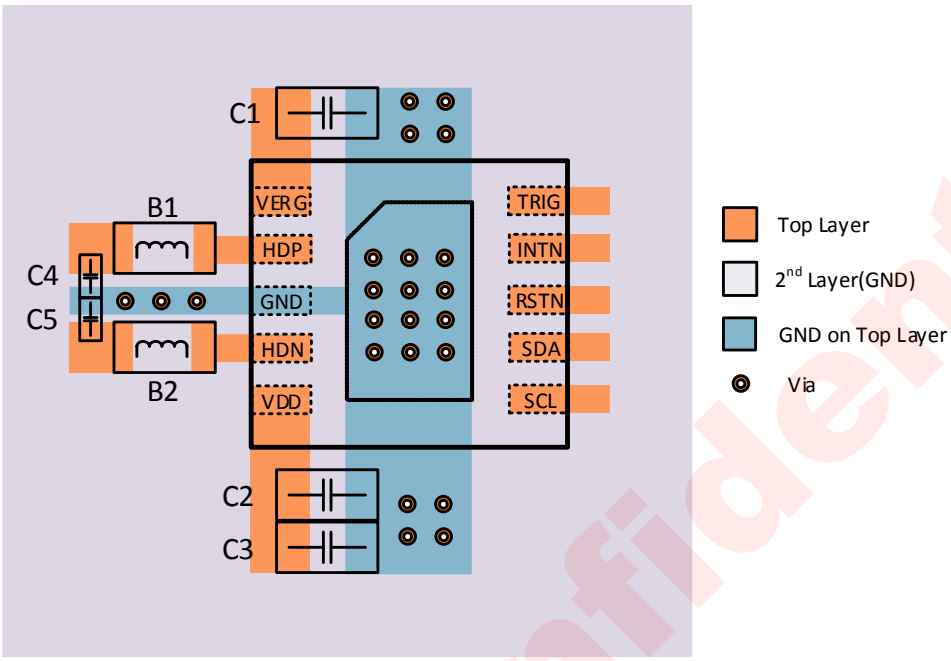


Figure 21 AW8623 External Components Placement

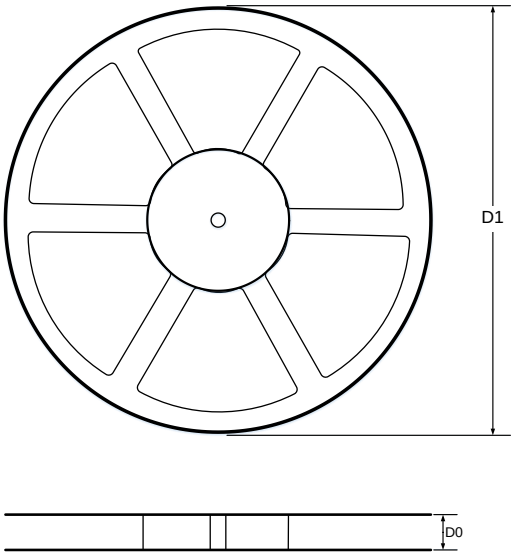
LAYOUT CONSIDERATIONS

To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

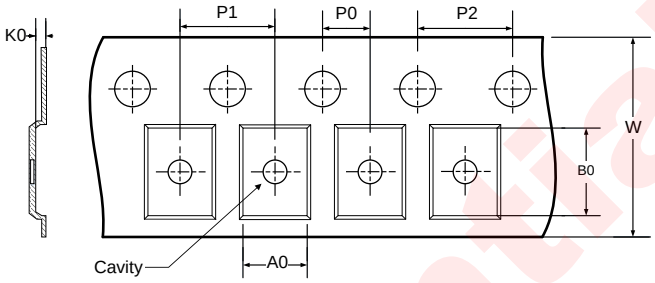
1. All of the external components close to IC in top layer PCB;
2. Create solid GND plane near and around the IC;
3. Try to provide a separate short and thick power line to the device, the copper width is recommended to be larger than 0.75mm.
4. The beads and capacitor should be placed near to the device HDN and HDP pin. The output line from the device to load should be as short and thick as possible. The width is recommended to be larger than 0.5mm;

TAPE AND REEL INFORMATION

REEL DIMENSIONS

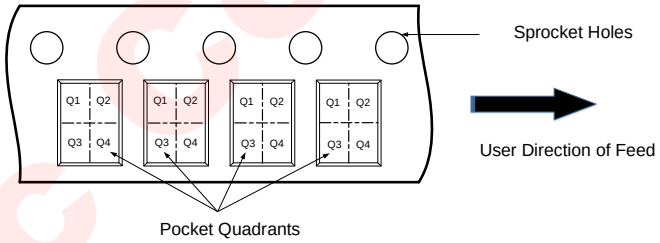


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

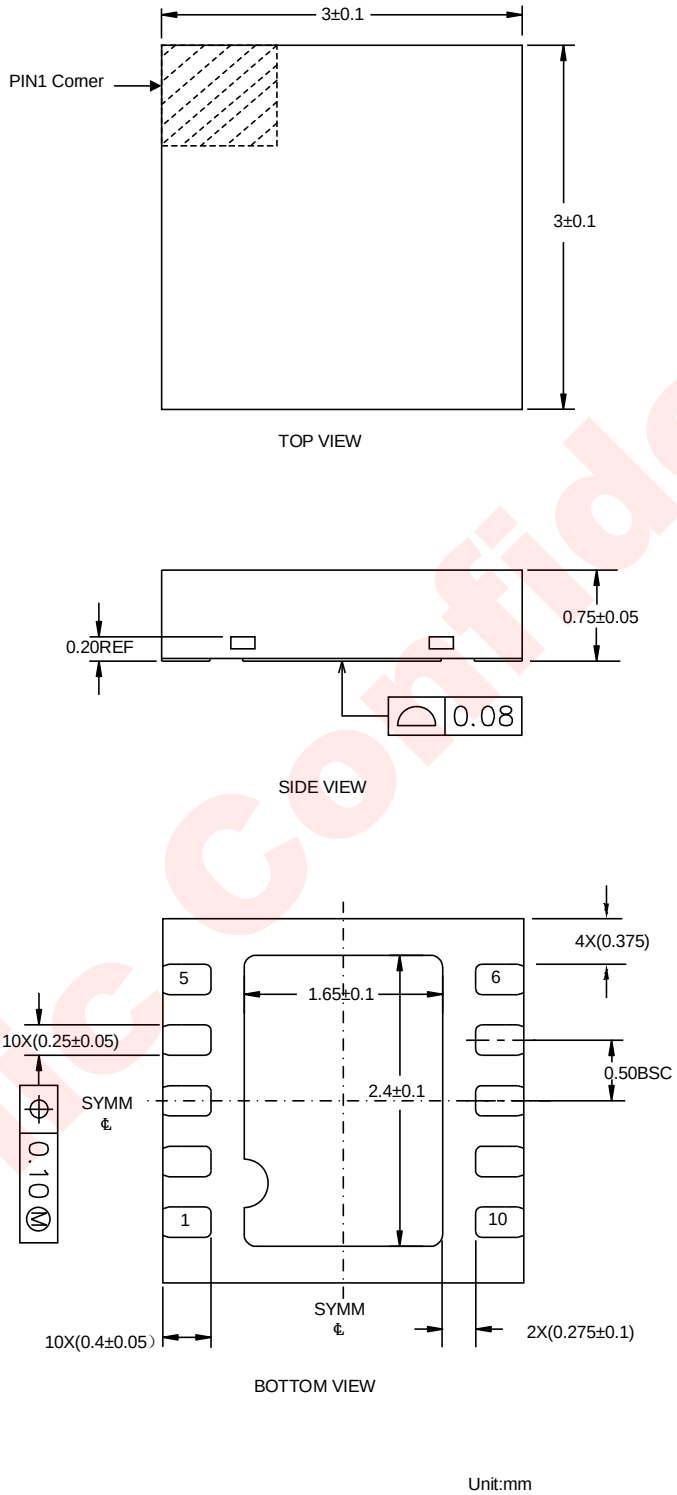
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

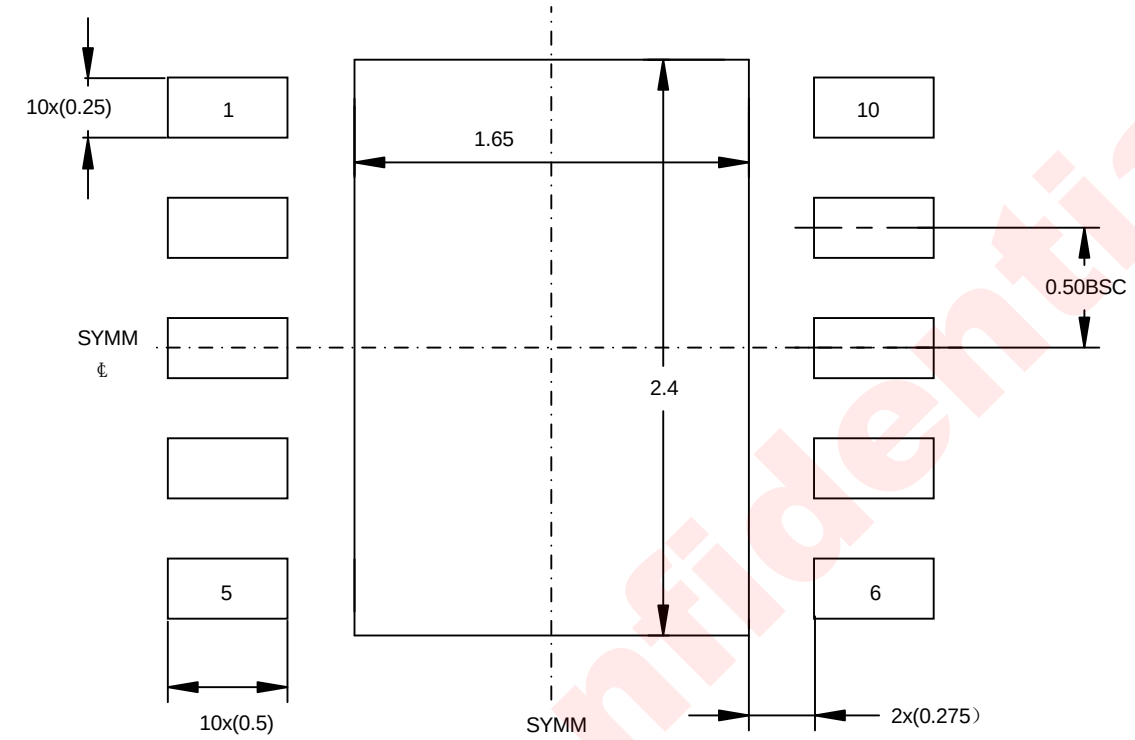
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

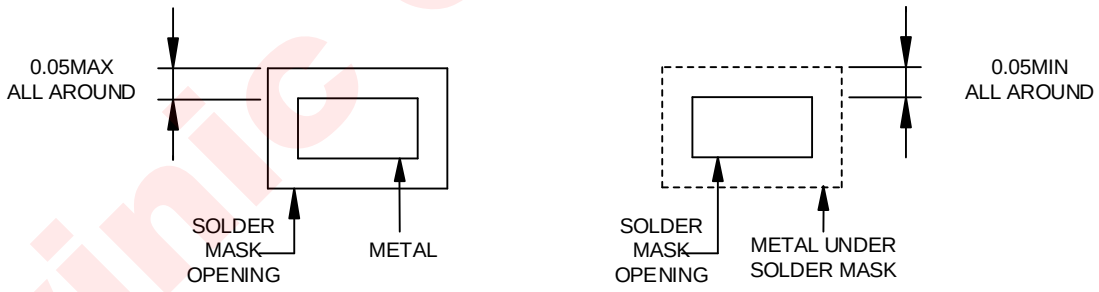
PACKAGE DESCRIPTION



Unit:mm

LAND PATTERN DATA





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit:mm

EVISION HISTORY

Vision	Date	Change Record
V1.0	September 2018	Officially Released

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