High Efficiency Low Noise Large Volume Receiver Stereo TLTR-AGC 3rd Generation Smart K Audio Amplifier

FEATURES

- Triple-Level Triple-Rate AGC algorithm to effectively eliminate noise, pure sound quality
- Innovation high efficient, large drive high voltage 2X DO- Chargepump, efficiency up to 90%
- Highest voltage：8.5V
- Hardware compatible with AW87319CSR
- Low noise：
  - 9 μV (Class AB RCV THD+N=0.4%)
  - 16 μV (Class D RCV THD+N=0.02%)
  - 38 μV (Speaker THD+N=0.02%)
- Support high power receiver stereo application
- Selectable speaker-guard power level：
  0.5W~1.5W@8ohm, 100mW/step
- Selectable receiver-guard power level：
  0.1W~1.5W@8ohm,100mW/step
  0.025W~0.375W@32ohm, 25mW/step
- Output Power：3W@8Ω 3.5W@6Ω
- Speaker & receiver 2-in-1 mode application
- Shutdown current：0.1μA
- Super TDD-Noise suppression
- Excellent pop-click suppression
- Support 1.8V logic I²C control
- High PSRR：-75dB（217Hz）
- Small 2.545mm*2.075mm CSP-18 package

APPLICATIONS

- Smart phone、Tablet PC

DESCRIPTION

AW87339 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality. It is a new high efficiency, low noise, constant large volume, 3rd generation Smart K audio amplifier. AW87339 integrates AWINIC's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87339 integrated high voltage DO-Chargepump technology with efficiency up to 90%, significantly improving the dynamic range of the music output. AW87339 noise floor is as low as to 38μV at speaker mode, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.02% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87339 supports speaker and high power receiver stereo applications, supports speaker and receiver 2-in-1 applications, class AB/D receiver optional, ultra-low noise is 9μV.

AW87339 controls internal registers through the I²C interface. Register parameters include chargepump output voltage, power amplifier gain, Triple-Level Triple-Rate AGC parameters, etc.

AW87339 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87339 features small 2.545mm*2.075mm CSP-18 package.

APPLICATION DIAGRAM

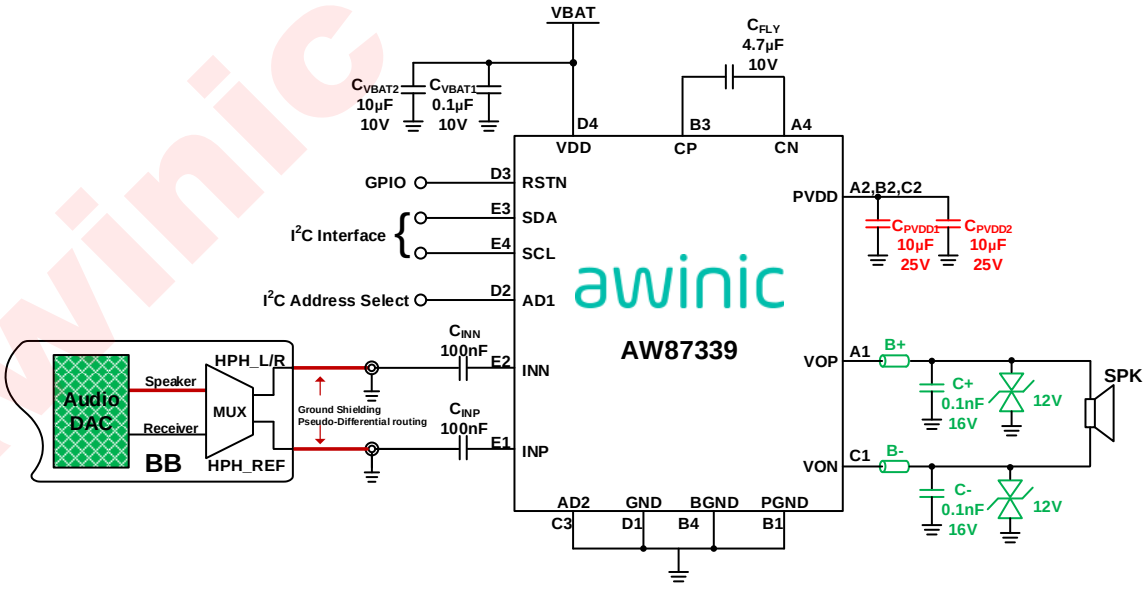


Figure 1 AW87339 Single-ended Input Mode Application Diagram

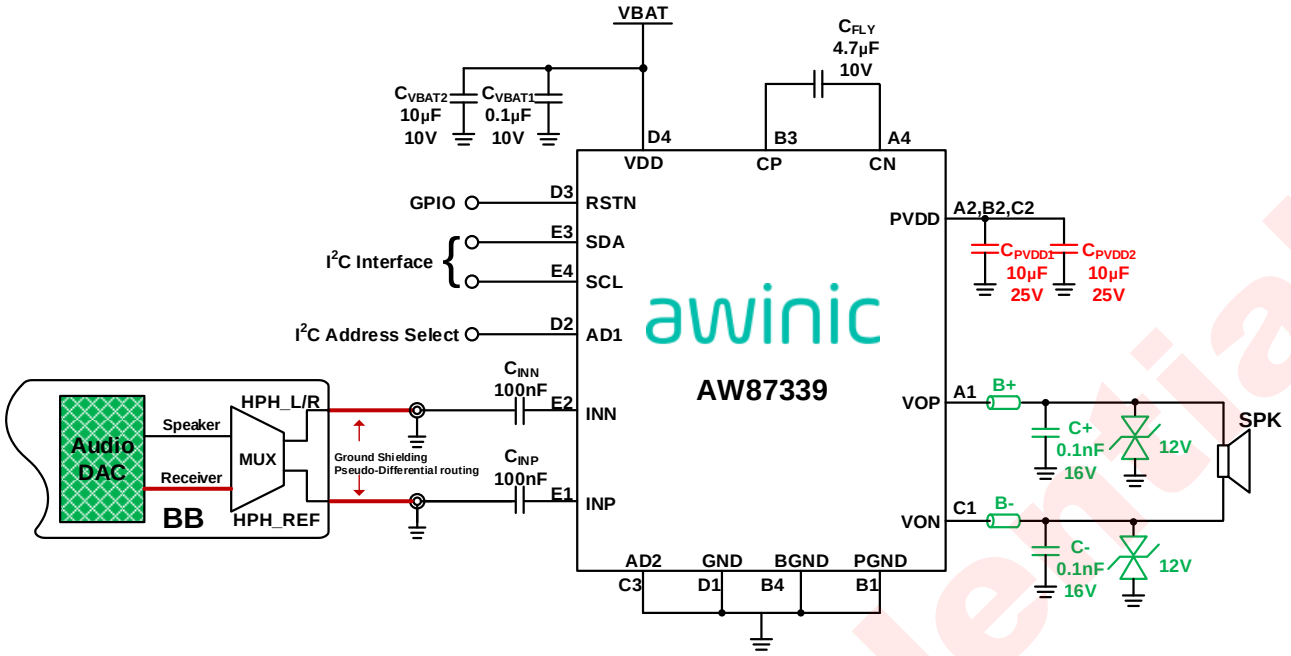


Figure 2 AW87339 Speaker & Receiver 2-in-1 Mode Application Diagram

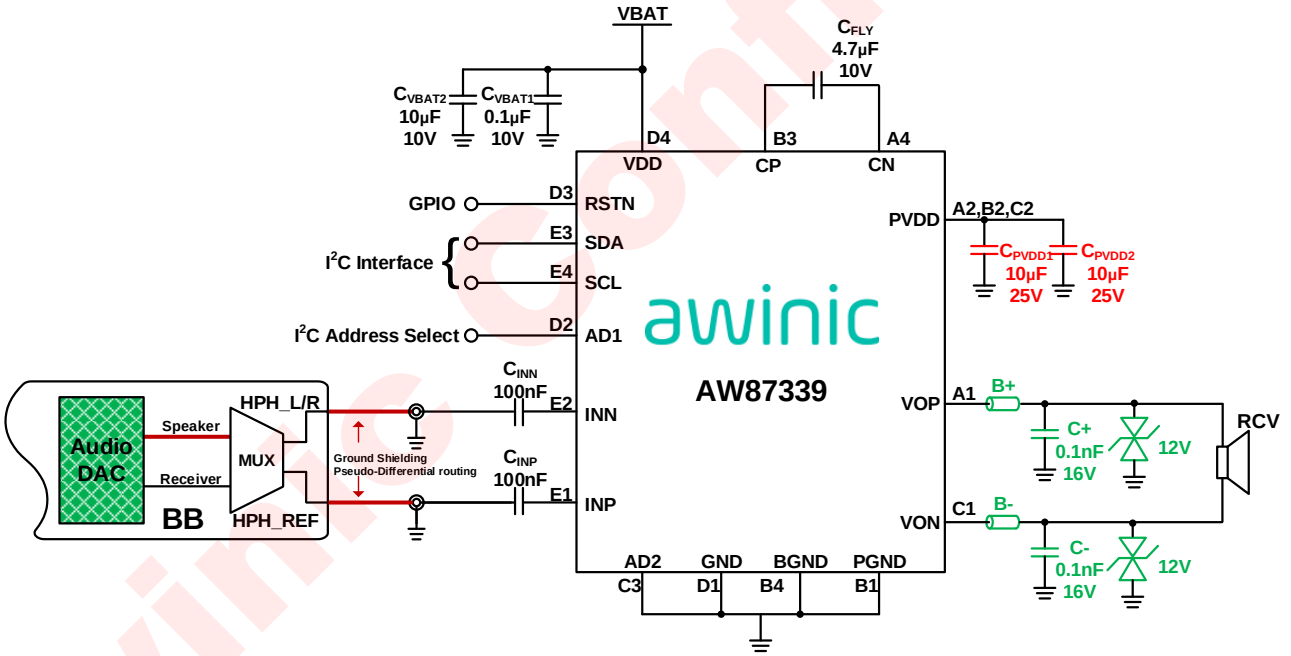


Figure 3 AW87339 High Power Receiver Stereo Mode Application

PIN CONFIGURATION AND TOP MARK

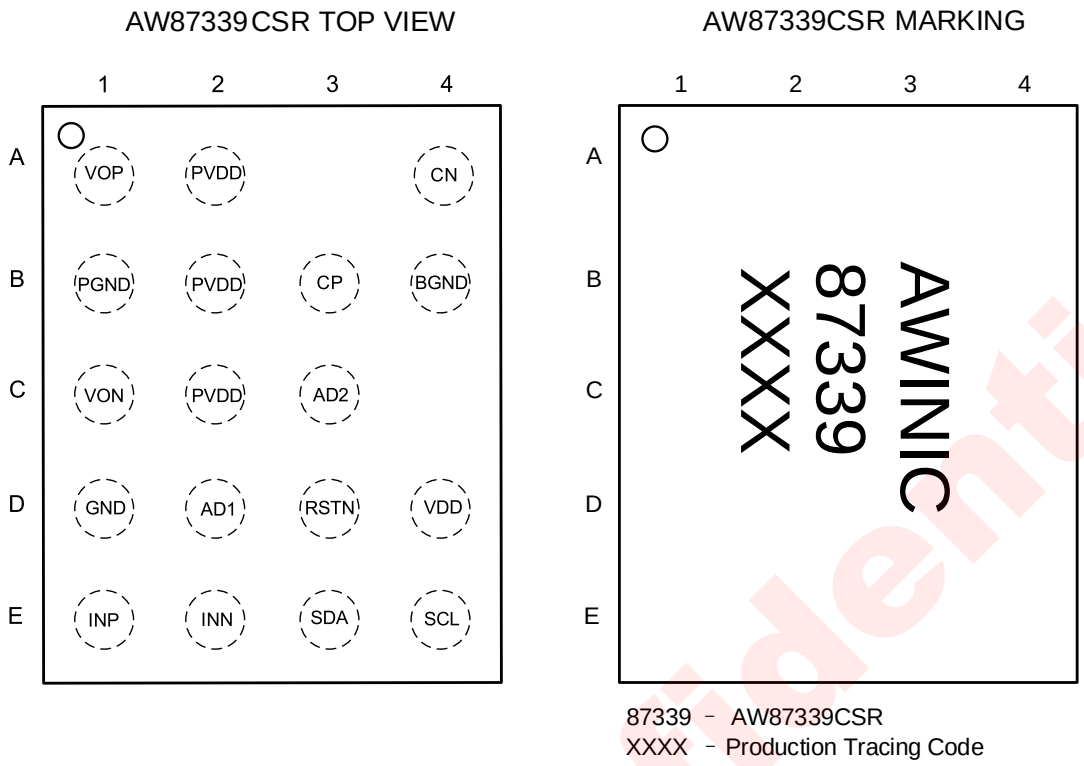


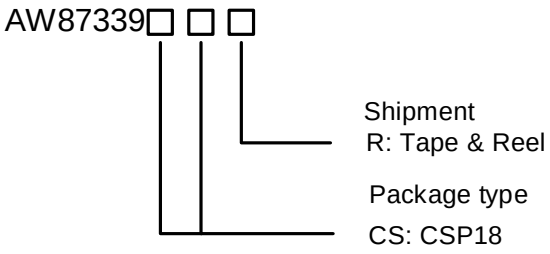
Figure 4 AW87339 Pin Diagram Top View and Device Marking

PIN DESCRIPTION

Number	Symbol	Description
A1	VOP	Positive audio output terminal
A2,B2,C2	PVDD	Chargepump output voltage
A4	CN	Negative input chargepump flying capacitor
B1	PGND	Amplifier power ground
B3	CP	Positive input chargepump flying capacitor
B4	BGND	Chargepump power ground
C1	VON	Negative audio output terminal
C3	AD2	I^2C address pin2
D1	GND	Ground
D2	AD1	I^2C address pin1
D3	RSTN	Reset pin, active low reset, the internal 300KΩ pull-down resistor in chip
D4	VDD	Power supply
E1	INP	Positive audio input terminal
E2	INN	Negative audio input terminal
E3	SDA	I^2C-bus data input/output
E4	SCL	I^2C-bus clock input

ORDERING INFORMATION

Product Type	Operation temperature range	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87339CSR	-40°C～85°C	CSP-18	87339	MSL1	ROHS+HF	Tape and Reel 6000 pcs



FUNCTIONAL DIAGRAM

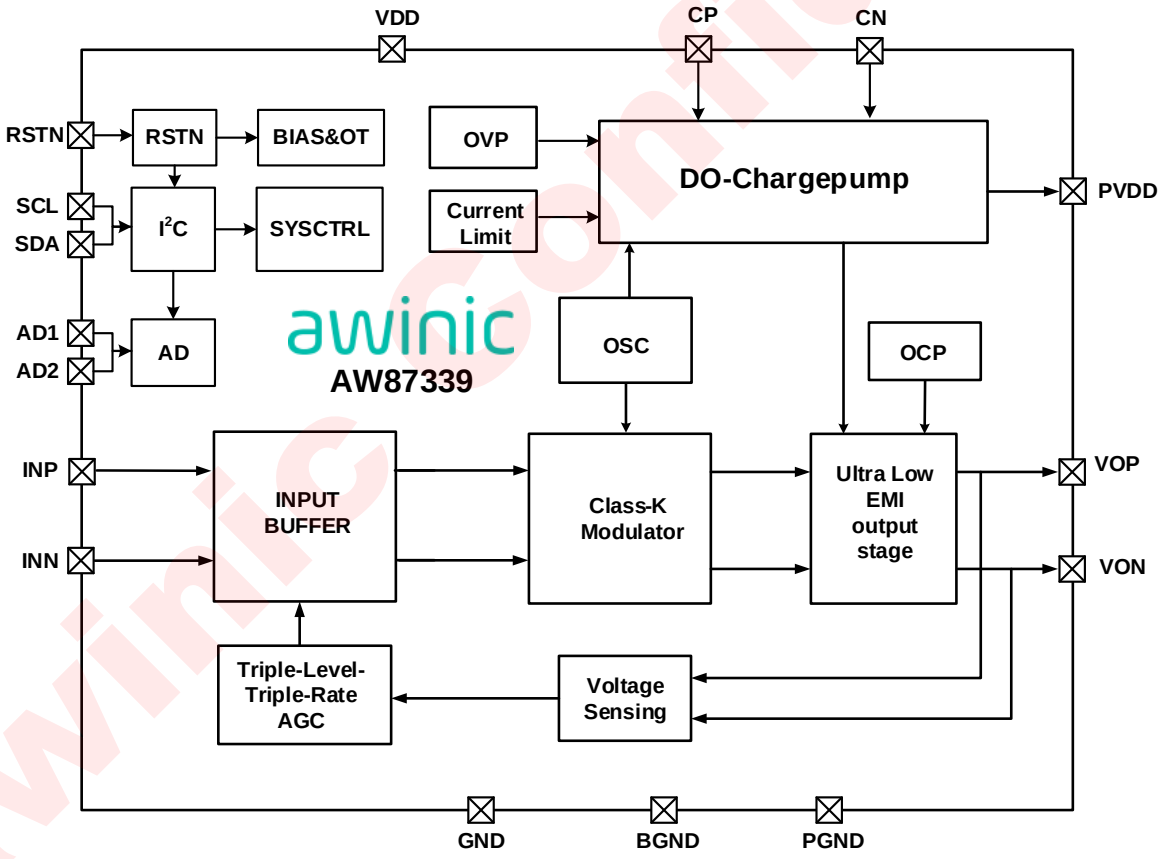


Figure 5 AW87339 Functional Diagram

ABSOLUTE MAXIMUM RATING (Note1)

Parameter	Range
Supply Voltage V_{DD}	-0.3V to 6V
Chargepump output voltage PVDD	-0.3V to 9.5V
VOP,VON	-0.3V to PVDD+0.3V
CP	-0.3V to PVDD+0.3V
CN	-0.3V to VDD+0.3V
INN,INP	-0.3V to VDD+0.3V
Minimum load resistance R_L	5Ω
Package Thermal Resistance θ_{JA}	60°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (Note 2)	
HBM（human body model）	±2kV
MM（machine model）	±400V
CDM（charged-device model）	±2kV
Latch-up	
Test Condition：JEDEC STANDARD NO.78E SEPTEMBER 2016	+IT：450mA -IT：-450mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

Test method of the charge device model: JEDEC EIA/JESD22-C101F

Test method of the machine model: JEDEC EIA/JESD22-A115

ELECTRICAL CHARACTERISTICS

Test condition：T_A=25°C, VDD=3.6V, PVDD OVP=8V, R_L=8Ω+33μH, f=1kHz（unless otherwise noted）

Parameter		Test conditions		Min	Typ	Max	Units
V_{DD}	Power supply voltage			2.8		5.5	V
UVLO	Under-voltage protection voltage				2.5		V
	Under-voltage protection hysteresis voltage				100		mV
V_{IH}	RSTN, SCL, SDA, AD1, AD2 high-level input voltage			1.3		V_{DD}	V
V_{IL}	RSTN, SCL, SDA, AD1, AD2 low-level input voltage			0		0.45	V
I_{SD}	Shutdown current	V_{DD}=3.6V, RSTN=0V			0.1	1	μA
T_{TG}	Thermal AGC start temperature threshold				150		℃
T_{TGR}	Thermal AGC exit temperature threshold				130		℃
T_{SD}	Over temperature protection threshold				160		°C
T_{SDR}	Over temperature protection recovery threshold				130		°C
T_{ON}	Turn-On time				40		ms
DO-Chargepump							
PVDD	The maximum Output voltage	V_{DD}=2.8V to 4V, PVDD OVP=8V			2*VDD		V
		V_{DD} >4V			8 (Note3)		V
OVP	OVP voltage	V_{DD} >4V			8 (Note3)		V
	OVP hysteresis voltage	V_{DD} >4V			50		mV
F_{CP}	Chargepump operating frequency	V_{DD}=2.8V to 5.5V		1.2	1.6	2.0	MHz
η_{CP}	Chargepump efficiency	V_{DD}=4.2V, I_{load}=200mA			90		%
T_{ST}	Softstart Time	No load, COUT=4.7μF		1	2	3	ms
I_{SHORT}	Current limit when PVDD short to ground			200	300	400	mA
Class K MODE							
V_{OS}	Output offset voltage	No input		-30	0	30	mV
η	total efficiency（CP+Class D）	V_{DD}=4.2V, Po=2.5W, R_L=8Ω+33μH, PVDD OVP=8.5V			80		%
I_q	Speaker Quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			14		mA
Vinp	Recommended input signal amplitude	V_{DD}=2.8V to 5.5V				1	Vp
Fosc	Modulation frequency	V_{DD}=2.8V to 5.5V		600	800	1000	kHz
Pagc	TLTR AGC power	R_L=8Ω+33μH		0.72	0.8 (Note3)	0.88	W
		R_L=6Ω+33μH		0.96	1.067(Note3)	1.17	W
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vpp_sin=200mV	217Hz		-75		dB
			1kHz		-72		dB
SNR	Signal-to-noise ratio	V_{DD}=4.2V, PVDD OVP=8.5V, Po=3W, Av=8V/V , THD+N=1%,R_L=8Ω+33μH,			102		dB

Parameter		Test conditions		Min	Typ	Max	Units
SNR	Signal-to-noise ratio	V_{DD}=4.2V, PVDD OVP=8.5V, Po=0.8W, Av=8V/V, R_L=8Ω+33μH			94		dB
E_N	Speaker Output noise	Av=16 V/V	20Hz to 20kHz, input ac grounded, A-weighting		48		μV
		Av=8 V/V			38		
Av	Speaker gain	V_{DD}=2.8V to 5.5V			24 (Note3)		dB
Rini	Speaker Inner input resistance	Av=16 V/V			9		kΩ
	Speaker Inner input resistance	Av=8 V/V			18		
Fin	Speaker input Cut-off frequency	Cin=68nF, Av=16 V/V			260		Hz
	Speaker input Cut-off frequency	Cin=68nF, Av=8 V/V			130		
	Speaker input Cut-off frequency	Cin=100nF, Av=16 V/V			177		
	Speaker input Cut-off frequency	Cin=100nF, Av=8 V/V			88.5		
THD+N	Total harmonic distortion + noise	V_{DD}=4.2V, Po=0.6W, R_L=8Ω+33μH, f=1kHz, PVDD OVP=8.5V			0.02		%
Po	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD OVP=8.5V			3.01		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD OVP=8.5V			3.64		W
		THD+N=1%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD OVP=8.5V			3.51		W
		THD+N=10%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD OVP=8.5V			4.26		W
2-in-1 Receiver MODE							
I_q	D Receiver quiescent current（overall）	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			5.8		mA
	AB Receiver quiescent current（overall）	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			4.3		mA
η	D Receiver efficiency	V_{DD}=4.2V,Po=0.8W, R_L=8Ω+33μH			87		%
	AB Receiver efficiency	V_{DD}=4.2V,Po=0.8W, R_L=8Ω+33μH			67		%
Av	gain	V_{DD}=2.8V to 5.5V			0 (Note3)		dB
Rini	D Receiver Inner input resistance	Av=1 V/V			96		kΩ
	AB Receiver Inner input resistance	Av=1 V/V			48		kΩ
Fin	D Receiver input cut-off frequency	Cin=100nF, Av=1 V/V			17		Hz
	AB Receiver input cut-off frequency	Cin=100nF, Av=1 V/V			33		Hz
E_N	D Receiver output noise	Av=1V/V	20Hz to 20kHz, input ac grounded, A-weighting		16		μV
	AB Receiver output noise	Av=1V/V			9		μV
THD+N	Total harmonic distortion + noise	V_{DD}=4.2V, Po=0.1W,R_L=8Ω+33μH, f=1kHz, D Receiver			0.02		%
		V_{DD}=4.2V, Po=0.1W,R_L=8Ω+33μH, f=1kHz, AB Receiver			0.4		%
PSRR	D Receiver Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		-78		dB
			1kHz		-76		dB
	AB Receiver Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		-69		dB
			1kHz		-68		dB
Po	D Receiver Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.95		W

Parameter		Test conditions	Min	Typ	Max	Units
Po	D Receiver Output Power	THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V		1.19		W
	AB Receiver Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V		0.875		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V		1.15		W
Triple-Level Triple-Rate AGC						
T_{AT1}	AGC1 Attack Time			0.08 (Note3)		ms/dB
T_{AT2}	AGC2 Attack Time			0.64 (Note3)		ms/dB
T_{AT3}	AGC3 Attack Time			41 (Note3)		ms/dB
T_{RLT}	Release time			21 (Note3)		ms/dB
A_{MAX}	The maximum attenuation gain	V_{DD}=2.8V to 5.5V , RCV_LOAD=0		-13.5		dB
		V_{DD}=2.8V to 5.5V , RCV_LOAD=1		-10.5		dB

Note 3：*Registers are adjustable; Refer to the list of registers.*

MEASUREMENT SETUP

AW87339 features switching digital output, as shown in Figure 6. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

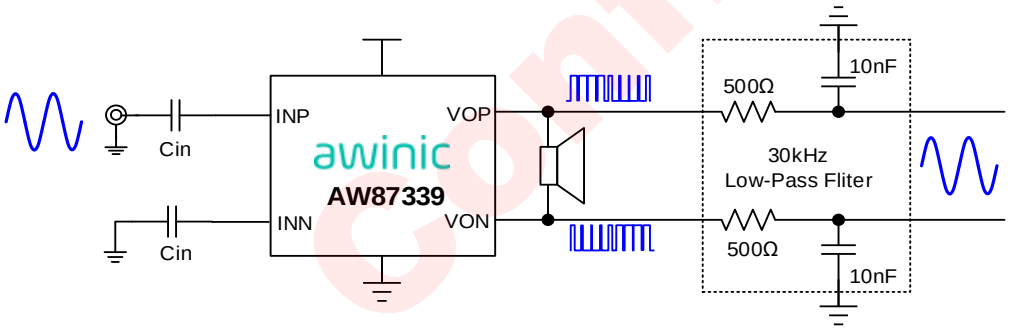


Figure 6　AW87339 Test Setup

Low pass filter uses resistance and capacitor values listed in Table 1.

R_{filter}	C_{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Table 1　AW87339 Recommended Values for Low Pass Filter

Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal , as shown in Figure 7：

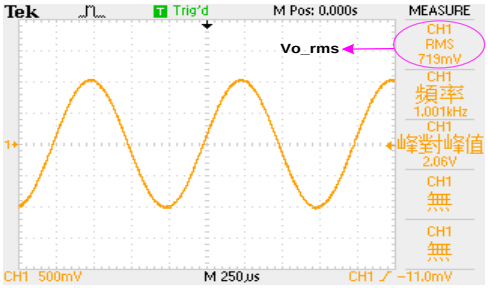


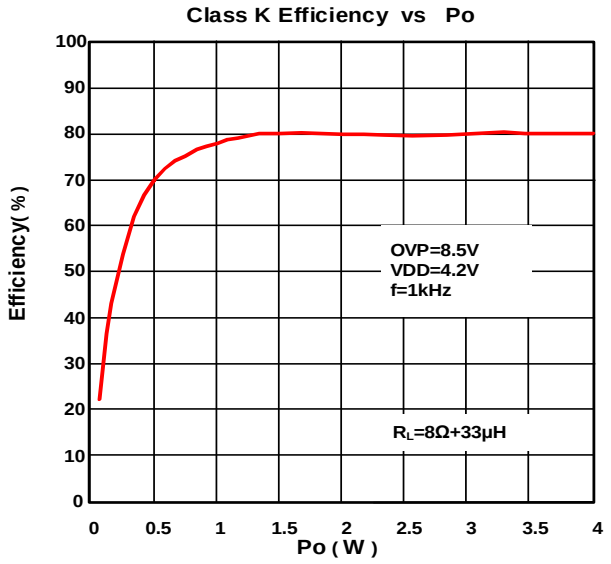
Figure 7 Output RMS Value

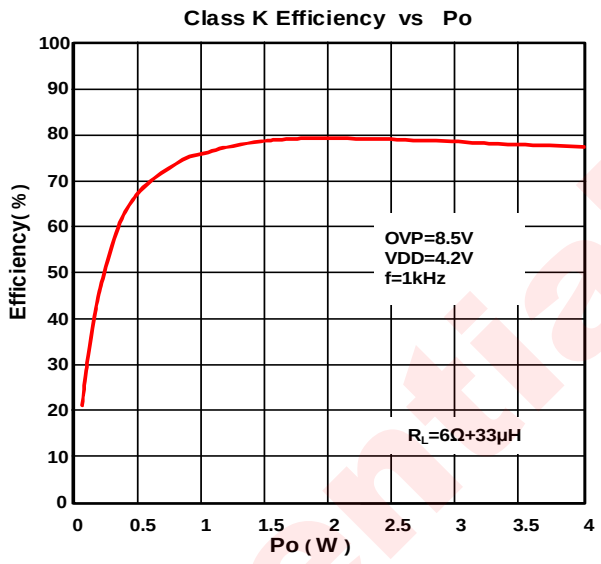
The power calculation of Speaker is as follows：

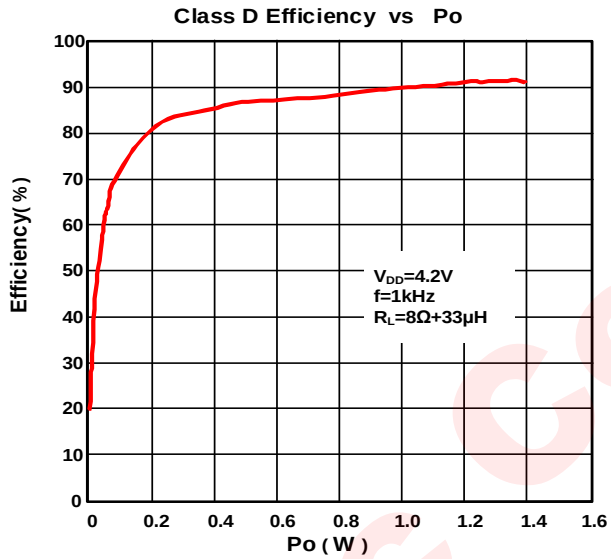
$$P_L = \frac{(V_{O\_rms})^2}{R_L}$$

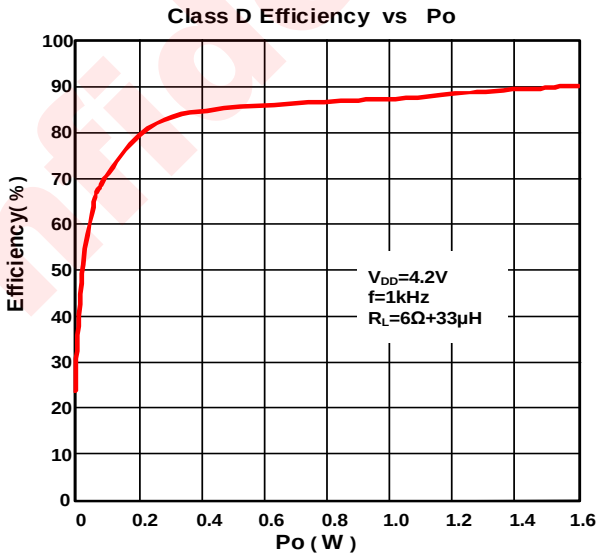
R_L: load impedance of the speaker

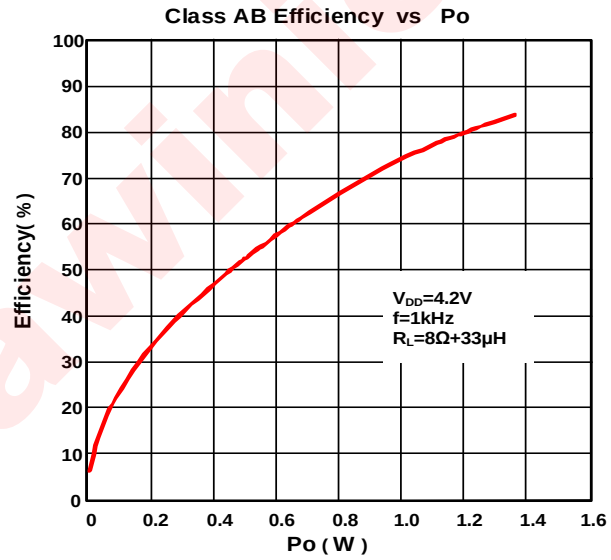
TYPICAL CHARACTERISTICS

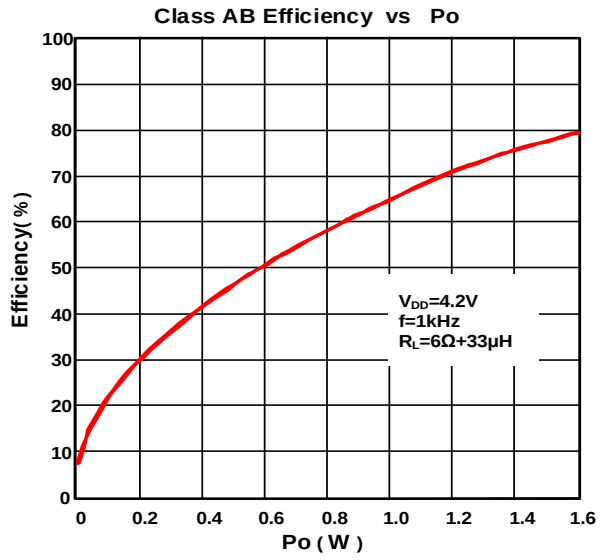




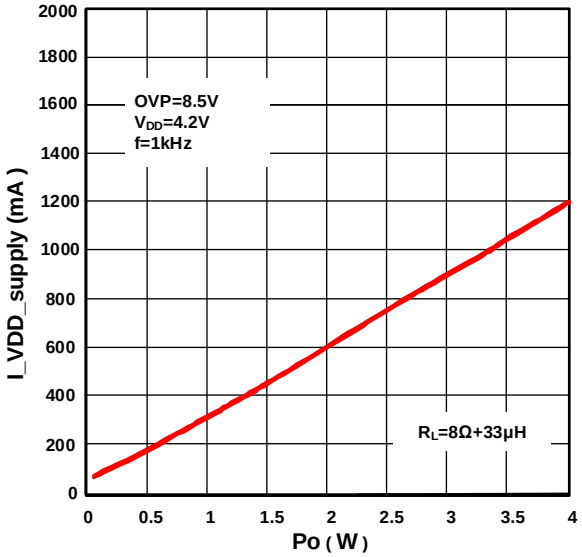




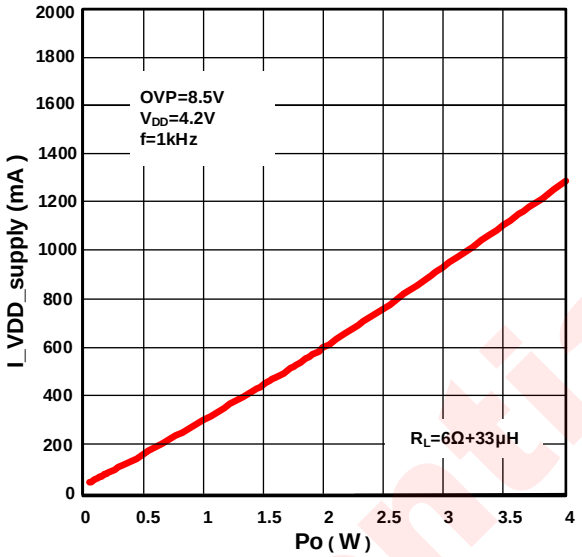




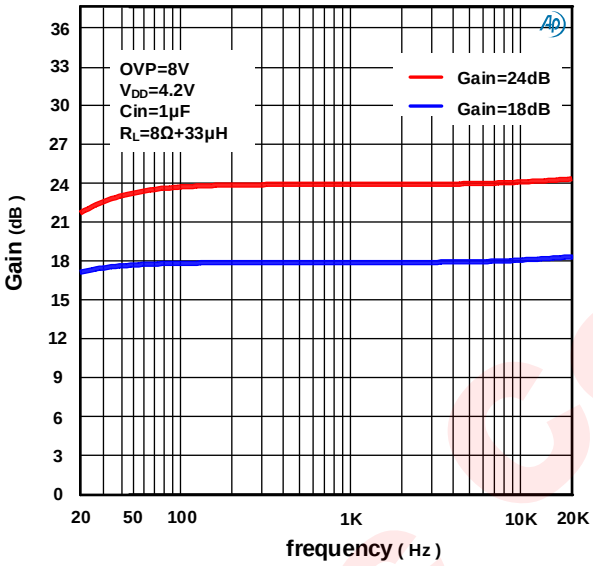
Class K I_VDD_supply vs Po



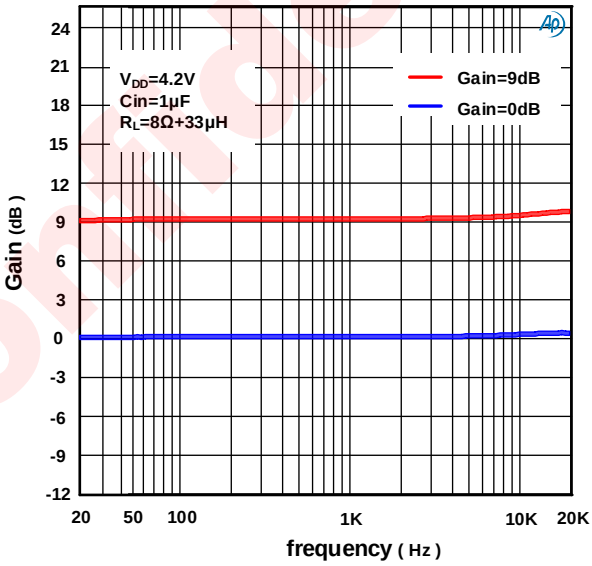
Class K I_VDD_supply vs Po



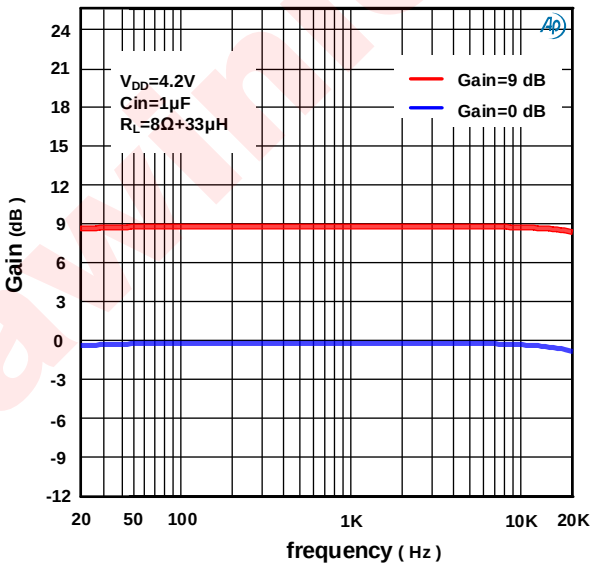
Class K Gain vs frequency



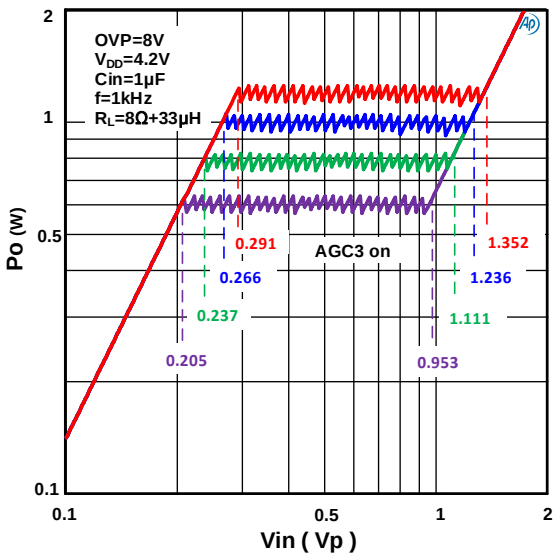
Class D Gain vs frequency



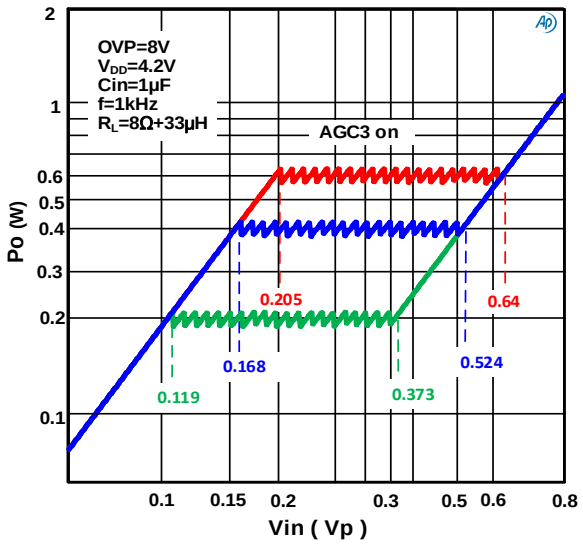
Class AB Gain vs frequency



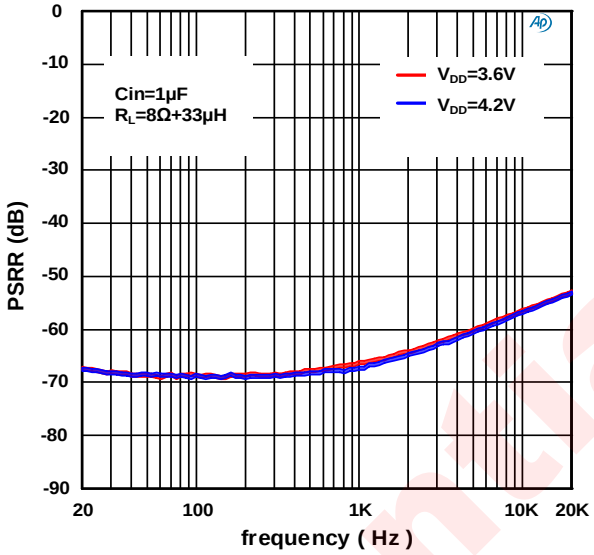
Po vs Vin



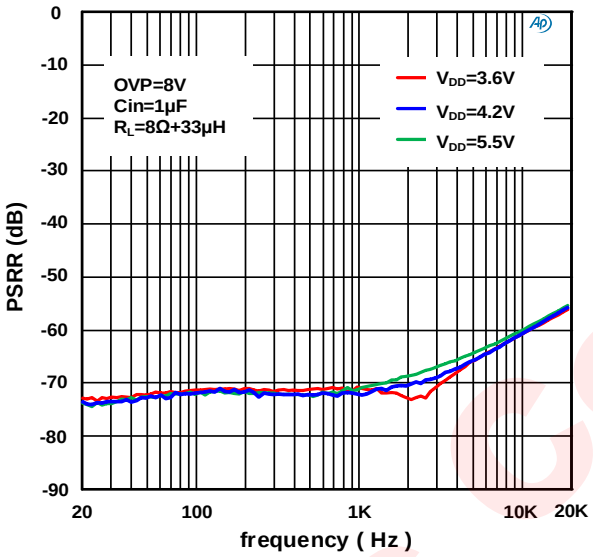
Po vs Vin



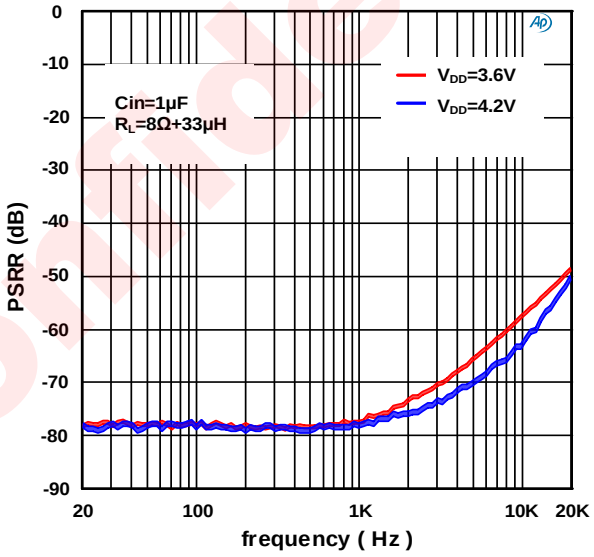
Class AB PSRR vs frequency



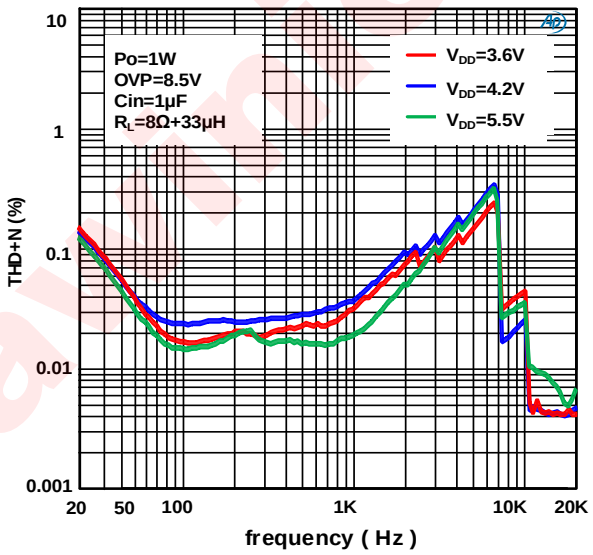
Class K PSRR vs frequency



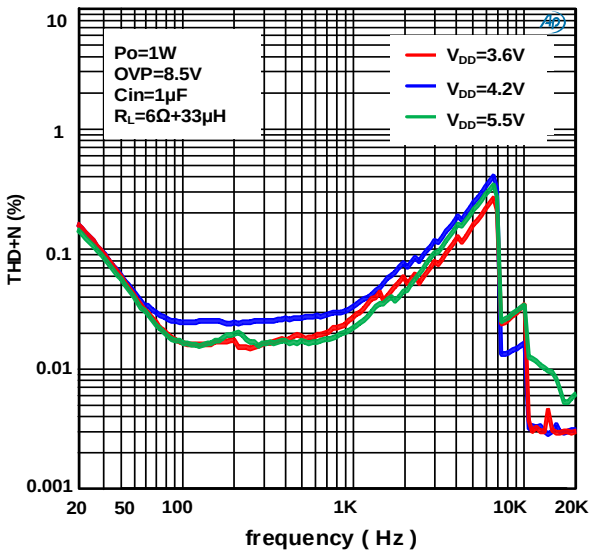
Class D PSRR vs frequency



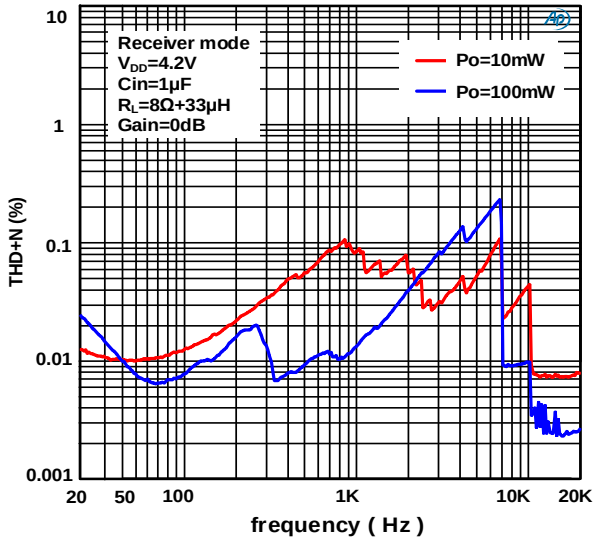
Class K THD+N vs frequency



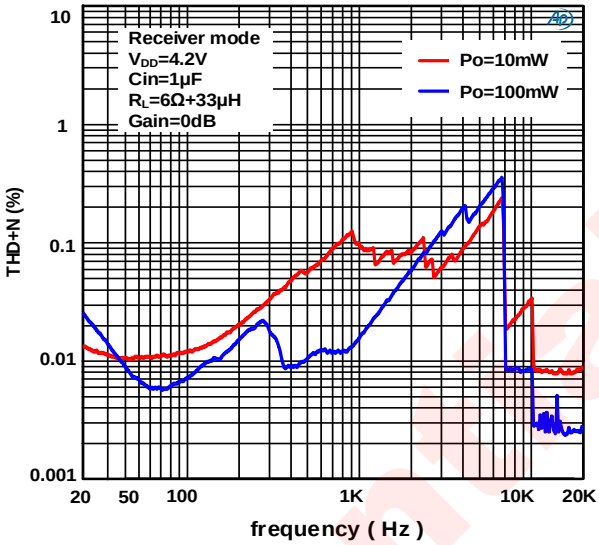
Class K THD+N vs frequency



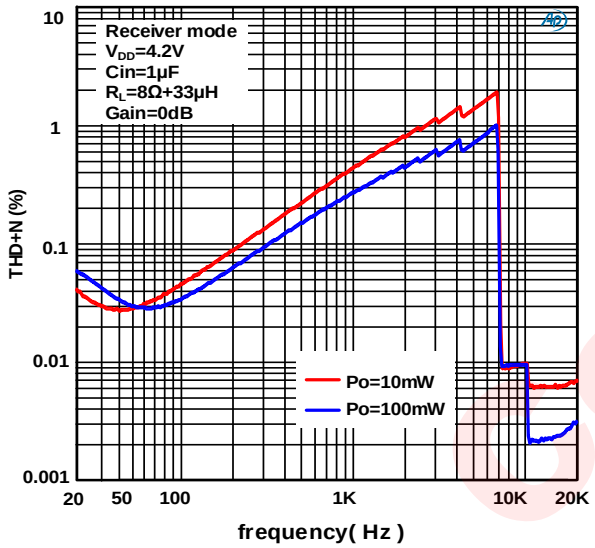
Class D THD+N vs frequency



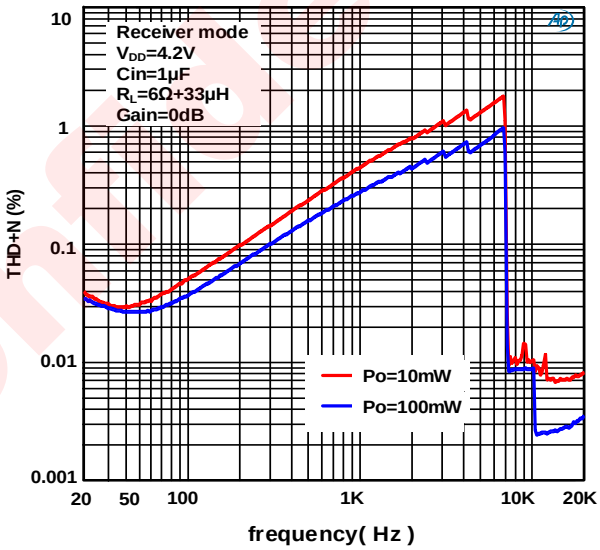
Class D THD+N vs frequency



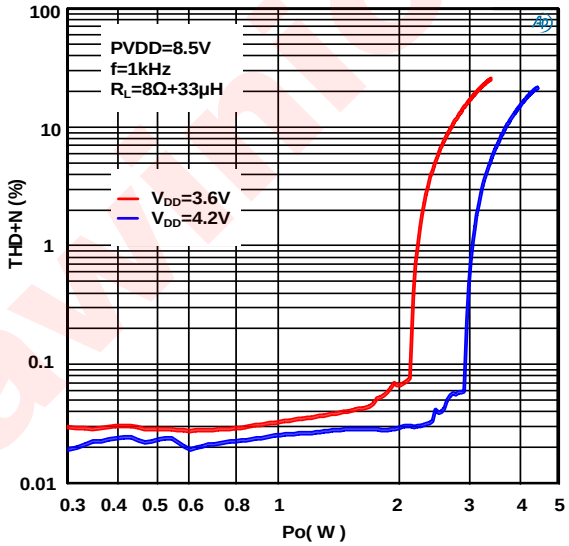
Class AB THD+N vs frequency



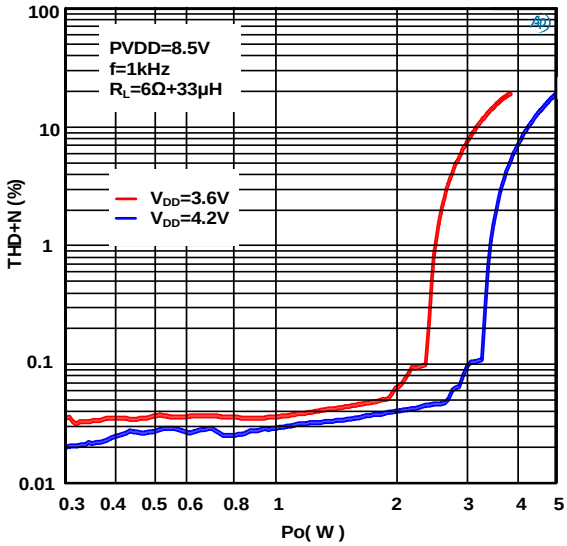
Class AB THD+N vs frequency



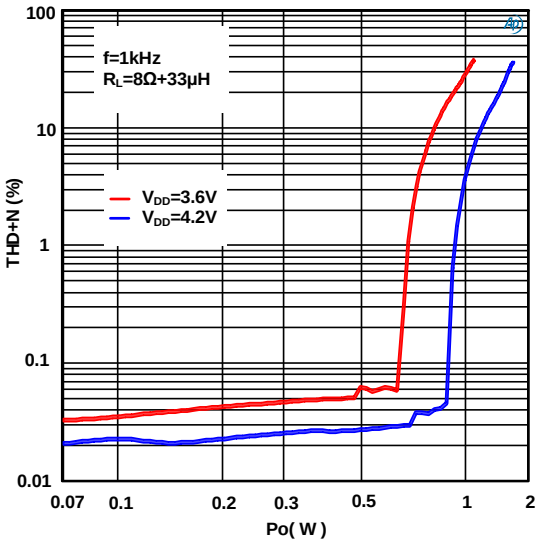
Class K THD+N vs Po



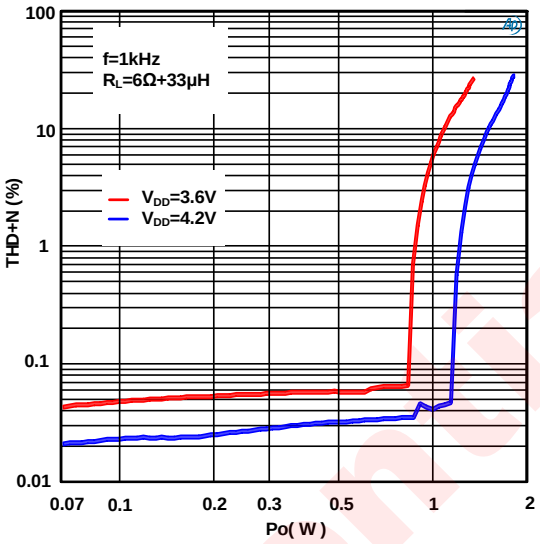
Class K THD+N vs Po



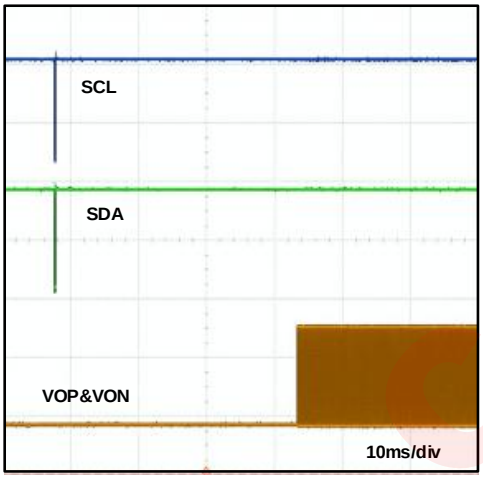
Class D THD+N vs Po



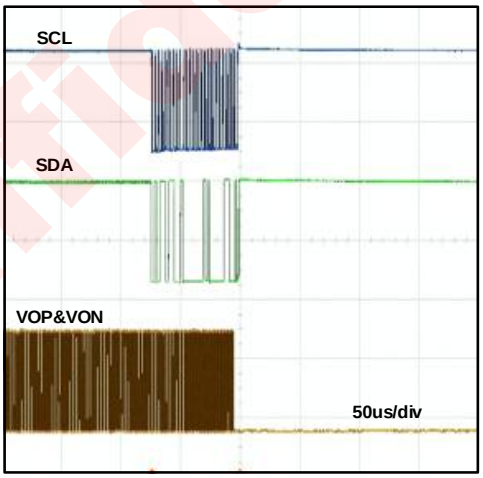
Class D THD+N vs Po



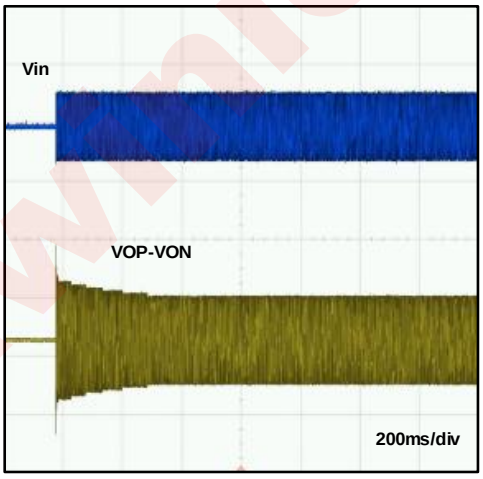
Start-up sequence



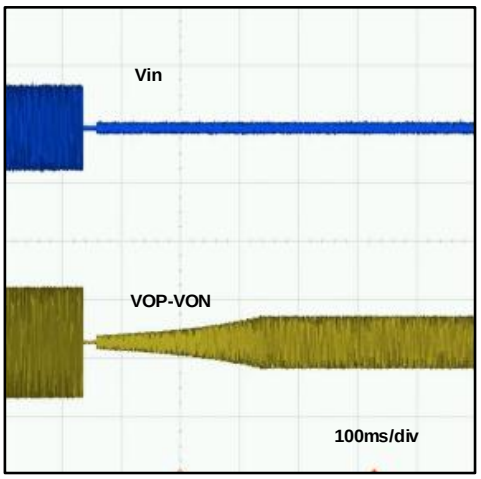
Shutdown sequence



Triple-Level Triple-Rate AGC Attack Timing



Triple-Level Triple-Rate AGC Release Timing



WORKING PRINCIPLE

AW87339 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, 3rd generation Smart K audio amplifiers. AW87339 integrates AWINIC's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87339 integrated efficiency up to 90% of High voltage DO-Chargepump technology, significantly improving the dynamic range of the music output.AW87339 noise floor is as low as to 38μV, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.02% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87339 supports speaker and high power receiver stereo applications, supports speaker and receiver 2-in-1 applications, AB/D Receiver optional, ultra-low noise is 9μV.

AW87339 controls internal registers through the I^2C interface. Register parameters include chargepump output voltage, power amplifier gain, Triple-Level Triple-Rate AGC parameters etc.

AW87339 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87339 features small 2.545mm*2.075mm CSP-18 package.

CONSTANT OUTPUT POWER

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually. So, it is hard to provide high quality music within the battery voltage range. AW87339 uses unique Triple-Level Triple-Rate technology, within lithium battery voltage range (3.3V~4.35V), to guarantee that output power is constant, and the output power will not drop along with the decrease of lithium battery voltage. In the process of using the phone, even if the battery voltage drops, AW87339 can still provide high quality large volume music enjoyment. The output power of AW87339 can be configured from 0.5W to 1.5W via I^2C, matching general speakers. Unique Triple-Level Triple-Rate AGC technology can bring high-quality music enjoyment.

Triple-Level Triple-Rate AGC technology

AWINIC proprietary Triple-Level Triple-Rate AGC technology is designed for the protection of the high voltage power amplifier, which is divided into AGC1, AGC2 and AGC3 power levels, to obtain a large volume while maintaining excellent sound quality.

In practical applications, speaker can continuously work long hours at rated power, and also can work short-term at high power. For example, in the standard reliability of the loudspeaker experiment, the powder of peak power reached around four times of the rated power. For achieving larger volume and better sound quality, speakers need to work at high power for short periods of time, in order to improve the performance of the speaker. AW87339 Triple-Level Triple-Rate AGC technology can fit the speaker better and perform better overall performance. AGC1 prevents output signal clipping by detecting output voltage in a very short time after clipping, which can effectively restrain the noise clipping; AGC2 can improve the dynamic range of the music in a relatively short period of time; AGC3 can make the speaker work under rated power, which can effectively improve the volume and protect the speaker. Triple-Level Triple-Rate AGC can obtain more excellent overall performance.

Triple-Level Triple-Rate AGC detects the peak output voltage of the power amplifier, when the output peak voltage is higher than the compression threshold voltage, the amplifier gain decreases in 0.5dB step. When the output peak voltage is lower than the release threshold voltage, the amplifier gain is recovery to the initial gain in 0.5dB step. The detailed process can be described as follows:

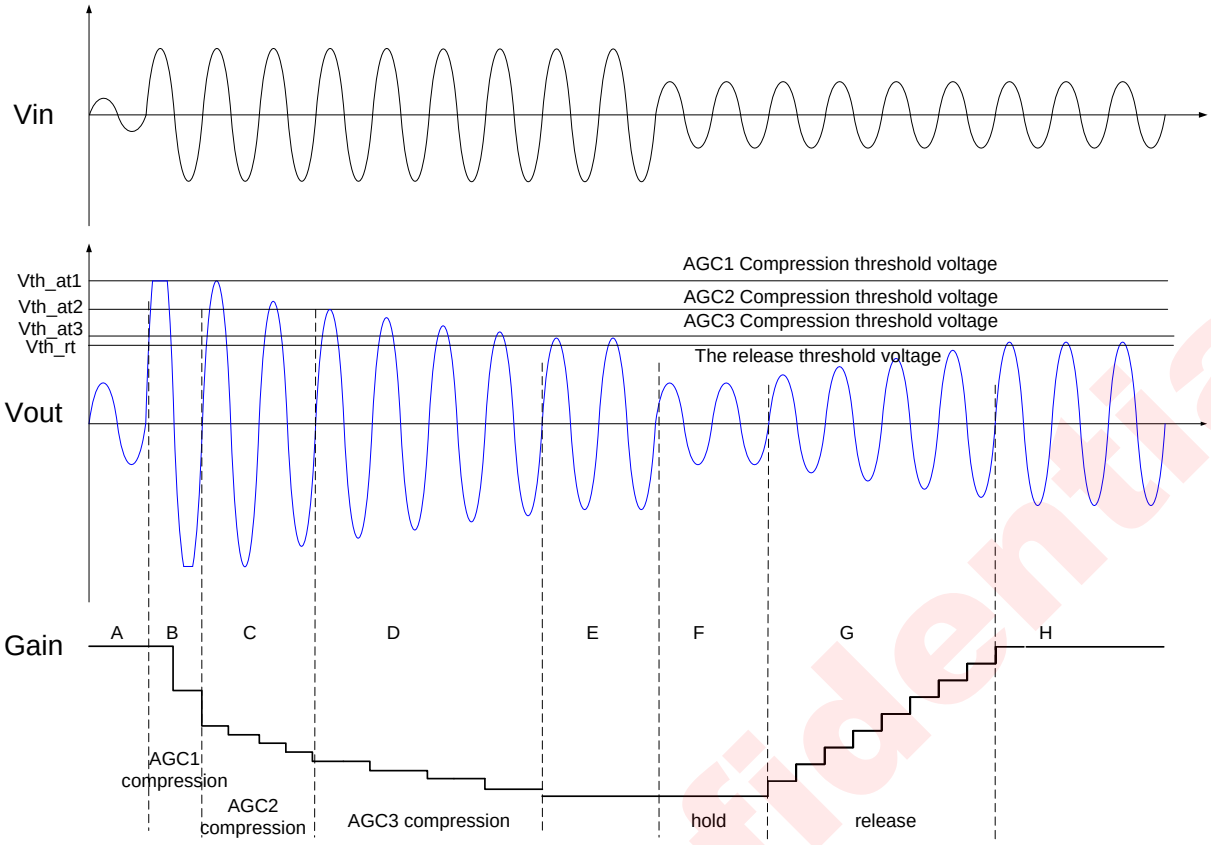


Figure 8 Triple-Level Triple-Rate AGC Operation Principle

A: Small input signal, the output voltage is lower than threshold voltage Vth of AGC, AGC don't work.

B: Input voltage becomes large. It leads to the output voltage clipping, AGC1 starts fast compression, the attack time is set through the I^2C register 0x0Ah [3:2], when the output voltage is higher than Vth_at1, and gain register began to decrease. Gain decreases when the output signal passes through the zero. It eliminates the clipping noise as soon as possible.

C: When the output voltage is not clipping and higher than threshold voltage Vth_at2, AGC2 starts work, the attack time is set through the I^2C register 0x09h [4:2], gain register begins to decrease at a certain rate. Gain register began to decrease. Gain decreases when the output signal passes through the zero. The output voltage gradually decreases to below the AGC2 attack threshold voltage Vth_at2, which can protect the speaker and enhance the sound.

D: When the output voltage is lower than the AGC2 attack threshold voltage Vth_at2 and higher than the AGC3 attack threshold voltage Vth_at3, AGC3 starts work, the attack time is set through the I^2C register 0x07h [4:2], and gain register began to decrease at a certain rate. Gain decreases when the output signal passes through the zero, so the output voltage gradually decreases to below of the AGC3 attack threshold voltage Vth_at3, matching the speaker to achieve greater volume and better sound quality.

E: Triple-Level Triple-Rate AGC attack time ends, Amplifier output power is close to the speaker rated power.

F: Input voltage decreases, the output voltage becomes lower than the release threshold voltage Vth_rt, at this point, gain remains the same in the maintain time (10ms~20ms).

G: Gain increases when the time of output voltage lower than the release threshold voltage Vth_rt is longer than the holding time. The release time can be set through I^2C register 0x07h [7:5].

H: Stop release when the output signal is larger than the release threshold or the gain is equal to the initial value. The output voltage remains constant.

Triple-Level Triple-Rate AGC can switch independently according to different application requirements.

Such as close AGC1 and AGC2, retain only AGC3, this is the single-AGC mode, similar to AW8736 (AGC3 attack time is set to 1.28ms/dB; release time is set to 41ms/dB); Close AGC2, open AGC1 and AGC3, this is Multi_level AGC. It can be set similar to AW8738 (AGC1 attack time is set to 80us/dB; AGC3 attack time is set to 0.64ms/dB; release time is set to 10.24ms/dB).

Zero-Crossing Adjustment Technology

Traditional AGC doesn't contain zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click.

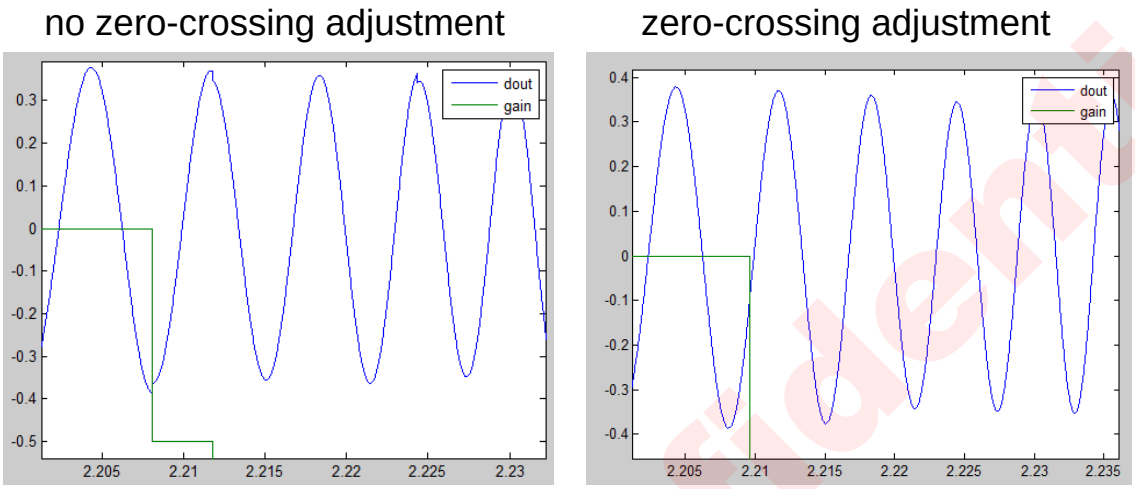


Figure 9 Zero-adjust Comparison

As shown above, when there is no zero-adjustment technology, it can be seen the obvious step change at the peak of large signal, the steps sound slightly perceived in special audio. Gain changes at zero. The steps disappear by using zero-crossing detection technology. Using zero detection technology can make the music pure and natural.

DO-Chargepump

AW87339 features DO-chargepump technology, with high efficiency and high drive capability, operating frequency 1.6MHz, built-in soft start circuit, current limiting control loop and over-voltage control loop to ensure circuit stable and reliable work.

High efficiency

AW87339 features DO-chargepump architecture, the output voltage PVDD is twice of the input voltage VDD, ideal efficiency up to 100%. The efficiency of the DO-chargepump is the ratio of the output power to input power:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\%$$

For example, in an ideal M times the DO-chargepump, the input current I_{IN} is M times of I_{OUT}, the efficiency formula is:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\% = \frac{V_{OUT} * I_{OUT}}{V_{IN} * M * I_{OUT}} * 100\% = \frac{V_{OUT}}{M * V_{IN}} * 100\%$$

Where M is the operating mode variable of the chargepump, V_{IN} is the output voltage of chargepump, I_{OUT} is the load current. For the DO-chargepump, the output voltage is twice of the input voltage, can greatly

improve the power efficiency, taking into account the chargepump internal switching losses and IC quiescent current loss, the actual efficiency is as high as 90%.

AW87339 DO-chargepump can be set to pass-through mode and 2X chargepump mode via the register 0x01h [2] to supply power to the Class D output stage.

Chargepump structure

The basic diagram of the chargepump shows in Figure 10, the chargepump in AW87339 has four switches, the output voltage PVDD can reach twice of the input voltage through the four switches of the timing control.

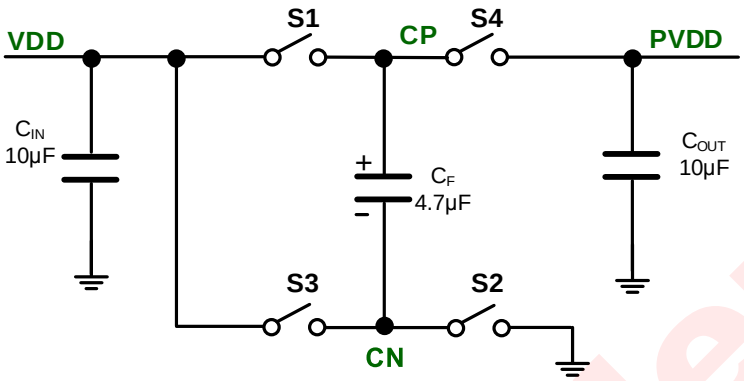


Figure 10 Chargepump Schematic Diagram

The chargepump works with two phases, in Φ1, as shown in the Figure 11：S1, S2 on, VDD charges the capacitor C_F.

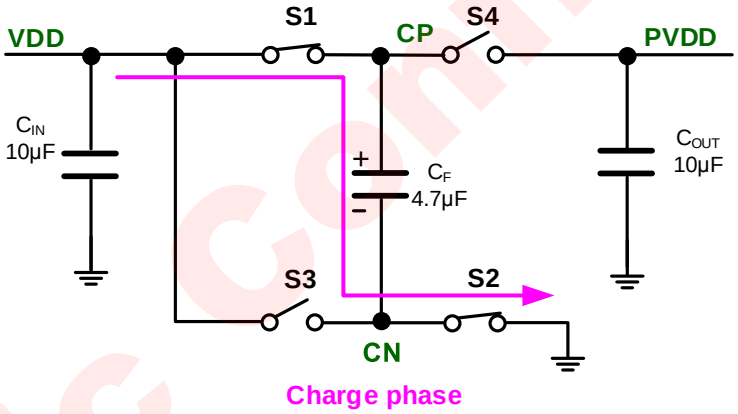


Figure 11 Φ1： Flying Capacitor Charging

In Φ2, as shown in the Figure 12：S1 and S2 off, S3 and S4 on, since the voltage across the capacitor cannot be changed abruptly, the capacitors C_F are superimposed on VDD, causing the PVDD to rise to a higher voltage.

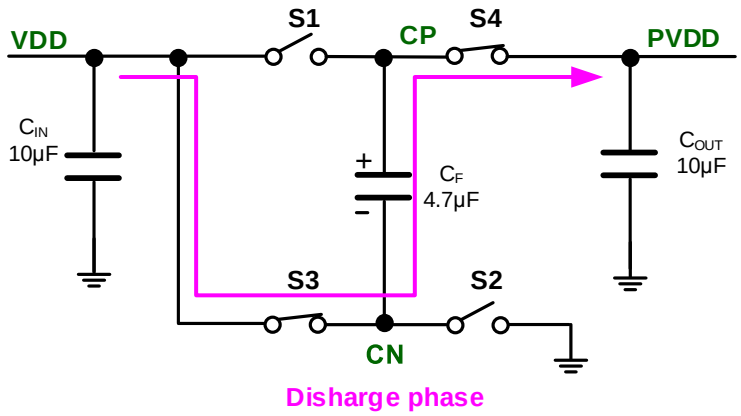


Figure 12 Φ2：Flying Capacitor Charge is Transferred to C_{OUT}

Soft start

In order to limit the inrush current of the power supply during the start of the chargepump, the chargepump has a soft start function. The current limit is 300mA during start-up. Soft start time is 2ms.

Current limiting control

DO-chargepump architecture integrates the current limiting control loop, in normal operation, the current limiting control loop controls the maximum output current capability of the chargepump when the load is too heavy or the chargepump flows through a large current.

Over-voltage protection(OVP) control

The output voltage PVDD is twice of the input voltage VDD in DO-chargepump structure, providing high voltage rail for internal power amplifier circuits, allowing the amplifier in the lithium battery voltage range to provide greater output dynamic range, in order to achieve high volume, high-quality class K audio amplifier playback sound quality. DO-chargepump integrated over-voltage protection control loop, when the input voltage VDD is greater than 4V, the output voltage PVDD is not twice of VDD, it is determined by the over-voltage control loop. And PVDD is stable at 8.0V.

Speaker & Receiver 2-in-1 application

AW87339 built-in speaker and receiver 2-in-1 application mode, through the register settings, there are class AB-type 2-in-1 receiver mode and class D-type 2-in-1 receiver mode can be selected, the gain can be adjusted through the I^2C register 0x05, adjustable range of 0~10.5dB, the application is very flexible. The 2-in-1 receiver mode uses the signal path of the speaker, with ultra-low distortion and strong drive capability, and eliminates the need for additional peripheral components, saving system cost and PCB layout space.

In the typical application case of Figure 2, the input capacitance Cin=100nF, the gain is 16V/V in the speaker application mode, the input high-pass cutoff frequency is 177Hz; In 1V/V gain class D-type 2-in-1 receiver application mode, The output noise is 16μV, the input high-pass cut-off frequency is 17Hz; In 1V/V gain class AB-type 2-in-1 receiver application mode, the output noise is as low as 9μV, the input high-pass cut-off frequency is 33Hz, which is very suitable for high-definition voice applications. AW87339 can achieve speaker and receiver's 2-in-1 application without changing any hardware in the case.

High Power Receiver Stereo Applications

AW87339 built-in high-power receiver stereo application mode, makes full use of the receiver, not only takes the voice calls into account and uses the receiver as speaker, but also combines the AWINIC's propriety TLTR-AGC technology, significantly enhancing the stereo sound quality and volume, enhancing the dynamic music, therefore, high power receiver stereo application has gradually become a mainstream application in smart phone.

AW87339 is in the high-power receiver stereo application mode, when the register 0x02h [4] is set to 1. Gain adjustable range is 0~ 27dB by adjusting the I²C register 0x05h [4: 0], AGC3 power adjustable range is 0.1W~1.5W@8ohm receiver, 0.025W~0.375W@32ohm receiver through adjusting the I²C register 0x06h [3:0]. AW87339 can flexibly match a variety of high-power Receiver, combined with TLTR AGC technology, significantly enhance the stereo sound quality and volume, and enhance music dynamic listening.

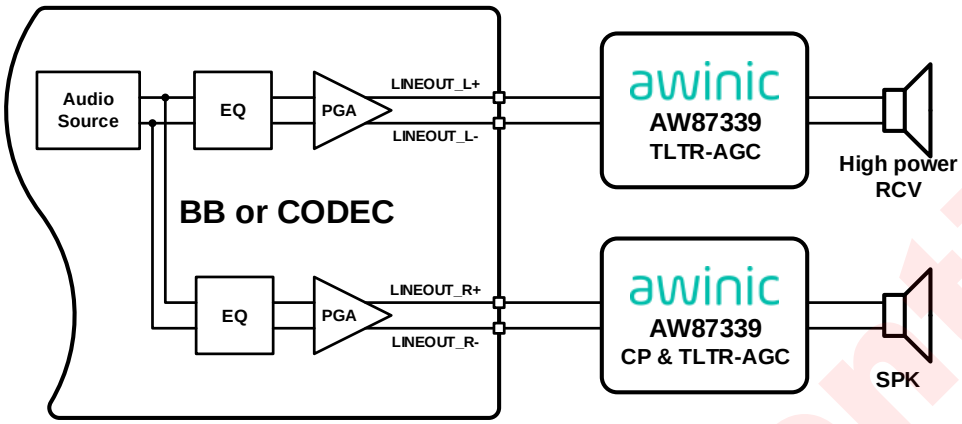


Figure 13 AW87339 High Power Receiver Stereo Mode Application

RNS(RF TDD Noise Suppression)

TDD Noise Causes

GSM cell phones use TDMA (Time Division Multiple Access) slot sharing technology. The time is divided into periodic frames in TDMA, and each frame is subdivided into a plurality of time slots. In order to transmit signals to the base station, the signals sent from the base stations to the plurality of mobile terminals are arranged in a predetermined time slot in the transmission. In this case, each TDMA frame contains 8 time slots, the entire frame is about 4.615ms long, and each slot time is 0.577ms.

With GSM handset, the RF power amplifier will transmit once every 4.615ms (217Hz), and the signal will produce intermittent Burst current and strong electromagnetic radiation. Intermittent Burst current will form a power fluctuation of 217 Hz; High frequency (900MHz and 1800MHz) RF signals form a 217Hz RF envelope signal. 217Hz power fluctuations will be conducted through the conduction to the audio signal path, 217Hz RF envelope signal will be coupled through the radiation into the audio signal path, if the protection is not good, it will produce an audible TDD Noise, which includes the 217Hz noise And a harmonic noise signal of 217 Hz.

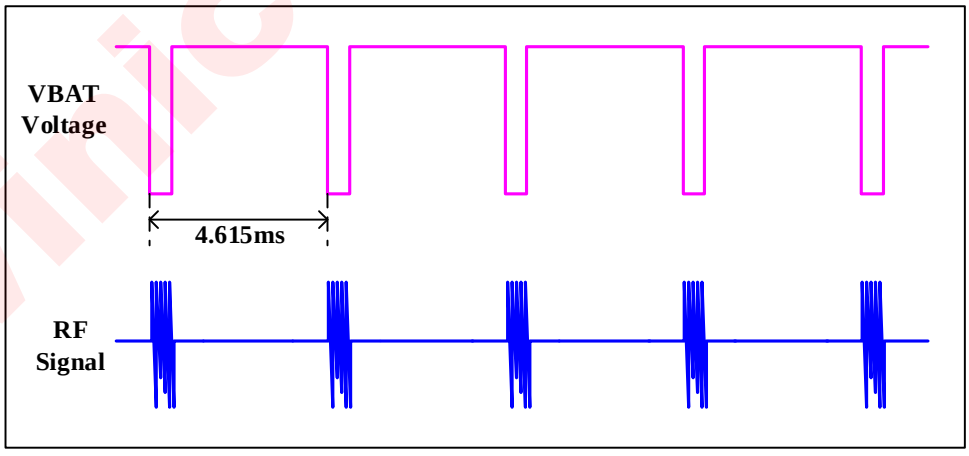


Figure 14 Schematic Diagram of Power Supply Voltage and RF Signal during GSM RF Operation

RNS fully inhibit the conduction and radiation interference by the AWINIC unique circuit architecture. Effectively improve the ability to suppress TDD Noise.

Conduction noise suppression

When the RF power amplifier is operating, it will draw the current from the battery by 217Hz frequency, Power supply will be introduced to 217Hz power ripple since the battery has a certain internal resistance, it will be coupled to the speaker through the audio power amplifier. The ability to suppress power fluctuations depends on the PSRR of the audio power amplifier.

$$PSRR = 20\log(\frac{vout_{ac}}{vdd_{ac}})$$

Due to the input and output of the fully differential amplifier is perfectly symmetrical, theoretically, the effect of the power supply fluctuation on the two outputs is exactly the same, and the differential output is completely unaffected by the power supply fluctuation. In practice, due to process bias and other factors, the amplifier will have a certain mismatch, PSRR is generally better than -60dB, it shows the output relative to the power fluctuations can be reduced by 1000 times, such as 500mVp power fluctuations, the differential output of 0.5 MV, which basically can meet the application requirements.

But in practical applications, the power amplifier may encounter conduction of TDD Noise problem even if its PSRR is -60dB or -80dB, why is this? Because we also need to consider the impact of peripheral power mismatches of audio power amplifiers

For conventional audio power amplifiers, when the input resistor Rin and the input capacitor Cin mismatch, will greatly affect the audio power amplifier PSRR indicators, in the case of 24 times the gain, PSRR will be weakened to -46dB or so if the input resistance and Capacitor with 1% mismatch. PSRR will be weakened to -28dB or so if the input resistance and input capacitance mismatch with 10% mismatch, when the power fluctuations, it is easy to produce audible TDD Noise.

In order to enhance the audio power amplifier PSRR in the input resistance and input capacitance mismatch case, AW87339 features a unique conduction noise suppression circuit, making the power amplifier to maintain a high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Radiation noise suppression

Input traces, output traces, horn loops, and even power and ground loops are likely to be subject to RF radiation interference in the audio signal module, longer input traces and output traces similar to the antenna, especially vulnerable RF radiation effects.

The reasonable PCB layout can reduce the influence of RF radiation in the design, such as shorten the line length of input and output as much as possible; audio devices should be shielded and far away from the RF antenna, maintain the integrity of the device to audio signal pathway; to increase the small bypass capacitor RF signals in the sensitive nodes. However, in practical applications, PCB layout is difficult to fully consider the influence of RF radiation on the audio signal path, and some RF energy will still be coupled to the audio signal path to form audible TDD Noise. Therefore, AW87339 features a unique RF radiation suppression circuit, a shielding layer inside the chip, effectively prevent high frequency energy into RF chip, to ensure that the drive single of the amplifier provided to the speaker will not be affected by the antenna RF radiation, thus avoiding the antenna RF Radiation caused by TDD Noise.

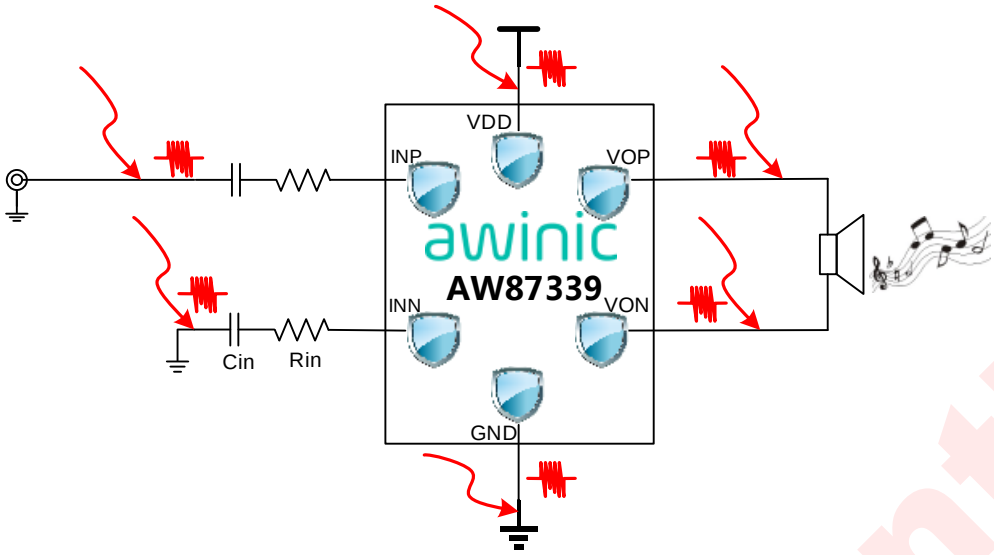


Figure 15 RF Radiation Coupling Graph

Class D amplifier without filter

When the traditional class D amplifier is in idle state of no input signal, the output will have the inverse square wave, it will directly above the load of the speaker, will form a large current power switch on the speaker, therefore we need to increase the LC filter to restore the analog audio signal at the amplifier output. The LC filter increase the cost and PCB layout area, while increase the power consumption, reduce the performance of THD+N.

The AW87339 features a Class D amplifier without a filter, eliminating the need for an output LC filter. In the idle state of no input signal, the two outputs (VOP, VON) of the amplifier are in-phase square waves and not generate idle switching currents on the speaker load. When the input signal is added to the input terminal, the duty ratio of the output is changed. The duty cycle of the VOP becomes larger and the duty cycle of the VON becomes smaller, and the difference value of the output forms the differential amplified signal on the speaker.

EEE

The AW87339 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth, fully meet FCC CLASS B specification requirements.

Pop-Click Suppression

The AW87339 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Thermal AGC/ over temperature protection

The AW87339 features the thermal AGC patented technology, can according to the chip temperature, automatically adjust the gain of the system, reduce the power consumption of the chip, to prevent damage in case of excessive temperature.

The AW87339 has an automatic temperature detection mechanism, when the chip temperature exceeds the preset threshold of thermal AGC temperature (150°C), the chip will start the automatic gain control circuit to decrease the gain of the system, thereby reducing the energy consumption of the chip, thus slow or stop chip temperature continues to rise. When the chip temperature is restored to normal operating range (below 130°C), the automatic gain control circuit will restore the system gain to the original state. When the chip operates in a fault condition, the chip temperature is too high, up to a preset temperature protection

temperature threshold (160°C), the system starts overheating protection, the chip will be turned off, restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C).

Automatic recovery of overcurrent protection

AW87339 with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, AW87339 internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting.

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

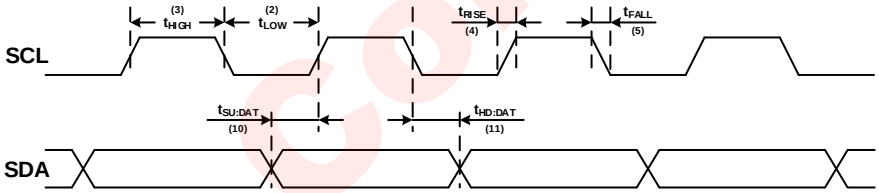


Figure 16 SCL and SDA timing relationships in the data transmission process

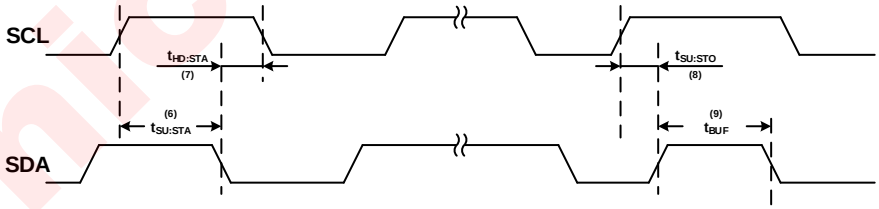


Figure 17 the Timing Relationship between START and STOP State

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue

START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 18.

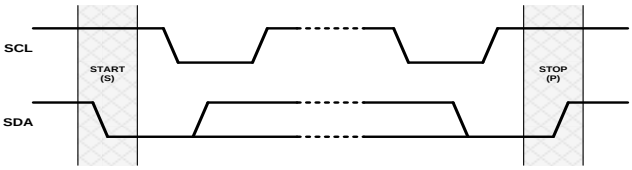


Figure 18 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 19. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 20. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

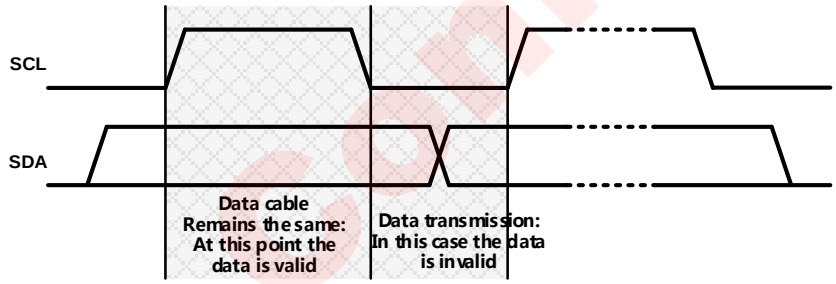


Figure 19 The Data Transfer Rules on the I²C Bus

The whole process of actual data transmission is shown in Figure 20. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

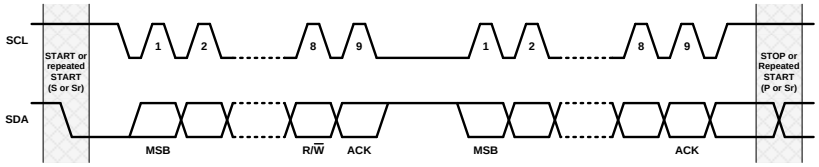


Figure 20 Data Transmission on the I²C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87339 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 21:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87339 register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87339, within AW87339 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

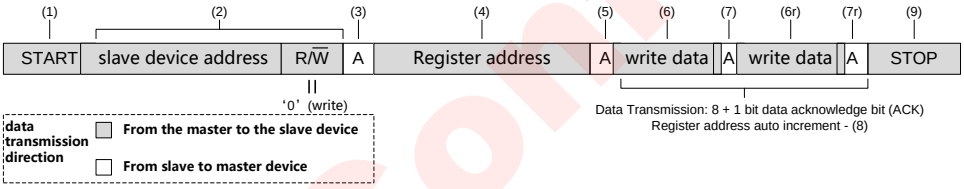


Figure 21 Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87339 as the slave device, the transmission process carried out by following steps listed in Figure 22:

Master device asserts a start condition;

Master device transmits the 7 bits address of AW87339, and followed by a "read / write" flag ($R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device sends the 8bit address that the AW87339 register needs to read the data;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START.

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W} = 1$) again.

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not.

The master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully. AW87339 automatically increment register address once after the slave sent each acknowledge bit (ACK). The master device generates the STOP state to end the data transmission.

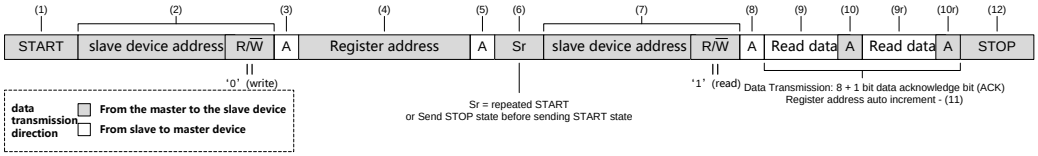


Figure 22 Reading Process (Data Transmission Direction Remains the Same)

Register List

name	addr ess	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Chip ID	0x00	0	0	1	1	1	0	0	1
SYSCTRL	0x01	0	0	0	0	EN_SW	EN_CP	EN_PA	0
MODECTRL	0x02	1	0	1	RCV_LOAD(1)	RCV_MODE(2)	EN_ABRCV(3)	1	1
CPOVP	0x03	0	0	0	0	CP_OVP(4) [3]	CP_OVP(4) [2]	CP_OVP(4) [1]	CP_OVP(4) [0]
CPP	0x04	0	0	0	0	0	1	0	1
Gain	0x05	0	0	0	Gain [4]	Gain [3]	Gain [2]	Gain [1]	Gain [0]
AGC3_Po	0x06	0	0	0	0	AGC3_Po[3]	AGC3_Po[2]	AGC3_Po[1]	AGC3_Po[0]
AGC3	0x07	AGC3_RT[2]	AGC3_RT[1]	AGC3_RT[0]	AGC3_AT[2]	AGC3_AT[1]	AGC3_AT[0]	1	0
AGC2_Po	0x08	0	0	0	0	AGC2_Po[3]	AGC2_Po[2]	AGC2_Po[1]	AGC2_Po[0]
AGC2	0x09	0	0	0	AGC2_AT[2]	AGC2_AT[1]	AGC2_AT[0]	0	0
AGC1	0x0A	1	0	0	1	AGC1_AT[1]	AGC1_AT[0]	1	PD_AGC1

(1) RCV_LOAD: enable high power receiver (32ohm or 8ohm) stereo application
(2) RCV_MODE: enable 2-in-1 receiver application
(3) EN_ABRCV: enable 2-in-1 class AB receiver application
(4) CP_OVP: chargepump OVP voltage

register	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A
Default	0x39	0x06	0xA3	0x06	0x05	0x00 (RCV_LOAD||RCV_MODE=1) 0x10 (RCV_LOAD||RCV_MODE=0)	0x07	0x52	0x06	0x08	96

Table 2 AW87339 Register Default Value

Any register address which is more than 0x0A and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87339's I²C address is 10110A2A1, as shown in Table 3, in order to avoid conflict with other I²C devices address, you can pull up or pull-down AW87339 of AD2 and AD1 pins to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	1	0	A2	A1	R/W

Table 3 AW87339 Address Byte

CHIP ID* Register *(address: 0x00)

I²C Bit	Name	R/W	Default	Description
7:0	IDCODE	R	0x39	Chip ID will be returned after reading. All configuration registers will be reset to default values after 0xAA is written.

SYSTEM CONTROL (SYSCTRL)* Register *(address: 0x01)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3	EN_SW	R/W	0	Chip Software Enable 0: Chip Software Disable: Shutdown the whole chip except PORN. 1: Chip Software Enable
2	EN_CP	R/W	1	Chargepump Enable: This bit must be unchanged when EN_SW=1. 0: Disable Chargepump, PVDD=VBAT 1: Enable Chargepump
1	EN_PA	R/W	1	PA output Enable 0: Disable PA 1: Enable PA
0	--	--	0	Reserved and Unused

MODE CONTROL (MODECTRL)* Register *(address: 0x02)

I²C Bit	Name	R/W	Default	Description
7:5	--	--	101	Reserved and Unused
4	RCV_LOAD	R/W	0	High power Receiver load stereo application Enable
				0: high power receiver stereo application Disable
				1: high power receiver stereo application Enable
3	RCV_MODE	R/W	0	Speak & Receiver 2-in-1 application
				0: Speak & Receiver 2-in-1 application Disable
				1: Speak & Receiver 2-in-1 application Enable
2	EN_ABRCV	R/W	0	2-in-1 Class AB Receiver application
				0: 2-in-1 Class D Receiver application Enable
				1: 2-in-1 Class AB Receiver application Enable
1:0	--	--	11	Reserved and Unused

CHARGEPUMP OUTPUT VOLTAGE (CPOVP)* Register *(address: 0x03)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	CP_OVP	R/W	0110	Setting Chargepump OVP Voltage
				1001~1111: Unavailable
				1000: 8.5V
				0111: 8.25V
				0110: 8.0V
				0101: 7.75V
				0100: 7.5V
				0011: 7.25V
				0010: 7.0V
				0001: 6.75V
				0000: 6.5V

CHAREPUMP PARAMETER (CPP)* Register *(address: 0x04)

I²C Bit	Name	R/W	Default	Description
7:0	--	--	00000101	Reserved and Unused

GAIN CONTROL (*Gain*) Register *(address: 0x05)*

For RCV_MODE=1, RCV_LOAD=x (Speaker & Receiver 2-in-1Mode and Receiver stereo Mode):

I²C Bit	Name	R/W	Default	Description		
7:5	--	--	000	Reserved and Unused		
4:0	Gain	R/W	0000	Setting Class D Amplifying Gain		
				Gain	EN_ABRCV=0	EN_ABRCV=1
				00000: 0dB	R_{ini}=96kΩ	R_{ini}=48kΩ
				00001: 1.5dB	R_{ini}=80kΩ	R_{ini}=48kΩ
				00010: 3dB	R_{ini}=68kΩ	R_{ini}=48kΩ
				00011: 4.5dB	R_{ini}=56kΩ	R_{ini}=48kΩ
				00100: 6.0dB	R_{ini}=48kΩ	R_{ini}=48kΩ
				00101: 7.5dB	R_{ini}=60kΩ	R_{ini}=48kΩ
				00110: 9.0dB	R_{ini}=48kΩ	R_{ini}=48kΩ
				00111: 10.5dB	R_{ini}=56kΩ	R_{ini}=48kΩ
				10011~11111: Unavailable		

For RCV_MODE=0, RCV_LOAD=0 (Speaker Mode):

I²C Bit	Name	R/W	Default	Description	
7:5	--	--	000	Reserved and Unused	
4:0	Gain	R/W	10000	Setting Class D Amplifying Gain	
				Gain	
				01000: 12dB	R_{ini}=36.5kΩ
				01001: 13.5dB	R_{ini}=30kΩ
				01010: 15.0dB	R_{ini}=25kΩ

				01011: 16.5dB	R_{ini}=21.5kΩ
				01100: 18.0dB	R_{ini}=18kΩ
				01101: 19.5dB	R_{ini}=15.5kΩ
				01110: 21dB	R_{ini}=12.5kΩ
				01111: 22.5dB	R_{ini}=11kΩ
				10000: 24dB	R_{ini}=9kΩ
				10001: 25.5dB	R_{ini}=7.5kΩ
				10010: 27dB	R_{ini}=6.5kΩ
				10011~11111: Unavailable	

For RCV_MODE=0, RCV_LOAD=1 (Receiver stereo Mode):

I²C Bit	Name	R/W	Default	Description	
7:5	--	--	000	Reserved and Unused	
4:0	Gain	R/W	00000	Setting Class D Amplifying Gain	
				Gain	
				00000: 0dB	R_{ini}=144kΩ
				00001: 1.5dB	R_{ini}=120kΩ
				00010: 3dB	R_{ini}=101kΩ
				00011: 4.5dB	R_{ini}=86kΩ
				00100: 6.0dB	R_{ini}=72kΩ
				00101: 7.5dB	R_{ini}=60kΩ
				00110: 9.0dB	R_{ini}=51kΩ
				00111: 10.5dB	R_{ini}=42kΩ
				01000: 12dB	R_{ini}=36.5kΩ
				01001: 13.5dB	R_{ini}=30kΩ
				01010: 15.0dB	R_{ini}=25kΩ
				01011: 16.5dB	R_{ini}=21.5kΩ
				01100: 18.0dB	R_{ini}=18kΩ
				01101: 19.5dB	R_{ini}=15.5kΩ
				01110: 21dB	R_{ini}=12.5kΩ
				01111: 22.5dB	R_{ini}=11kΩ
				10000: 24dB	R_{ini}=9kΩ
				10001: 25.5dB	R_{ini}=7.5kΩ
				10010: 27dB	R_{ini}=6.5kΩ
				10011~11111: Unavailable	

CLASS D AGC3 OUTPUT POWER (AGC3_Po)* Register *(address: 0x06) (When RCV_LOAD=1)

I²C Bit	Name	R/W	Default	Description		
7:4	--	--	0000	Reserved and Unused		
3:0	AGC3_Po	R/W	0111	Setting AGC3 Output Power for Protecting Speaker and stereo Receiver		
				0000: 0.1W@8Ω	0.133W@6Ω	0.025W@32Ω
				0001: 0.2W@8Ω	0.267W@6Ω	0.05W@32Ω
				0010: 0.3W@8Ω	0.4W@6Ω	0.075W@32Ω
				0011: 0.4W@8Ω	0.533W@6Ω	0.1W@32Ω
				0100: 0.5W@8Ω	0.667W@6Ω	0.125W@32Ω
				0101: 0.6W@8Ω	0.8W@6Ω	0.15W@32Ω
				0110: 0.7W@8Ω	0.933W@6Ω	0.175W@32Ω
				0111: 0.8W@8Ω	1.067W@6Ω	0.2W@32Ω
				1000: 0.9W@8Ω	1.2W@6Ω	0.225W@32Ω
				1001: 1.0W@8Ω	1.333W@6Ω	0.25W@32Ω
				1010: 1.1W@8Ω	1.467W@6Ω	0.275W@32Ω
				1011: 1.2W@8Ω	1.6W@6Ω	0.3W@32Ω
				1100: 1.3W@8Ω	1.733W@6Ω	0.325W@32Ω
				1101: 1.4W@8Ω	1.867W@6Ω	0.35W@32Ω
				1110: 1.5W@8Ω	2.0W@6Ω	0.375W@32Ω
				1111: AGC3 Disable		

CLASS D AGC3 OUTPUT POWER (AGC3_Po)* Register *(address: 0x06) (When RCV_LOAD=0)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC3_Po	R/W	0111	Setting AGC3 Output Power for Protecting Speaker
				0000~0011: Unavailable
				0100: 0.5W@8Ω / 0.667W@6Ω / 0.125W@32Ω
				0101: 0.6W@8Ω / 0.8W@6Ω / 0.15W@32Ω
				0110: 0.7W@8Ω / 0.933W@6Ω / 0.175W@32Ω
				0111: 0.8W@8Ω / 1.067W@6Ω / 0.2W@32Ω
				1000: 0.9W@8Ω / 1.2W@6Ω / 0.225W@32Ω
				1001: 1.0W@8Ω / 1.333W@6Ω / 0.25W@32Ω
				1010: 1.1W@8Ω / 1.467W@6Ω / 0.275W@32Ω
				1011: 1.2W@8Ω / 1.6W@6Ω / 0.3W@32Ω
				1100: 1.3W@8Ω / 1.733W@6Ω / 0.325W@32Ω
				1101: 1.4W@8Ω / 1.867W@6Ω / 0.35W@32Ω
				1110: 1.5W@8Ω / 2.0W@6Ω / 0.375W@32Ω
				1111: AGC3 Disable

CLASS D AGC3 PARAMETER (AGC3)* Register *(address: 0x07)

I²C Bit	Name	R/W	Default	Description
7:5	AGC3_RT	R/W	010	Setting Release Time of AGC3:
				000: 5.12ms/dB
				001: 10.24ms/dB
				010: 21 ms/dB
				011: 41 ms/dB
				100: 82 ms/dB
				101: 164 ms/dB
				110: 328 ms/dB
				111: Unavailable
4:2	AGC3_AT	R/W	100	Setting Attack Time of AGC3:
				000: 0.64ms/dB
				001: 1.28ms/dB
				010: 2.56ms/dB
				011: 10.24ms/dB
				100: 41ms/dB
				101: 82ms/dB
				110: 164ms/dB
				111: 328ms/dB
1:0	--	--	10	Reserved and Unused

CLASS D AGC2 OUTPUT POWER(AGC2_Po)* Register *(address: 0x08)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC2_Po	R/W	0110	Setting AGC2 Output Power:
				0000: 0.4W@8Ω / 0.533W@6Ω / 0.1W@32Ω
				0001: 0.6W@8Ω / 0.8W@6Ω / 0.15W@32Ω
				0010: 0.8W@8Ω / 1.067W@6Ω / 0.2W@32Ω
				0011: 1.0W@8Ω / 1.333W@6Ω / 0.25W@32Ω
				0100: 1.2W@8Ω / 1.6W@6Ω / 0.3W@32Ω
				0101: 1.4W@8Ω / 1.867W@6Ω / 0.35W@32Ω
				0110: 1.6W@8Ω / 2.133W@6Ω / 0.4W@32Ω
				0111: 1.8W@8Ω / 2.4W@6Ω / 0.45W@32Ω
				1000: 2.0W@8Ω / 2.667W@6Ω / 0.5W@32Ω
				1001: AGC2 Disable
				1010~1111: Unavailable

CLASS D AGC2 PARAMETER (AGC2)* Register *(address: 0x09)

I²C Bit	Name	R/W	Default	Description
7:5	--	--	00	
4:2	AGC2_AT	R/W	010	Setting Attack Time of AGC2: 000: 0.16ms/dB 001: 0.32ms/ dB 010: 0.64ms/dB 011: 2.56ms/dB 100: 10.24ms/dB 101: 41ms/dB 110: 82ms/dB 111: 164ms/dB
1:0	--	--	00	Reserved and Unused

CLASS D AGC1 PARAMETER (AGC1)* Register *(address: 0x0A)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	1001	Reserved and Unused
3:2	AGC1_AT	R/W	01	Setting Fastest Level AGC Attack Time: 00: 0.04ms/dB 01: 0.08ms/dB 10: 0.16ms/dB 11: 0.32ms/dB
1	--	--	1	Reserved and Unused
0	PD_ AGC1	R/W	0	AGC1 control bit 0: AGC1 Enable 1: AGC1 Disable

APPLICATION INFORMATION

Capacitor Selection

The output capacitor of chargepump is usually within the range 0.1μF~47μF, It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO3), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

a) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive. X5R capacitance change within ±15% in temperature range of 55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The output capacitance of the AW87339's chargepump recommends X5R ceramic capacitors.

b) Voltage Stability

Class II type capacitor has poor voltage stability ——Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V, the package size is 0805, 1206 or 0603, the capacitance value is 10μF. The capacitor's voltage stability of different types of capacitor is as shown below:

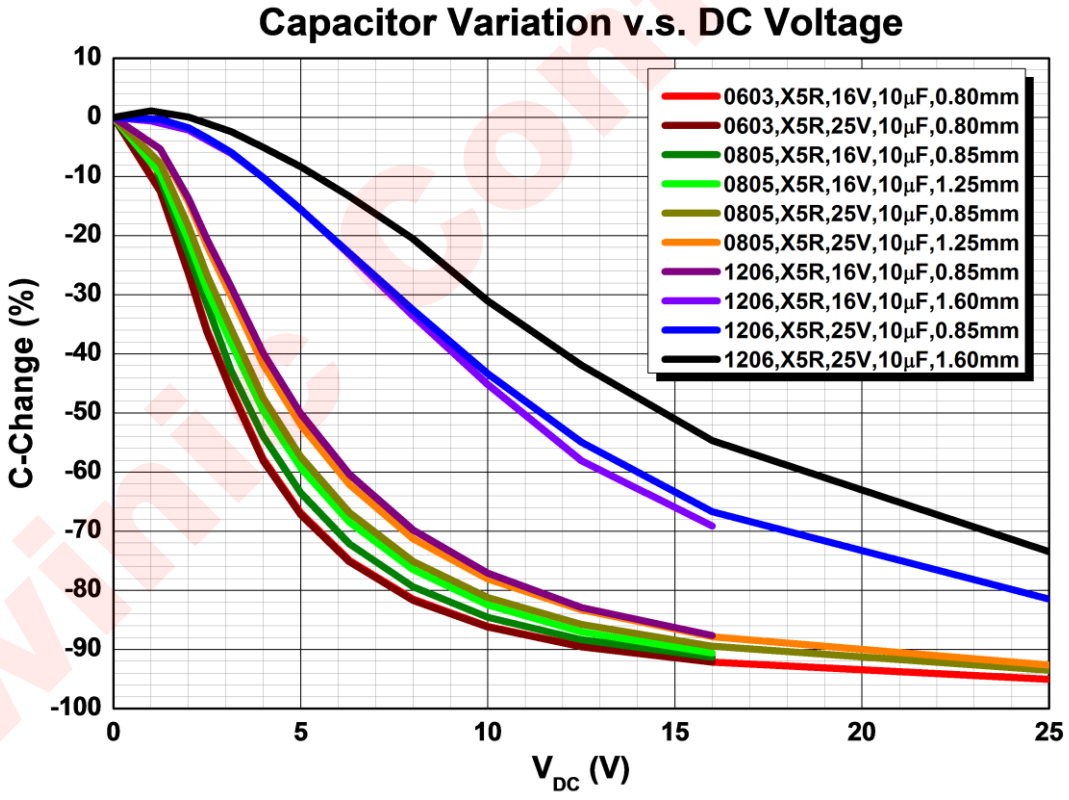


Figure 23 Different Types of Capacitive Voltage Stability

Among them, the space remaining value of different types of capacitors at VDC = 8.5V as shown below:

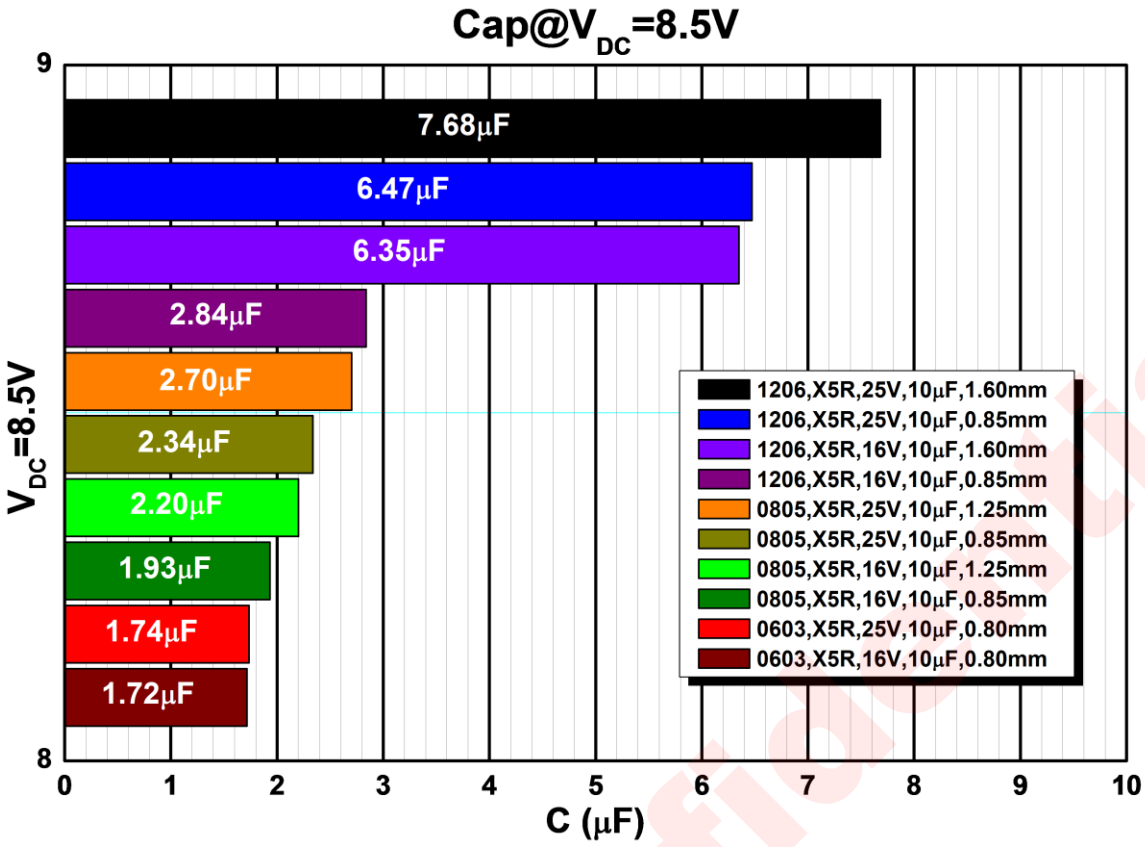


Figure 24 The Space Remaining Value of Different Types of Capacitors at V_{DC} = 8.5V

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. the higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In AW87339 typical applications, it is necessary to ensure the output value of the PVDD capacitor ≥3μF when PVDD=8.5V.

Input Capacitor-C_{in}（input high-pass cutoff frequency）

The input capacitors and input resistors form a high-pass filter to filter out the DC component of the input signal. The -3dB frequency points of the high pass filter is shown below：

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} (Hz)$$

The selection of a smaller Cin capacitor in the application helps to filter out 217Hz noise, which comes from the input coupling, and the smaller capacitor is advantageous to reduce the pop-click noise when the power amplifier turn on.Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise. A capacitor value deviation of 10% or better capacitance is recommended.

Take typical application as an example, the input high-pass cutoff frequency is calculated as below:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 9k\Omega * 100nF} (Hz) = 177Hz$$

Class D-type speaker & receiver 2-in-1 application (Gain=1), the input high pass frequency is as follows:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 96k\Omega * 100nF}(Hz) = 17Hz$$

Class AB-type speaker & receiver 2-in-1 (Gain=1), the input high pass frequency is as follows:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 48k\Omega * 100nF}(Hz) = 33Hz$$

Supply Decoupling Capacitor（C_S）

A good decoupling capacitor can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance, the ESR value of the capacitor should be as small as possible. In AW87339 applications, low ESR (equivalent-series-resistance) X7R or X5R ceramic capacitors are recommended. Generally, 10μF ceramic capacitors are used to bypass the VDD to the ground, and the decoupling capacitor should be placed as close to the VDD chip as possible in the layout. If you want to filter out low-frequency noise better, you need to add a 10μF or greater decoupling capacitor depending on your application. Meanwhile, a 33pF~0.1μF ceramic capacitor is placed on the pin of the power supply to filter the high frequency interference on the power supply. The capacitor should be placed as close as possible to the D4 pin and inductor.

Chargepump Flying capacitor (C_F)

The Flying capacitor is used to transfer energy between the power supply and the chargepump load, the value of the Flying capacitor directly affects the load regulation rate and the output drive capability of the chargepump. If flying capacitor is too small, it will affect the chargepump load adjustment rate and output drive capability, thereby affecting the power output of the amplifier, and the larger the Flying capacitor, the better the load regulation ability, driving ability is also stronger. Recommended use of 4.7μF, low ESR X7R, X5R ceramic capacitors, it is recommended to use more than 10V pressure capacitor.

Output capacitance of chargepump（C_{OUT}）

The output capacitance of the chargepump and the ESR directly affect the ripple of the output, thus affecting the performance of the power amplifier. Recommended use of 10μF, low ESR X7R or X5R ceramic capacitors, you need to select the 25V voltage resistance capacitor.

Output beads, capacitors, TVS

Using EEE technology, in the class K mode, the AW87339 can also meet the FCC CLASS B specification requirements. It is recommended to Use ferrite chip beads and capacitors if device near the EMI sensitive circuits, there are long leads from amplifier to speaker, placed as close as possible to the output pin.

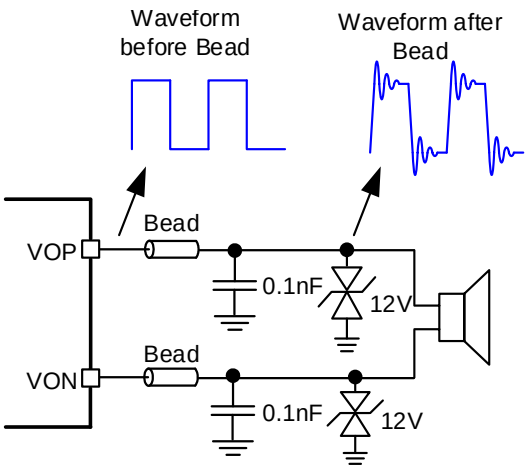


Figure 25 Ferrite Chip Bead and Capacitor

Amplifier output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

Power amplifier output PWM signals of high voltage to PVDD voltage, voltage to 8.5 V, will produce some ringing after bead capacitor, resulting in higher peak voltage. Recommended choose the operating voltage of 12V TVS.

PCB AND DEVICE LAYOUT CONSIDERATION

EXTERNAL COMPONENTS PLACEMENT

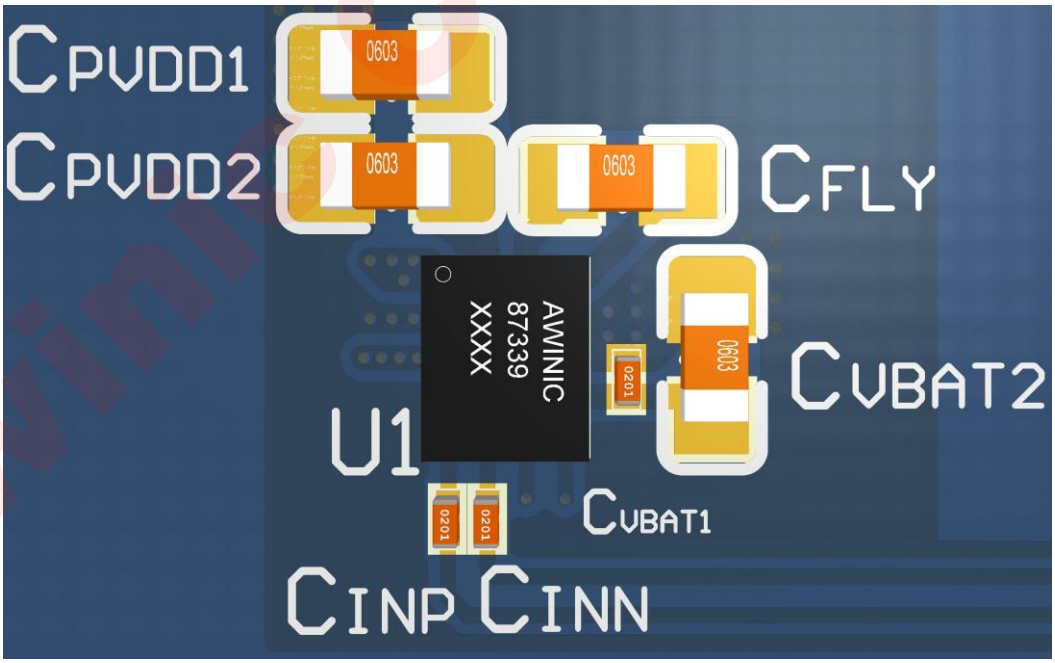


Figure 26 AW87339 External Components Placement

LAYOUT CONSIDERATIONS

This device is a power a power amplifier chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

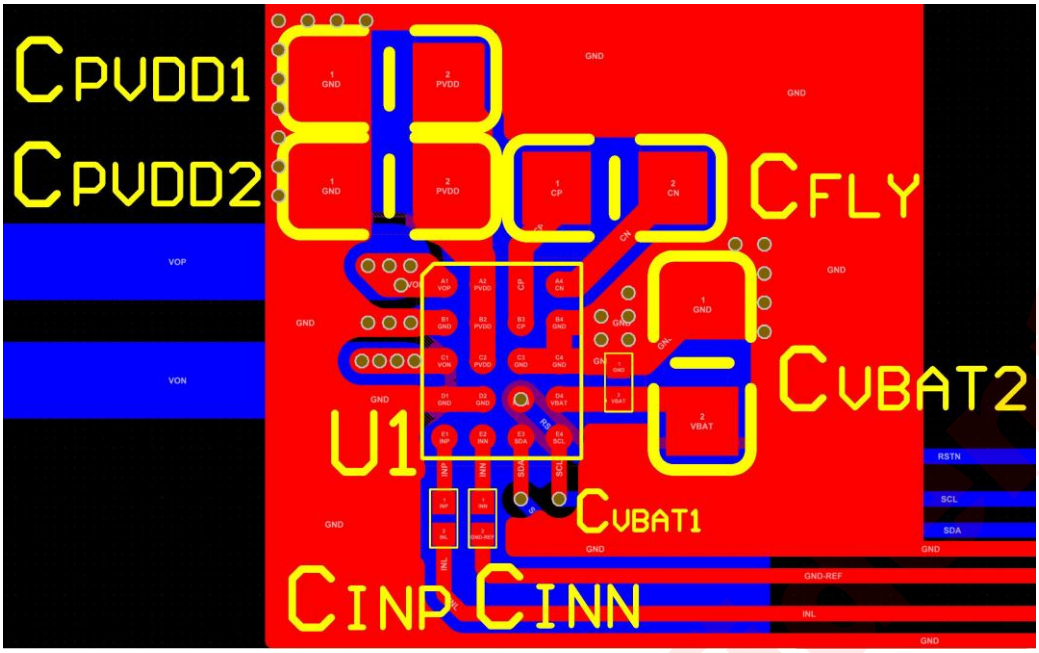


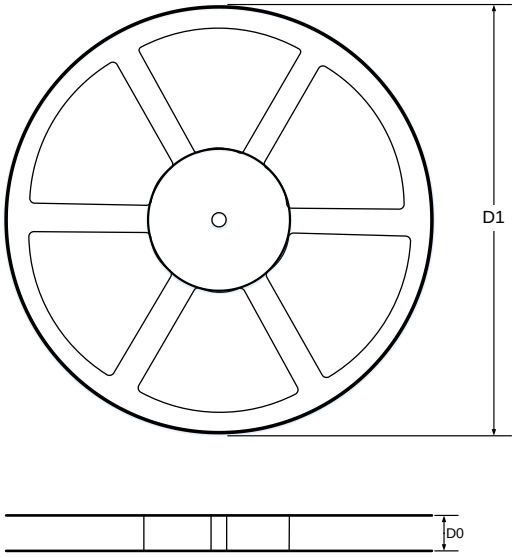
Figure 27 AW87339 Board Layout

In order to obtain excellent performance of AW87339, PCB layout must be carefully considered. The design consideration should follow the following principles:

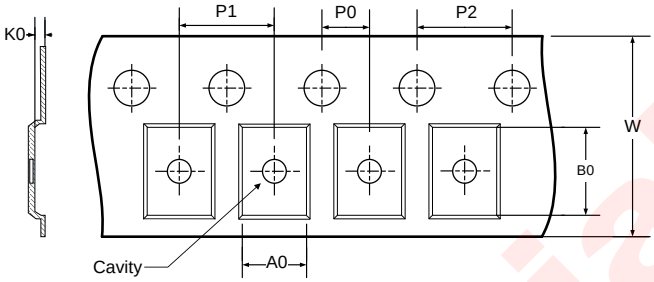
1. In AW87339 peripheral device layout, you first need to guarantee the chargepump output capacitance close to PVDD pin.
2. Try to provide a separate short and thick power line to AW87339, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin.
3. The input capacitors should be close to AW87339 INN and INP input pin, the input line should be parallel to suppress noise coupling.
4. The beads and capacitor should be placed near to AW87339 VON and VOP pin. The output line from AW87339 to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.

TAPE & REEL DESCRIPTION

REEL DIMENSIONS

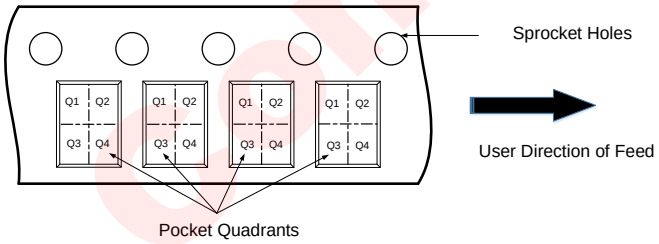


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

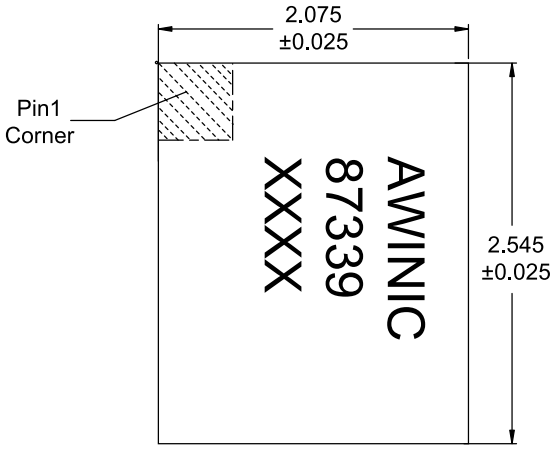
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



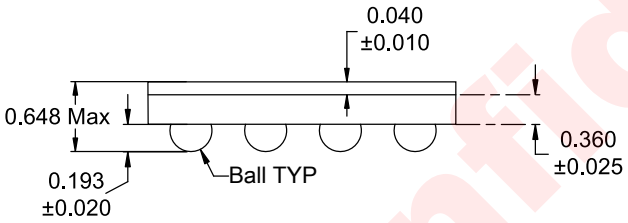
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	2.20	2.67	0.83	2.00	8.00	4.00	12.00	Q1

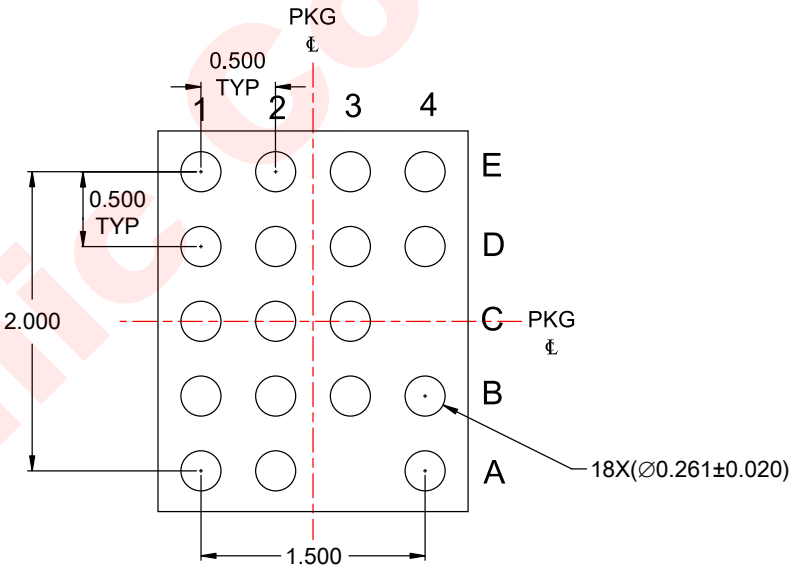
PACKAGE DESCRIPTION



Top View



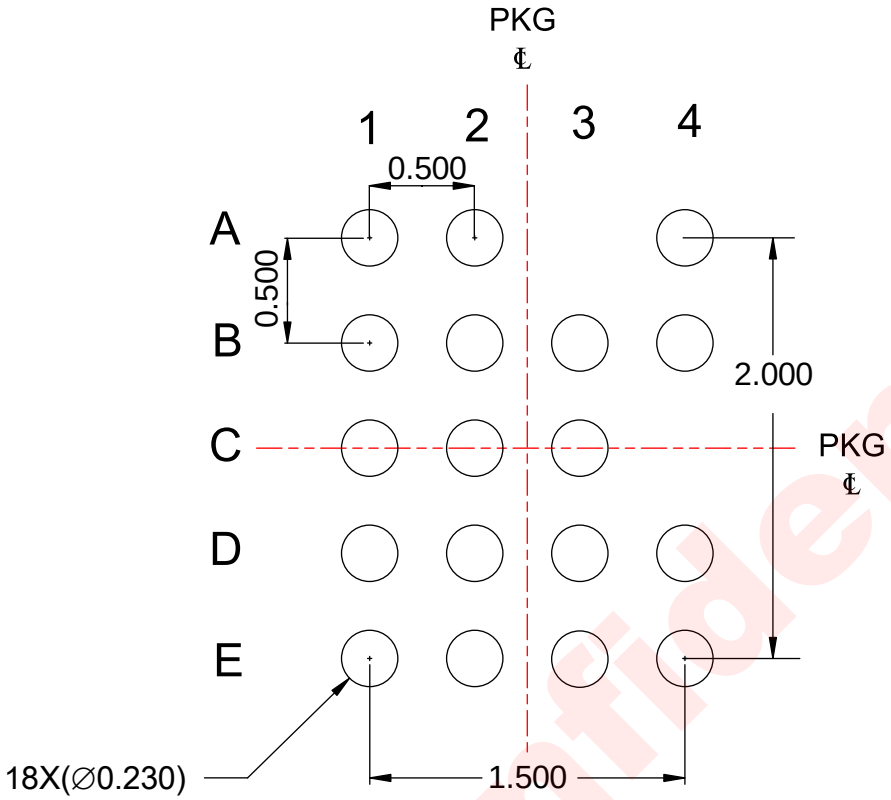
Side View

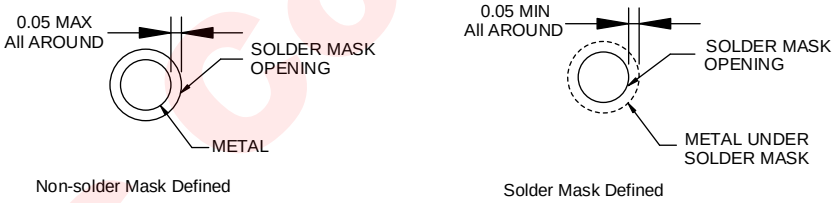


Bottom View

Dimensions are all in millimeters

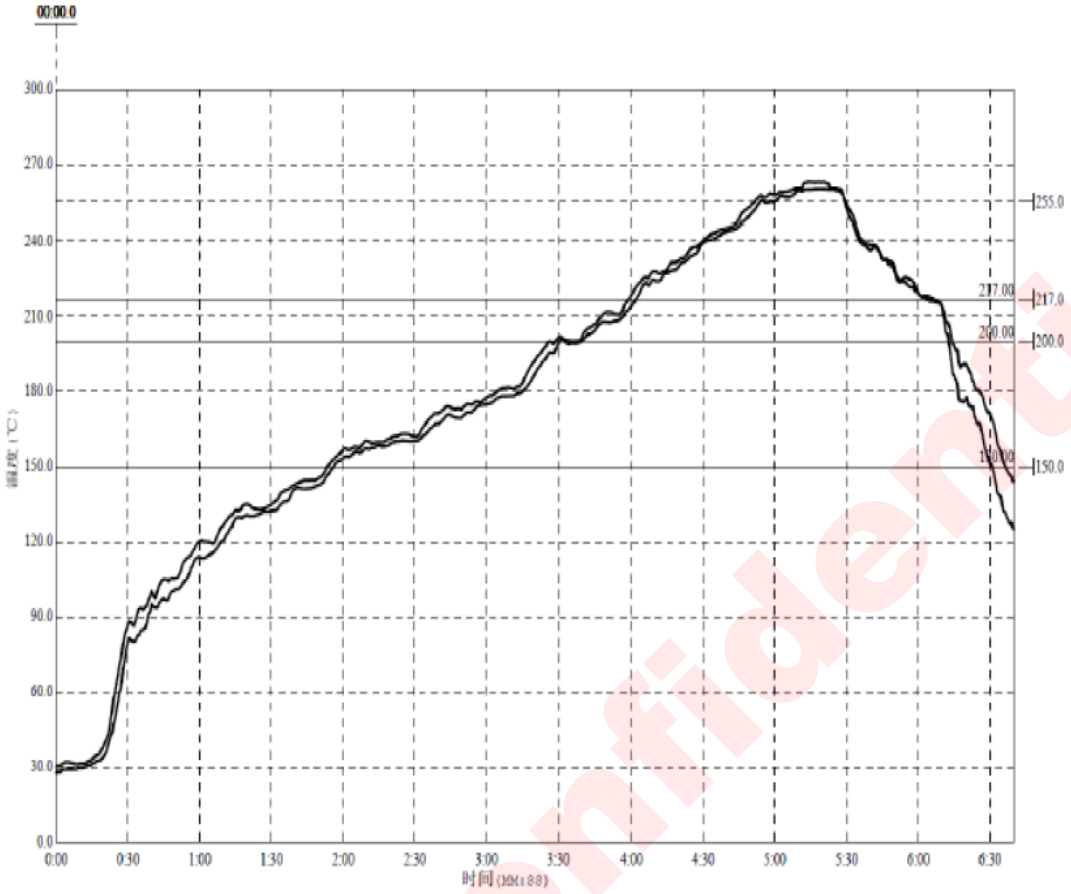
LAND PATTERN DATA





Dimensions are all in millimeters

REFLOW SOLDERING CURVE



Reflow Note	Spec
Average ramp-up rate (217℃c to Peak)	Max. 3℃/sec
Time of Preheat temp.(from 150℃ to 200℃)	60-120sec
Time to be maintained above 217℃	60-150sec
Peak Temperature	>260℃
Time within 5℃ of actual peak temp	20-40sec.
Ramp-down rate	Max. 6℃/sec
Time from 25℃ to peak temp	Max. 8min.

VERSION INFORMATION

Version	Date	Description
V1.0	2017-05-13	AW87339CSR datasheet V1.0
V1.1	2017-10-22	1. Add Po@6ohm 2. modify device marking： 87339 3. modify description
V1.2	2018-02-01	Add Reflow soldering curve Modify size 2.545mm*2.075mm
V1.3	2018-06-18	Add CDM test method Update tape & reel description

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