I²S Input, High Efficiency, Feed-Forward Multi-Level AGC 2nd Digital Smart K Audio Amplifier

FEATURES

- **New generation Feed-Forward Multi-Level AGC algorithm**
- **Feed-forward algorithm prevents clipping noise**
- **Bass and Treble enhancement to increase loudness and improve sound quality**
- **Supports Speaker, Receiver 2-in-1 application**
- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 26uV**
- **THD+N: 0.015%**
- **Adaptive BOOST with efficiency up to 93%, total efficiency up to 86%**
- Supports 6Ω Speaker
- Extensive Pop-Click Suppression
- Volume control(from -96dB to 0dB)
- I²C-bus control interface(400kHz)
- I²S-bus：
  - I²S, Left-Justified and Right-Justified
  - Input Sample Rates from 8kHz to 48kHz
  - Data Width: 16, 20, 24, 32 Bits
- Power Supplies：
  - VDD：3V-5.5V
  - DVDD：1.65V-1.95V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- WLCSP 2.55mm×1.94mm-28B package

APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

DESCRIPTION

The AW8896 is an I²S input, high efficiency and 2nd AWINIC digital Smart K audio amplifier with an integrated adaptive boost converter, sound quality enhancement algorithms and speaker protection. Due to its 26uV noise floor and ultra-low distortion, clean listening is guaranteed. It can delivers 2.62W (RMS, THD+N = 1%) output power into a 6Ω speaker at a battery voltage of 4.2V.

The AW8896 features AWINIC new generation Feed-Forward Multi-Level AGC algorithm that prevents clipping noise and improves sound quality. The AW8896 also incorporates Bass and Treble enhancement function for increasing loudness and enhancing the quality of audio signal.

The AW8896 supports speaker and receiver 2-in-1 applications. In the receiver application, it connects VDD directly to the Class-D amplifier supply.

The AW8896 integrates a high-efficiency and adaptive boost converter as the Class-D amplifier supply rail. The boost converter output voltage is only raised when necessary. This improves the output dynamic range of audio signal while limiting quiescent power consumption.

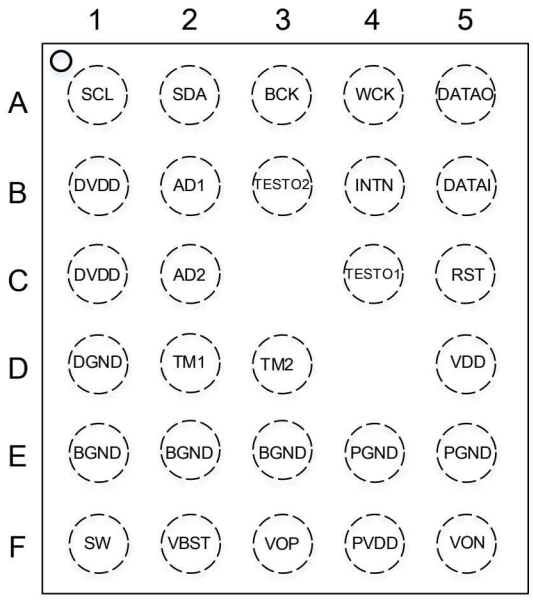
The AW8896 features high RF suppression and eliminates TDD noise completely benefited from the audio input is I²S interface. General settings are communicated via an I²C-bus interface, and its I²C address is configurable.

The AW8896 offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

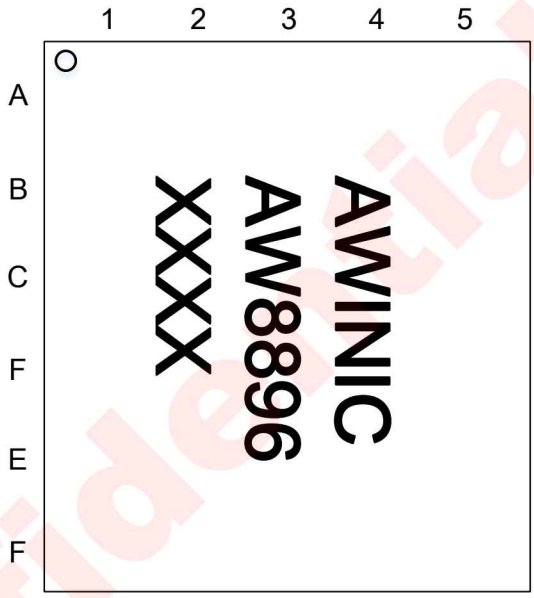
The AW8896 is available in a WLCSP 2.55mm×1.94mm-28B package with 400um pitch.

PIN CONFIGURATION AND TOP MARK

AW8896CSR TOP VIEW



AW8896CSR Marking



AW8896 – AW8896CSR
XXXX – Production Tracing Code

Figure 1 AW8896CSR pin diagram top view and device marking

PIN DESCRIPTION

Number	Symbol	Description
A1	SCL	I²C clock input
A2	SDA	I²C data I/O
A3	BCK	I²S bit clock input
A4	WCK	I²S word select input
A5	DATAO	I²S data out
B1,C1	DVDD	Digital Power supply
B2	AD1	I²C address select input 1(Do not float the AD1 Input)
B3	TESTO2	TEST output 2, connect to ground
B4	INTN	Interrupt output(Open-Drain)
B5	DATAI	I²S data input
C2	AD2	I²C address select input 2(Do not float the AD2 Input)
C4	TESTO1	TEST output 1, connect to ground

C5	RST	Reset signal, active high
D1	GND	GND
D2	TM1	TEST mode 1, connect to ground
D3	TM2	TEST mode 2, connect to ground
D5	VDD	Battery power supply
E1,E2,E3	BGND	Boost GND
E4,E5	PGND	Power GND
F1	SW	Boost switch pin
F2	VBST	Boost output
F3	VOP	Non-inverting Class-D output
F4	PVDD	Class-D power supply
F5	VON	Inverting Class-D output

AWINIC DIGITAL Smart K FAMILY

	AW8895	AW8896	AW8890
Feed-Forward Multi-Level AGC	N	Y	Y
Audio Effect Processing	N	Y	Y
Package	WLCSP-28	WLCSP-28	ECP-38

FUNCTIONAL BLOCK DIAGRAM

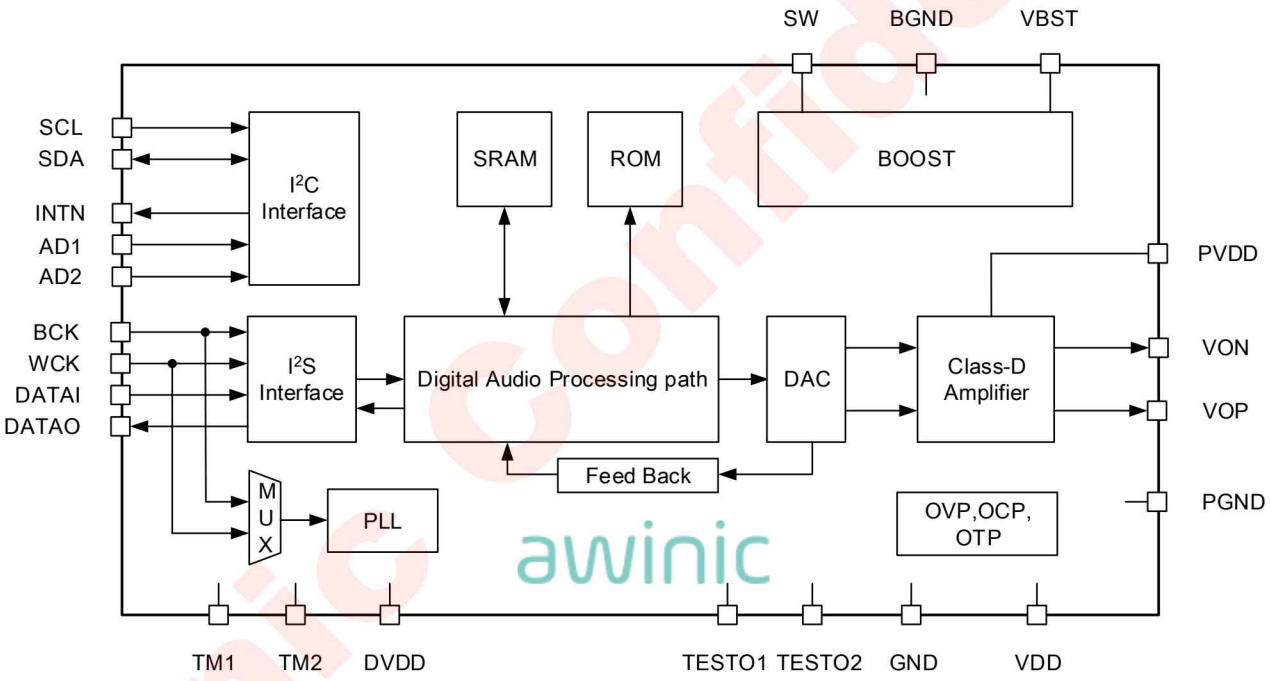


Figure 2 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION DIAGRAM

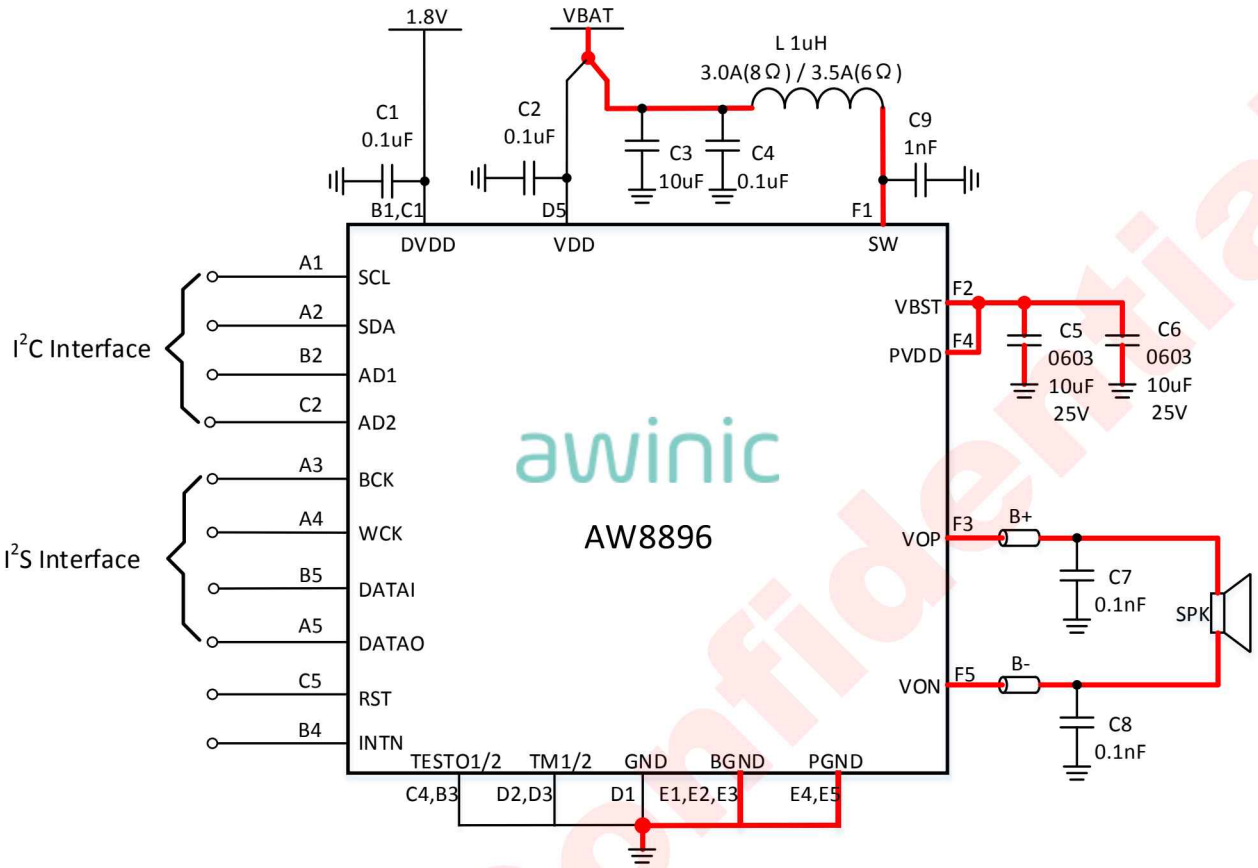


Figure 3 AW8896 Application Circuit

Note: Traces carry high current are marked in red in the above figure

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ORDERING INFORMATION

Product Type	Temperature	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8896CSR	-40℃~85℃	WLCSP 2.55mmx1.94 mm-28B	AW8896	MSL1	RoHS+HF	Tape and Reel 6000 pcs

AW8896 □□□

Shipping
R: Tape & Reel

Package Type
CS: WLCSP

ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage V_{DD}	-0.3V to 5.5V
Digital Supply Voltage V_{DDD}	-0.3V to 1.95V
Minimum load resistance R_L	5Ω
Package Thermal Resistance θ_{JA}	60℃/W
Ambient Temperature Range	-40℃ to 85℃
Maximum Junction Temperature T_{JMAX}	165℃
Storage Temperature Range T_{STG}	-65℃ to 150℃
Lead Temperature（Soldering 10 Seconds）	260℃
ESD Rating (Note 2)	
HBM（Human Body Model）	±2000V
CDM(Charge Device Model)	±1000V
MM(Machine Model)	±200V
Latch-up	
Test Condition：JEDEC STANDARD NO.78B DECEMBER 2008	+IT：450mA -IT：-450mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition：T_A=25℃，VDD=3.6V，DVDD=1.8V，PVDD=5.75V，R_L=8Ω+33μH，f=1kHz(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{DD}	Battery supply voltage	On pin VDD	3		5.5(1)	V
V_{DDD}	Digital supply voltage	On pin DVDD	1.65	1.8	1.95	V
I_{vdd}	Battery supply current	Operating mode, Boost off		4		mA
		Operating mode, Boost on		9		mA
		Power down mode		0.25	1	μA
I_{dvdd}	Digital supply current	Operating mode		10.5		mA
		Power down mode		10		μA
T_{ON}	Startup time			2		ms
T_{OFF}	Shutdown time			2		μs
Note (1)：When the voltage of VDD is higher than 5V, DC-DC converter should be worked in Pass-through mode.						
Boost						
PVDD	Boost output voltage	VDD=3V to 5V		5.75		V
OVP	Over-voltage threshold			1.1*V_{PVDD}		V
	OVP hysteresis voltage			500		mV
I_{L_PEAK}	Inductor peak current limit			2.75		A
I_{SHORT}	Current limit when PVDD short to ground			300		mA
F_{BST}	Operating Frequency	fs = 48KHz, DVDD=1.65V to 1.95V		1.6		MHz
D_{MAX}	The maximum duty cycle			90		%
T_{ST}	Soft-start time			0.4		ms
η_{BST}	Boost converter efficiency	VDD=4.2V, R_L=8Ω		92.6		%
Class-D						
R_{dson}	Drain-Source on-state resistance			100		mΩ
Po	Speaker Output Power	THD+N=1%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD=5.75V		2.62		W

		THD+N=10% , R_L=6Ω+33μH, V_{DD}=4.2V, PVDD=5.75V		3.3		W
		THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD=5.75V		1.96		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD=5.75V		2.46		W
V_{OS}	Output offset voltage	I^2S signal input 0	-30	0	30	mV
η	total efficiency (Boost+Class-D)	V_{DD}=4.2V, Po=1.96W, R_L=8Ω+33μH, PVDD=5.75V		85.5		%
THD+N	Total harmonic distortion plus noise	V_{DD}=4.2V, Po=0.5W, R_L=8Ω+33μH, f=1kHz , PVDD=5.75V		0.02		%
E_N	Speaker Mode Output noise	A-weighting		38		μV
	Receiver Mode Output noise	A-weighting		26		μV
SNR	Signal-to-noise ratio	V_{DD}=4.2V, PVDD=5.75V, Po=1.96W, R_L=8Ω+33μH, A-weighting		101.2		dB
PSRR	Power supply rejection ratio	V_{DD}=4.2V, V_{p-p_sin}=200mV BOOST OFF, 217Hz		-63		dB
		V_{DD}=4.2V, V_{p-p_sin}=200mV BOOST OFF, 1kHz		-63		dB
		V_{DD}=4.2V, V_{p-p_sin}=200mV BOOST ON, 217Hz		-85		dB
		V_{DD}=4.2V, V_{p-p_sin}=200mV BOOST ON, 1kHz		-85		dB
Digital Logical Interface						
V_{IL}	Logic input low level				0.4	V
V_{IH}	Logic input high level		1.3			V
V_{OL}	Logic output low level	I_{OUT}=4mA			0.4	V
V_{OH}	Logic output low level	I_{OUT}=-4mA	1.3			V
Protection						
T_{SD}	Over temperature protection threshold			160		℃
T_{SDR}	Over temperature protection recovery threshold			130		℃
UVP	Under-voltage protection voltage			2.5		V
	Under-voltage protection hysteresis voltage			100		mV

I²C INTERFACE TIMING

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

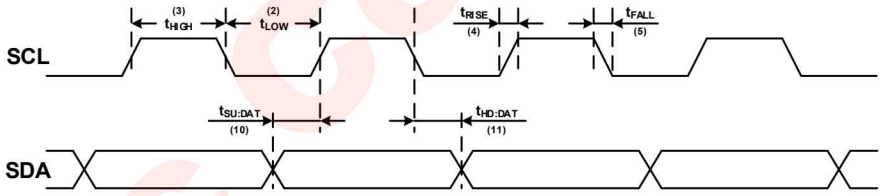


Figure 4 SCL and SDA timing relationships in the data transmission process

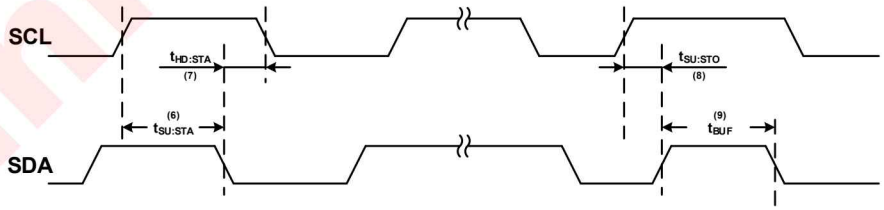


Figure 5 The timing relationship between START and STOP state

I²S INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8		48	kHz
f_{bck}	Bit clock frequency, on pin BCK	32*fs		64*fs	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns
t_d	DATAO output delay time to BCK			50	ns

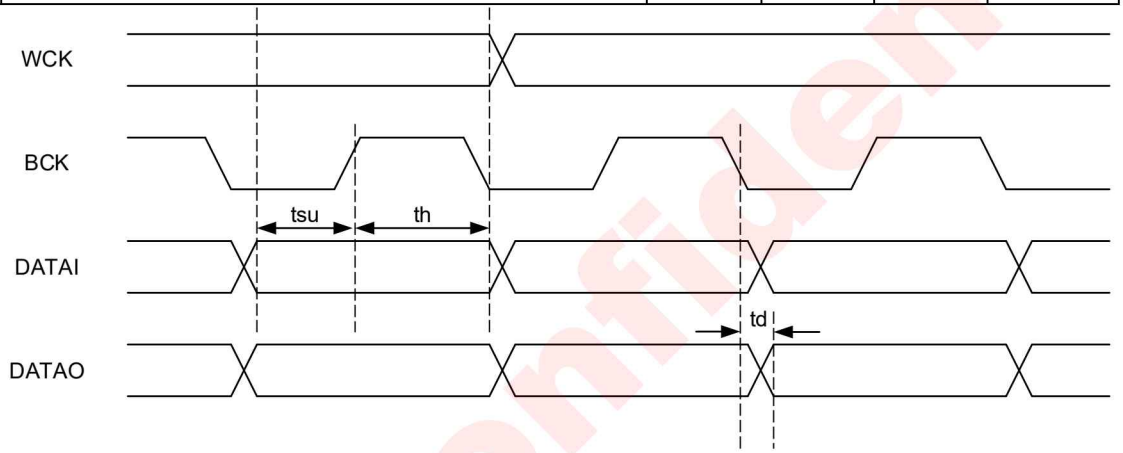
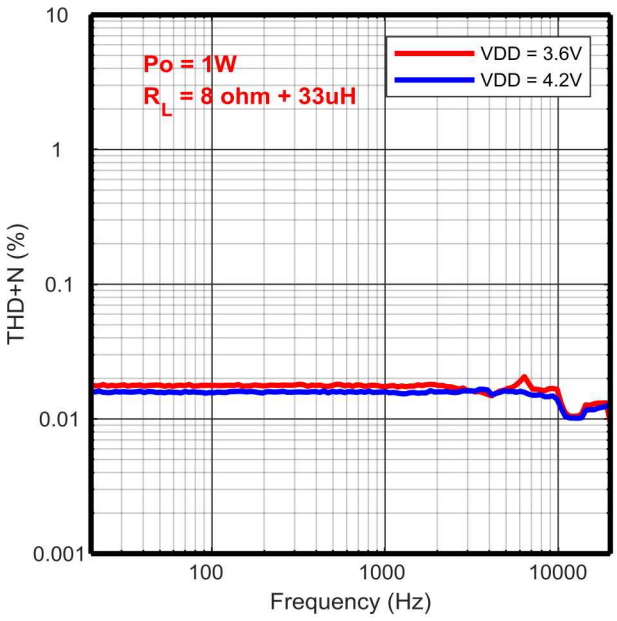


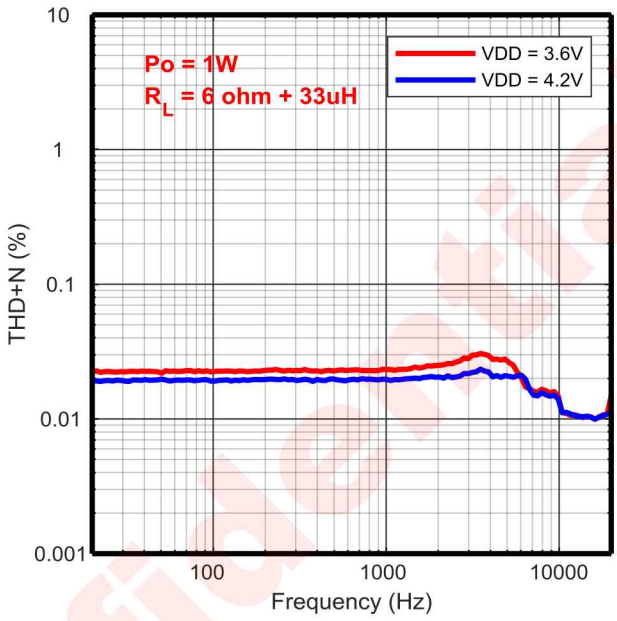
Figure 6 I²S Interface Timing

TYPICAL CHARACTERISTIC CURVES

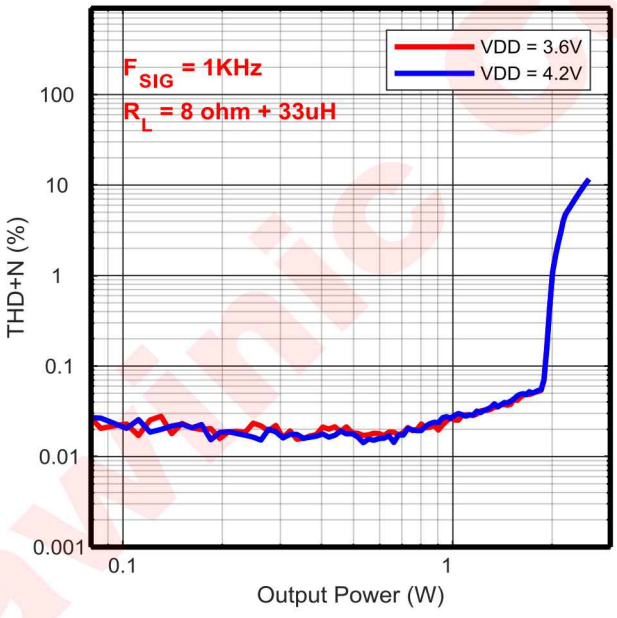
THD+N VS. FREQUENCY



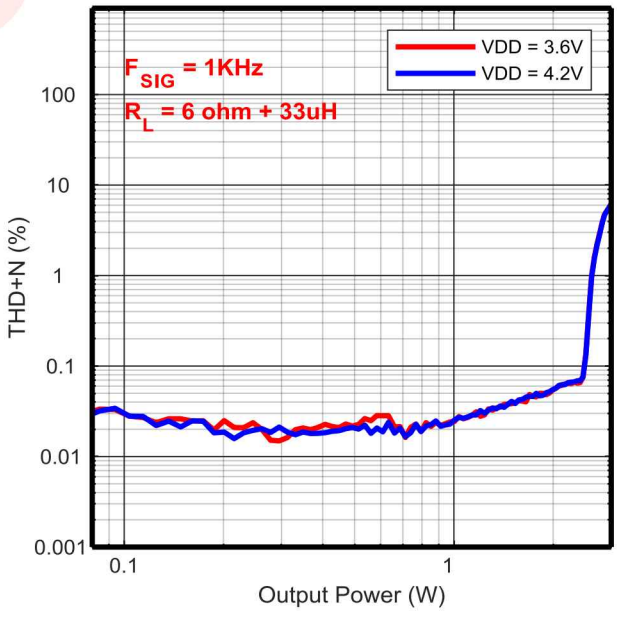
THD+N VS. FREQUENCY



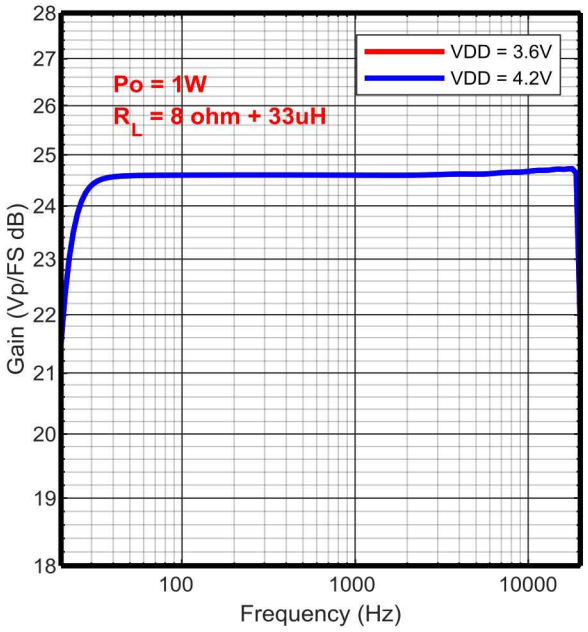
THD+N VS. OUTPUT POWER



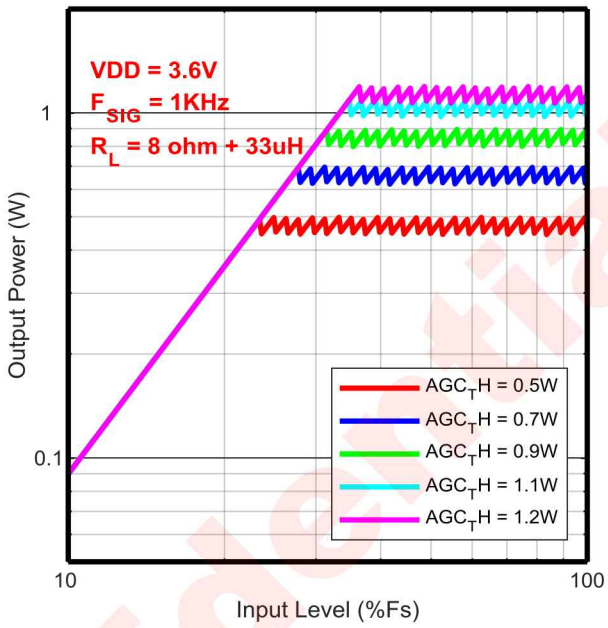
THD+N VS. OUTPUT POWER



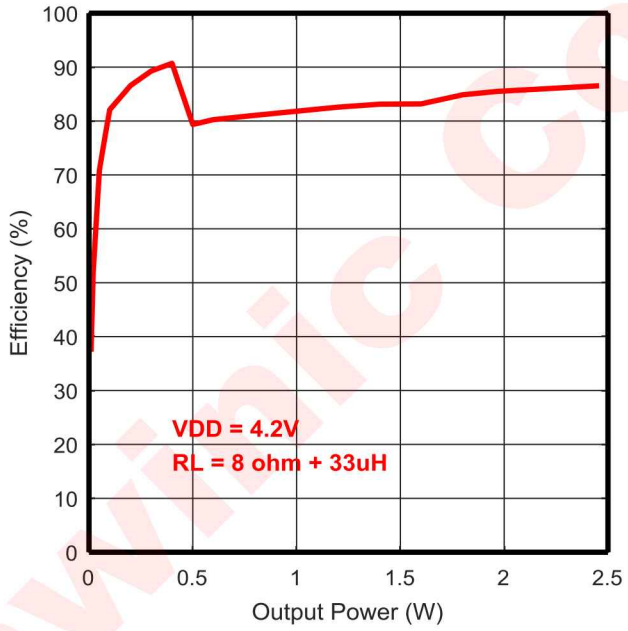
GAIN VS. FREQUENCY



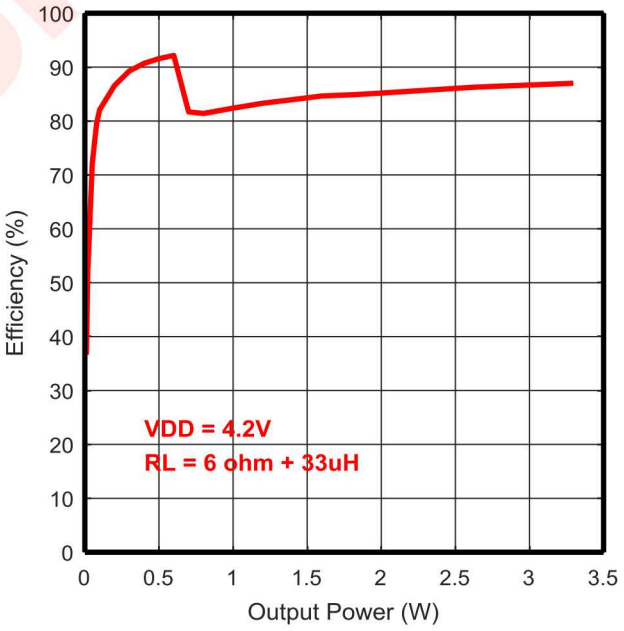
OUTPUT POWER VS. Din



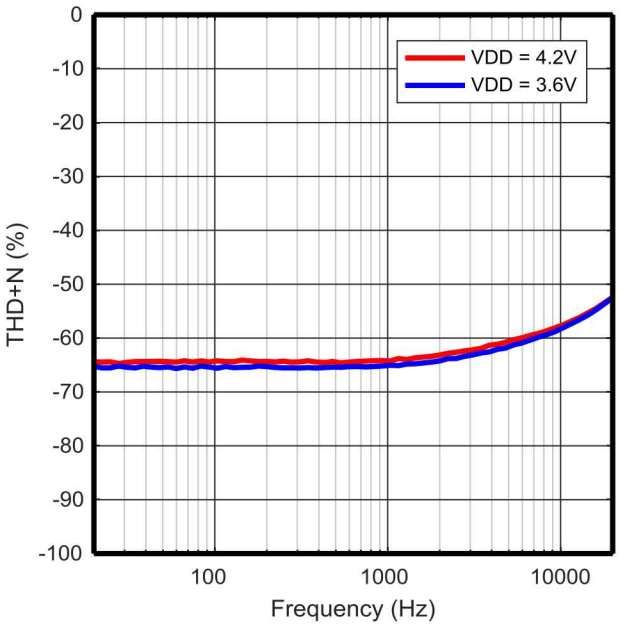
EFFICIENCY VS. OUTPUT POWER



EFFICIENCY VS. OUTPUT POWER



PSRR VS FREQUENCY



DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDD and DVDD supply voltage. When the VDD supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers. The interrupt bit SYSINT.UVLI will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected power-on event has taken place.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{DD} < 2.1V V_{DDD} < 1.1V	Power supply is not ready, chipset is power down.
Stand-By	V_{DD} > 3V V_{DDD} > 1.65V	Power supply is ready, most parts of the device are power down for low power consumption except I^2C interface
Configuring	PWDN = 0	Device is biased while boost and class-K output is floating. Configuring DAP(Digital Audio Processor)
Operating	BSTPD = 0	Amplifier is fully operating

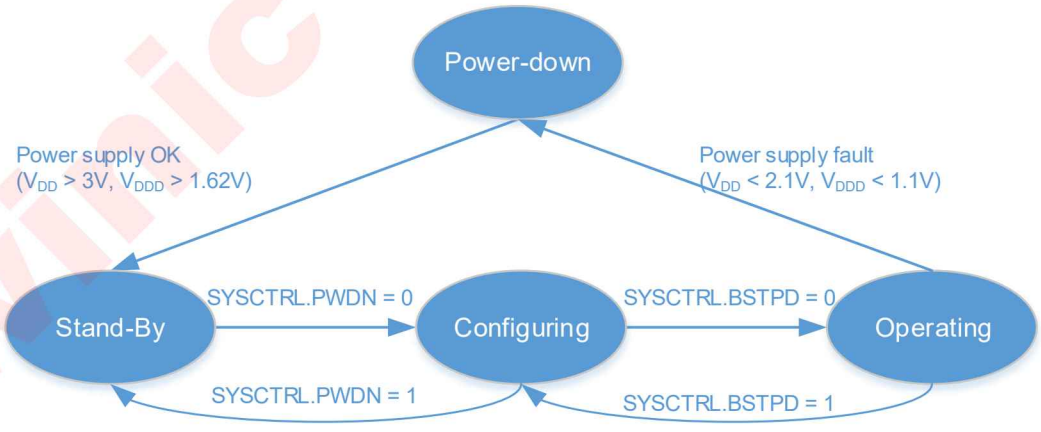


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when the supply voltage under the threshold:

- V_{DDD} < 1.1 V
- V_{DD} < 2.1 V

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

V_{DDD} > 1.65 V and V_{DD} > 3 V

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

CONFIG MODE

The device switches to OFF mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.BSTPD = 1;

In this mode the internal bias, OSC, PLL will start to work

OPERATING MODE

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.BSTPD = 0 to make device in this mode.

POWER UP SEQUENCE

This device power up sequence is illustrated in the following figure:

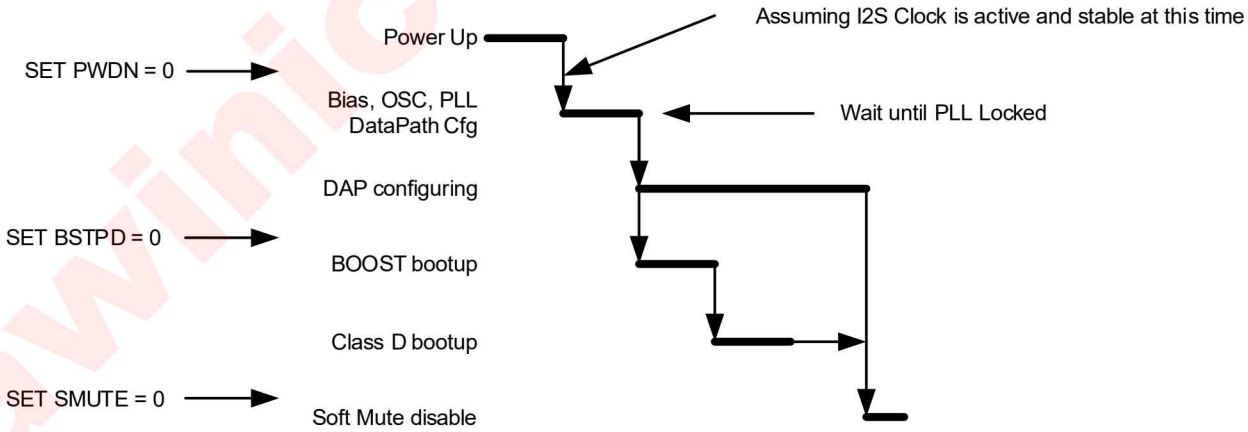


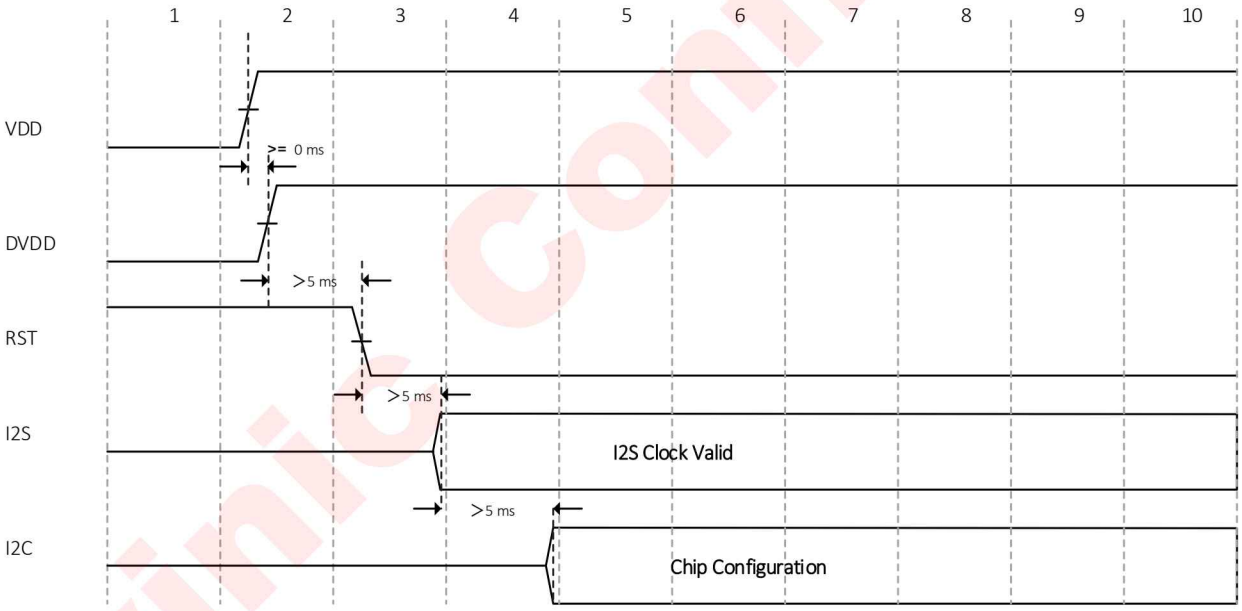
Figure 8 Power up sequence

Detail description for each step is listed in the following table.

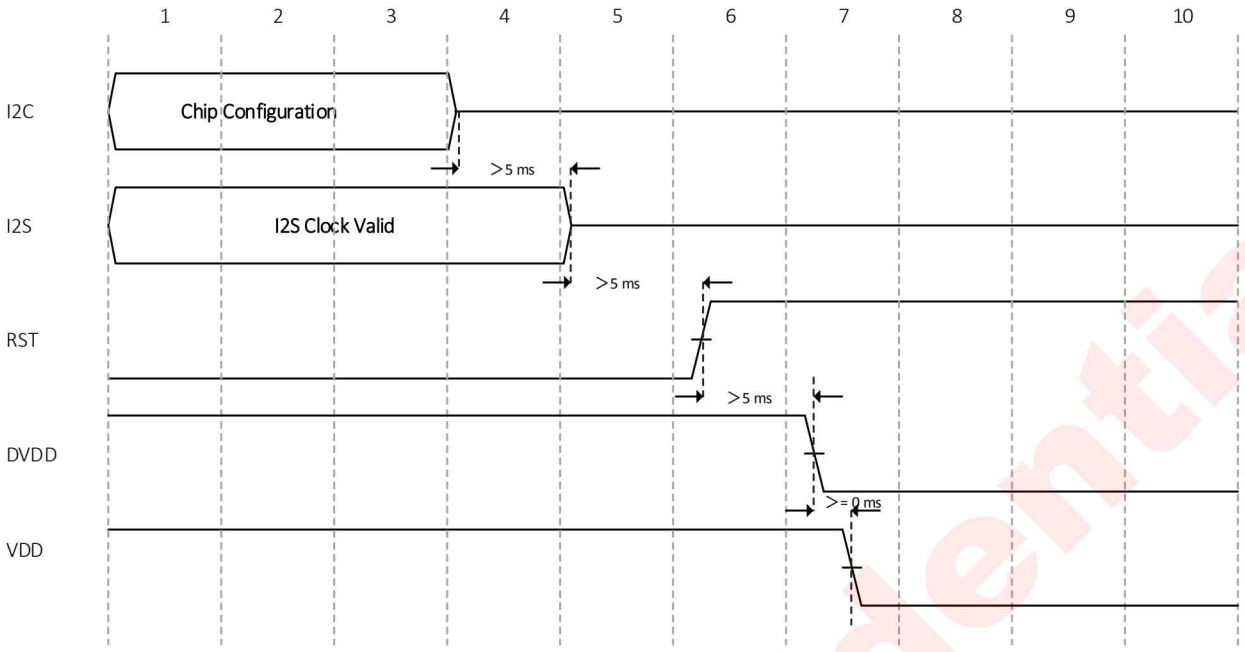
Table 2 Detail Description of Power up sequence

Index	description	Mode
1	Wait for VDD、DVDD supply power up	Power-Down
2	I²S + Data Path Configuration	Stand-By
3.1	Enable system (SYSCTRL.PWDN = 0)	Configuring
3.2	Bias, OSC, PLL active	
3.3	Waiting for PLL locked	
4a.1	DAP Configuration	
4a.2	DAP enable	
4b.1	Enable Boost and amplifier (SYSCTRL.BSTPD =0) Boost and Amplifier boot up	Operating
4b.2	wait SYSST.SWS =1	
5	Release Hard-Mute Data Path active	

Power up sequence considering I2S, I2C timing shows as below:



Power down sequence considering I2S, I2C timing shows as below:



SOFTWARE RESET

Writing 0x55AA to register ID via I²C interface will reset the device internal circuits and all configuration registers.

I²S INTERFACE

Audio data is transferred between the host processor and the AW8896 via the I²S interface. The I²S interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S interface supported, including standard I²S mode, left-justified mode and right-justified data mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. Configuring register I2SCTRL.I2SMD for I²S interface mode and I2SCTRL.I2SFS for data width.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the maximum of the sampling frequencies. The AW8896 supports nine I²S sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz and 48 kHz. It is selected via configurable register I2SCTRL.I2SSR.

The bit clock BCK is used to clock in and clock out the digital audio data across the I²S interface. The number of bit-clock pulses in a frame may need adjustment to accommodate various word lengths. Three BCK frequencies are supported (32, 48 or 64 times fs) via configurable register I2SCTRL.I2SBCK.

The word select and bit clock signals of the I²S input are the reference signals for the I²S input/output interface and the Phased Locked Loop (PLL).

The audio data of input I²S interface can be selected as attenuated -6dBFS or original by configuring bit I2SCTRL.INPLEV. The audio source can be selected from left channel, right channel or the average of the left and right channel via configurable bits I2SCTRL.CHSEL.

Table 3 Supported I²S interface parameters

Interface format(MSB first)	Data width	BCK frequency
Standard I²S	16b 20b/24b/32b	32fs/48fs /64fs 48fs /64fs
left-justified	16b 20b/24b/32b	32fs/48fs /64fs 48fs /64fs
right-justified 16b right-justified 20b/24b/32b	16b 20b/24b/32b	32fs /48fs /64fs 48fs /64fs

The I²S output, DATAO, can be enabled or disabled via bit I2STXCFG.I2STXEN. When be enabled the output data can be selected in left channel or right channel and the unused channel can be selected zero or Hi-Z. When be disabled, the output data of both channels can be selected zero or Hiz. They can be configured by register I2STXCFG.I2SCHS and I2STXCFG.DOHZ.

STANDARD I²S MODE

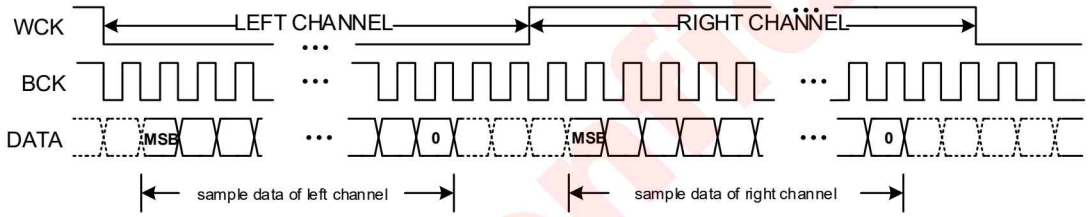


Figure 9 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

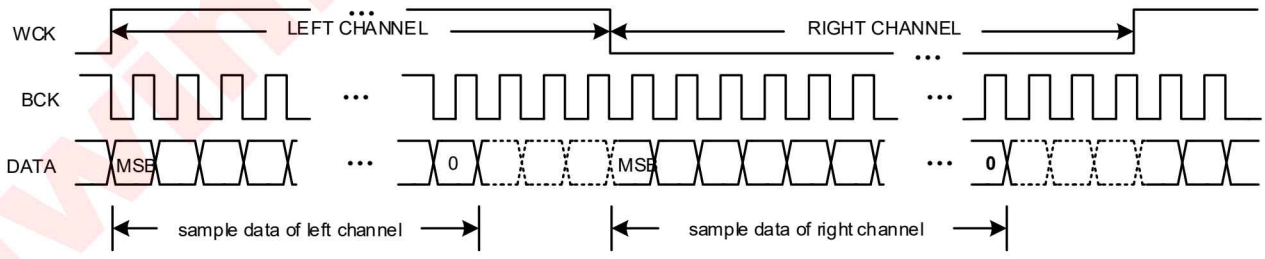


Figure 10 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the rising edge of the word clock.

RIGHT-JUSTIFIED MODE

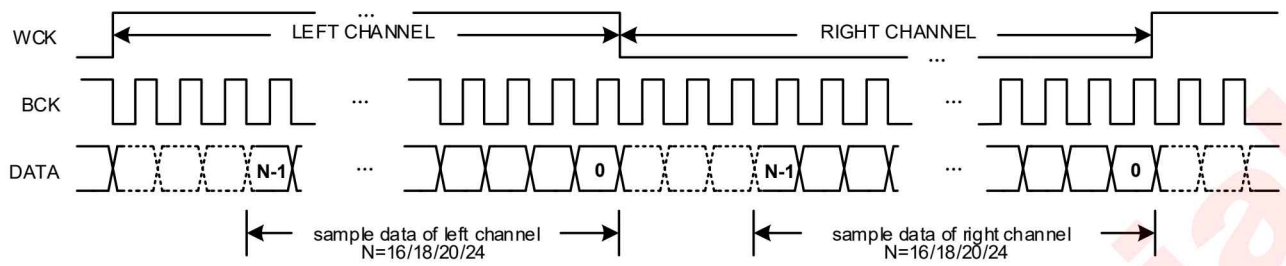


Figure 11 I²S Timing for Right-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- Low cut, Bass, Treble
- Anti-F0
- Feed-Forward Multi-Level AGC
- Volume control
- Soft mute

The signal processing flow in the DAP(Digital Audio Processor) is illustrated in the following figure.

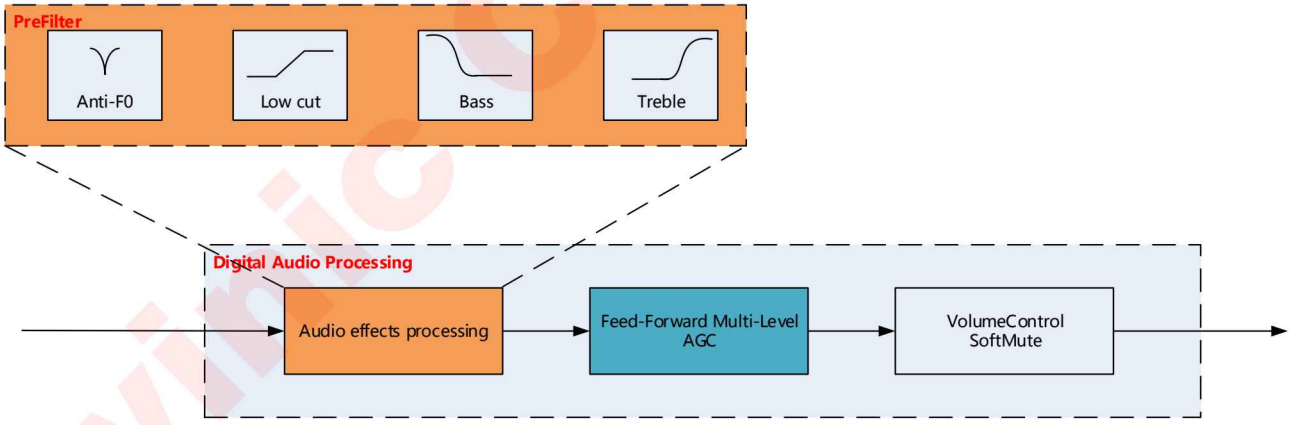


Figure 12 Block Diagram of DAP

AUDIO EFFECTS PROCESSING

Four EQ filters are available and each of the filters can be fully programmable. It's possible to implement any type of second-order filter (high-pass, low-pass, peak, notch etc.) with different design methodologies (butterworth, chebyshev etc.) to achieve the required frequency response.

FEED-FORWARD MULTI-LEVEL AGC

The gain control is implemented in digital algorithm, which provides more flexibility for output power control and make it easy to fix with different applications and varies voltage in power stage.
This module provides Feed-Forward Multi-Level AGC processing after initial gain applied. It performs a perfect clip control to avoid clip occurring when suddenly a high level peak encountered with safe and stable power control.
It checks the level of input signal, once find the peak in a half-waveform is higher than the saturation point (which means clip will occur at this point), it applied an attenuation on all of the points in this half-waveform to avoid clip occurring.

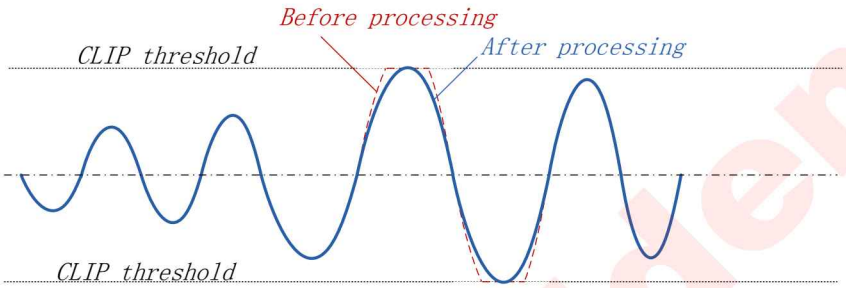


Figure 13 Feed-Forward Multi-Level AGC

A feed-forward delay is required when this function is enabled. And the following parameters are configurable

- DelayTime: the delay time required by this function
- LimiterTh: saturation threshold setting

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -96db with 0.5db/step

SOFT MUTE

The audio signal will be fade-out while this function is enabled. And the speed of fade-in, fade-out is configurable via DAPCFG.SMAT

DC-DC CONVERTER

This device using adaptive boost converter generates the amplifier supply rail, working in 1.6MHz. The DC-DC converter can work in different mode via BSTCFG.BST_MODE:

- **Pass-through mode**: the voltage of VDD is transparently passed to output of converter PVDD
- **Force boost mode**(1): the output voltage is boosted to the programmed output voltage
- **Adaptive boost mode**(1): the output voltage can be switch between VDD and programmed output voltage according to the input audio level.

Pass-through mode

The internal boost circuit is not working; the voltage of VDD is passed to PVDD directly.

Force boost mode

The boost circuit is always working and converts the voltage of VDD to the programmed output voltage. The output voltage is configured via GENCTRL.BSTVOUT

Adaptive boost mode

The boost circuits working dynamically according to the input audio level. When the level of input audio signal is below the setting threshold, the boost circuit will not work. Till the level of input audio signal raised up and above the threshold, the boost circuit starts to work and boost the amplifier supply rail to programmed voltage before the audio signal arriving amplifier power stage.

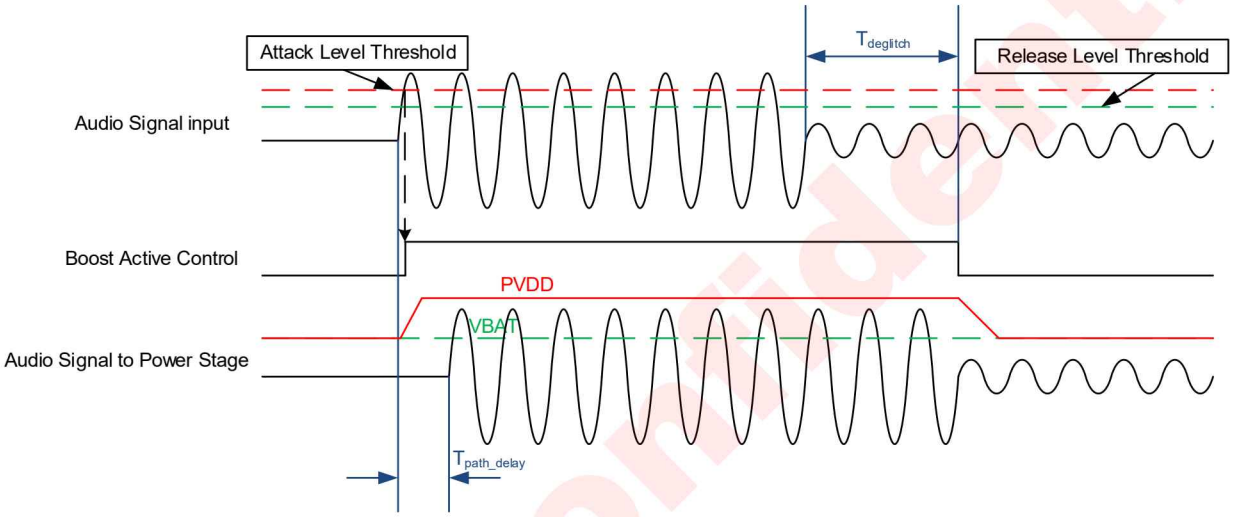


Figure 14 Boost Circuit Behavior in Adaptive Boost Mode

NOTE (1): When the voltage of VDD is higher than 5V, DC-DC converter should be worked in Pass-through mode.

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

The boost circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the boost circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160℃). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130℃), the output stages will start to operate normally again

Over current (short) protection (OCP)

The short circuit protection function is triggered when VOP/VON is short too PVDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. If the receiver magnification is one times, the noise floor will be 26μV. Speaker and Receiver combo applications can be realized without changing any hardware.
When the device is set to receiver mode, the power supply of Class D driver stage is from VDD directly without boost.

AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP\_NORM\_V \times D_{in}$$

D_{in}: the level of input signal with a range from -1 to +1
AMP_NORM_V: the equivalent amplifier output voltage when D_{in} is 1. In receiver mode the AMP_NORM_V is 4V, in speaker mode it's 6V.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD1, AD2 pins according to the following table: The AD1, AD2 pins configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7bit) through 0x37(7-bit).

Table 4 Address Selection

AD2	AD1	I²C address (7-bit)
0	0	0x34
0	1	0x35
1	0	0x36
1	1	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

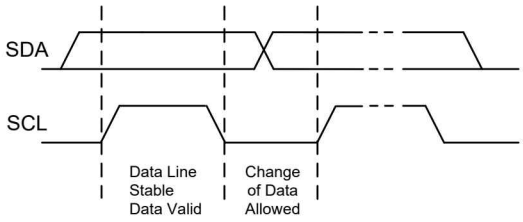


Figure 15 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

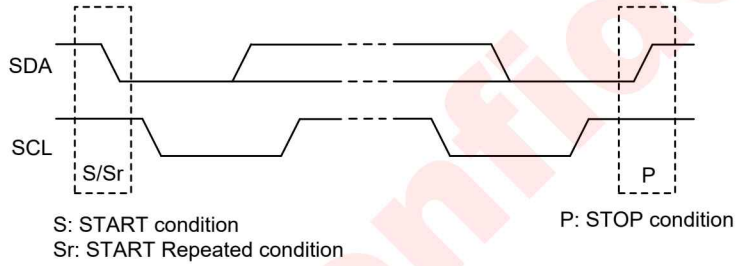


Figure 16 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

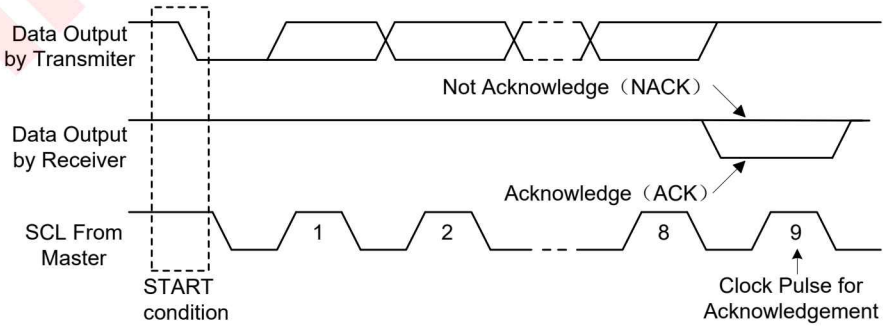


Figure 17 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends high data byte of 16-bit data to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends low data byte of 16-bit data to be written to the addressed register

i) Slave sends acknowledge signal

j) If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)

k) Master generates STOP condition to indicate write cycle end

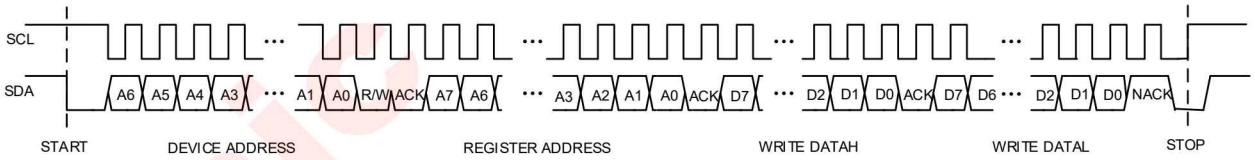


Figure 18 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

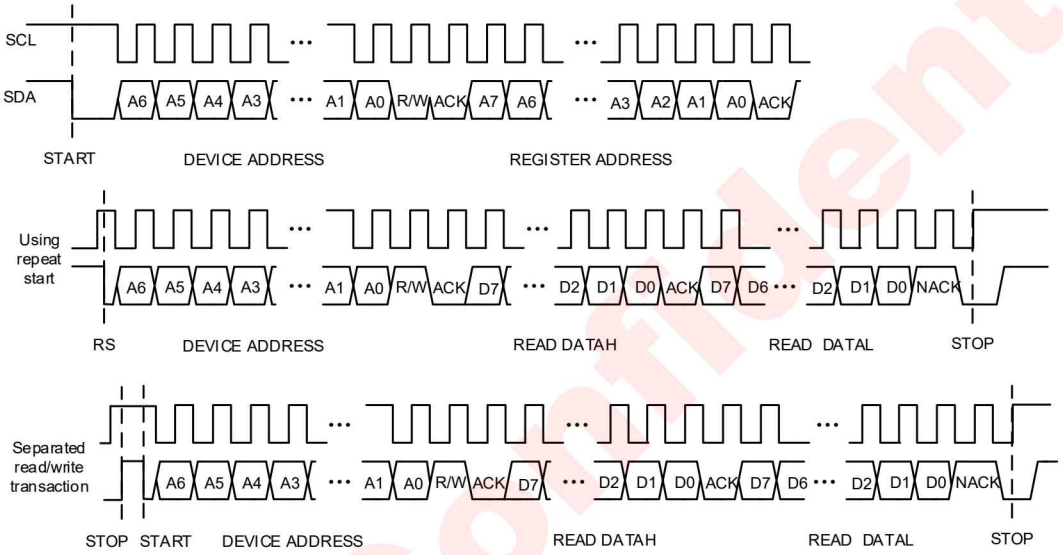


Figure 19 I²C Read Byte Cycle

REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

AW8896 Registers Bitmap

ADDR	NAME	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ID	IDCODE															
0x01	SYSST		UVLS	ADPS	DAPS	BSTOCS		BSTS	SWS	CLIPS	WDS	NOCLKS	CLKS	OCDS	OTLS	OTHS	PLLS
0x02	SYSINT		UVLI	ADPI	DAPI	BSTOCI		BSTI	SWI	CLIPI	WDI	NOCLKI	CLKI	OCDI	OTLI	OTHI	PLLI
0x03	SYSINTM		UVLM	ADPM	DAPM	BSTOCM		BSTM	SWM	CLIPM	WDM	NOCLKM	CLKM	OCDM	OTLM	OTHM	PLLM
0x04	SYSCTRL							INTMOE		RCV_MODE	I2SEN	WSINV	BCKINV	IPLL	DAPBY	BSTPD	PWDN
0x05	I2SCTRL			INPLEV	STEREO_EN	CHSEL		I2SMD		I2SFS		I2SBCK		I2SSR			
0x06	I2STXCFG											DRVSTREN	DOHZ	DSEL		I2SCHS	I2STXEN
0x07	DAPCFG	VOL								SMODE	SMAT						SMUTE
0x08	PWMCTRL	Reserved				PWMDELA				PWMDELB				PWMSH	PWMRE	HDCCE	HMUTE
0x09	HAGCCFG1		SRAMPD	PWMPSC					HAGCE	ATTH							
0x0a	HAGCCFG2	RTTH								HOLDTH							
0x20	DBGCTRL	LPBK		PDUVL	NAMUTE	DISNCKRST	DISPLLRST	CLKMD	OSCPD	AMPPD	PLLPD	I2SRST	SYSRST	DAPDRST	DAPDCE	DAPFCE	SYSCE
0x21	I2SCFG	RX_FLS		RX_THRS		TX_FLS		TX_THRS									I2SRXEN
0x22	I2SSTAT														DPSTAT	I2SROVS	I2STOVS
0x23	I2SCAPCNT			CAP_L_CNT								CAP_R_CNT					
0x40	DAPMADD	MADD															
0x41	DAPMDAT	MDAT															
0x42	WDT									WDT							
0x61	BSTCTRL				BST_MODE		BST_TDEG			BST_RTH				BST_ATH			

DETAILED REGISTER DESCRIPTION

ID: Chip ID Register (Address 00h)

Bit	Symbol	R/W	Description	default
15:0	IDCODE	R	Chip ID (0310h) will be returned after read. All configuration registers will be reset to default value after 0x55aa is written	0x0310

SYSST: System Status Register (Address 01h)

Bit	Symbol	R/W	Description	default
15	Reserved	-	Reserved	
14	UVLS	R	VDD under voltage indicator 1: V_{DD} < 2.5V 0: V_{DD} > 2.6V	
13	ADPS	R	Boost Adaptive status. 0:transparent; 1: boost	
12	DAPS	R	Set when at least one DAP acknowledge request flag is set	
11	BSTOCS	R	Boost over current indicator	
10	Reserved	-	Reserved	
9	BSTS	R	Boost soft start finish indicator, 1: finished	
8	SWS	R	Amplifier switching status. 1: switching; 0: not switching	
7	CLIPS	R	Amplifier clipping status. 1: clipping 0: not clipping	
6	WDS	R	DAP watchdog is triggered; device will be restarted	
5	NOCLKS	R	The reference clock of PLL is not available	
4	CLKS	R	All internal clock are stable CLKS = PLLS & ~IDP	
3	OCDS	R	Over current status in amplifier	
2	OTLS	R	Junction temperature is above 150℃	
1	OTHS	R	Junction temperature is above 160℃	
0	PLLS	R	PLL locked status. 1: locked; 0: unlocked	

SYSINT: System Interrupt Register (Address 02h)

Bit	Symbol	R/W	Description	default
15	Reserved	RC	Reserved	
14	UVLI	RC	Interrupt indicator for Power On and UVLS	
13	ADPI	RC	Interrupt indicator for ADPS	
12	DAPI	RC	Interrupt indicator for DAPS.	
11	BSTOCI	RC	Interrupt indicator for BSTOCS.	
10	Reserved	-	Reserved	
9	BSTI	RC	Interrupt indicator for BSTS.	
8	SWI	RC	Interrupt indicator for SWS.	
7	CLIPI	RC	Interrupt indicator for CLIPS.	
6	WDI	RC	Interrupt indicator for WDS	
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	
4	CLKI	RC	Interrupt indicator for CLKS.	
3	OCDI	RC	Interrupt indicator for OCDS	
2	OTLI	RC	Interrupt indicator for OTLS	
1	OTHI	RC	Interrupt indicator for OTHS.	
0	PLLI	RC	Interrupt indicator for PLLS.	
Note: It will be set to '1' once corresponding interrupt bit changed				

SYSINTM: System Interrupt mask Register (Address 03h)

Bit	Symbol	R/W	Description	default
15	Reserved	RW	Reserved	
14	UVLM	RW	Interrupt mask for UVLI.	0x1
13	ADPM	RW	Interrupt mask for ADPI	0x1
12	DAPM	RW	Interrupt mask for DAPI.	0x1
11	BSTOCM	RW	Interrupt mask for BSTOCI.	0x1
10	Reserved	-	Reserved	0x1
9	BSTM	RW	Interrupt mask for BSTI.	0x1
8	SWM	RC	Interrupt indicator for SWI.	0x1
7	CLIPM	RC	Interrupt indicator for CLIPI.	0x1
6	WDM	RW	Interrupt mask for WDI.	0x1
5	NOCLKM	RW	Interrupt mask for NOCLKI.	0x1
4	CLKM	RW	Interrupt mask for CLKI.	0x1
3	OCDM	RW	Interrupt mask for OCDI.	0x1
2	OTLM	RW	Interrupt mask for OTLI.	0x1
1	OTHM	RW	Interrupt mask for OTHI.	0x1
0	PLLM	RW	Interrupt mask for PLLI.	0x1
Note: Corresponding interrupt will be masked when the mask bit is set to '1'				

SYSCTRL: System Control Register (Address 04h)

Bit	Symbol	R/W	Description	default
15:10	Reserved	-	Reserved	
9:8	INTMODE	RW	interrupt mode 10: active low，open drain output others: reserved	0x2
7	RCV_MODE	RW	Receiver mode enable	0x0
6	I2SEN	RW	Enable/Disable whole I²S interface module 0: disable 1: enable	0x0
5	WSINV	RW	I²S WCK signal invert control 0: not invert 1: inverted	0x0
4	BCKINV	RW	I²S bit clock invert control 0: not invert 1: inverted	0x0
3	IPLL	RW	PLL reference clock selection 0: bit clock 1: word selection signal	0x0
2	DAPBY	RW	DAP bypass control bit 0: normal working 1: bypass DAP	0x1
1	BSTPD	RW	Boost power down control bit: 0: Boost active, (Class D loop will boot up automatically after boost boot up finished) 1: Boost power down	0x1
0	PWDN	RW	System power down control bit 0: active 1: All circuits will enter power down mode	0x1

I2SCTRL: I²S interface Control Register (Address 05h)

Bit	Symbol	R/W	Description	default
15:14	Reserved	-	Reserved	
13	INPLEV	RW	input level initial attenuation 0: 0dB (default value) 1: -6dB	0x0
12	STEREO_EN	RW	when set 1, left and right channel data will be written to DAP	0x0
11:10	CHSEL	RW	Left/right channel selection for I²S input 00: reserved 01: left 10:right 11: mono;(L+R)/2	0x1
9:8	I2SMD	RW	I²S interface mode 00: Philip standard I²S (default) 01: MSB justified 10: LSB justified 11: Reserved	0x0
7:6	I2SFS	RW	I²S data width 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	0x3
5:4	I2SBCK	RW	I²S BCK mode 00: 32*fs 01: 48*fs 10: 64*fs 11: Reserved	0x2
3:0	I2SSR	RW	I²S interface sample rate configuration: 0000: 8 kHz 0001: 11.025kHz 0010: 12 kHz 0011: 16 kHz 0100: 22.5kHz 0101: 24 kHz 0110: 32 kHz 0111: 44.1 kHz 1000: 48 kHz	0x8

I2STXCFG: I²S Tx Channel Configuration Register (Address 06h)

Bit	Symbol	R/W	Description	default
15:5	Reserved	-	Reserved	
5	DRVSTREN	RW	DATAO PAD driving strength setting 0: 2mA 1: 8mA	0x1
4	DOHZ	RW	unused channel data mode 0: 0 1: HiZ	0x1

3:2	DSEL	RW	Control for content in I²S Tx port channel 00: all zero 01: gain 10: DAP processed data Others: reserved	0x0
1	I2SCHS	RW	I²S Tx Channel output selection 0: Left channel 1: Right channel	0x0
0	I2STXEN	RW	Enable/Disable I²S transmitter module 0: disable 1: enable	0x0

DAPCFG: DAP Configuration Register (Address 07h)

Bit	Symbol	R/W	Description	default
15:8	VOL	RW	Volume control, range from 0 to -100db in unit of 0.5db 0: 0db 1: -0.5db … 200: -100db 201~255: Reserved	0x00
7	SMODE	RW	soft mute mode 0: fade per sample 1: fade per 8 samples	0x01
6:1	SMAT	RW	Soft mute attack time, in unit of 333us 0: 32ms 1: 64ms 2: 96ms … 63: 2048ms	0x10
0	SMUTE	RW	Soft mute control 1: soft mute enable, 0: soft mute not enable	0x0

PWMCTRL: PWM Control Register (Address 08h)

Bit	Symbol	R/W	Description	default
15:12	Reserved	-	Reserved	0x0A
11:8	PWMDELA	RW	VON delay setting， in unit of 1/256 PWM cycle	0x0
7:4	PWMDELB	RW	VOP delay setting, in unit of 1/256 PWM cycle	0x0
3	PWMSH	RW	PWM generator reference signal selection 0: Saw-tooth waveform 1: Triangle waveform	0x1
2	PWMRE	RW	PWM reslution.0：7bit；1：8bit (default)	0x1
1	HDCCE	RW	Hardware DC Canceling control 0: hard DC cancel disable; 1: hard DC cancel enable.	0x1
0	HMUTE	RW	Hardware mute control 0: hard mute disable; 1: hard mute enable.	0x1

DAPMADD: DAP Memory Address Register for accessing (Address 40h)

Bit	Symbol	R/W	Description	default
15:0	MADD	RW	Accessing address of DAP memory through I²C interface in unit of 16-bit	0x0000

DAPMDAT: DAP Memory Data Register for accessing (Address 41h)

Bit	Symbol	R/W	Description	default
15:0	MDAT	RW	Accessing entry to DAP memory through I²C interface. Value write to this register will be written into DAP memory in address MADD pointed Value read from this register corresponding to the content in address MADD in DAP memory MADD will be increased by 1 automatically once the MDAT is read or written.	0x0000

WDT: Watchdog timer (Address 42h)

Bit	Symbol	R/W	Description	default
15:8	reserved	-	Reserved	
7:0	WDT	RO	watch dog timer counter	0x00

BSTCTRL: Boost Control Register (Address 61h)

Bit	Symbol	R/W	Description	default
15:13	Reserved	-	Reserved	
12:11	BST_MODE	RW	Boost mode selection 00: Pass-through Mode 01: Force boost Mode 10: Adaptive boost Mode 11: Reserved	0x2
10:8	BST_TDEG	RW	Small signal detection deglitch time 000: 21ms 001: 42ms 010: 84ms 011: 168ms 100: 336ms 101: 672ms 110: 1.3s 111: 2.7s	0x6
7:4	BST_RTH	RW	Adaptive boost release threshold setting: Release Output Power threshold = (BST_RTH *6/32)²/2/R_L Release threshold @ R_L = 8Ω: 0010: 8.8mW 0011: 19.8mW 0100: 35.1mW … 1111: 494mW	0x8
3:0	BST_ATH	RW	Adaptive boost attack threshold setting: Attack Output Power threshold = (BST_ATH *6/32)²/2/R_L Attack threshold @ R_L = 8Ω: 0001: 2.2mW 0010: 8.8mW 0011: 19.8mW … 1110: 430.7mW	0x2

APPLICATION INFORMATION

EXTERNAL COMPONENTS

BOOST INDUCTOR SELECTION

Selecting inductor needs to consider Inductance, size, magnetic shielding, saturation current and temperature current.

a) Inductance

Inductance value is limited by the boost converter's internal loop compensation. In order to ensure phase margin sufficient under all operating conditions, recommended 1μH inductor.

b) Size

For a certain value of inductor, the smaller the size, the greater the parasitic series resistance of the inductor DCR, the higher the loss, corresponds to the lower efficiency.

c) Magnetic shielding

Magnetic shielding can effectively prevent the inductance of the electromagnetic radiation interference. It is much better to choose inductance with magnetic shielding in the application of EMI sensitive environment.

d) Saturation current and temperature rise of current

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, on the one hand, since the magnetic core begins to saturate, inductance value will decline; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. In general, the current value is defined as the saturation current I_{SAT} when the inductance value drops to 70%; the current value is defined as temperature rise current I_{RMS} when inductance temperature rise 40℃.

For particular applications, need to calculate the maximum I_{L_PEAK} and I_{L_RMS}, which is a basis of selecting the inductor. When VDD = 4.2V, PVDD=5.75V, R_L = 8Ω， amplifier R_{DSON} = 100mΩ, when THD = 1% (the maximum power without distortion), the output power is calculated as follows:

$$P_{out} = \frac{\left(V_{out} \times \frac{R_L}{R_L + 2 \times R_{DSON}}\right)^2}{2 \times R_L} = \frac{\left(5.75 \times \frac{8}{8 + 2 \times 0.1}\right)^2}{2 \times 8} = 1.97W$$

In such a large output power, the overall efficiency of the power amplifier is typically 85.5%, in order to calculate the maximum average current $I_{MAX\_AVG\_VDD}$ and maximum peak current $I_{MAX\_PEAK\_VDD}$ drawn from VDD:

$$I_{MAX\_AVG\_VDD} = \frac{P_{out}}{V_{in} \times \eta} = \frac{1.97}{4.2 \times 0.855} = 0.55A$$

$$I_{MAX\_PEAK\_VDD} = 2 \times I_{MAX\_AVG\_VDD} = 2 \times 0.55A = 1A$$

If inductor DCR is 50mΩ, then when the output power of 1.97W, the inductor power loss is:

$$P_{DCR\_LOSS} = 1.5 \times I^2_{MAX\_AVG\_VDD} \times \mathrm{DCR} = 1.5 \times 0.55^2 \times 0.05W = 23mW$$

Wherein the coefficient 1.5 is the square of the ratio of the sine wave current RMS value and average value (there is no consideration of the impact of the inductor ripple, the actual DCR loss will be even greater). If the loss which is resulting from DCR is less than 1% at the 1% THD efficiency (P_{OUT} = 1.97W, η = 85.5%), then:

$$\mathrm{DCR} = \frac{P_{DCR\_LOSS}}{1.5 \times I^2_{MAX\_AVG\_VDD}} \le 1\% \times \frac{P_{out}}{1.5 \times I^2_{MAX_{AVG_{VDD}}} \times \eta} = \frac{0.01 \times 1.97}{1.5 \times 0.55^2 \times 0.855}\Omega = 50.8m\Omega$$

According to the working principle of the Boost, we can calculate the size of the inductor current ripple Δ_{IL}:

$$\Delta I_L = \frac{V_{in} \times (V_{out} - V_{in})}{V_{out} \times f \times L} = \frac{4.2 \times (5.75 - 4.2)}{5.75 \times 1.6 \times 10^6 \times 1 \times 10^{-6}} = 0.71A$$

Thus, the maximum peak inductor current I_{L_PEAK} and maximum effective inductor current I_{L_RMS} is:

$$I_{L\_PEAK} = I_{MAX\_PEAK\_VDD} + \frac{\Delta I_L}{2} = 1 + \frac{0.71}{2}A = 1.355A$$

$$I_{L\_RMS} = \sqrt{I_{MAX\_PEAK\_VDD}^2 + \frac{\Delta I_L^2}{12}} = \sqrt{1^2 + \frac{0.71^2}{12}}A = 1.02A$$

From the above calculation results:

1) For typical DCR about 60mΩ inductance, the efficiency loss caused by around1.5%;
2) In practice, the maximum output power of the amplifier is likely to reach 3W in an instant, so the selected inductor saturation current I_{SAT} requires more than the maximum inductor peak current I_{L_PEAK};
3) In some cases, if the I_{L_PEAK} calculated according to the above method is greater than the set of input inductor current limit value I_{LIMIT}, shows the power amplifier is restricted by inductance input current limit, the actual maximum output power is less than the calculated value, the measured value shall prevail, and I_{SAT} need greater than the set current limiting value I_{LIMIT}, and cannot be less than 3.5A;
4) Take PVDD = 5.75V for example, under different conditions, the typical method of selecting I_{SAT} in the following table:

V_{DD} (V)	**PVDD (V)**	**R_L (Ω)**	**I_{LIMIT} (A)**	**Efficiency(η) (%)**	**P_O (W)**	**I_{L_PEAK} (A)**	Inductor saturation current ISAT minimum value (A)
4.2	5.75	8	2.75	85.5	1.96	1.355	3
4.2	5.75	6	2.75	86	2.62	1.78	3.5

5) As the result of the action of AGC，amplifier will not work long hours at maximum power without distortion, the actual average inductor current is far less than the maximum inductor current effective I_{L_RMS}, so when selecting the inductor, the inductor temperature rise current is not usually a limiting factor;
6) Inductor Selection example: the inductor package size is 201610, inductance value is 1μH, DCR Typical value is 60mΩ, the typical saturation current I_{SAT} is 3.05A, the typical temperature rise current I_{RMS} is 2.55A, suitable for VDD=3.6V, PVDD=5.75 V, speaker impedance R_L=8Ω, inductor input current limit I_{LIMIT}= 2.75A. If you choose I_{SAT} or I_{RMS} of the inductance is too small, it is possible to cause the chip don't work properly, or the temperature of the inductance is too high.

Inductance value	size	DCR (Ω)	I_{SAT} (A)	I_{RMS} (A)
1uH	2.0×1.6×1.0mm	0.060	3.05	2.55
1uH	2.0×1.6×1.0mm	0.060	3.5	3

BOOST CAPACITOR SELECTION

Boost output capacitor is usually within the range 0.1uF~47uF. It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

A) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive; X5R capacitance change within ± 15% in temperature range of 55 ℃ to 85 ℃, X7R capacitance change within ±15% in temperature range of -55 ℃~125 ℃. The Boost output capacitance of AW8896 recommends X5R ceramic capacitors.

B) Voltage Stability

Class II type capacitor has poor voltage stability Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take TDK C series X5R for example, its pressure voltage value is 16V or 25V; the package size is 0805, 1206 or 0603, the capacitance value is 10uF. The capacitor's voltage stability of different types of capacitor is as shown below:

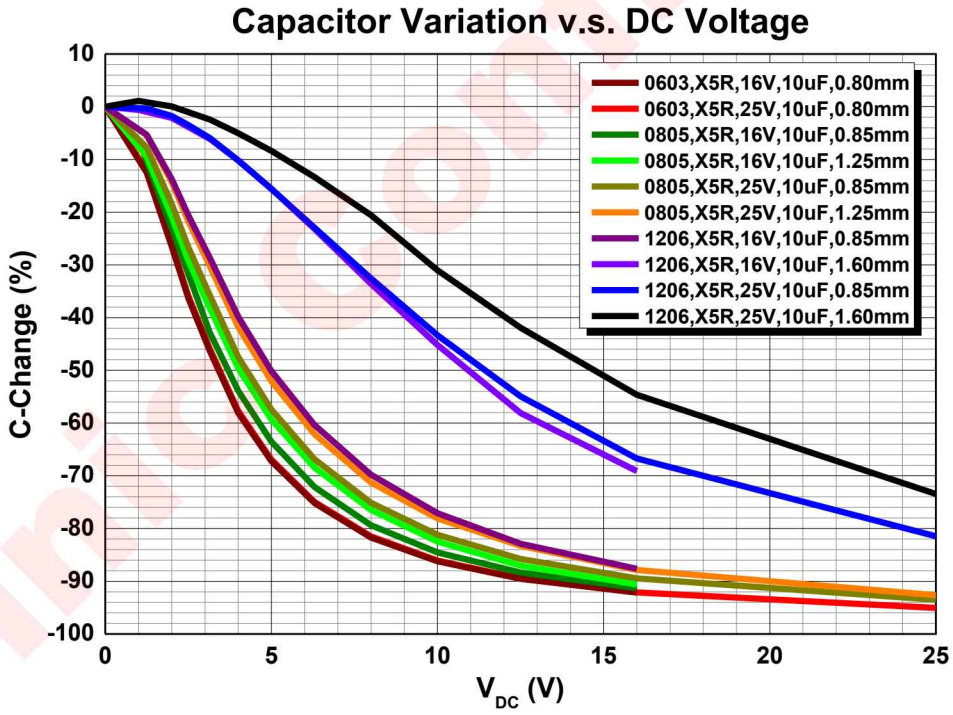


Figure 20 Different types of capacitive voltage stability

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. The higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In typical applications, it is necessary to ensure the residual capacitance should **≥5uF** when PVDD=5.75V. Take

the following capacitances as the Boost of the output capacitor for example:

value	material	size (mm^3)	rated voltage (V)	quantity	value@5.75V
10uF	X5R	1.60×0.80×0.80 (0603)	16	2	5.8uF
10uF	X5R	1.60×0.80×0.80 (0603)	25	2	5.8uF

As for the different manufacturers' capacitors, it's important to determine the type and quantity of the capacitors through the capacitor voltage stability data provided by the manufacturer.

SUPPLY DECOUPLING CAPACITOR (C_S)

The device is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW8896 is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

PCB LAYOUT CONSIDERATIONS

EXTERNAL COMPONENTS PLACEMENT

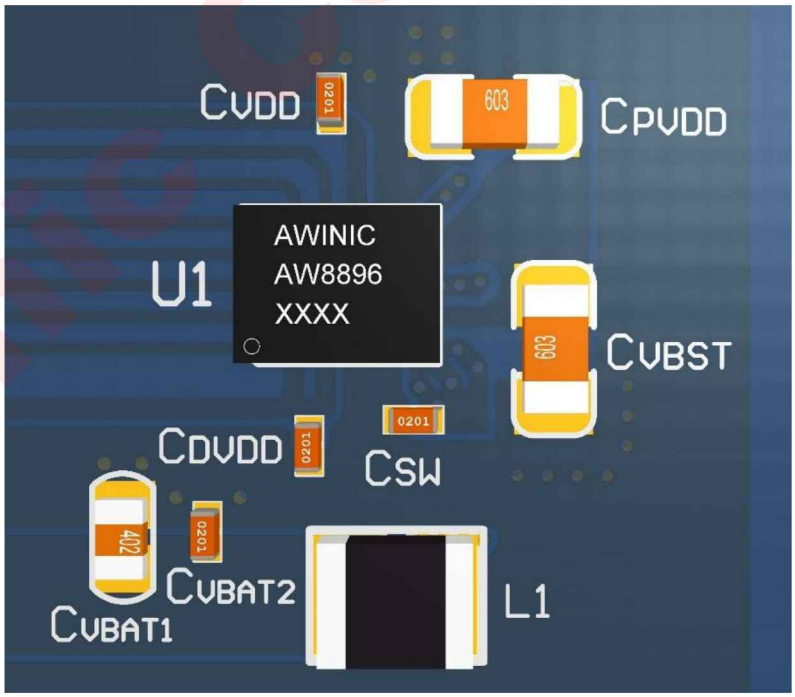


Figure 21 AW8896 External Components Placement

LAYOUT CONSIDERATIONS

This device is a power amplifier chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

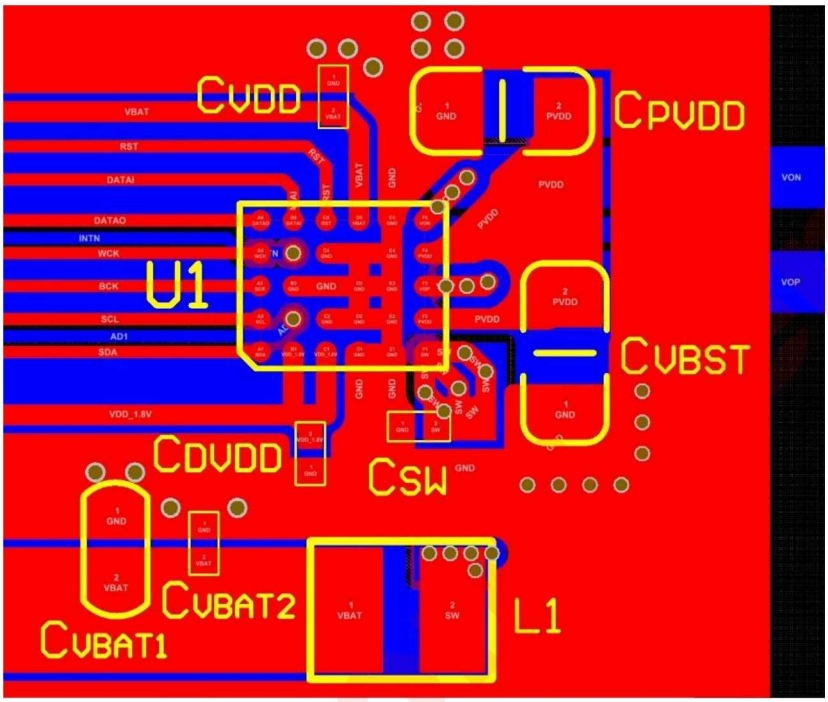
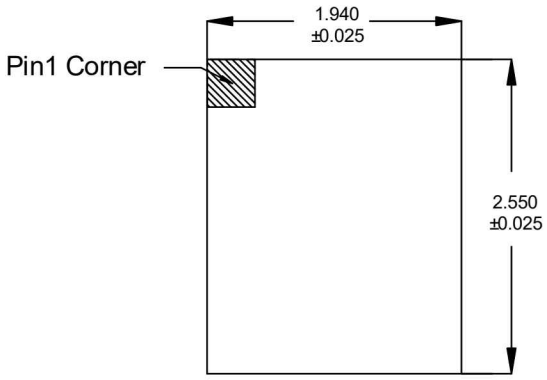


Figure 22 AW8896 Board Layout

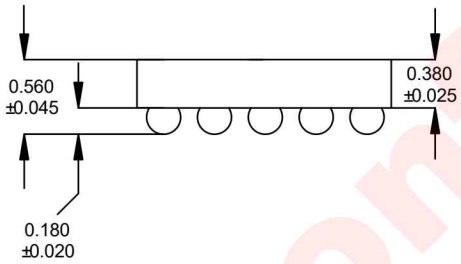
Here are some guidelines:

1. All of the external components close to IC in top layer PCB
2. All filter capacitors close to the corresponding pins of IC.
3. No vias in traces from IC pin PVDD through C_{PVDD} to IC pin PGND, keep the trace as short as possible
4. No vias in trace from IC pin VBST through C_{VBST} to IC pin BGND, keep the trace as short as possible
5. Create solid GND plane near and around the IC, connect BGND, PGND and GND together.
6. The VBAT trace should be split into two paths: one is to inductor(high-current path), the other is to IC's VDD pin
7. C_{VBAT1}, C_{VBAT2} should be placed close to L1.

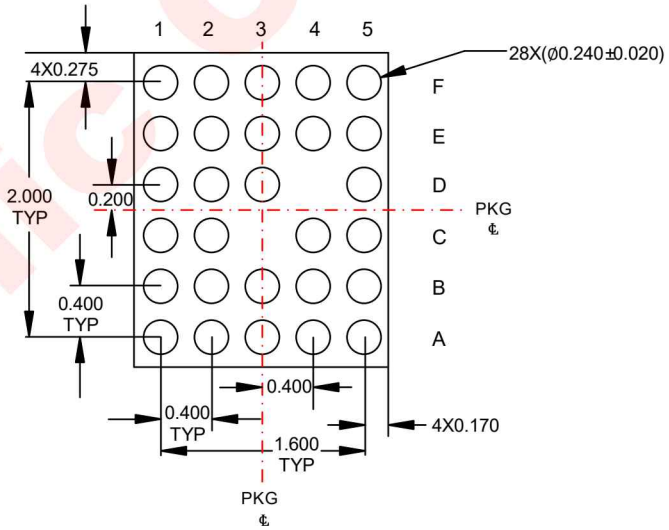
PACKAGE DESCRIPTION



Top View

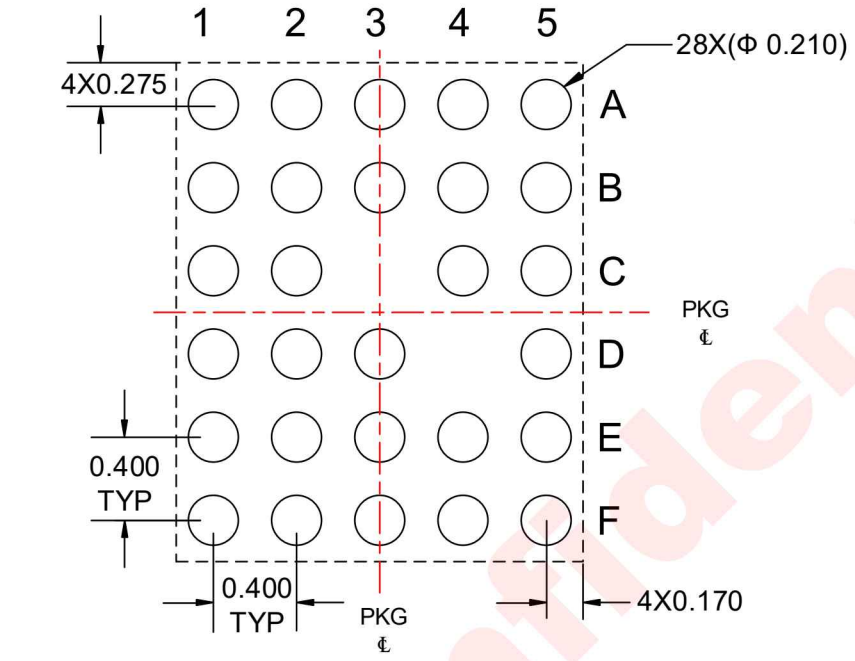


Side View



Bottom View Unit:mm

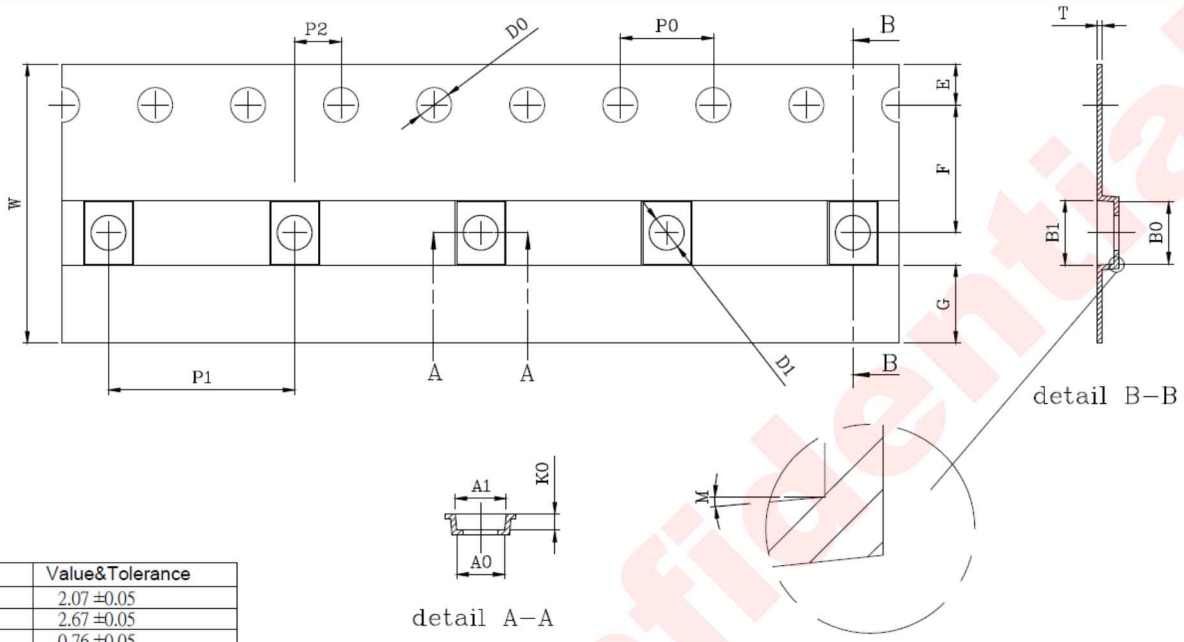
LAND PATTERN DATA



Unit: mm

TAPE AND REEL INFORMATION

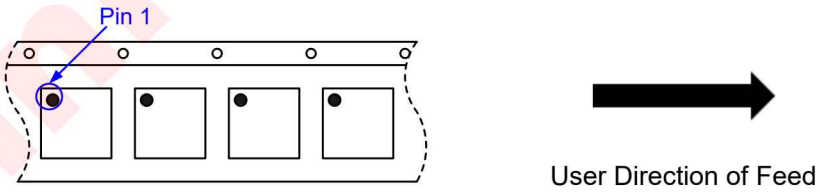
CARRIER TAPE



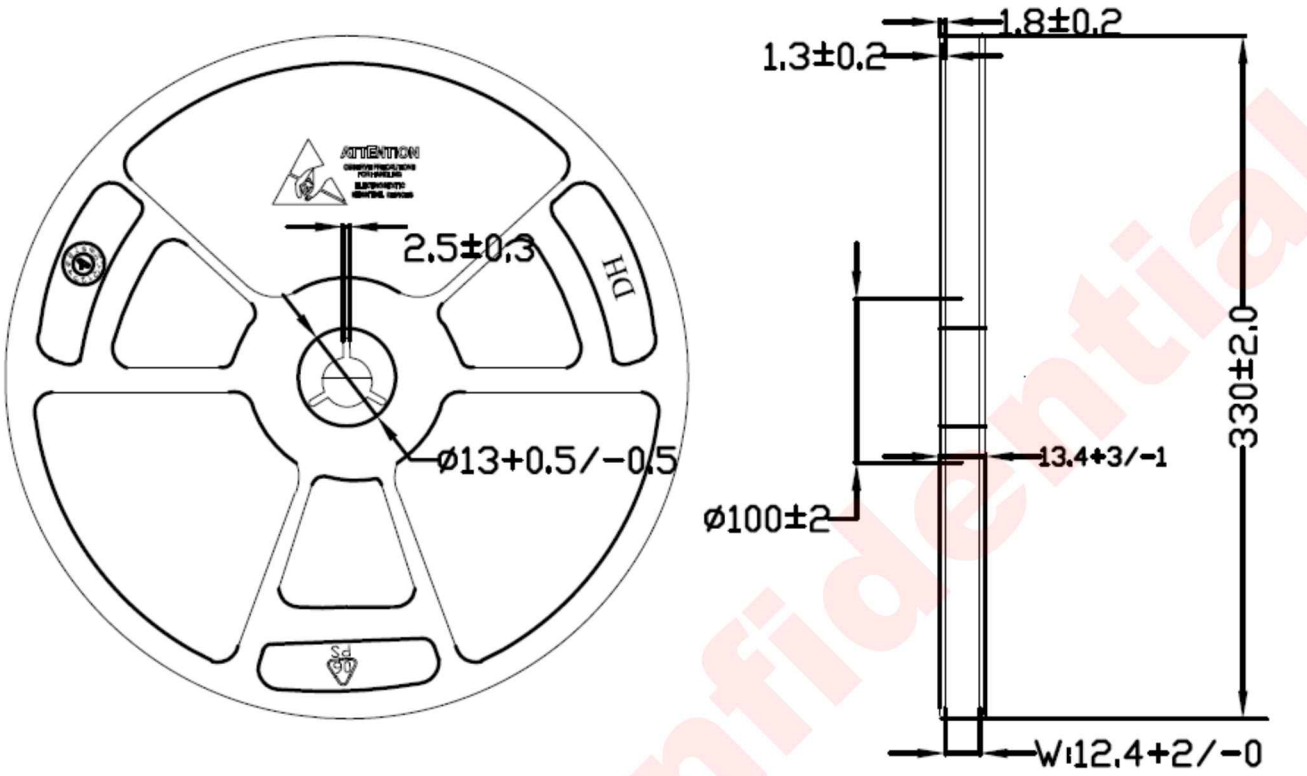
Item	Value&Tolerance
A0	2.07 ±0.05
B0	2.67 ±0.05
K0	0.76 ±0.05
A1	NA
B1	NA
D0	1.50 +0.10/-0.00
D1	1.50 +0.25/-0.00
P0	4.00±0.10
P1	8.00±0.10
P2	2.00±0.05
E	1.75±0.10
F	5.50±0.05
G	NA
T	0.25±0.03
W	12.00+0.30/-0.10
M	Max 5°

NOTE: ALL DIMS IN mm.

PIN 1 DIRECTION



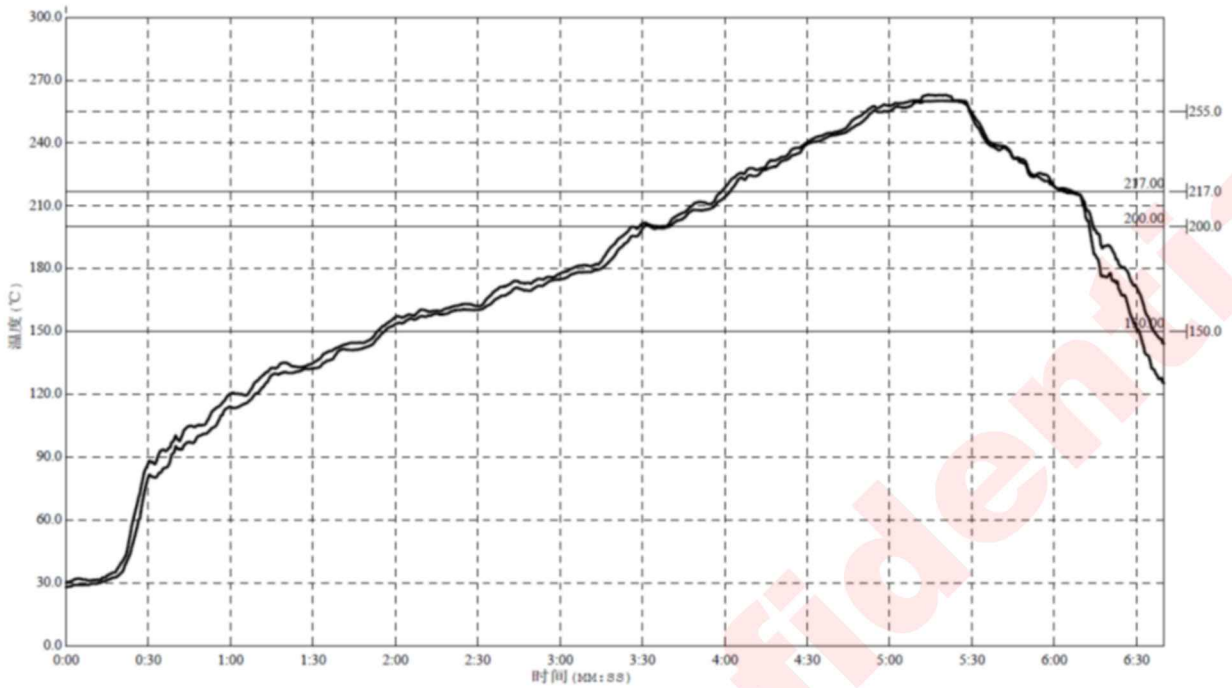
REEL



Note:

1. surface resistivity: 10^{5} to 10^{11} ohms/sq.
2. The colour of reel is deep blue.
3. Restriction criterion of hazardous substance for packing material follow GP-M001.

REFLOW



Reflow Note	Spec
Average ramp-up rate (217℃ to peak)	Max. 3℃/sec
Time of Preheat temp. (from 150℃ to 200℃)	60-120sec
Time to be maintained above 217℃	60-150sec
Peak Temperature	>260℃
Time within 5℃ of actual peak temp	20-40sec
Ramp-down rate	Max. 6℃/sec
Time from 25℃ to peak temp	Max. 8min

REVISION HISTORY

Version	Date	Change Record
V1.0	Jan. 2017	Officially Released
V1.1	Dec. 2017	1. Added the Moisture Type in Ordering Information 2. Added the Environmental Information in Ordering Information 3. Added the User Direction of Feed in Pin 1 direction 4. Added the Land Pattern Data 5. Updated the register map
V1.2	Mar. 2019	Added Power Up Sequence timing
V1.3	May. 2019	1. Updated Typical Characteristic Curves 2. Updated the Package Description 3. Updated the Land Pattern Data
V1.4	Aug. 2019	Update PSRR characteristics

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