

## 5-Channel Capacitive In-Ear Detection and Touch Key Controller

### FEATURES

- 5-channel capacitive sensing
  - Self-capacitive sensing technology
  - Capacitance resolution down to 1fF
  - Maximum offset capacitance up to 150pF
  - Auto-Offset-Tuning (AOT)
  - Each Channel configurable independently
- 400kHz I<sup>2</sup>C interface
  - Default address: 0x12
  - Address configurable via pin CS2
- External interrupt pin INTN, open-drain output
  - Support multi-level distance interrupt
- In-ear detection channels: up to 2 pairs
- Touch key channels: 1~5
- Low power consumption
  - Active mode: 32μA
  - Doze mode: 8.7μA
  - Sleep mode: 7.5μA
  - Deep Sleep mode: 3.3μA
- 1.7V~3.6V power supply
- Operation temperature range: -40°C~85°C
- DFN 2.1mmx1.8mmx0.55mm -10L package

### APPLICATIONS

Mobile phones  
Wearable devices, TWS  
Tablets, Notebooks

### GENERAL DESCRIPTION

AW93105DNR is 5-channel low-power capacitive controller mainly used for in-ear detection and touch key detection in TWS headset. Each channel can be independently configured as sensor input, shield output.

Advanced self-capacitance technology is adopted, which supports parasitic capacitance compensation for each channel up to 150pF. The device has a high resolution ADC, the minimal capacitance that can be detected is as low as 1fF.

A high performance 32bit MCU is integrated by executing the firmware-program in the ROM, it implements all AFE sampling controlling and complicated data processing algorithms including signal filtering, RF noise suppression, baseline calculation, touch status decision, in-ear detection , etc.

With the proprietary sensing algorithm of AWINIC, the device is able to accurately identify the operations such as putting on and taking off the TWS headset, single tap, double tap, slide and so on.

TYPICAL APPLICATION CIRCUIT

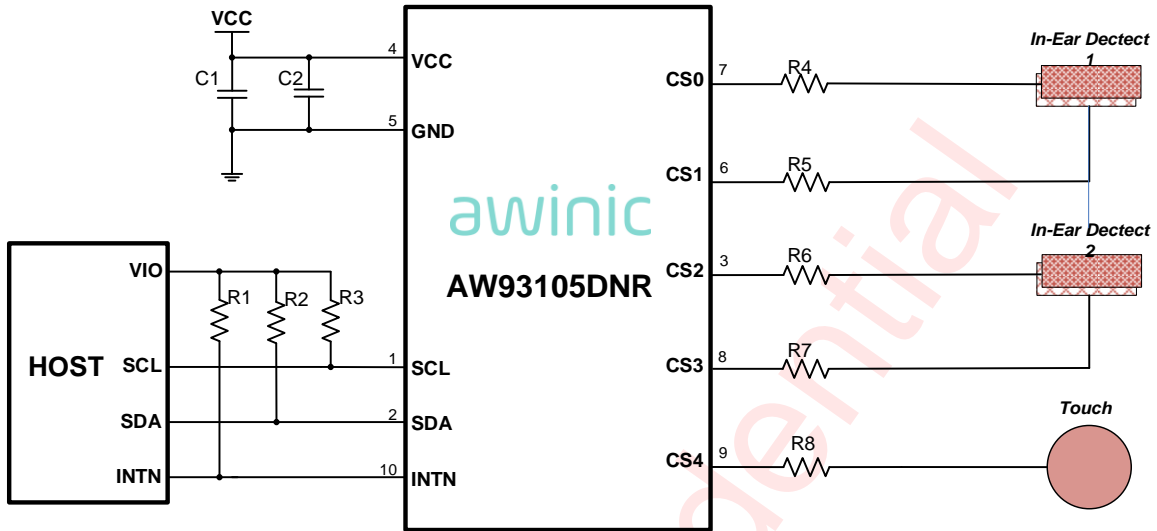


Figure 1 AW93105DNR Typical Application Circuit (in-ear and touch)

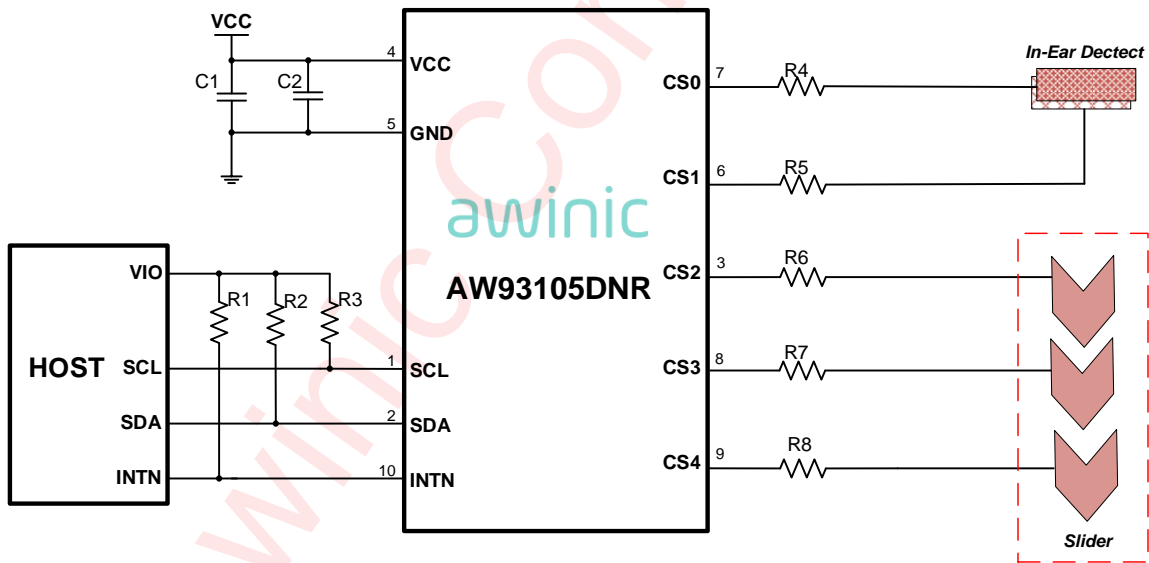
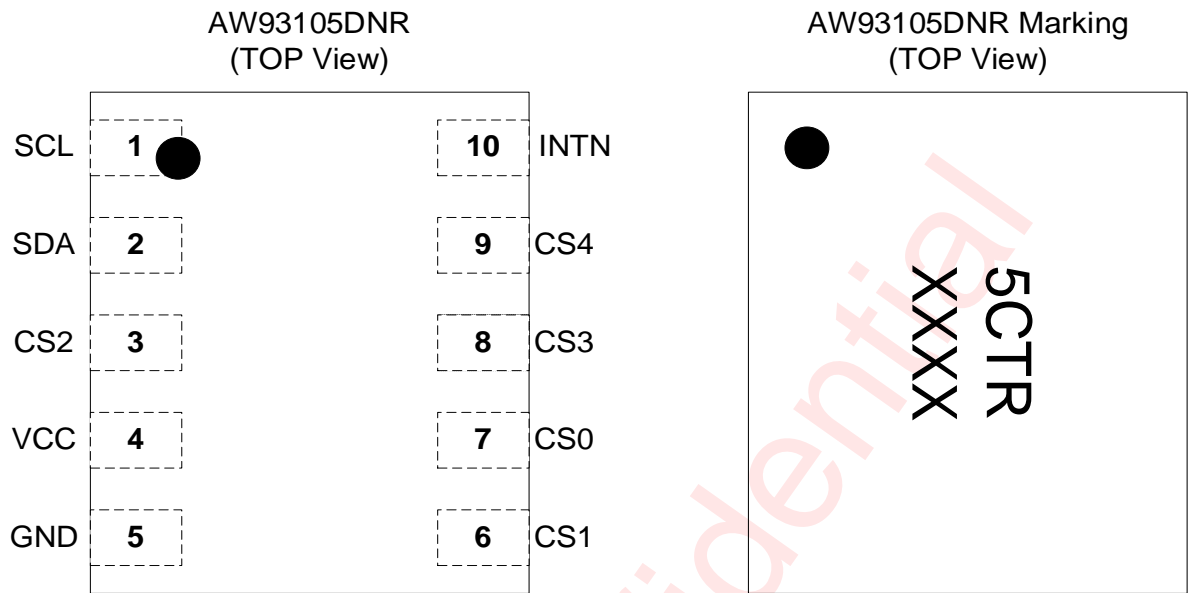


Figure 2 AW93105DNR Typical Application Circuit (in-ear and slide)

## PIN CONFIGURATION AND TOP MARK

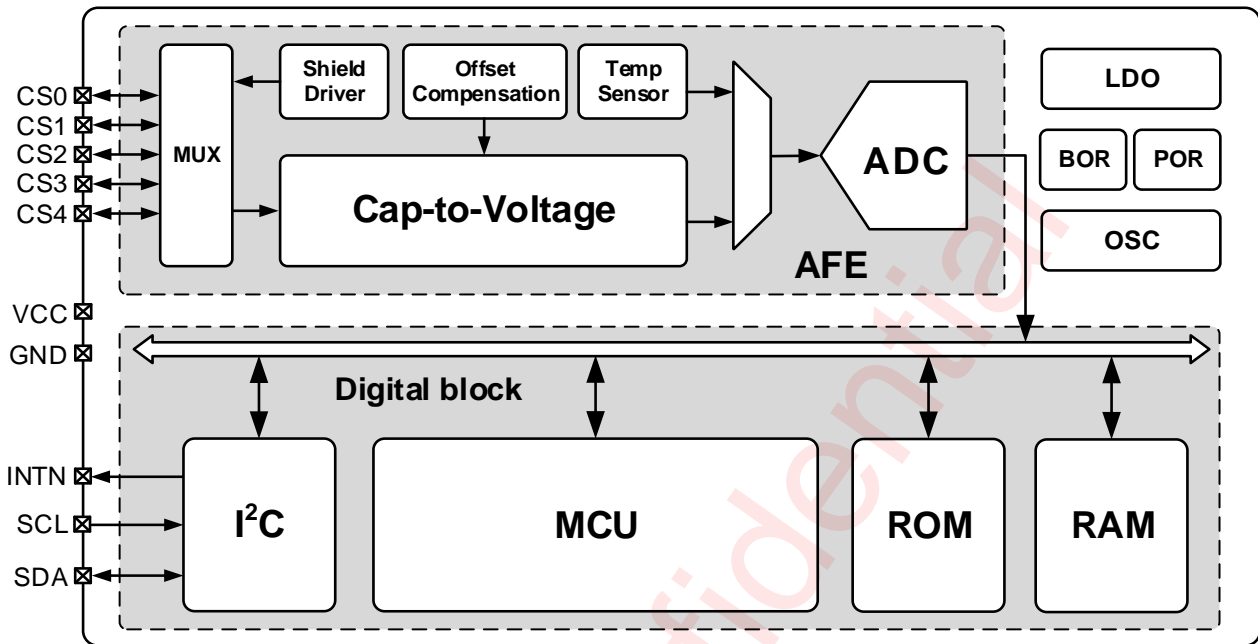


5CTR - AW93105DNR  
XXXX - Production Tracing Code

## PIN DEFINITION

No.	NAME	DESCRIPTION
1	SCL	I <sup>2</sup> C clock, requires pull-up resistor
2	SDA	I <sup>2</sup> C data, requires pull-up resistor
3	CS2	Capacitive Sensor input/shield or I <sup>2</sup> C address select Input (Floating: 0x12, GND: 0x13, VCC: 0x14)
4	VCC	Power supply (1.7V~3.6V), requires decoupling capacitor
5	GND	Ground
6	CS1	Capacitive sensor input/shield
7	CS0	Capacitive sensor input/shield
8	CS3	Capacitive sensor input/shield
9	CS4	Capacitive sensor input/shield
10	INTN	Interrupt output, open drain, requires pull-up resistor

### FUNCTIONAL BLOCK DIAGRAM



Notes: AFE means Analog Front-End.

Figure 3 Functional Block Diagram

### ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93105DNR	-40°C~85°C	DFN 2.1mm×1.8mm×0.55mm-10L	5CTR	MSL1	ROHS+HF	3000 units/ Tape and Reel

**ABSOLUTE MAXIMUM RATINGS**<sup>(NOTE1)</sup>

PARAMETERS		RANGE
Supply voltage range $V_{CC}$		-0.5V to 3.6V
Input voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Output voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Junction-to-ambient thermal resistance $\theta_{JA}$		128.6°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature $T_{JMAX}$		150°C
Storage temperature $T_{STG}$		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (Including HBM CDM) <sup>(NOTE 2)</sup>		
HBM	Pins CSx (x=0,1,2,3,4)	±8kV
	Other pins	±6kV
CDM		±1.5kV
Latch-Up		
Test condition: according to JESD78E		+IT: 350mA -IT: -350mA

**NOTE1:** Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

**NOTE2:** The HBM test method: MIL-STD-883J, the CDM test method: ANSI/ESDA/JEDEC JS-002-2018.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETERS	SYMBOL	MIN	MAX	UNIT
Supply voltage	$V_{DD}$	1.7	3.6	V
Pull-up voltage	$V_{IO}$	1.6	3.6	V
Ambient temperature	$T_A$	-40	85	°C

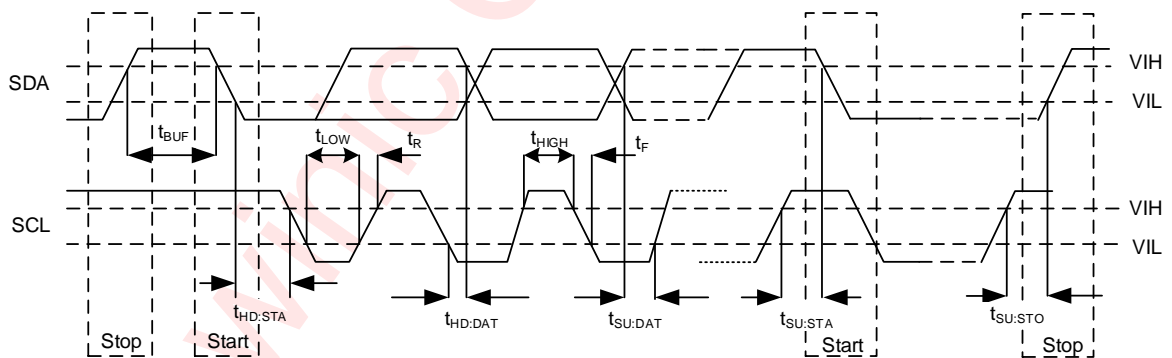
## ELECTRICAL CHARACTERISTICS

Note: Typical values are given for  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 2.8\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
<b>CHIP CURRENTS</b>						
$I_{\text{SLEEP}}$	Sleep Mode Current		7.5	10	$\mu\text{A}$	
$I_{\text{DOZE}}$	Doze Mode Current		8.7	16	$\mu\text{A}$	
$I_{\text{ACTIVE}}$	Active Mode Current		32	45	$\mu\text{A}$	
<b>CAPACITANCE SENSING</b>						
$C_{\text{RANGE}}$	Measurement Range		$\pm 0.55$	$\pm 2.2$	$\pm 9.9$	$\text{pF}$
$N_{\text{BIT}}$	Measurement Resolution		16			bits
$C_{\text{RES}}$		$C_{\text{RANGE}} = 0001$		1		fF
$F_{\text{OSC}}$	Nominal OSC Frequency		4			MHz
$F_{\text{Trim}}$	OSC Trim Accuracy	Around Nominal Value $T_A = 25^\circ\text{C}$ , $V_{CC} = 2.8\text{V}$	-4		4	%
$F_{\text{Temp}}$	OSC Temp. Dependency	Around Nominal Value $T_A = 25^\circ\text{C}$ , $V_{CC} = 2.8\text{V}$		$\pm 1$		%
$F_{\text{VCC}}$	OSC VCC Dependency	Around Nominal Value $T_A = 25^\circ\text{C}$ , $V_{CC} = 2.8\text{V}$		$\pm 0.6$		%
$F_{\text{S}}$	Nominal Sampling Frequencies	Programmable with $F_{\text{REQ}}$			250	kHz
$C_{\text{DCEXT}}$	External DC Cap. to GND per Measurement Channel	One CSx as measured input			150	$\text{pF}$
$R_{\text{FILTN}}$	Input driving Res		0		30	$\text{k}\Omega$
$R_{\text{INT}}$	Compensation Res		125		1k	$\Omega$
<b>TEMPERATURE SENSING</b>						
$T_{\text{INRANGE}}$	Input Range	Ambient Temperature ( $T_A$ )	-40		85	$^\circ\text{C}$
$T_{\text{OUTRANGE}}$	Output Range		0		32767	LSB
<b>I<sup>2</sup>C INTERFACE</b>						
$I_{\text{OL}}$ (SDA, INTN)	Output low current	$V_{\text{OL}} \leq 0.4\text{V}$	8			mA
$V_{\text{IH}}$	Input high level	SCL, SDA	1.35		3.6	V
$V_{\text{IL}}$	Input low level	SCL, SDA	-0.5		0.45	V

**I<sup>2</sup>C INTERFACE TIMING**

PARAMETER		MIN	TYP	MAX	UNIT
F <sub>SCL</sub>	Interface Clock frequency			400	kHz
T <sub>HD:STA</sub>	(Repeat-start) Start condition hold time	0.6			μs
T <sub>LOW</sub>	Low level width of SCL	1.3			μs
T <sub>HIGH</sub>	High level width of SCL	0.6			μs
T <sub>SU:STA</sub>	(Repeat-start) Start condition setup time	0.6			μs
T <sub>HD:DAT</sub>	Data hold time	0			μs
T <sub>SU:DAT</sub>	Data setup time	0.1			μs
T <sub>R</sub>	Rising time of SDA and SCL			0.3	μs
T <sub>F</sub>	Falling time of SDA and SCL			0.3	μs
T <sub>SU:STO</sub>	Stop condition setup time	0.6			μs
T <sub>BUF</sub>	Time between start and stop condition	1.3			μs
T <sub>SP</sub>	Input glitch suppression			50	ns

**Figure 4 I<sup>2</sup>C Interface Timing**

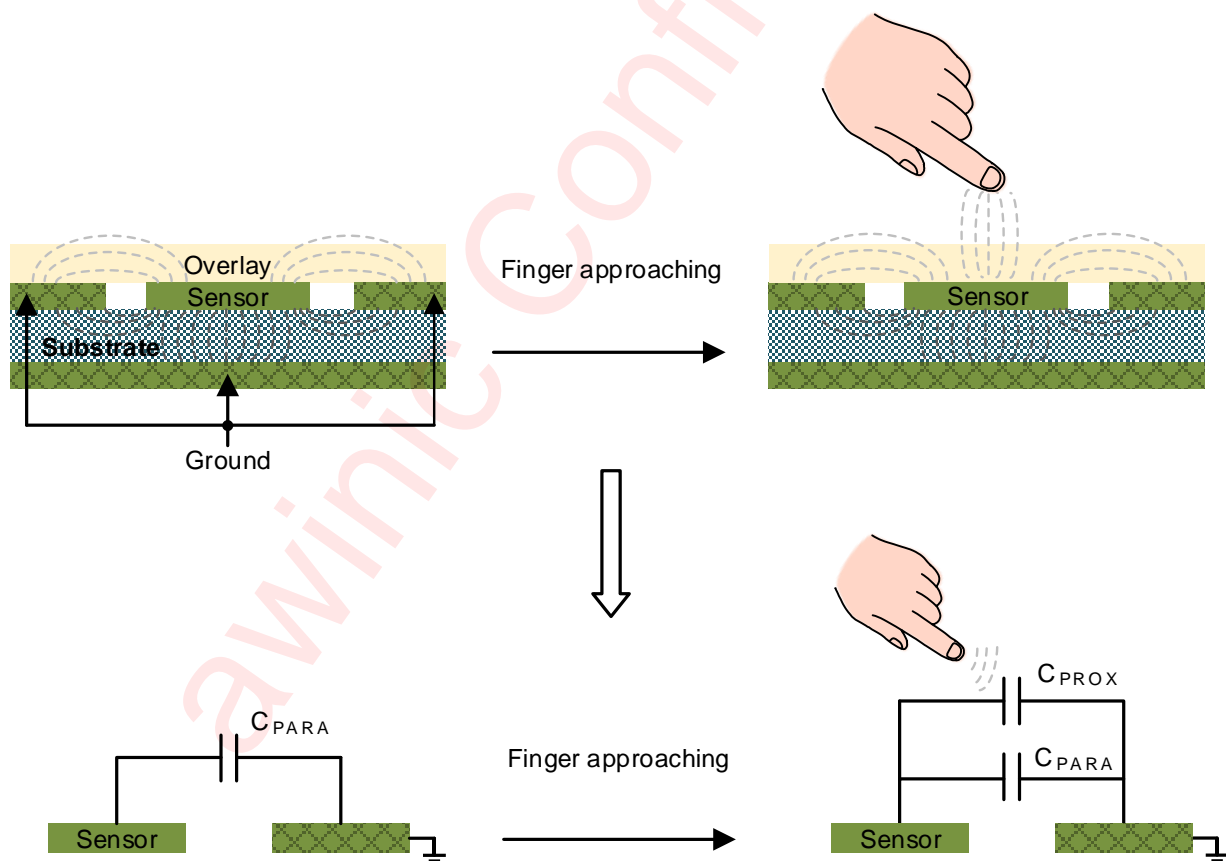
## DETAILED FUNCTIONAL DESCRIPTION

### OVERVIEW

AW93105DNR is a capacitive in-ear detection and touch key controller with built-in a low power MCU mainly used for in-ear detection and touch key detection in TWS headset. It is comprised of high-performance self-capacitance detecting Analog-Front-End (AFE), imbedded 32bit MCU, ROM, RAM, OSC and I<sup>2</sup>C interface, etc. The AFE drive the sensor and shield electrode, and convert the capacitance of sensor to digital data. The MCU executes the algorithm program stored in the ROM, and perform complicated data process such as signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency(RF) noise suppression, proximity decision, etc. It is able to accurately identify the operations such as putting on and taking off the TWS headset, single tap, double tap and slide.

### CAPACITIVE SENSOR INTRODUCTION

Self-capacitance sensing technology detects the capacitance change of a touch or proximity sensor caused by a target object approaching the sensor. The target object could be a human finger, face, or any conductive object. The figure below shows the basic structure and equivalent model of a capacitance sensor. The top layer is the overlay, and the middle green area below is a copper sensor pad. The sensor is usually surrounded by ground, resulting in a parasitic capacitance ( $C_{PARA}$ ).



**Figure 5 Capacitive sensor structure**

When a voltage is forced on a sensor, an electric field is created around the sensor. As the target object approaches the electrode, some of the electric field lines couples to the target object and add a small amount of finger capacitance ( $C_{PROX}$ ) to the existing  $C_{PARA}$ . This feature can be used to detect proximity, in-ear or touch key action.



## CAPACITIVE SENSING TECHNIQUES

The proximity sensing system consists of three parts, capacitive sensor, AFE and DSP. The sensor capacitance will change when the target object is approaching or moving away. AFE drives the capacitive sensors and shield electrodes, and converts the sensor capacitance to digital data. DSP deals with the data from AFE, and transmits the sensor capacitance value (Diff) and proximity status (Status) to the host.

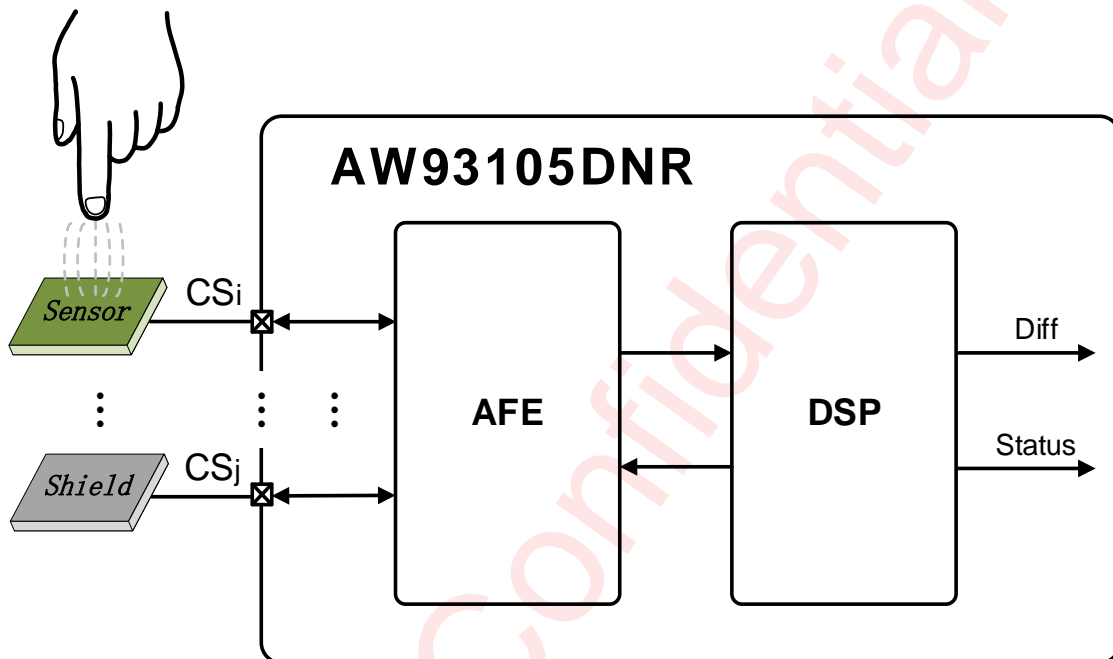


Figure 6 Proximity Sensor Operation Overview

## AFE DESCRIPTION

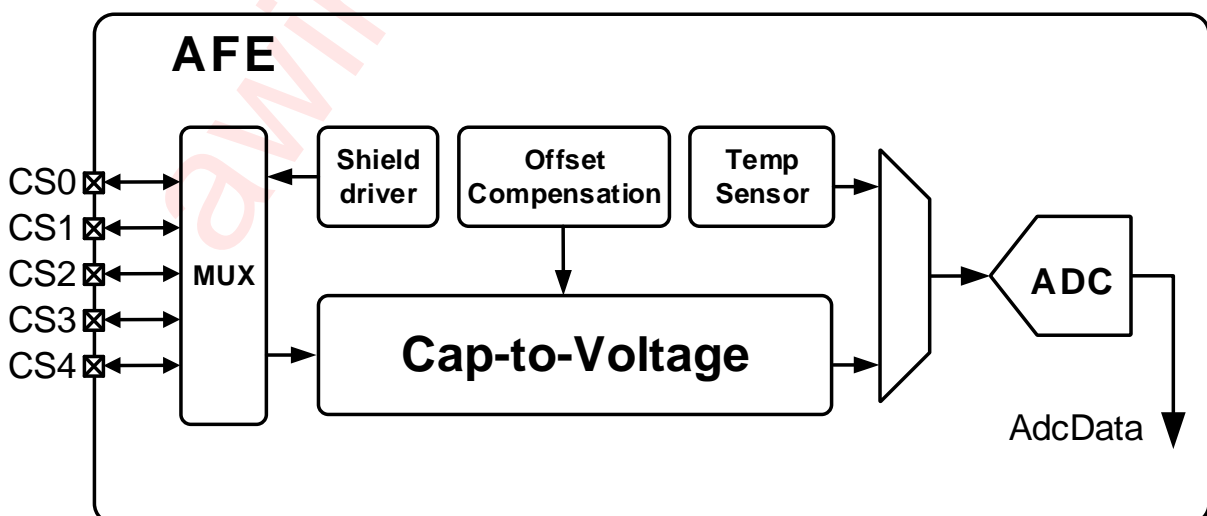
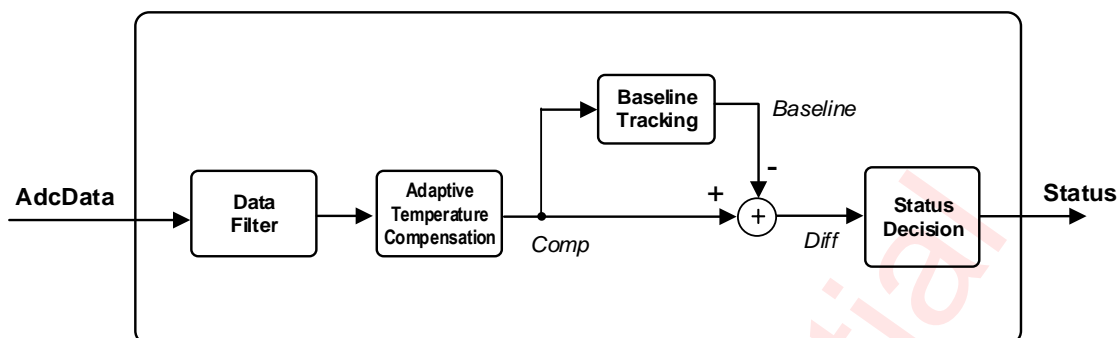


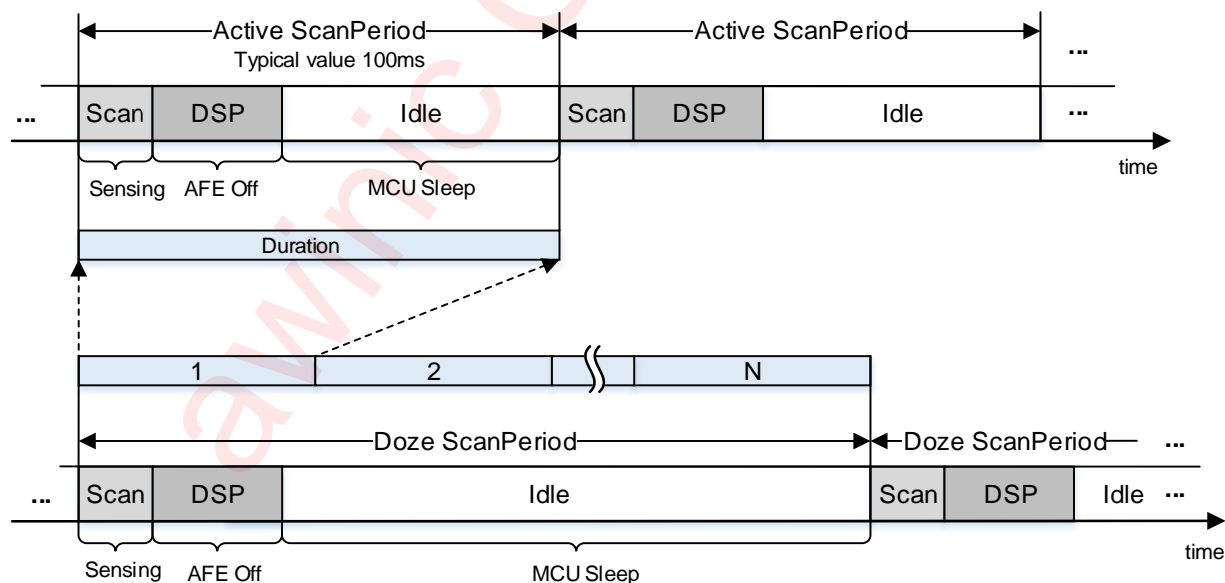
Figure 7 AFE Block Diagram

- ※ MUX selects CSx as capacitance measurement input or shield output.
- ※ If CSx is used as shield electrode, it is excited by shield driver. The driven shield signal is a replica of the sensor signal. Shield electrode around can protect the sensor from noisy environment, and reduce the parasitical capacitance.
- ※ Cap-to-Voltage module integrates a charge amplifier, with a charge-transfer method it converts the capacitance of sensor into voltage signal, as the input of ADC.
- ※ Offset Compensation module is used to eliminate parasitic capacitance( $C_{PARA}$ ) and ensure that the compensated capacitance is within the measurable range of C/V convertor.
- ※ Temp Sensor measures the internal temperature of the chip, and its output is converted by ADC into a digital data. The data can be used to correct the result of capacitance measurement.
- ※ ADC converts voltage signals obtained by Cap-to-Voltage or Temp Sensor into AdcData.

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**DSP DESCRIPTION****Figure 8 Digital signal processing diagram**

- ※ DSP processes the AdcData from the AFE, and finally outputs a series of reliable proximity status.
- ※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio.
- ※ The adaptive temperature compensation module can automatically compensate for environmental drift in real time, especially temperature drift. Thereby it can be ensured that the final proximity status will not be misjudged due to temperature drift.
- ※ The role of the baseline is to further track the slow changes caused by the residual temperature compensation or other slow environmental drift.
- ※ Finally, the Status Decision module output a certain and reliable proximity status based on the Diff data and the proximity threshold etc.

**SCAN PERIOD****Figure 9 Active mode and Doze mode scan period**

Each period is divided into 3 segments. Firstly the AFE scan the sensor channels to get the AdcData. And then AFE is off and DSP starts processing the AdcData. After all data processing are completed, the chip enters idle state both AFE and MCU don't work for low-power consumption.

The figure above also shows the scanning period of active mode and doze mode. The scan period of active

mode can be configured by register SCANCTRL1 (Address: 0x0004) and AFECFG3\_CHx (x=1,...,5). The doze period can be configured independently for each channel by register AFECFG4\_CHx (x=1,...,5). Generally, doze mode consumes much lower power than active mode.

## CLOCK

The chip uses a built-in 4MHz OSC clock.

## RESET

### POWER ON RESET (POR)

Reset operation is triggered during power up. When nRST released, the initialization process starts to perform and it will last for about 20ms. After initialization being completed, pin INTN will be pull down to low, then I<sup>2</sup>C interface can communicate normally.

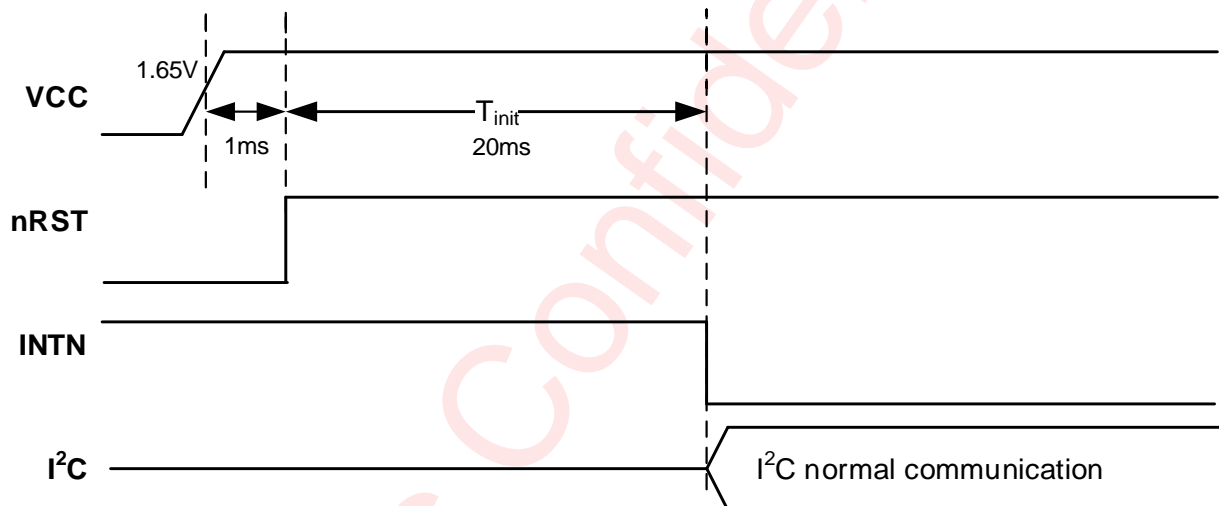


Figure 10 Power On Timing

### BROWN OUT RESET (BOR)

Reset operation is triggered when VCC drop below the threshold of BOR. After the reset operation, all the registers will be reset to the default value. The chip returns to normal operation mode until the power supply rises to a normal value.

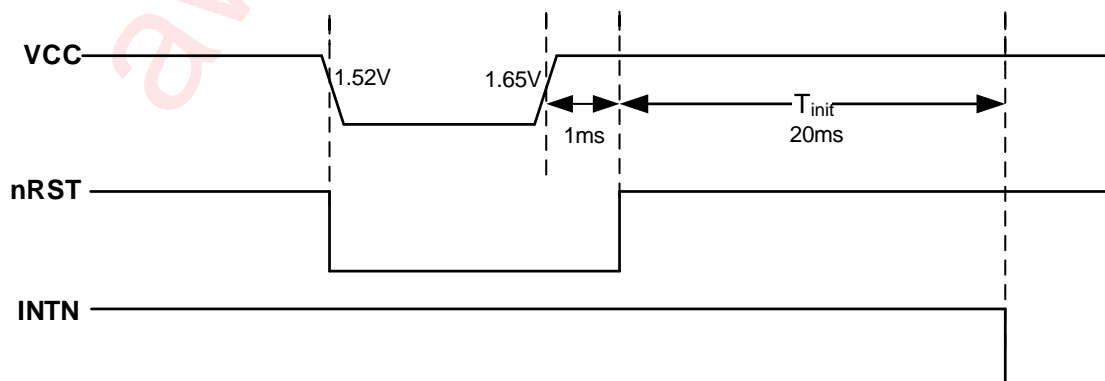


Figure 11 Brown Out Timing

## SOFT RESET

Write "0" to register RESET (Address: 0xFF0C) to reset the whole chip. After the reset, all the registers will be reset to the default value.

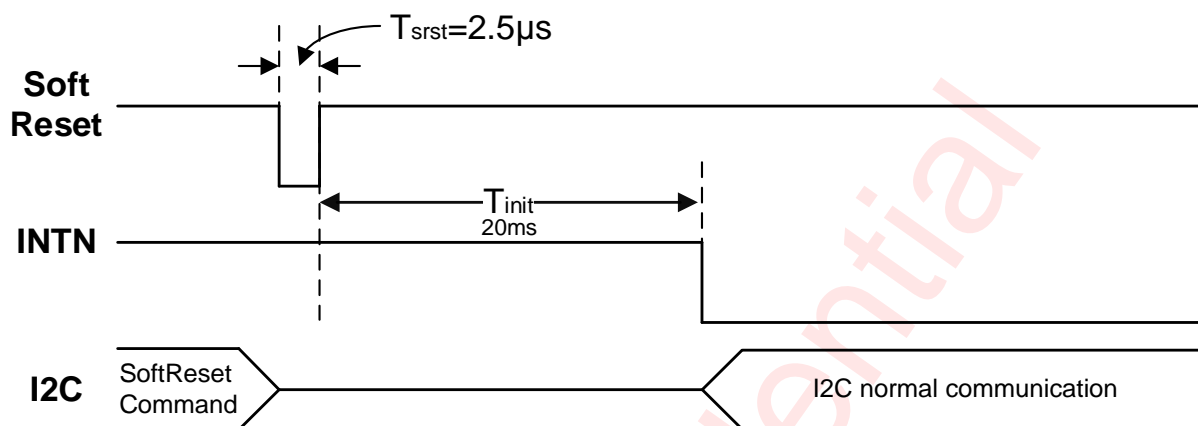


Figure 12 Soft Reset Timing

## INITIALIZATION

After power on, OSC works normally, and MCU starts to execute the initialization program. It performs the following operations.

- Read information from NVM
- Set I<sup>2</sup>C device address according to the status of pin CS2
- Issue an interrupt after initialization and then enters into sleep mode.

## OPERATION MODE

There are three operation modes in the chip: Sleep, Active and Doze.

### SLEEP

The device is in a low power state. OSC is on, AFE is off, and MCU is sleeping, waiting for interrupt to wake up.

### ACTIVE

The device works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When no touch or proximity has been detected for some time, it will automatically switch to Doze mode. In this mode the external HOST can send SLEEP command to switch the device to sleep mode.

### DOZE

The scan period is long, MCU and AFE work intermittently. During the large part of period, most modules are in idle state. So the average power consumption is lower.

Once a proximity is detected in doze mode, it will automatically return to active mode. The external HOST can also send SLEEP command to switch the device to sleep mode.

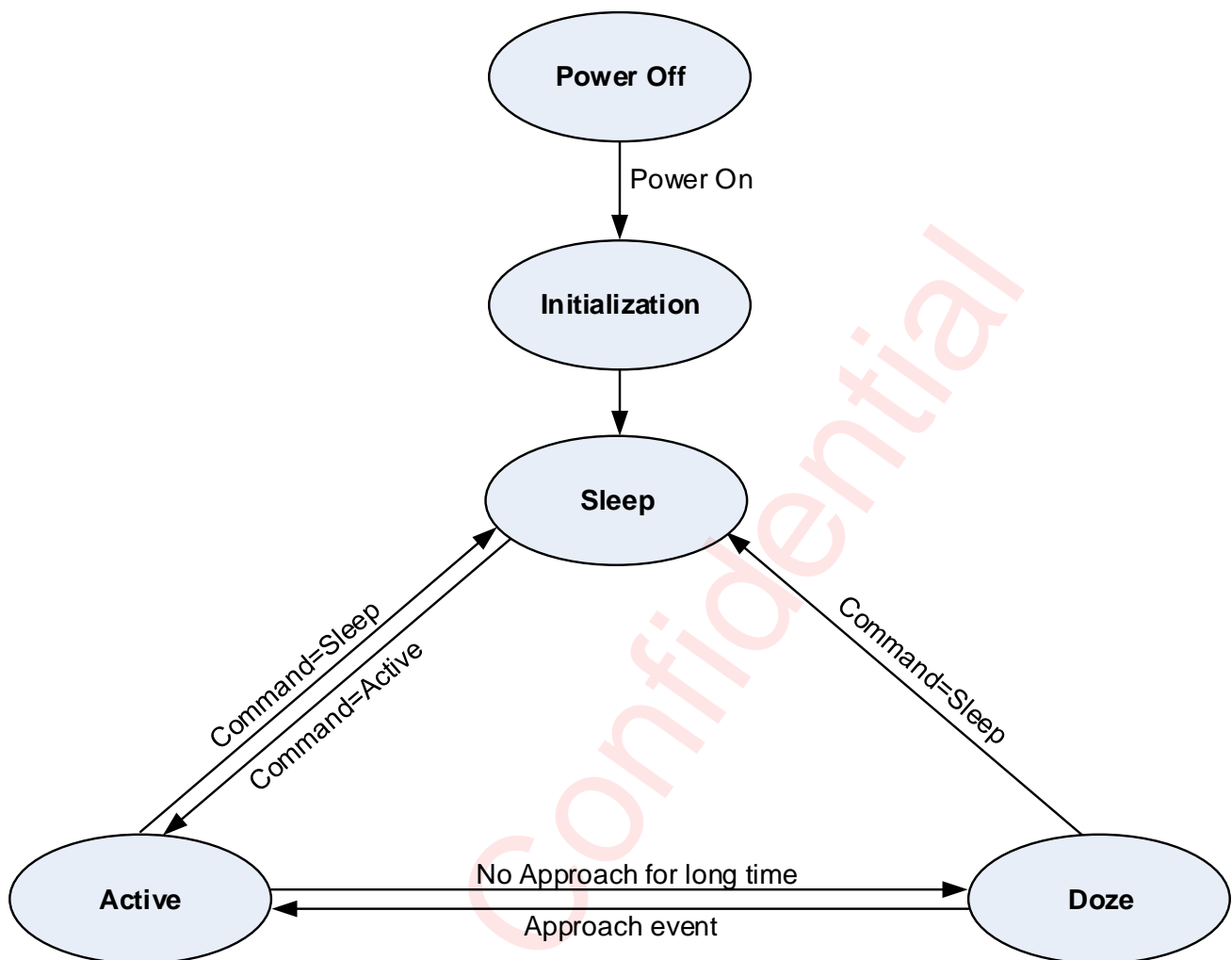


Figure 13 Operation Mode Switching

## INTERRUPT

The chip reports the interrupt signal to the host through the pin INTN. Register IRQSRC (Address: 0xF080) stores interrupt information, including scan interruption, calibration completion interruption, human body approach interruption, etc. Register IRQSRC is cleared after reading. Each specified interrupt triggered or not can be configured by register IRQEN (Address: 0xF084).

## I<sup>2</sup>C INTERFACE

AW93105DNR supports the I<sup>2</sup>C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I<sup>2</sup>C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW93105DNR can support different high level of the I<sup>2</sup>C interface. Additionally, the I<sup>2</sup>C device supports continuous read and write operations. The register address is 16 bits, the register data is 32 bits, and the data transmission is in big-endian mode.

**DEVICE ADDRESS****I<sup>2</sup>C device address configuration**

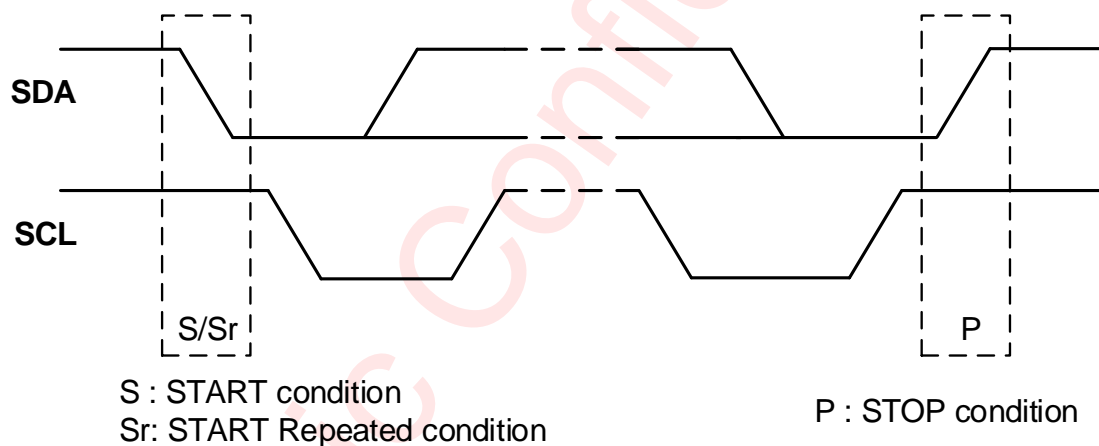
CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

The I<sup>2</sup>C device address (7-bit, followed by the R/W bit (Read=1/Write=0)) of AW93105DNR depends on the pin CS2 status. The default value of I<sup>2</sup>C device address is 0x12, connecting pin CS2 to GND or VCC will change the device address as showed in table above. Note that when pin CS2 is connected to GND or VCC, it can't be used as sensor pad.

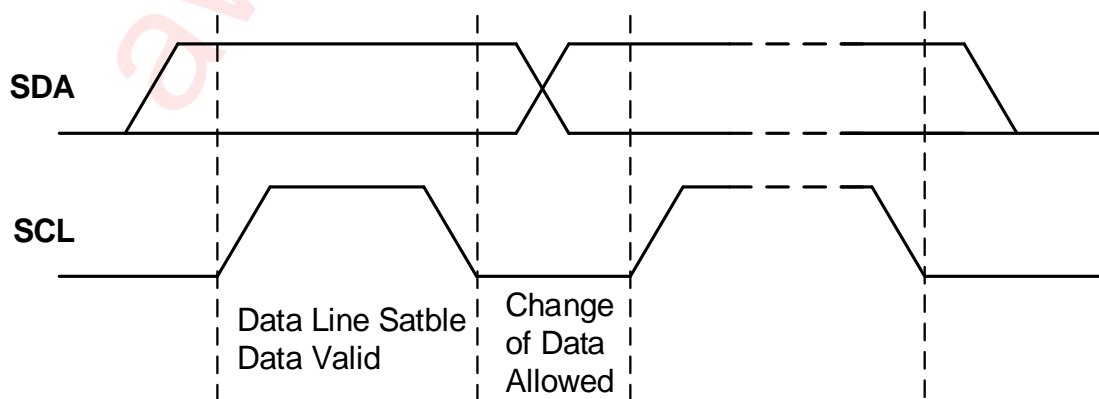
**I<sup>2</sup>C START/STOP**

I<sup>2</sup>C start: SDA changes from high level to low level when SCL is high level.

I<sup>2</sup>C stop: SDA changes from low level to high level when SCL is high level.

**Figure 14 I<sup>2</sup>C Start/Stop Condition Timing****DATA VALIDATION**

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

**Figure 15 Data Validation Diagram**

**ACK (ACKNOWLEDGEMENT)**

ACK means the successful transfer of I<sup>2</sup>C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I<sup>2</sup>C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I<sup>2</sup>C stop.

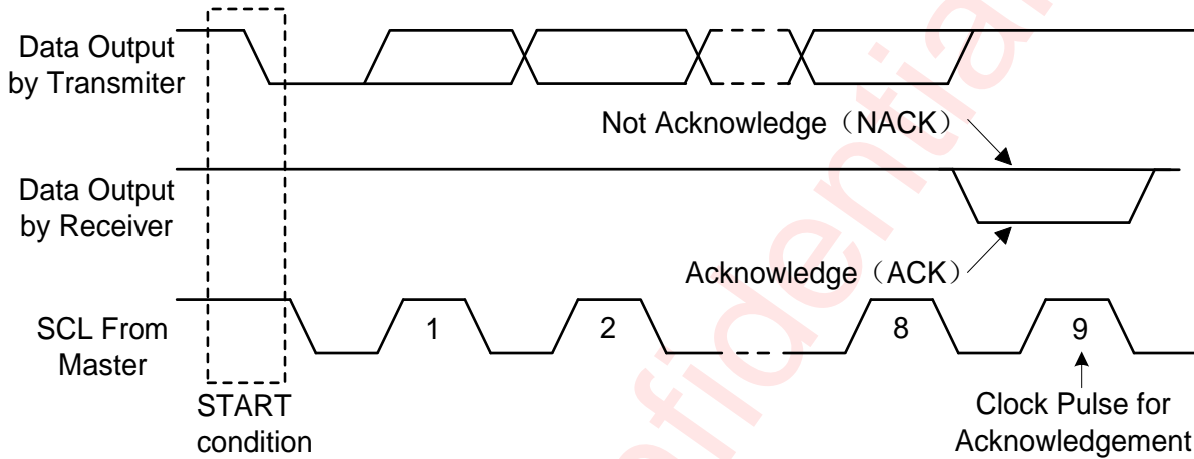


Figure 16 I<sup>2</sup>C ACK Timing

**WRITE CYCLE**

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I<sup>2</sup>C Register address is 16-bit and register data is 32-bit. Note that I<sup>2</sup>C also support 8-bit data transfer. Writing process of I<sup>2</sup>C is showed as below picture.

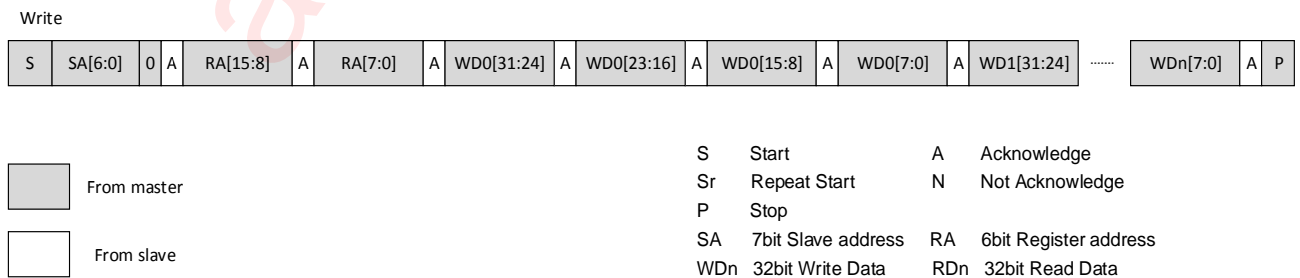
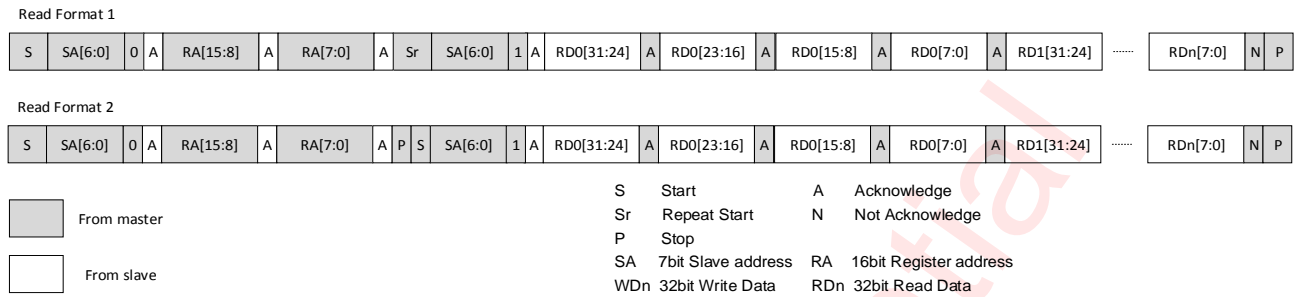


Figure 17 I<sup>2</sup>C Write Byte Cycle



**READ CYCLE**

I<sup>2</sup>C supports read operation data format with repeated start conditions, so there are two formats of I<sup>2</sup>C read operations. Read process of I<sup>2</sup>C is showed as below picture.



**Figure 18 I<sup>2</sup>C Read Byte Cycle**

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## APPLICATION INFORMATION

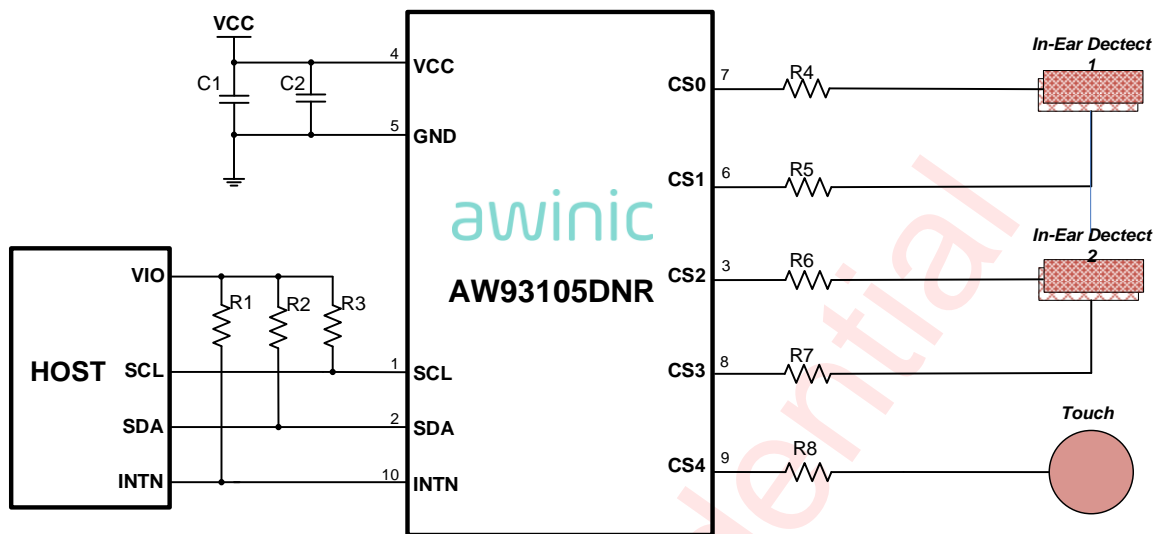


Figure 19 AW93105DNR Typical Application Circuit (in-ear and touch)

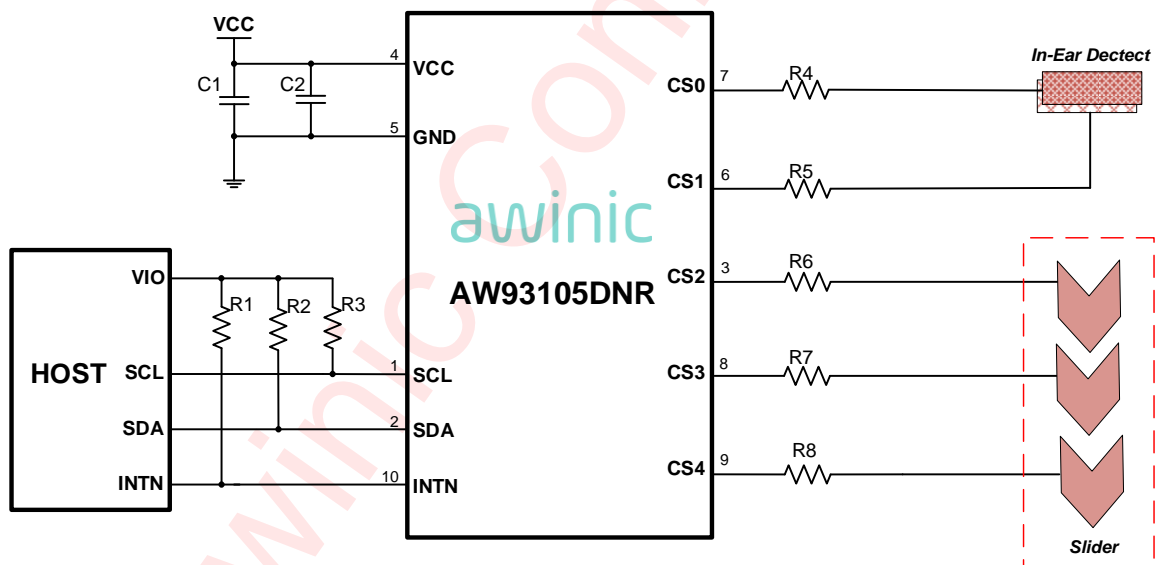


Figure 20 AW93105DNR Typical Application Circuit (in-ear and slide)

## Capacitors Selection

The recommended value of the capacitance C1 is 1 $\mu$ F and C2 is 0.1 $\mu$ F.

## Resistor Selection

The recommended values of the resistor R1~R3, which were applied in pins SCL, SDA and INTN, are 4.7k $\Omega$ . The recommended values of the resistor R4~R8, which were applied in pins CS0~CS4, are 0 $\Omega$ .

## RECOMMENDED COMPONENTS LIST

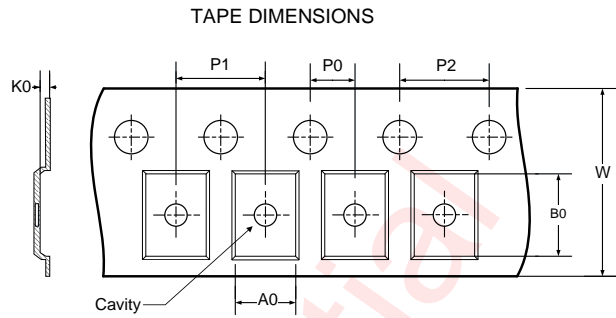
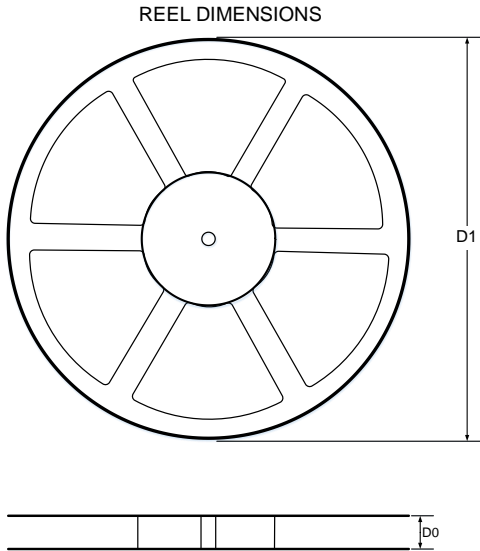
Component	Name	DESCRIPTION	TYP	UNIT
C	C1	-	1	$\mu$ F
	C2	-	0.1	$\mu$ F
R	R1,R2,R3	5% resolution	4.7	k $\Omega$
	R4,R5,R6,R7,R8	5% resolution	0	$\Omega$

## PCB LAYOUT CONSIDERATION

AW93105DNR is a 5-channel capacitive in-ear detection and touch key controller, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

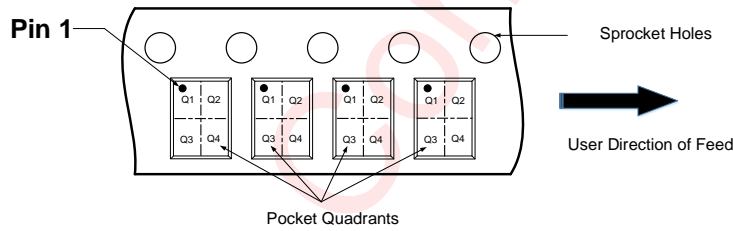
1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC. Avoid connecting peripheral devices and chip pins with two different layers of copper, use the same layer of copper instead.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic and earphone line, because capacitive sensor will disturb audio line.
4. Place reference channel along with sensor channel to get better performance.
5. Use low noise power supply for SAR sensor.

## TAPE AND REEL INFORMATION



- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

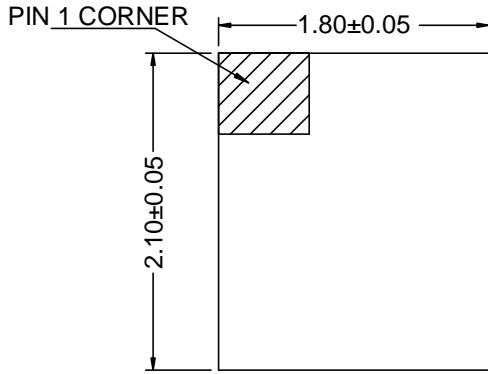


### DIMENSIONS AND PIN1 ORIENTATION

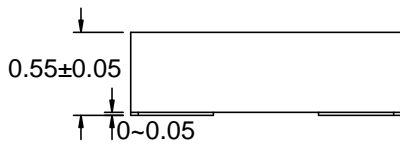
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2	2.3	0.75	2	4	4	8	Q1

All dimensions are nominal

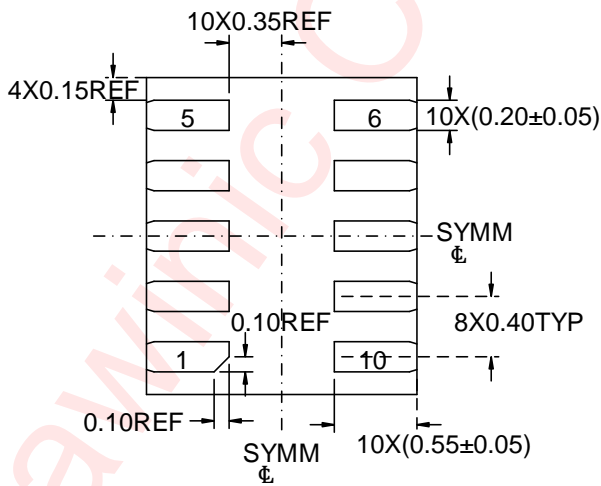
PACKAGE DESCRIPTION



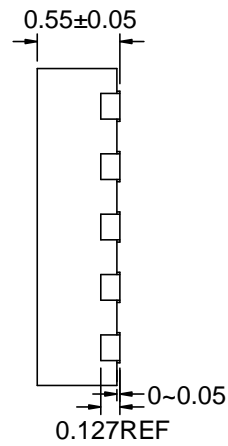
TOP VIEW



SIDE VIEW



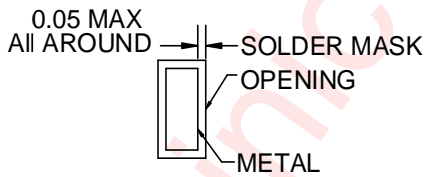
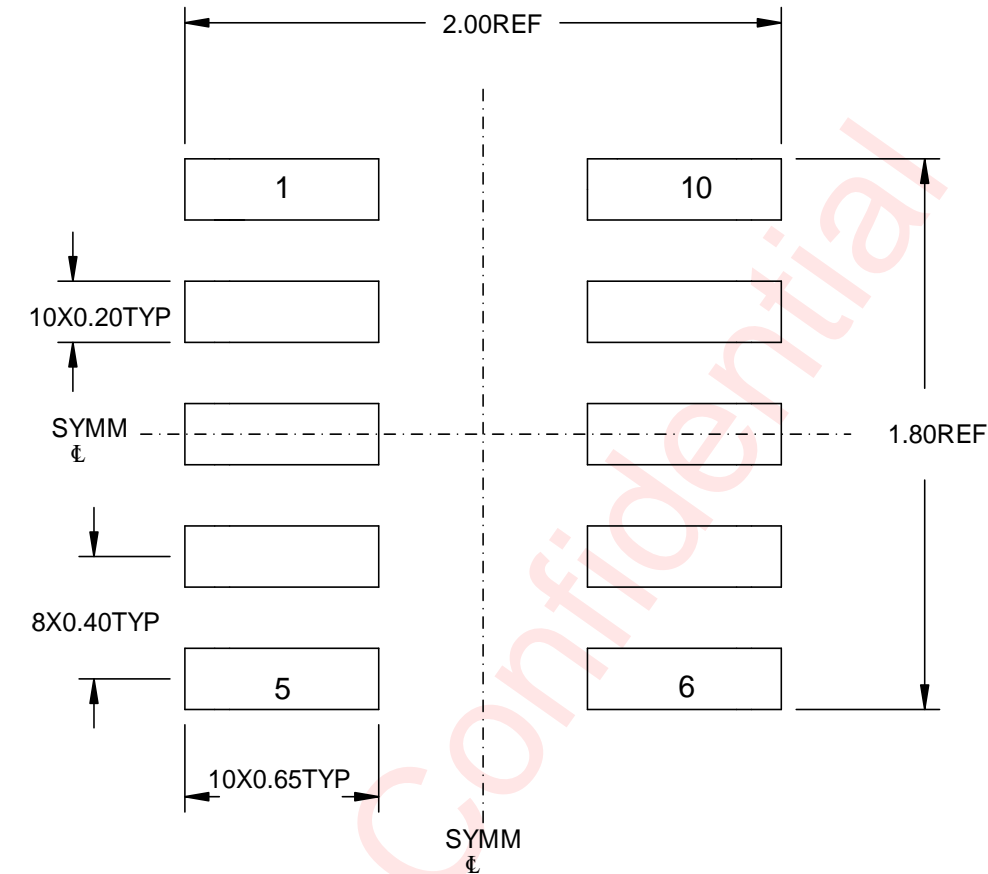
BOTTOM VIEW



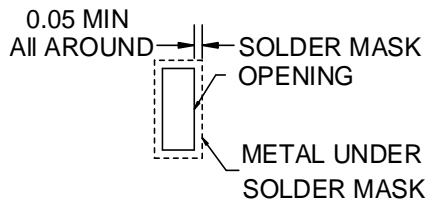
SIDE VIEW

Unit : mm

LAND PATTERN DATA



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit : mm

## Revision History

Version	Date	Change Record.
V1.0	June.2020	Officially released.
V1.1	June.2021	Optimized application block diagram.

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