



## IQS228AS/B DATASHEET

Single channel capacitive proximity  
and touch controller

The ProxSense® **IQS228AS/B** is a single channel self-capacitive sensor with Dynamic Calibration (DYCAL™) to allow for sensor drift during prolonged activation.

### Features

- > 1 Self capacitive channel
- > DYCAL™: Intelligent Hysteresis
- > Proximity and Touch outputs
- > Automatic Tuning
- > Internal Reference Capacitor
- > Minimum external components
- > 1-Wire data streaming
- > I²C Debug option
- > User selectable options (OTP):
- > Ext sync control or Ext filter control
- > I/O Sink or Source selection
- > Time-out for stuck key
- > Proximity and Touch sensitivity selections
- > Low Power modes
- > Low power mode 2.5µA
- > Supply voltage: 1.8V to 3.6V



### Applications

- > Proximity sensors
- > SAR detection for Tablets
- > On-ear detection for mobile phones
- > 3D glasses
- > Personal Media Players
- > White goods and appliances
- > Human Interface Devices
- > Proximity activated backlighting

### Available Options

T <sub>A</sub>	TSOT23-6	WLCSP-8	DFN-6
-20°C to 85°C	IQS228AS	-	-
-40°C to 85°C	IQS228B	IQS228B	IQS228B



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## List of Abbreviations

ATI	Automatic Tuning Implementation
BP	Boost Power Mode
CS	Counts (Number of Charge Transfers)
C <sub>s</sub>	Internal Reference Capacitor
DYCAL™	Dynamic Calibration
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
FTB/EFT	(Electrical) Fast Transient Bursts
GND	Ground
HC	Halt Charge
LP	Low Power Mode
LTA	Long Term Average
ND	Noise Detect
THR	Threshold
TM	Touch Mode



## 1 Overview

### 1.1 Device

The IQS228AS/B is a single channel capacitive proximity and touch device which employs an internal voltage regulator and reference capacitor ( $C_s$ ).

The IQS228AS/B device has a dedicated pin(s) for the connection of a sense electrode(s) ( $C_x$ ) and output pin(s) for proximity and touch events on OUT. The polarity of the output pins can be configured. A 1-wire open drain data streaming protocol OR I<sup>2</sup>C interface is implemented for debugging purposes.

Special device configuration can be done by setting one time programmable (OTP) options.

The device automatically tracks slow varying environmental changes via various signal processing algorithms and has an Automatic Tuning Implementation (ATI) algorithm to calibrate the device to the sense electrode.

DYCAL™ (Dynamic Calibration) is a special form of hysteresis that can track slow varying environmental change even while the sensor is in a touch state. This is ideal for portable applications.

The *charge transfer* method of capacitive sensing is employed on the IQS228AS/B. (The

charge transfer principle is thoroughly described in the application note: “AZD004 - Azoteq Capacitive Sensing”.)

### 1.2 Operation

The device has been designed to be used in applications where proximity is required and touch conditions can prevail for an extended period of time which may result in uncompensated drift in conventional capacitive sensors.

A low threshold is used to detect the proximity of an object, with a higher threshold for touch detection.

Dynamic Calibration is performed when a TOUCH condition is detected for longer than  $t_{DYCAL}$ . The hysteresis algorithm will now check for the release condition of the touch, while still tracking environmental changes

### 1.3 Applicability

All specifications, except where specifically mentioned otherwise, provided by this datasheet are applicable to the following ranges:

- > Temperature:
  - IQS228AS: -20°C to +85°C
  - IQS228B: -40°C to +85°C
- > Supply voltage ( $V_{DDHI}$ ): 1.8V to 3.6V



## 2 Packaging and Pin-Out

The IQS228AS/B is available in a TSOT23-6 package. the IQS228B is available in TSOT23-6, DFN-6 or WLCSP-8 package

### 2.1 IQS228AS/B

#### 2.1.1 Pin-out TSOT23-6

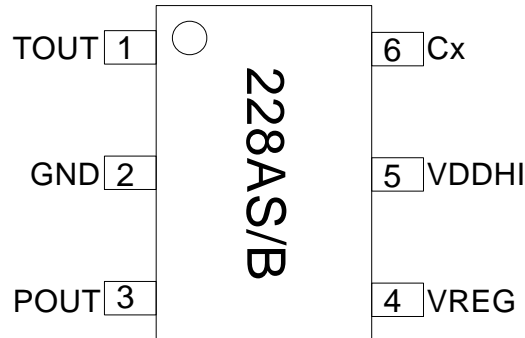


Figure 2.1: Pin-out of IQS228AS/B in the TSOT23-6 package.

Table 2.1: Pin-out description

IQS228AS/B in TSOT23-6			
Pin	Name	Type	Function
1	OUT	Digital Out	Output
2	GND	Ground	GND Reference
3	CTRL / ND	Digital Input/Output	Control input or proximity output / ND pin
4	VREG	Analogue Output	Internal Regulator Pin (Connect 1µF bypass capacitor)
5	VDDHI	Supply Input	Supply Voltage Input
6	CX	Analogue	Sense Electrode



## 2.1.2 Pin-out WLCSP-8

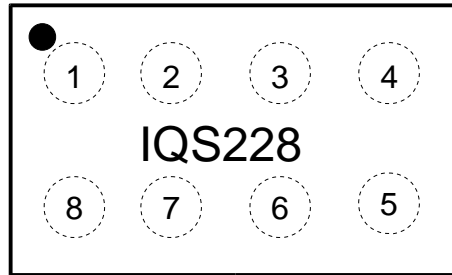


Figure 2.2 IQS228B 8-pin WLCSP

Table 2.2 8 -pin WLCSP Pin-out Description

IQS228B 8-pin WLCSP			
Pin	Name	Type	Function
1	Cx	Sense electrode	Connect to conductive area intended for sensor
2	OUT	Digital Out	Output
3	VREG	Regulator output	Requires external capacitor
4	VSS	Signal GND	
5	INPUT	Digital Input	Floating input during runtime. Recommended: Connect to POUT
6	POUT / ND	Digital Input/Output	Control input or proximity output / ND pin
7	VDDHI	Supply Input	Supply Voltage Input
8	PGM	Configuration pin	Connection for OTP programming. Floating input during runtime. Recommended: Connect to OUT pin. Programming can still be performed using this pin, provided a diode is used. (See AZD026 – Configuration Tools Overview)

### 2.1.3 Pin-out DFN-6

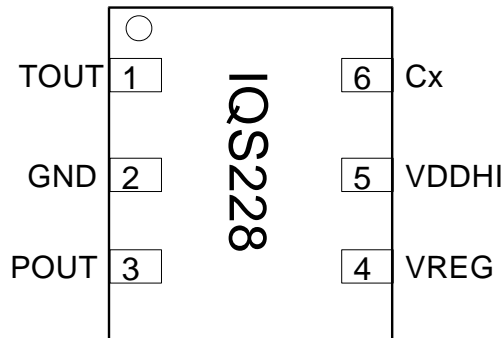


Figure 2.3: Pin-out of IQS228B in DFN-6 package.

Table 2.3: Pin-out description.

IQS228B 6-pin DFN			
Pin	Name	Type	Function
1	OUT	Digital Out	Output
2	GND	Ground	GND Reference
3	CTRL / ND	Digital Input/Output	Control input or proximity output / ND pin
4	VREG	Analogue Output	Internal Regulator Pin (Connect 1µF bypass capacitor)
5	VDDHI	Supply Input	Supply Voltage Input
6	CX	Analogue	Sense Electrode





## 2.2 Schematic

### 2.2.1 TSOT23-6

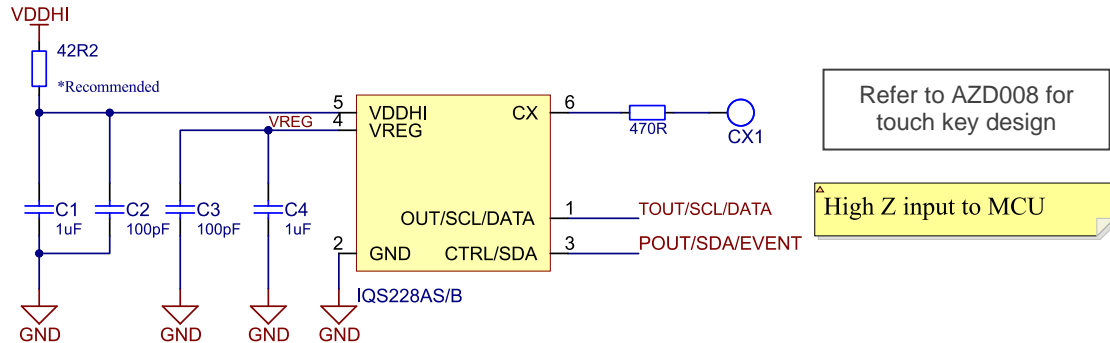


Figure 2.4: Typical application reference schematic of IQS228AS/B. C2 & C3 are optional for added RF immunity.

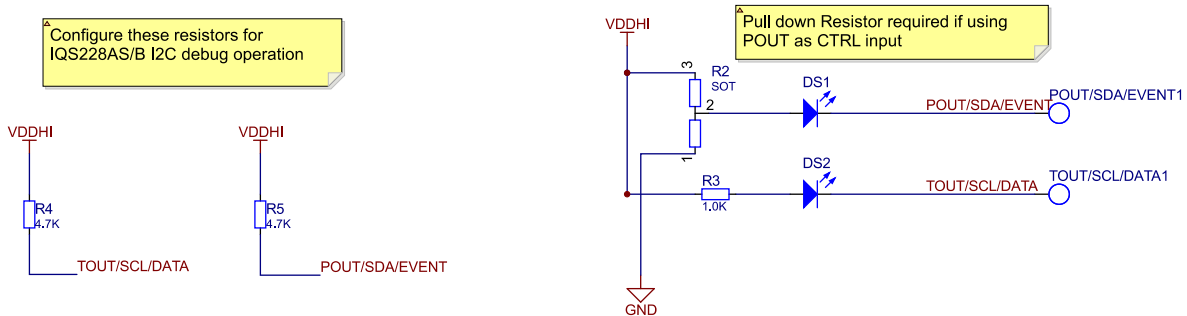


Figure 2.5: IQS228AS/B output pin configuration for I2C debug operation, or driving LEDs (active high or low option available).

Where a system level ESD strike is found to cause the IC to go into ESD induced latch-up, it is suggested that the supply current to the IQS228 IC is limited by means of a series resistor that could limit the maximum supply current to the IC to <80mA.



### 2.2.2 WLCSP-8

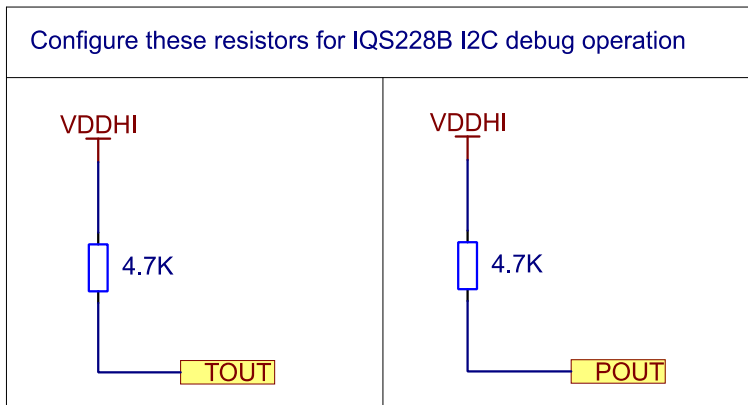
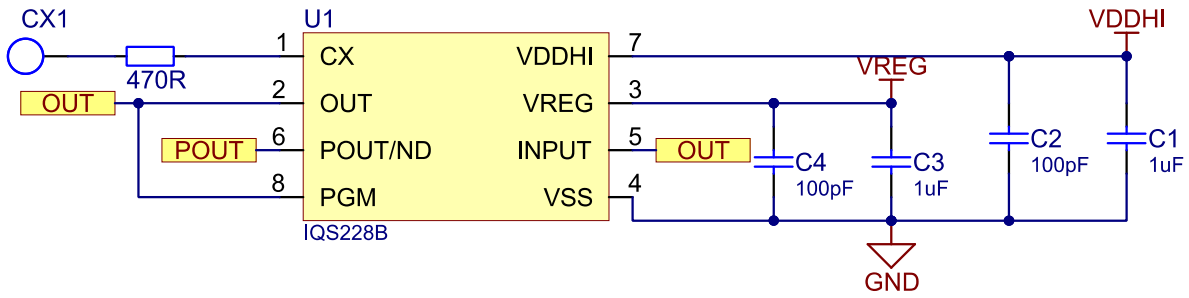


Figure 2.6 Typical application reference schematic of IQS228B WLCSP-8 Package. C2 & C3 are optional for added RF immunity.



### 2.2.3 DFN-6

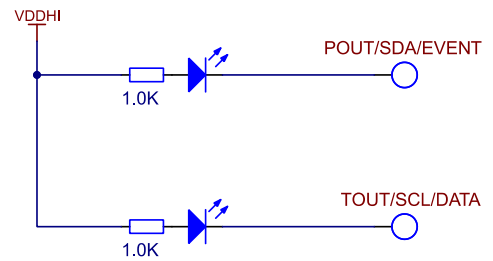
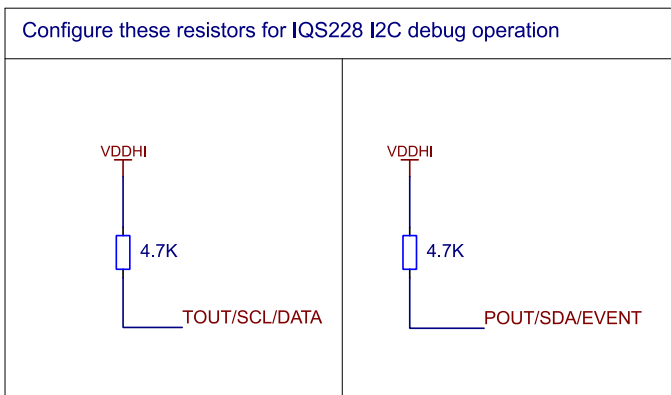
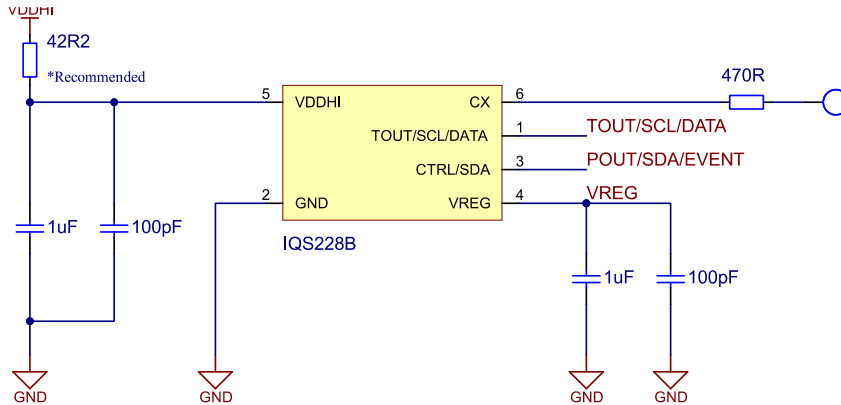


Figure 2.7 Typical application reference schematic of IQS228B DFN-6 Package. C2 & C3 are optional for added RF immunity.



### 3 User Configurable Options

This section lists the user configurable settings.

The device is fully functional in its default state, but some applications may require alternative configuration settings. These settings are enabled by configuring One Time Programmable (OTP) user options.

Configuration can be done on packaged devices or in-circuit. In-circuit configuration may be limited by values of external components chosen.

Popular configurations are available ex-stock – please check with the local distributor for availability. Azoteq can supply pre-configured devices for large quantities.

### 3.1 Configuring Devices

Azoteq offers a Configuration Tool (CT210/20) and accompanying software (USBProg.exe) that can be used to program the OTP user options for prototyping purposes. More details regarding the configuration of the device with the USBProg program is explained by application note: “AZD007 – USBProg Overview” which can be found on the Azoteq website.

Alternative programming solutions for the IQS228AS/B also exist. For further enquiries regarding this, please contact Azoteq at ProxSenseSupport@azoteq.com or the local distributor

#### 3.1.1 IQS228AS/B User Selectable Options

Table 3.1: IQS228AS/B Bank 0 User Selectable Options (0xC4H)

Bit	7	6	5	4	3	2	1	0
Name	IN_EN	REL <sub>THR</sub>	LOGIC	T <sub>THR2</sub>	T <sub>THR1</sub>	T <sub>THR0</sub>	P <sub>THR1</sub>	P <sub>THR0</sub>

**bit 7**      **IN\_EN:** Input Enable [Section 10.2](#)  
 0 = Output (Proximity)  
 1 = Input

**bit 6**      **REL<sub>THR</sub>:** Release Threshold [Section 10.1](#)  
 0 = 75%  
 1 = 87%

**bit 5**      **LOGIC:** Output logic select (Only when STREAMING mode is disabled) [Section 7.2](#)  
 0 = Software Open Drain Active Low  
 1 = Active High

**bit 4-2**    **T<sub>THR</sub>:** Touch Threshold Selections [Section 7.5](#)  
 000 = 72/256  
 001 = 4/256  
 010 = 8/256  
 011 = 24/256  
 100 = 48/256  
 101 = 96/256  
 110 = 128/256  
 111 = 160/256

**bit 1-0**    **P<sub>THR</sub>:** Proximity Threshold Selections [Section 7.4](#)  
 00 = 4  
 01 = 2  
 10 = 8  
 11 = 16



Table 3.2: User Selectable Configuration Options: Bank 1 – Full ATI (0xC5H)

t <sub>HALT1</sub>	t <sub>HALT0</sub>	~	~	TURBO	BASE <sub>2</sub>	BASE <sub>1</sub>	BASE <sub>0</sub>
bit 7				bit 0			
<b>Bank1: bit 7-6</b>	t <sub>HALT</sub> : Halt times 00 = 20 seconds 01 = 40 seconds 10 = Never 11 = 3 seconds			<a href="#">Section 7.11</a>			
<b>Bank1: bit 5-4</b>	<b>Not used</b>						
<b>Bank1: bit 3</b>	<b>TURBO</b> : DYCAL TURBO 0 = Disabled 1 = Enabled			<a href="#">Section 7.10</a>			
<b>Bank1: bit 2-0</b>	<b>BASE</b> : Base Value 000 = 200 001 = 50 010 = 75 011 = 100 100 = 150 101 = 250 110 = 300 111 = 500			<a href="#">Section 9.3</a>			

Table 3.3: User Selectable Configuration Options: Bank 1 – Partial ATI

t <sub>HALT1</sub>	t <sub>HALT0</sub>	MULT <sub>SENSE1</sub>	MULT <sub>SENSE0</sub>	MULT <sub>COMP3</sub>	MULT <sub>COMP2</sub>	MULT <sub>COMP1</sub>	MULT <sub>COMP0</sub>
bit 7				bit 0			
<b>Bank1:7-6</b>	t <sub>HALT</sub> : Halt times 00 = 20 seconds 01 = 40 seconds 10 = Never 11 = 3 seconds			<a href="#">Section 7.11</a>			
<b>Bank1: bit 5-4</b>	<b>MULT</b> : Multiplier for Sensitivity 00 01 10 11			<a href="#">Section 7.6</a>			
<b>Bank1: bit 3-0</b>	<b>MULT</b> : Multiplier for Compensation 0000 to 1111			<a href="#">Section 7.6</a>			



Table 3.4: User Selectable Configuration Options: Bank 2 (0xC6H)

STREAM	TRANS	COMMS	ND	Target	ATI	LP <sub>1</sub>	LP <sub>0</sub>
bit 7							bit 0
<b>Bank2: bit 7</b>	<b>STREAM:</b> Steaming Method 0 = 1-wire 1 = 2-wire (I <sup>2</sup> C)					<a href="#">Section 8.2</a>	
<b>Bank2: bit 6</b>	<b>TRANS:</b> Charge Transfer Frequency 0 = 512kHz 1 = 250kHz					<a href="#">Section 7.7</a>	
<b>Bank2: bit 5</b>	<b>COMMS:</b> Streaming 0 = Disabled 1 = Enabled					<a href="#">Section 8</a>	
<b>Bank2: bit 4</b>	<b>ND:</b> Noise Detect 0 = Disabled 1 = Enabled (1-wire comms only)					<a href="#">Section 7.3</a>	
<b>Bank2: bit 3</b>	<b>Target:</b> ATI target counts 0 = 1200 1 = 1024					<a href="#">Section 7.8</a>	
<b>Bank2: bit 2</b>	<b>ATI:</b> ATI Selection 0 = Full 1 = Partial					<a href="#">Section 7.9</a>	
<b>Bank2: bit 1-0</b>	<b>LP:</b> Power mode Selection 00 = BP, 9ms (64ms if zoom is disabled) 01 = NP, 128ms 10 = LP1, 256ms 11 = LP2, 512ms					<a href="#">Section 7.12</a>	

Table 3.5: User Selectable Configuration Options: Bank 3 (0xC7H)

~	~	~	~	Zoom	~	~	CTRL
bit 7							bit 0
<b>Bank3: bit 7-4</b> <b>System Use</b>							
<b>Bank3: bit 3</b>	<b>Zoom:</b> Zoom Disable 0 = Zoom Enabled 1 = Zoom Disabled					<a href="#">Section 7.13</a>	
<b>Bank3: bit 2-1</b> <b>System Use</b>							
<b>Bank3: bit 0</b>	<b>CTRL:</b> Control Input 0 = Halt Charge 1 = Filter Halt					<a href="#">Section 7.1</a>	



## 4 Measuring Capacitance Using the *Charge Transfer* Method

The *charge transfer* method of capacitive sensing is employed on the IQS228AS/B.

A charge cycle is used to take a measurement of the capacitance of the sense electrode (connected to Cx) relative to ground. It consists of a series of pulses charging Cx and discharging Cx to the reference capacitor, at the charge transfer frequency ( $F_{CX}$  - refer to Section 11). The number of the pulses required to reach a trip voltage on the reference capacitor is referred to as the **Count** value (CS) which is the instantaneous capacitive measurement. The Counts (CS) are used to determine if either a physical contact or proximity event occurred, based on the change in CS detected. The typical values of CS, without a touch or proximity condition range between 1344 and 1865 counts, although higher and lower counts can be used based on the application requirements. With CS larger than +/-1865 the gain of the system may become too high causing unsteady operation.

The IQS228AS/B schedules a charge cycle every  $t_{SAMPLE}$  seconds to ensure regular samples for processing of results. The duration of the charge cycle is defined as  $t_{CHARGE}$  and varies according to the counts required to reach the trip voltage. Following the charge cycle other activities such as data streaming is completed (if in streaming mode), before the next charge cycle is initiated.

**Please note: Attaching a probe to the Cx pin will increase the capacitance of the sense plate and therefore  $C_s$ . This may have an immediate influence on the Counts value (decrease  $t_{CHARGE}$ ) and cause a proximity or touch event. After  $t_{HALT}$  seconds the system will adjust to accommodate for this change. If the total load on Cx, with the probe attached is still lower than the maximum Cx load the system will continue to function normally after  $t_{HALT}$  seconds with the probe attached.**

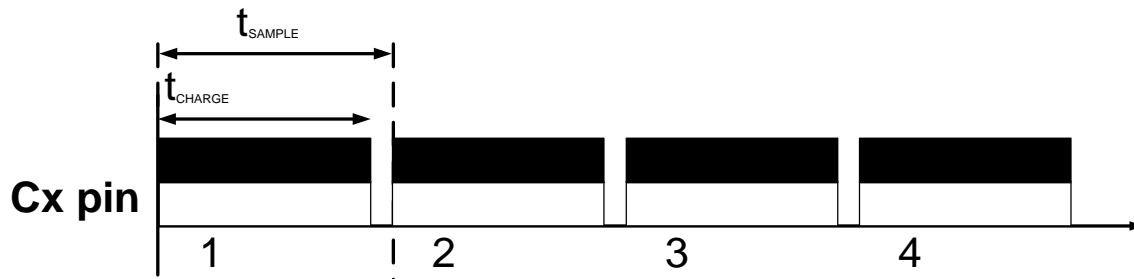


Figure 4.1: Charge cycles as can be seen on CX.



## 5 DYCAL™ Operation

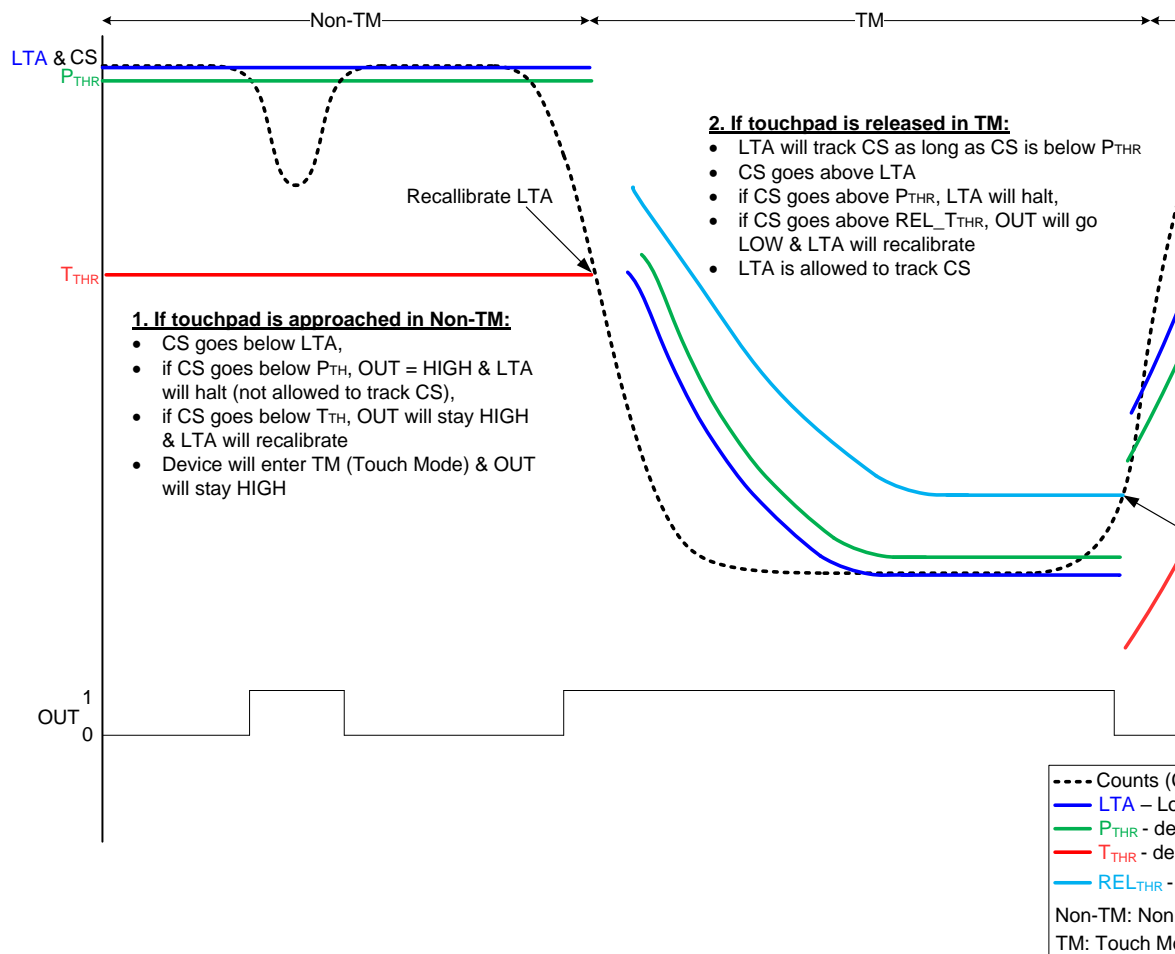


Figure 5.1: DYCAL Operation (Self Capacitive Sensing)





## 6 Operating Principle

Figure 5.1 is a visual representation of the DYCAL functionality. The OUT pin is used to indicate the status of a DYCAL event (both proximity and a touch event). The DYCAL functionality is summarised below.

### Non-Touch Mode

The OUT pin is activated on the successful detection of a proximity event and will remain activated for the duration of the proximity event, permitting that this event is no longer than the filter halt timings. The LTA will be halted in this time.

As soon as a touch condition is detected (Count values, or CS, fall below  $T_{THR}$ ), the controller will dynamically re-calibrate its LTA to the halted  $LTA - T_{THR}$ . The IC is now in Touch Mode.

### Touch Mode

After the re-calibration of the LTA, it will follow the Counts (CS) and be allowed to track slow varying environmental changes. If the Counts (CS) were to exceed the LTA by the release threshold ( $REL_{T_{THR}}$ ) the touch detection will stop and the OUT pin will return to its original state.

## 7 Configurable Settings

This section describes the user configurable options of the IQS228AS/B in more detail.

User programmable options are selected by configuring the OTP selections. Please refer to

Section 2.2.2 for an overview of the configurable settings.

### 7.1 CTRL: External Control

The user has the option to control some parameters of the IQS228AS/B from an external source. The IC can be used in default mode (CTRL unconnected) or the user can use the CTRL pin to select whether the master should halt the charge transfers (i.e. stop operation) or to halt LTA filter tracking on the IQS228AS/B.

#### 7.1.1 Charge Halt

If CTRL is sampled high for longer than  $T_{EXT\_HALT}$ , the charge conversion cycle will be halted, once the current conversion has been completed. The device will remain in this standby mode until the CTRL line is sampled low again. An automatic reseed is performed directly after CTRL is released to compensate for any environmental changes which might have occurred during the standby mode.

#### 7.1.2 Halt LTA Filter

When configured in this mode, CTRL can be used to control the LTA halt times when sampled high. The CTRL pin has precedence over the configurations bits selected for the halt timings.

If CTRL is sampled high for longer than  $T_{EXT\_HALT}$ , the filter will be halted until this pin is sampled low.

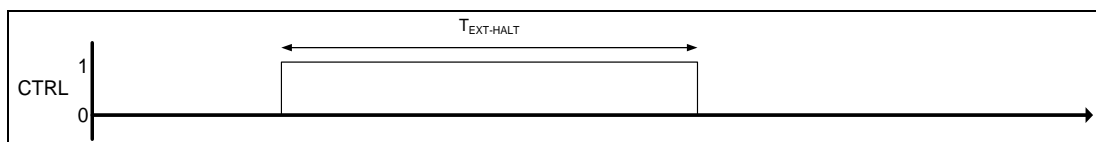


Figure 7.1: Master Output signal on CTRL pin to Halt Operation or Filter Halt

#### 7.1.3 Pulse on CTRL:

The pulse on the CTRL pin needs to adhere to the following timing constraints:

$$25ms < T_{PULSE} < 35ms$$

##### 7.1.3.1 IQS228AS/B: Reseed

A reseed condition can be initiated by generating a pulse on the CTRL pin. The LTA

will be reset to the count, forcing the OUT pin to its original state.

If the count value is outside its allowable limits, the device will force an ATI event to reset the system sensitivity. (Please refer to section 8.1 for more detail).



### 7.1.3.2 IQS228AS/B: re-ATI

A re-ATI condition can be initiated by generating a pulse on the CTRL pin. This function can be issued at any time.

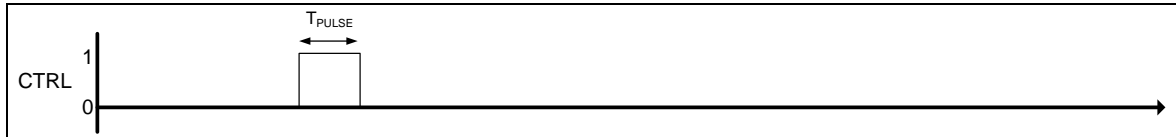


Figure 7.2: Master Output signal on CTRL to force a Reseed Condition.

## 7.2 LOGIC

The logic used by the device can be selected as active HIGH or active LOW. The output pins OUT and CTRL will function based on this selection. When configured as Active High, the outputs will remain high after POR until ATI has completed. The ATI time will vary according to the capacitive load on the sensor, but typically does not exceed 500ms.

**Configuration:** [Bank0 bit5: Logic Output Selection](#)

Bit	Selection
0	Software Open Drain Active Low
1	Active High

A software open drain output is implemented for the OUT pin when configured in active low mode. The voltage on the pull-up resistor is limited to the IQS228AS/B supply voltage. A 4k7-10kΩ resistor between OUT and VDDHI is recommended.

## 7.3 RF Noise on IQS228AS/B

### 7.3.1 ND: RF Noise Detection

The IQS228AS/B has RF Noise Detect (ND) functionality. If ND function is enabled, the IQS228AS/B is able to detect RF Noise on the TOUT/ND pin. Further details on the working of this can be found in the Application Notes: AZD015 and AZD015b.

Note: ND input enable is a legacy input and is not recommended for use in new designs. The input has been desensitized by default and is not tested to trigger at a specific RF input power level

### 7.3.2 IQS228AS/B RF Noise Immunity

The IQS228AS/B has advanced immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices. Design guidelines should however be followed to ensure the best noise immunity. The design of capacitive sensing applications can encompass a large range of situations but as a summary the following should be noted to improve a design:

- > A ground plane should be placed under the IC, except under the Cx line.
- > All the tracks on the PCB must be kept as short as possible.
- > The capacitor between VDDHI and GND as well as between VREG and GND, must be placed as close as possible to the IC.
- > A 100 pF capacitor should be placed in parallel with the 1uF capacitor between VDDHI and VSS. Another 100 pF capacitor can be placed in parallel with the 1uF capacitor between VREG and GND.
- > If the device is too sensitive for a specific order option, a parasitic capacitor (typically 20pF) can be added between the Cx line and ground.
- > Proper sense electrode and button design principles must be followed.
- > Unintentional coupling of sense electrode to ground and other circuitry must be limited by increasing the distance to these sources.

In some instances a ground plane some distance from the device and sense electrode may provide significant shielding from undesired interference.



When the capacitance between the sense electrode and ground becomes too large the sensitivity of the device may be influenced.

### 7.4 Proximity Threshold

The IQS228AS/B has 4 proximity threshold settings indicated in counts. The proximity threshold is selected by the designer to obtain the desired sensitivity and noise immunity. A proximity event is triggered if the Counts (CS) diverges more than the selected threshold from the LTA for 6 consecutive cycles.

**Configuration: Bank0 bit 1-0**  
**P<sub>THR1</sub>:P<sub>THR0</sub>:Proximity Thresholds**

Bit	Selection
00	4
01	2 (Most sensitive)
10	8
11	16 (Least sensitive)

### 7.5 Touch Threshold

The IQS228AS/B has 8 touch threshold settings indicated in counts. The touch threshold is selected by the designer to obtain the desired touch sensitivity. A touch event is triggered if the Counts (CS) diverges more than the selected threshold from the LTA for 2 consecutive cycles.

In the NO-TOUCH state the Counts (CS) must diverge more than the touch threshold value below the LTA. Operating in the TOUCH STATE, the CS must diverge more than REL\_T<sub>THR</sub> of the touch threshold value above the LTA.

The following equation is used to determine if a touch or release event occurred.

NO TOUCH STATE:  $LTA - CS \leq T_{THR}$   
 TOUCH STATE:  $CS - LTA \geq REL\_T_{THR}$

**Configuration: Bank0 bit 4-2** T<sub>THR2</sub>:T<sub>THR0</sub>  
**Touch Thresholds**

T <sub>THR2</sub> :T <sub>THR0</sub> : Touch Thresholds	
Bit	Selection
000	72/256
001	4/256 (Most sensitive)
010	8/256
011	24/256
100	48/256
101	96/256
110	128/256
111	160/256 (Least sensitive)

### 7.6 Multipliers

When using partial ATI, the base value is set up using the multipliers. Compensation will still be added automatically to reach the target.

### 7.7 Charge Transfer

The charge transfer frequency of the IQS228AS/B is adjustable. Changing the transfer frequency will affect sensitivity and response rate. Two options are available:

**Configuration: Bank2 bit6**

TRANS: Charge Transfer Frequency	
Bit	Selection
0	512kHz
1	250kHz

### 7.8 Target Counts

The target of the ATI algorithm can be adjusted between 1200 (default) and 1024 counts. When less sensitivity is required, the lower counts will also increase response rate:

**Configuration: Bank2 bit3**

Target: ATI target counts	
Bit	Selection
0	1200
1	1024

### 7.9 Enable Partial ATI

In some applications the startup time of the IQS228AS/B may be required to be decreased. This is possible by enabling partial ATI, if the multipliers required can be determined, and the compensation alone is adequate to account for environmental change.



**Configuration: [Bank2 bit2](#)**

<b>ATI: Partial ATI</b>	
<b>Bit</b>	<b>Selection</b>
0	Disabled
1	Enabled

### 7.10 DYCAL TURBO

In some applications, it may be required to improve the entry and exit speed of Touch Mode by removing the entry reseed delay, as well as turning off the AC-filters. This can be done by enabling the DYCAL TURBO mode.

**Configuration: [Bank1 bit3](#)**

<b>TURBO: DYCAL TURBO</b>	
<b>Bit</b>	<b>Selection</b>
0	Disabled
1	Enabled

Note that if Dycal Turbo is enabled, the LTA will halt at the reseed point for  $t_{HALT}$  if Touch Mode is entered before a proximity event is registered.

### 7.11 Filter Halt

The LTA filter only executes while no proximity events are detected to ensure compensation only for environmental changes. Once a touch event is detected the filter will resume operation and will no longer be halted. The halt timing configuration settings determine how long the filter is halted.

**Configuration: [Bank1 bit 7-6](#)**

<b>Bit</b>	<b>Selection</b>
00	20 seconds
01	40 seconds
10	Never
11	3 seconds

The presence of a proximity condition for a time exceeding the halt time will be deemed as a fault state which would trigger a reseed event where after the output state on the OUT pin will be reset to its original condition.

### 7.12 Low Power Modes

There exist 4 LP modes. The LP modes will decrease the sampling frequency of CS which will reduce the [power consumption](#) of the device. However, this will also increase the response time of the device.

**Configuration: [Bank2 bit 1-0](#)**

<b>Bit</b>	<b>Selection</b>
00	9.1ms (BP) 64ms if Zoom disabled
01	128ms (Normal Power Mode)
10	256ms (Low Power Mode 1)
11	512ms (Low Power Mode 2)

### 7.13 Zoom

The IQS228AS/B has the option to disable the zoom function. This means that the sample time will stay fixed, even when proximity and touch events are made. When this is activated, boost power mode will change from a 9ms sample time, to 64ms.

**Configuration: [Bank3 bit3](#)**

<b>Zoom: Zoom Disable</b>	
<b>Bit</b>	<b>Selection</b>
0	Enabled
1	Disabled



## 8 Streaming Mode

For a more complete description of the data streaming protocol, please refer to Application Note AZD017 on the Azoteq website.

The IQS228AS/B has the capability to stream data to a MCU. This provides the designer the ability to obtain the parameters and sensor data within the device in order to aid design into applications. Data streaming is performed as a 1-wire data protocol on the OUT pin OR I<sup>2</sup>C interface. The output function of this pin is therefore lost when the device is configured in streaming mode. Data Streaming can be enabled as indicated below:

### Configuration: **Bank2 bit5: Streaming Mode**

Bit	Selection
0	Disabled
1	Enabled

Figure 8.1 illustrates the communication protocol for initialising and sending data with the 1 wire communication protocol.

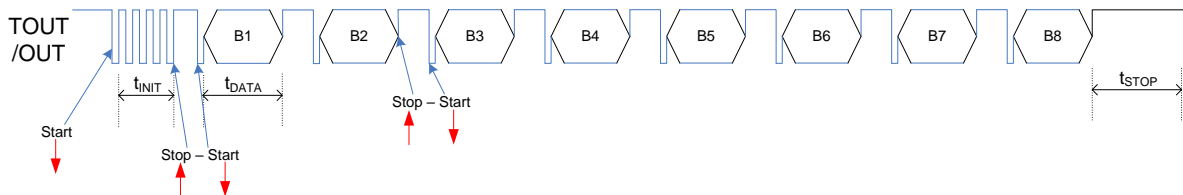


Figure 8.1: Debug: 1-wire streaming Debug Mode.

The following table defines the bit definitions for the IQS228AS/B devices during Streaming Mode.

1. Communications initiated by a START bit. Bit defined as a low condition for  $T_{START}$ .
2. Following the START bit, is a synchronisation byte ( $T_{INIT} = 0xAA$ ). This byte is used by the MCU for clock synchronisation.
3. Following  $T_{INIT}$  the data bytes will be sent. 8 Bytes will be sent after each charge cycle.
4. Each byte sent will be preceded by a START bit and a STOP bit will follow every byte.
5. STOP bit indicated by taking pin 1 high. The STOP bit does not have a defined period.



Table 8.1: Byte Definitions for Streaming Mode

Byte (B)	Bit	Value
0		AA
1	7:0	CS High byte
2	15:8	CS Low byte
3	23:16	LTA High byte
4	31:24	LTA Low byte
5 Sys Flags	39	~
	38	~
	37	Active High
	36	Filter Halt
	35	LP active
	34	ATI Busy
	33	Noise Found
	32	In Zoom
6	47	Touch
	46	Proximity
	45	Multipliers
	44	Multipliers
	43	Multipliers
	42	Multipliers
	41	Multipliers
40	Multipliers	
7	55:48	Compensation
8	63:56	Counter

The IQS228AS/B can communicate on an I2C compatible bus structure. Note that 4.7kΩ pull-up resistors should be placed on SDA and SCL.

The Control byte indicates the 7-bit device address (0x44H) and the Read/Write indicator bit.

## 8.1 Event Mode

The IQS228AS/B has Event Mode implemented during 1-wire communication. This allows the MCU to monitor the POUT pin for status changes (proximity or touch made or released events) instead of capturing data continuously. Upon a status change, the IQS228AS/B will pull the POUT pin for low to indicate to the MCU to read data. The POUT pin will stay low for 1.6ms.

## 8.2 I<sup>2</sup>C

The IQS228AS/B also allow for I<sup>2</sup>C streaming for debugging. Data Streaming can be changed from 1-wire protocol to I<sup>2</sup>C as shown below:

### Configuration: [Bank2 bit7: Streaming Mode](#)

Bit	Selection
0	1-Wire Protocol
1	I <sup>2</sup> C Streaming

The Memory Map for the IQS228AS/B can be found in Appendix A.



## 9 Auto Tuning Implementation (ATI)

ATI is a sophisticated technology implemented in the latest generation ProxSense® devices that optimises the performance of the sensor in a wide range of applications and environmental conditions (refer to application note AZD0027 - Auto Tuning Implementation).

ATI makes adjustments through external reference capacitors unnecessary (as required by most other solutions) to obtain optimum performance.

### 9.1 Full ATI

The IQS228AS/B implements an automatic ATI algorithm. This algorithm automatically adjusts the ATI parameters to optimise the sensing electrodes connection to the device.

The device will execute the ATI algorithm whenever the device starts-up and or when the counts are not within a predetermined range.

There are 2 important definitions to understand for ATI:

### 9.2 ATI Target

ATI adjusts internal circuitry according to two parameters, the **ATI multiplier** and the **ATI compensation**.

- > The **ATI multiplier** can be viewed as a coarse adjustment of the Counts (CS), used to achieve the ATI BASE value.
- > The **ATI compensation** is a fine adjustment used to reach the ATI TARGET value.

With these two parameters the Counts (CS) of the IQS228AS/B is tuned until an ATI target value of 1200 is achieved.

### 9.3 ATIBASE: Significance of ATI Base

As mentioned above, the **ATI multiplier** is used to select a base value for the ATI. The ATI BASE value is important, as this determines the sensitivity of the device. The sensitivity can be defined as:

$$\text{Sensitivity} = \text{ATI TARGET} / \text{ATI BASE}$$

The ATI Target remains fixed at 1200 and it can thus be seen from this that a larger base value will result in a less sensitive device. The designer has the option to increase/reduce the sensitivity of the system through the ATI BASE

value. For most applications the ATI BASE should be kept default.

The options for the ATI BASE values are as follows:

#### Configuration: Bank1 bit 2-0

Bit	Selection
000	200
001	50
010	75
011	100
100	150
101	250
110	300
111	500

### 9.4 Sensitivity Due to ATI

The adjustment of the ATI parameters will result in variations in the count and sensitivity. Sensitivity can be observed as the change in count as the result of a fixed change in sensed capacitance. The ATI parameters have been chosen to provide significant overlap. It may therefore be possible to select various combinations of ATI multiplier and ATI compensation settings to obtain the same count. The sensitivity of the various options may however be different for the same count.

### 9.5 ATI Procedure

While the Automatic ATI algorithm is in progress this condition will be indicated in the streaming data and proximity and touch events cannot be detected. The device will only briefly remain in this condition and it will be entered only when relatively large shifts in the count has been detected.

The automatic ATI function aims to maintain a constant count, regardless of the capacitance of the sense electrode (within the maximum range of the device).

The effects of auto-ATI on the application are the following:

- > Automatic adjustment of the device configuration and processing parameters for a wide range of PCB and application designs to maintain a optimal configuration for proximity and touch detection.
- > Automatic tuning of the sense electrode at start-up to optimise the sensitivity of the application.



- > Automatic re-tuning when the device detects changes in the sensing electrodes capacitance to accommodate a large range of changes in the environment of the application that influences the sensing electrode.
- > Re-tuning only occurs during device operation when a relatively large sensitivity reduction is detected. This is to ensure smooth operation of the device during operation.
- > Re-tuning may temporarily influences the normal functioning of the device, but in most instances the effect will be hardly noticeable.
- > Shortly after the completion of the re-tuning process the sensitivity of a Proximity detection may be reduced slightly for a few seconds as internal filters stabilises.

Automatic ATI can be implemented so effectively due to:

- > Excellent system signal to noise ratio (SNR).
- > Effective digital signal processing to remove AC and other noise.
- > The very stable core of the devices.
- > The built-in capability to accommodate a large range of sensing electrode capacitances.





## 10 DYCAL Specific settings

### 10.1 Release Threshold

The IQS228AS/B has the option to increase the release threshold when in TM. This helps that small variations caused by moving a finger/hand on a touch pad will not cause the IC to exit TM, making the solution more robust. The options available are shown below:

**Configuration:** [Bank0 bit6](#)

Bit	Selection
0	75% of Entry Delta
1	87.5% of Entry Delta

After entering TM, as soon as the LTA follows to within 16 counts, a Entry Delta value is calculated as:

>  $\text{Entry Delta} = \text{LTA}_{\text{entry}} - \text{LTA}_{\text{current}}$

This calculated Entry Delta value is used for the Release Threshold as shown above.

If upon entry, the LTA value is already within 16 Counts, the Entry Delta is taken as the calculated touch threshold value.

### 10.2 Input Enable

The IQS228AS/B can be configured to have the CTRL pin function as an output on a Proximity event. Choosing the CTRL pin as output removes the Filter Halt and Halt Charge options of the pin as an input.

Using a touch event to activate OUT will make the system less sensitive which is needed in some applications. The LTA will still halt with the detection of a proximity but will not have an influence on the OUT pin. The LTA will still re-calibrate once a touch condition is detected.

**Configuration:** [Bank0 bit7](#)

Bit	Selection
0	Output
1	Input



## 11 Electrical Specifications

### 11.1 Absolute Maximum Specifications

*Exceeding these maximum specifications may cause damage to the device.*

Operating temperature:	IQS228AS	-20°C to 85°C
	IQS228B	-40°C to 85°C
Supply Voltage ( $V_{DDHI} - V_{SS}$ )		3.6V
Maximum pin voltage (OUT, CTRL)		$V_{DDHI} + 0.3V$
Pin voltage (Cx)		1.7V
Minimum pin voltage (VDDHI, VREG, OUT, CTRL, Cx)		$V_{SS} - 0.3V$
Minimum power-on slope		100V/s
ESD protection (VDDHI, VREG, $V_{SS}$ , OUT, CTRL, Cx)		8kV

### 11.2 General Characteristics

IQS228AS/B devices are rated for supply voltages between 1.8V and 3.6V.

*Table 11.1: IQS228AS/B General Operating Conditions*

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage		$V_{DDHI}$	1.8	3.3	3.6	V
Internal regulator output	$1.8 \leq V_{DDHI} \leq 3.6$	$V_{REG}$	1.64	1.7	1.75	V
Boost Power operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228AS/B\_BP}$	120	129	135	$\mu A$
Normal Power operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228AS/B\_NP}$	4.9	6.45	8.1	$\mu A$
Low power 1 operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228AS/B\_LP1}$	2.95	3.8	4.85	$\mu A$
Low power 2 operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228AS/B\_LP2}$	1.88	<2.5 <sup>1</sup>	3.2	$\mu A$
C <sub>x</sub> pin capacitance	$1.8 \leq V_{DDHI} \leq 3.6$	$C_{CxLoad}$			120	pF

Charge Transfer Timings for low power mode is found in Section 7.12.

*Table 11.2: Start-up and shut-down slope Characteristics*

DESCRIPTION	Conditions	PARAMETER	MIN	MAX	UNIT
POR	$V_{DDHI}$ Slope $\geq 100V/s$	POR	0.3 <sup>2</sup>	1.7	V
VDDHI reset level	$V_{DDHI}$ Slope $\geq 100V/s$	$RESET_{VDDHI}$	N/A	1.7	V
VREG reset level	$V_{DDHI}$ Slope $\geq 100V/s$	$RESET_{VREG}$	N/A	1.58 <sup>3</sup>	V

<sup>1</sup> All low power current values arise from characterization done from (-)35°C to (+)85°C at 3.3V.

<sup>2</sup> For a power cycle, ensure lowering VDDHI below the minimum value before ramping VDDHI past the maximum POR value

<sup>3</sup> Figure 2.4 Capacitors C1 & C3 should be chosen to comply with this specification



### 11.3 Output Characteristics<sup>1</sup>

Table 11.3: TOUT Characteristics

Symbol	Description	V <sub>OH</sub>	Conditions	MIN	TYP	MAX	UNIT
I <sub>SOURCE</sub>	Output High voltage	0.9*VDDHI	V <sub>DDHI</sub> = 3.6V	~	~	TBD	mA
		0.9*VDDHI	V <sub>DDHI</sub> = 3.3V	~	10	~	
		0.9*VDDHI	V <sub>DDHI</sub> = 1.8V	TBD	~	~	
Symbol	Description	V <sub>OL</sub>	Conditions	MIN	TYP	MAX	UNIT
I <sub>SINK</sub>	Output Low voltage	100mV	V <sub>DDHI</sub> = 3.6V			TBD	mA
		100mV	V <sub>DDHI</sub> = 3.3V		10		
		100mV	V <sub>DDHI</sub> = 1.8V	TBD			

Table 11.4: POUT Characteristics

Symbol	Description	V <sub>OH</sub>	Conditions	MIN	TYP	MAX	UNIT
I <sub>SOURCE</sub>	Output High voltage	0.9*VDDHI	V <sub>DDHI</sub> = 3.6V	~	~	TBD	mA
		0.9*VDDHI	V <sub>DDHI</sub> = 3.3V	~	10	~	
		0.9*VDDHI	V <sub>DDHI</sub> = 1.8V	TBD	~	~	
Symbol	Description	V <sub>OL</sub>	Conditions	MIN	TYP	MAX	UNIT
I <sub>SINK</sub>	Output Low voltage	0.1V	V <sub>DDHI</sub> = 3.6V			TBD	mA
		0.1V	V <sub>DDHI</sub> = 3.3V		10		
		0.1V	V <sub>DDHI</sub> = 1.8V	TBD			

Table 11.5: Combined Characteristics

Symbol	Description	V <sub>OH</sub>	Conditions	MIN	TYP	MAX	UNIT
I <sub>SOURCE</sub>	Output High voltage	0.9*VDDHI	V <sub>DDHI</sub> = 3.6V	~	~	TBD	mA
		0.9*VDDHI	V <sub>DDHI</sub> = 3.3V	~	17	~	
		0.9*VDDHI	V <sub>DDHI</sub> = 1.8V	TBD	~	~	
Symbol	Description	V <sub>OL</sub>	Conditions	MIN	TYP	MAX	UNIT
I <sub>SINK</sub>	Output Low voltage	0.1V	V <sub>DDHI</sub> = 3.6V			TBD	mA
		0.V	V <sub>DDHI</sub> = 3.3V		20		
		0.1V	V <sub>DDHI</sub> = 1.8V	TBD			

<sup>1</sup> I/O sink capabilities only in Active Low configuration. I/O source capabilities only in Active High configuration.



## 11.4 Packaging Information

### 11.4.1 TSOT23-6

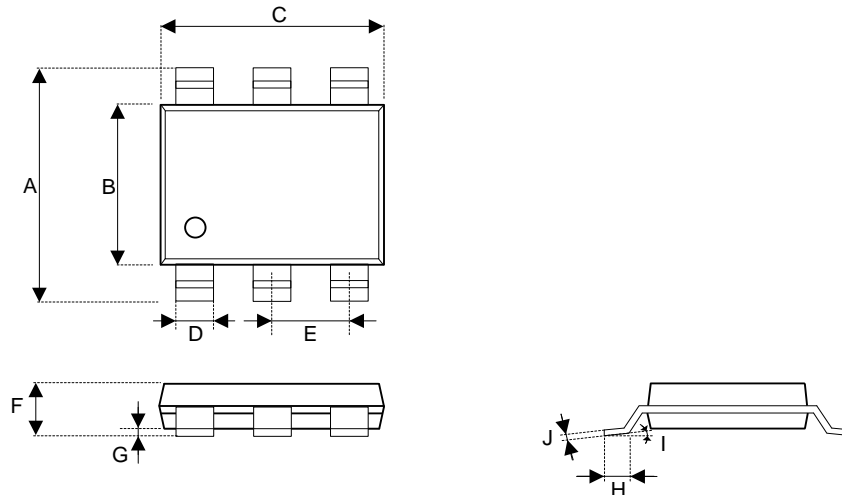


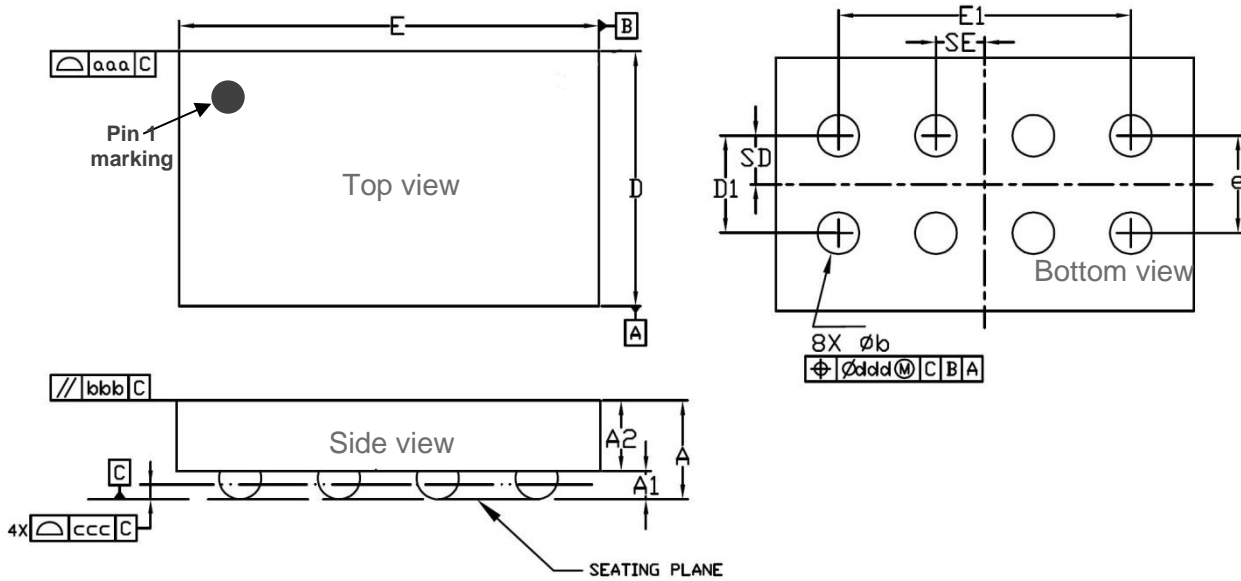
Figure 11.1: TSOT23-6 Packaging<sup>1</sup>

Table 11.6: TSOT23-6 Dimensions

Dimension	Min (mm)	Max (mm)
A	2.60	3.00
B	1.50	1.70
C	2.80	3.00
D	0.30	0.50
E	0.95 Basic	
F	0.84	1.00
G	0.00	0.10
H	0.30	0.50
I	0°	8°
J	0.03	0.20



### 11.4.2 WLCSP-8

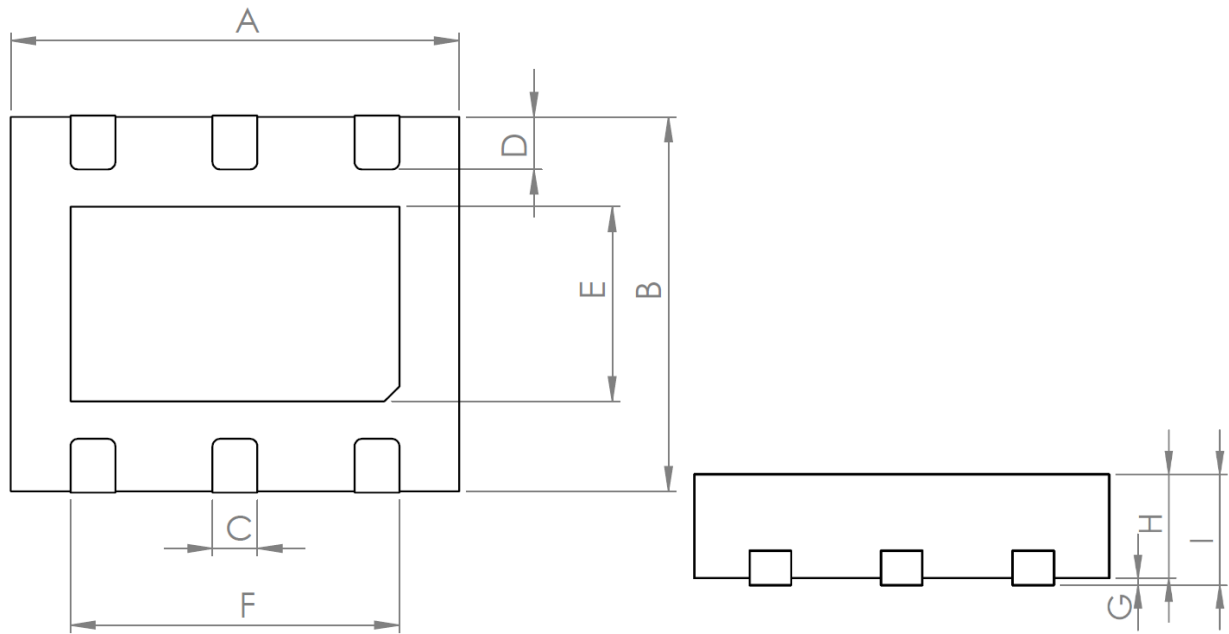


Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.310	0.350	0.390
A1	0.085	0.100	0.115
A2	0.225	0.250	0.275
D	0.865	0.880	0.895
E	1.455	1.470	1.485
D1	0.300	0.350	0.400
E1	1.000	1.050	1.100
b	0.125	0.150	0.175
e	0.350 BSC		
SD	0.175 BSC		
SE	0.175 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Figure 11.2 IQS228B WLCSP-8 Dimensions (in mm)



### 11.4.3 DFN-6



DFN-6 Packaging

DFN-6 Dimensions

Dimension	Min	Max
A	3.00mm	3.00mm
B	2.50mm	2.50mm
C	0.30mm	0.30mm
D	0.35mm	0.35mm
E	1.30mm	1.30mm
F	2.20mm	2.20mm
G	0.05mm	0.05mm
H	0.75mm	0.75mm
I	0.80mm	0.80mm



#### 11.4.4 MSL Level

**Moisture Sensitivity Level (MSL)** relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the time period in which a moisture sensitive device can be exposed to ambient room conditions (approximately 30°C/85%RH see J-STD033C for more info) before reflow occur.

Package	Level (duration)
TSOT23-6	MSL 1 (Unlimited at ≤30 °C/85% RH) Reflow profile peak temperature < 260 °C for < 30 seconds
WLCSP-8	Non-encapsulated device – not moisture sensitive Reflow profile peak temperature < 260 °C for < 30 seconds
DFN-6	MSL 1 (Unlimited at ≤30 °C/85% RH) Reflow profile peak temperature < 260 °C for < 30 seconds



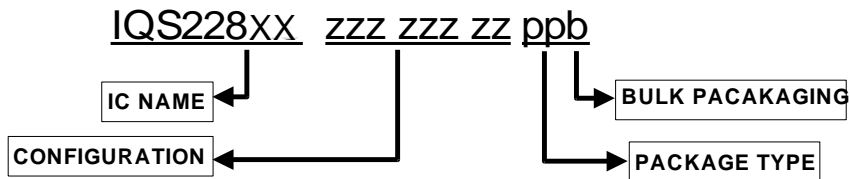
## 12 Datasheet and Part-number Information

### 12.1 Ordering Information

Orders will be subject to a MOQ (Minimum Order Quantity) of a full reel. Contact the official distributor for sample quantities. A list of the distributors can be found under the “Distributors” section of [www.azoteq.com](http://www.azoteq.com).

For large orders, Azoteq can provide pre-configured devices.

The Part-number can be generated by using USBProg.exe or the Interactive Part Number generator on the website.



IC NAME	IQS228AS	=	IQS228 Self Capacitive
	IQS228B	=	IQS228 Self Capacitive
CONFIGURATION	zzz zzz zz	=	IC Configuration (hexadecimal)
PACKAGE TYPE	TS	=	TSOT23-6 package
	CS	=	WLCSP-8 package
	DN	=	DFN-6 package
BULK PACKAGING	R	=	Reel
		=	TSOT23-6 and WLCSP-8: 3000pcs/reel DFN-6: 6000pcs/reel
		=	MOQ = 1 reel (orders shipped as full reels)





## 12.2 Device Marking – Top

### 12.2.1 TSOT23-6 Package Markings

There are 2 marking versions in circulation for IQS228AS and IQS228B:

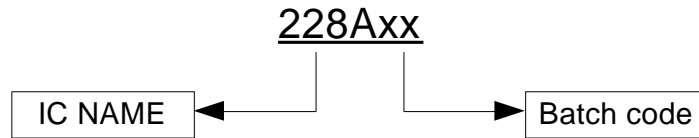


Figure 12.1: First Marking Variant of IQS228AS

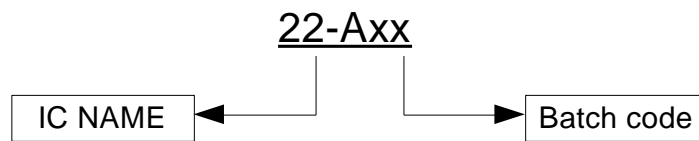


Figure 12.2: Second Marking Variant of IQS228AS

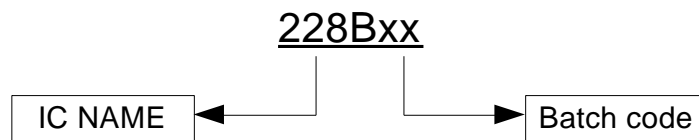


Figure 12.3: First Marking Variant of IQS228B

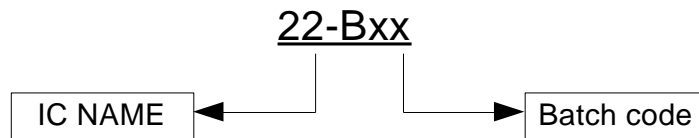


Figure 12.4: Second Marking Variant of IQS228B

<b>IC NAME</b>	228A	=	IQS228AS Self Capacitive
	22-A	=	IQS228AS Self Capacitive
	228B	=	IQS228B Self Capacitive
	22-B	=	IQS228B Self Capacitive
<b>Batch Code</b>	xx	=	AA to ZZ



### 12.2.2 WLCSP-8 Package Markings

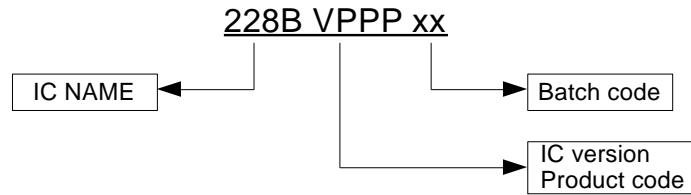


Figure 12.5 Top Marking of IQS228B WLCSP Package

<b>IC NAME</b>	228B	=	IQS228B Self Capacitive
<b>Batch Code</b>	xx	=	AA – ZZ
<b>IC VERSION</b>	V		
<b>Product Code</b>	PPP		

### 12.2.3 DFN-6 Package Markings

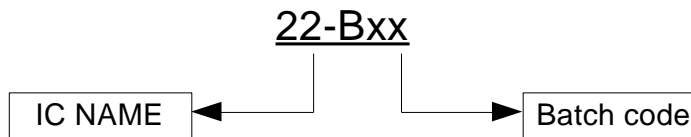


Figure 12.6 IQS228B DFN-6 Package Top Marking

<b>IC NAME</b>	22-B	=	IQS228B Self Capacitive
<b>Batch Code</b>	xx	=	AA to ZZ



### 12.3 Tape and Reel Specification

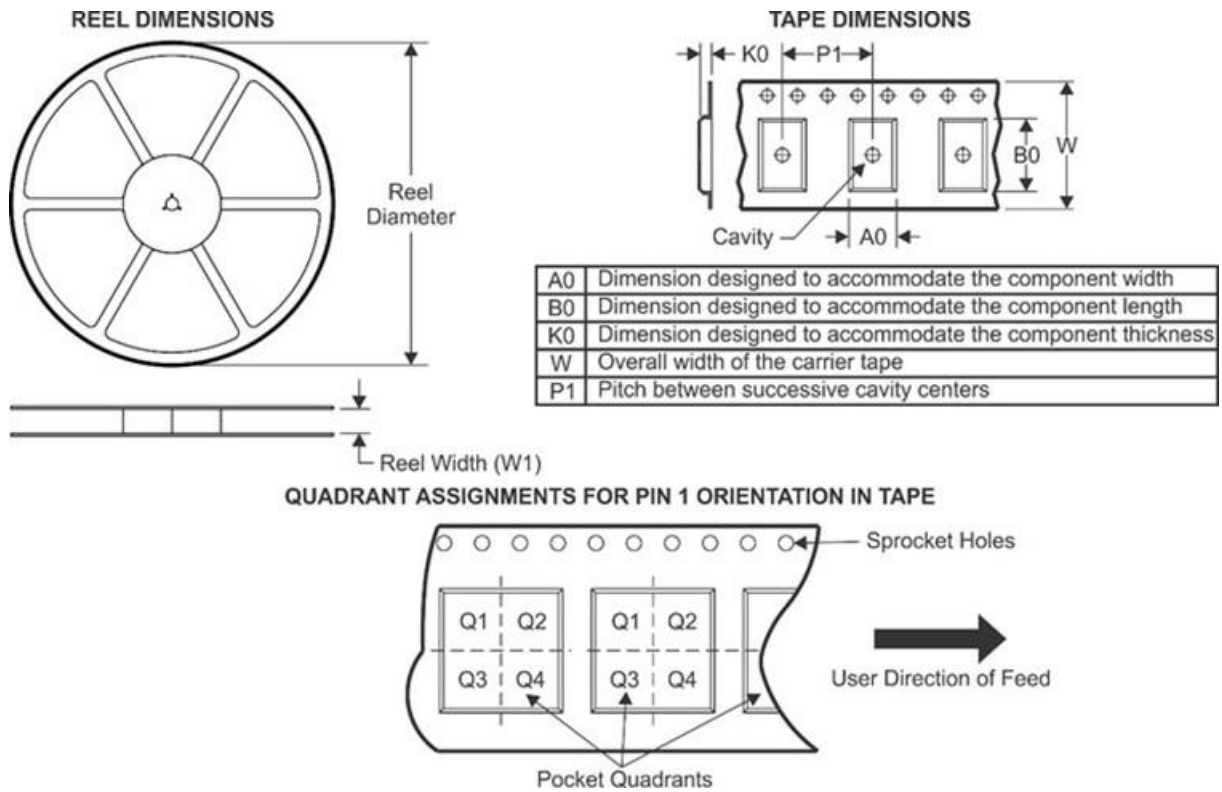


Figure 12.7: TSOT23-6 Tape Specification.

Table 12.1 Tape and Reel Dimensions

Device	Package Type	Package Drawing	Pins	QTY per reel	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
IQS228ASzzzzzzzTSR	TSOT23/6	TSOT23-6	6	3000	178	9.5	3.1	3.1	1.3	4	8	Q3
IQS228BzzzzzzzTSR	TSOT23/6	TSOT23-6	6	3000	178	9.5	3.1	3.1	1.3	4	8	Q3
IQS228BzzzzzzzCSR	WLCSP8	WLCSP-8	8	3000	179	8.4	1	1.55	0.48	4	8	Q3
IQS228BzzzzzzzDNR	DFN6	DFN-6	6	6000	330	12.4	2.8	3.3	1.2	4	12	Q1



## Appendix A. Memory Map

### Device Information

00H		Product Number (PROD_NR)							
		Bit	7	6	5	4	3	2	1
Access	Value	39 (Decimal)							
	Note								
R									

01H		Software Number (SW_NR)							
		Bit	7	6	5	4	3	2	1
Access	Value	29 (Decimal)							
	Note								
R									

#### [00H] PROD\_NR

The product number for the IQS228A is 39 (decimal).

#### [01H] SW\_NR

The software version number of the device ROM can be read in this byte. The latest software version is 29 (decimal).

10H		System Flags (Sys_Flags)							
		Bit	7	6	5	4	3	2	1
Access	Value		~	Logic	Halt	LP	ATI	ND	Zoom
	Note								
R									

#### [10H] SYSFLAGS0

*Bit 7-6:*       **SYSTEM\_USE**

*Bit 5:*         **Logic:** Logic Output Indication

0 = Active Low

1 = Active High

*Bit 4:*         **Halt:** Indicates Filter Halt status

0 = LTA not being Halted

1 = LTA Halted

*Bit 3:*         **LP:** Low Power Mode

0 = Sample time BP

1 = Sample time LP

*Bit 2:*         **ATI:** Status of automated ATI routine



0 = ATI is not busy  
1 = ATI in progress

**Bit 1:** **ND:** This bit indicates the presence of noise interference.

0 = IC has not detected the presence of noise  
1 = IC has detected the presence of noise

**Bit 0:** **ZOOM:** Zoom will indicate full-speed charging once an undebounced proximity is detected. In BP mode, this will not change the charging frequency.

0 = IC not zoomed in  
1 = IC detected undebounced proximity and IC is charging at full-speed (BP)

31H		Status								
		Bit	7	6	5	4	3	2	1	0
Access		Value	DYCAL						Touch	Proximity
R		Note								

**[31H] Status**

**Bit 7:** **Dycal:** Dycal Detection  
0 = Not Active  
1 = Active

**Bit 6:2:** **SYSTEM\_USE**

**Bit 1:** **Touch:** Touch Detection  
0 = Not Active  
1 = Active

**Bit 0:** **Prox:** Proximity Detection  
0 = Not Active  
1 = Active

42H		Counts_High (CS_H)								
		Bit	7	6	5	4	3	2	1	0
Access		Value	Counts High Byte							
R		Note								



43H	Counts_Low (CS_L)								
	Bit	7	6	5	4	3	2	1	0
	Access	Counts Low Byte							
	R	Note							

83H	LTA_High (LTA_H)								
	Bit	7	6	5	4	3	2	1	0
	Access	Long Term Average High Byte							
	R	Note							

84H	LTA_Low (LTA_L)								
	Bit	7	6	5	4	3	2	1	0
	Access	Long Term Average Low Byte							
	R	Note							

C4H	Fuse Bank 0 (FB_0)								
	Bit	7	6	5	4	3	2	1	0
	Access	See Table 3.1 for more details							
	R	Note							

C5H	Fuse Bank 1 (FB_1)								
	Bit	7	6	5	4	3	2	1	0
	Access	See Table 3.2 for more details							
	R	Note							



C6H		Fuse Bank 2 (FB_2)							
		Bit	7	6	5	4	3	2	1
Access		Value	See Table 3.4 for more details						
R		Note							

C7H		Fuse Bank 3 (FB_3)							
		Bit	7	6	5	4	3	2	1
Access		Value	See Table 3.5 for more details						
R		Note							

C8H		DEFAULT_COMMS_POINTER							
		Bit	7	6	5	4	3	2	1
Access		Value	(Beginning of Device Specific Data)						
R/W		Default	10H						

### **[C8H] Default Comms Pointer**

The value stored in this register will be loaded into the Comms Pointer at the start of a communication window. For example, if the design only requires the Proximity Status information each cycle, then the *Default Comms Pointer* can be set to ADDRESS '31H'. This would mean that at the start of each communication window, the comms pointer would already be set to the Proximity Status register, simply allowing a READ to retrieve the data, without the need of setting up the address.



## Appendix B. Errata

### Filter Halt Times

When the “[Zoom Disable](#)” bit is set, the halt times as specified in Section 3 will be scaled 16 x longer, due to added dead time when the IC core is turned off to reduce power consumption:

User Selectable Configuration Options: Bank 1 – Full ATI ([0xC5H](#))

$t_{\text{HALT1}}$	$t_{\text{HALT0}}$	~	~	TURBO	BASE <sub>2</sub>	BASE <sub>1</sub>	BASE <sub>0</sub>
bit 7							bit 0

**Bank1: bit 7-6**

$t_{\text{HALT}}$ : Halt times  
00 = 320 seconds  
01 = 640 seconds  
10 = Never  
11 = 48 seconds

[Section 7.11](#)






## Appendix C. Contact Information

	USA	Asia	South Africa
<b>Physical Address</b>	11940 Jollyville Suite 120-S Austin TX 78750 USA	Room 501A, Block A, T-Share International Centre, Taoyuan Road, Nanshan District, Shenzhen, Guangdong, PRC	1 Bergsig Avenue Paarl 7646 South Africa
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