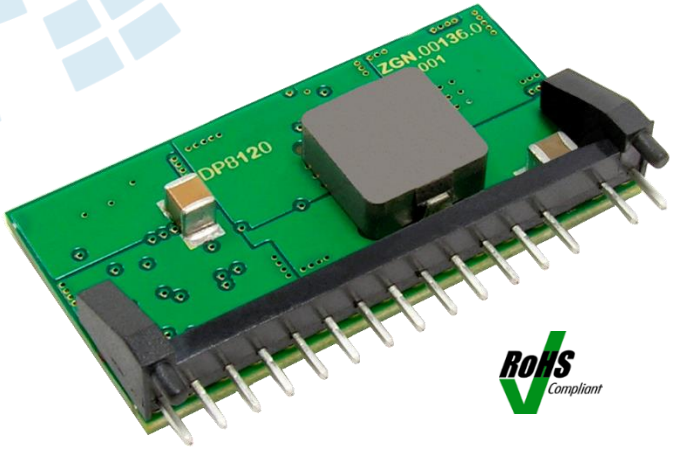
DP8120G

20A DC-DC Intelligent dPOL



Bel Power Solutions **DP8120G** is an intelligent, fully programmable step-down point-of-load DC-DC converter integrating digital power conversion and intelligent power management. It works with the DM7300 Series Digital Power Managers (DPM) which provides for synchronizing all system Power-On-Load regulators, for an elegant, flexible, low noise power system solution.

All key parameters, sequencing, tracking, fault protection, and compensation parameters of the DP8120G are programmable via Bel Power Solutions I^2C based GUI. All settings can be changed by a user at any time during product development and service. Once programmed, the DPM remembers all settings and configures the DP8120G through a self-clocking single wire communication bus.

FLASH memory in the DPM allows changes to be made without the need to solder or rewire the regulator.

Key Features & Benefits

- Input voltage range: 8–14 V
- Output voltage range: 0.7–5.5 V at 0 – 20 A.
- Programmable dynamic output voltage positioning for better load transient response
- Choice of 500 kHz switching for highest efficiency or 1 MHz for lowest ripple noise.
- Flexible Fault Response features
- Multiple turn-on/off slew rates and delays
- Digital Filter Compensation
- Synchronous operation with other supplies
- Real time performance monitoring
- GUI based configuration for short development time.
- package: 40.6 x 21.3 x 10.4 mm
- Approved to the latest edition and amendment of ITE Safety standards, UL/CSA 60950-1 and IEC60950-1

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1. ORDERING INFORMATION

DP	81	20	G	-	zz
Product Family	Series	Output Current	RoHS Compliance	Dash	Packaging Option[1]
d-pwer®	Intelligent dPOL Converter	20 A	**G -** RoHS compliant for all six substances		**T100** - 100pc T&R **Sample** quantity orders have no suffix.

Example: **DP8120G-T100:** A 100-piece reel of RoHS compliant dPOL converters. Each dPOL converter is labeled DP8120G.

Reference Documents

- DM7300 Digital Power Manager Data Sheet
- DM7300 Digital Power Manager Programming Manual
- I²C Graphical User Interface
- DM00056-KIT USB to I²C Adapter Kit. User Manual

2. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the converter.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Inductor Temperature	Input Voltage applied	-40	125	°C
Input Voltage	250 ms Transient		15	VDC
Output Current	(See Output Current De-rating Curves)	-16	20	ADC

3. ELECTRICAL SPECIFICATIONS

Specifications apply at the input voltage from 8V to 14V, output load from 0 to 20 A, ambient temperature from -40°C to 85°C. Test conditions include an output filter with 3 x 330 µF 20mΩ solid electrolytic, plus 2 x 22 µF X7R ceramic output capacitors, unless otherwise noted.

3.1. INPUT SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Input Voltage (V_{IN})		8		14	VDC
Input Current (at no load)	V_{IN} = 14.0 V, V_{OUT} = 3.3 V		50		mADC
Undervoltage Lockout	Ramping Up	5		7.5	VDC
	Ramping Down				VDC
VLDO Input Current	Current drawn from the external low voltage supply at VLDO = 8 V		50		mADC

[1] Packaging option is used only for ordering and not included in the part number printed on the dPOL converter label.

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3.2. OUTPUT SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Output Voltage Range (V_{OUT})		0.7		5.5	VDC
Output Voltage Setpoint Resolution			2.5 mV (1 LSB)		
Output Voltage Setpoint Accuracy	2nd Vo Loop Enabled		±(0.6% + 5 mV)		
Output Current (I_{OUT})	$V_{IN\ MIN}$ to $V_{IN\ MAX}$	-5.5[2]		20	ADC
Line Regulation	$V_{IN\ MIN}$ to $V_{IN\ MAX}$		±0.3		$\%V_{OUT}$
Load Regulation	0 to $I_{OUT\ MAX}$		±0.2		$\%V_{OUT}$
Dynamic Regulation Peak Deviation Settling Time	Slew rate 1A/µs, 50 -75% load step F_{SW} = 500 kHz to 10% of peak deviation See Output Load Transient Section		50 60		mV µs
Output Voltage Peak-to-Peak Ripple and Noise Scope BW = 20 MHz Full Load	V_{IN} = 8.0 V, V_{OUT} = 0.7 V V_{IN} = 8.0 V, V_{OUT} = 2.5 V V_{IN} = 8.0 V, V_{OUT} = 5.5 V V_{IN} = 14 V, V_{OUT} = 0.7 V V_{IN} = 14 V, V_{OUT} = 2.5 V V_{IN} = 14 V, V_{OUT} = 5.5 V		10 20 40 18 35 50		mV mV mV mV mV mV
Temperature Coefficient	V_{IN} = 12 V, I_{OUT} = 0.5×$I_{OUT\ MAX}$		20		ppm/°C
Switching Frequency	Default Programmable to		500 500/1000		kHz kHz
Duty Cycle Limit	Default Programmable, 1.56% steps	 3.125	90.5	 100	% %

3.3. PROTECTION SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Output Overcurrent Protection					
Type	Default Programmable		Non-Latching, 130 ms period Latching/Non-Latching		
Threshold	Default Programmable in 11 steps	 36	132	 132	$\%I_{OUT}$ $\%I_{OUT}$
Threshold Accuracy		-20		+20	$\%I_{OCP.SET}$
Output Overvoltage Protection					
Type	Default Programmable		Non-Latching, 130 ms period Latching/Non-Latching		
Threshold	Default Programmable in 10% steps	 110	130	 130	$\%V_{O.SET}$ $\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$ = 2.5 V	-2		2	$\%V_{OVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Turn Off Behavior[3]	Default Programmable to		Emergency Off Critical Off / Emergency Off		

[2] At negative (sink) output current (bus terminator mode) the efficiency of the DP8120 degrades resulting in increased internal power dissipation and switching noise. Therefore maximum allowable negative current under specific conditions is lower than the current determined from the de-rating curves shown in paragraph.
[3] Sequenced Off: The turn-off follows the turn-off delay and slew-rate settings; Critical Off: At turn-off both low and high switches are immediately disabled; Catastrophic Off: At turn-off the high side switch is disabled and the low side switch is enabled.

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Output Undervoltage Protection				
Type	Default	Non-Latching, 130ms period		
	Programmable	Latching/Non-Latching		
Threshold	Default	75		$\%V_{O.SET}$
	Programmable in 5% steps	75	90	$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$ = 2.5 V	-2	2	$\%V_{UVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated	6		µs
Turn Off BehaviorError! Bookmark not defined.	Default	Sequenced Off		
	Programmable to	Sequenced / Critical Off		
Overtemperature Protection				
Type	Default	Non-Latching, 130ms period		
	Programmable	Latching/Non-Latching		
Turn Off Threshold	Temperature is increasing	120		°C
Turn On Threshold	Temperature is decreasing after the module was shut down by OTP[4]	110		°C
Threshold Accuracy		-5	5	°C
Delay	From instant when threshold is exceeded until the turn-off command is generated	6		µs
Turn Off BehaviorError! Bookmark not defined.	Default	Sequenced Off		
	Programmable to	Sequenced / Critical Off		
Tracking Protection (when Enabled)				
Type	Default	Disabled		
	Programmable	Latching/Non-Latching, 130ms		
Threshold	Enabled during output voltage ramping up		±250	mVDC
Threshold Accuracy		-50	50	mVDC
Delay	From instant when threshold is exceeded until the turn-off command is generated	6		µs
Overtemperature Warning				
Threshold	Always enabled, reported in Status register (TW bit)[5]	110		°C
Threshold Accuracy	From Nominal Set Point	-5	+5	°C
Hysteresis		1.7		°C
Power Good Signal (PG pin)				
Logic	V_{OUT} is inside the PG window	High		
	V_{OUT} is outside the PG window	Low		
Lower Threshold	Default	90		$\%V_{O.SET}$
	Programmable in 5% steps	90	95	$\%V_{O.SET}$
Upper Threshold	Default	110		$\%V_{O.SET}$
	Programmable in 5% steps	105	110	$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$ = 2.5 V	-2	2	$\%V_{O.SET}$
PG On Delay[6]	Default	0		ms
	Programmable at	0, 10, 50, 150		
PG Off Delay	Default	PG disabled when $V_{OUT} \leq V_{UV}$ threshold		
	Programmable same as PG On Delay	PG disabled at turn-off command (Reset function)		

[4] OTP clears when Overtemp Warning (Status Register TW bit) turns off.
[5] Temp Warning error same sign and proportional with OTP error.
[6] From instant when threshold is exceeded until status of PG signal changes high

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3.4. FEATURE SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Current Share					
Type			Active, Single Line		
Maximum Number of Modules Connected in Parallel	$I_{OUT} \geq 0$		4		
Current Share Accuracy	$I_{OUT} \geq 20\%\ I_{OUT\ NOM}$			±20	$\%I_{OUT}$
Interleave					
Interleave (Phase Shift)	Default		0		Degree
	Programmable in 22.5° steps	0		337.5	Degree
Sequencing[7]					
Turn ON Delay	Default		0		ms
	Programmable in 1ms steps	0		255	ms
Turn OFF Delay	Default		0		ms
	Programmable in 1ms steps	0		63	ms
Tracking					
Turn ON Slew Rate	Default		0.05		V/ms
	Programmable in 8 steps	0.05		2.0[8]	V/ms
Turn OFF Slew Rate	Default		-0.05		V/ms
	Programmable in 8 steps	-0.05		-2.0[8]	V/ms
Optimal Voltage Positioning					
Load Regulation	Default		0		mV/A
	Programmable in 7 steps	0		2.45	mV/A
Feedback Loop Compensation					
Proportional (Kr)	Programmable	0.01		2	
Integral (Ti)	Programmable	1		100	µs
Differential (Td)	Programmable	1		100	µs
Differential Roll-Off (Tv)	Programmable	1		100	µs
Monitoring					
Voltage Monitoring Accuracy	12 Bit Resolution over 0.5…5.5V	-0.5		0.5	%
Current Monitoring Accuracy	$20\%\ I_{OUT\ NOM} < I_{OUT} < I_{OUT\ NOM}$	-20		+20	$\%I_{OUT}$
Temperature Monitoring Accuracy	Junction temperature of dPOL controller	-5		+5	°C
Remote Voltage Sense (+VS and -VS pins)[9]					
Voltage Drop Compensation	Between +VS and VOUT			300	mV
Voltage Drop Compensation	Between -VS and PGND			100	mV

[7] Timing based on SD clock and subject to tolerances of SD.
[8] Achieving fast slew rates under specific line and load conditions may require feedback loop adjustment. See Rising and Falling Slew Rates
[9] For remote sense, it is recommended to place a 0.01-0.1µF ceramic capacitor between +VS and –VS pins as close to the dPOL converter as possible.

3.5. SIGNAL SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
VDD	Internal supply voltage	3.15	3.3	3.45	V
Logic In Max	Pull Up Logic max safe input			VDD+.5	V
SYNC/DATA Line (SD pin)					
ViL_sd	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_sd	HIGH level input voltage	0.75 x VDD		VDD + 0.5	V
Vhyst_sd	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
VoL	LOW level sink current @ 0.5V	14		60	mA
Tr_sd	Maximum allowed rise time 10/90%VDD			300	ns
Cnode_sd	Added node capacitance		5	10	pF
Ipu_sd	Pull-up current source at Vsd=0V	0.3		1.0	mA
Freq_sd	Clock frequency of external SD line	475		525	kHz
Tsynq	Sync pulse duration	22		28	% of clock cycle
T0	Data=0 pulse duration	72		78	% of clock cycle
Inputs: ADDR0...ADDR4, EN, IM					
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	
RdnL_ADDR	External pull down resistance ADDRX forced low			10	kOhm
Power Good and OK Inputs/Outputs					
Iup_PG	Pull-up current source input forced low PG	25		110	µA
Iup_OK	Pull-up current source input forced low OK	175		725	µA
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	V
IoL	LOW level sink current at 0.5V	4		20	mA
Current Share Bus (CS pin)					
Iup_CS	Pull-up current source at VCS = 0V	0.84		3.1	mA
ViL_CS	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_CS	HIGH level input voltage	0.75 x VDD		VDD+0.5	V
Vhyst_CS	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
IoL	LOW level sink current at 0.5V	14		60	mA
Tr_CS	Maximum allowed rise time 10/90% VDD			100	ns

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4. PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN TYPE	BUFFER TYPE	PIN DESCRIPTION	NOTES
VIN	1	P		Input Voltage	
GND	2	P		Power Ground	
CS	3	I/O	PU	Current Share	Connect to CS pins of other dPOLs connected in parallel. Leave floating if not on shared bus
SD	4	I/O	PU	Sync/Data Line	Connect to SD pin of DPM
ADDR4	5	I	PU	POL Address Bit 4	Tie to GND for 0 or leave floating for 1
OK	6	I/O	PU	Fault/Status Condition	Connect to OK pin of DPM and other dPOLs in the same Group
ADDR0	7	I	PU	POL Address Bit 0	Tie to GND for 0 or leave floating for 1
ADDR1	8	I	PU	POL Address Bit 1	Tie to GND for 0 or leave floating for 1
ADDR2	9	I	PU	POL Address Bit 2	Tie to GND for 0 or leave floating for 1
ADDR3	10	I	PU	POL Address Bit 3	Tie to GND for 0 or leave floating for 1
PG	11	I/O	PU	Power Good	Pin state reflected in Status Register.
+VS	12	I	A	Positive Voltage Sense	Connect to the positive point close to the load or VOUT
VOUT	13	P		Output Voltage	
	14			No Pin	
PGND	15	P		Power Ground	
-VS	16	I	A	Negative Voltage Sense	Connect to the negative point close to the load or PGND

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up, NC=No Connection

5. TYPICAL PERFORMANCE CHARACTERISTICS

5.1. THERMAL DERATING CURVES

Figure 1. Available output current vs. ambient air temperature and airflow rates for converter DP8120G mounted horizontally with air flowing from input to output, MOSFET temperature ≤ 120 °C, Vin = 8 V, Vout = 5 V, and Fsw= 500KHz

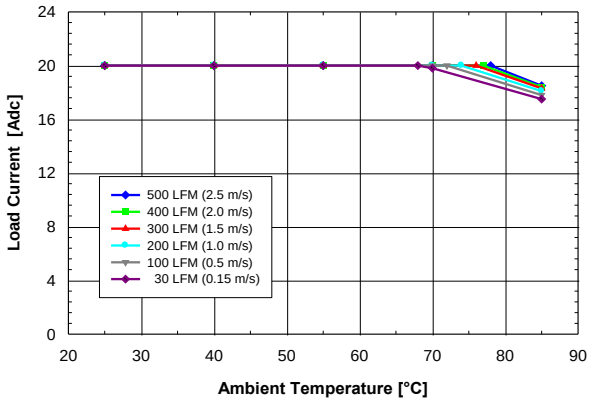

Figure 2. Available output current vs. ambient air temperature and airflow rates for converter DP8120G mounted horizontally with air flowing from input to output, MOSFET temperature ≤ 120 °C, Vin = 8 V, Vout = 5 V, and Fsw= 1MHz

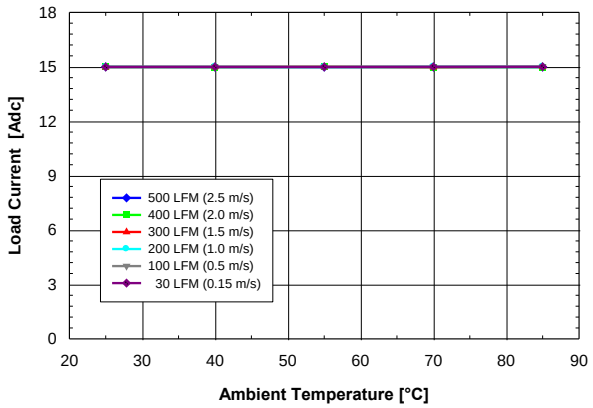

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Figure 3. Available output current vs. ambient air temperature and airflow rates for converter DP8120G mounted horizontally with air flowing from input to output, MOSFET temperature 120 C,Vin = 12 V, Vout = 5 V, and Fsw = 500KHz

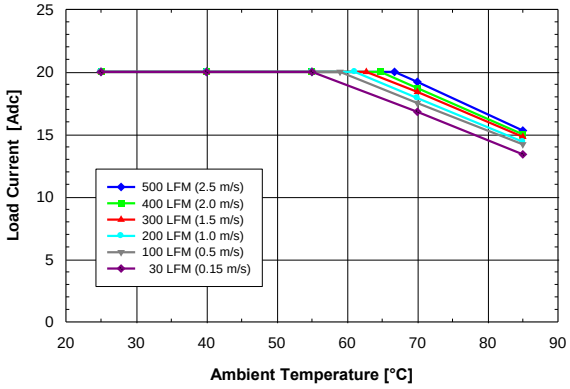
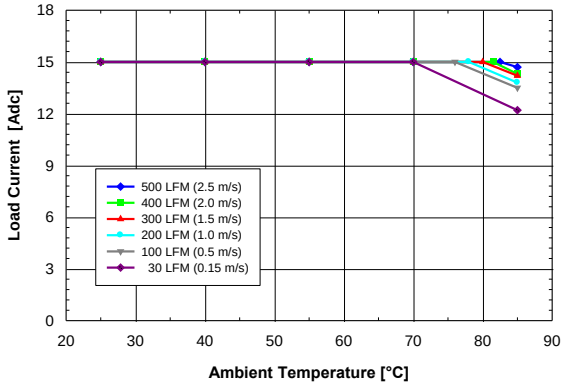


Figure 4. Available output current vs. ambient air temperature and airflow rates for converter DP8120G mounted horizontally with air flowing from input to output, MOSFET temperature 120C,Vin = 12 V, Vout = 5 V, and Fsw = 1MHz



5.2. EFFICIENCY CURVES

Figure 5. Efficiency vs. Load, Vin=8V, Fsw=500KHz

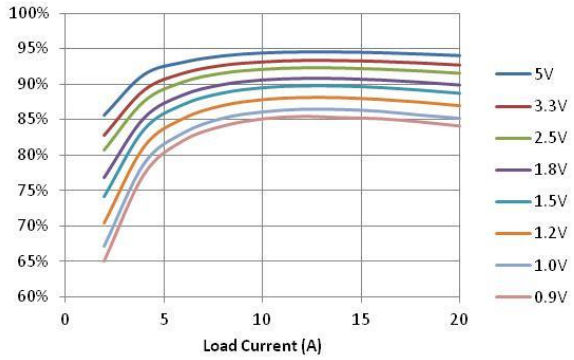


Figure 6. Dissipation vs Load, Vin=8V, Fsw=500KHz

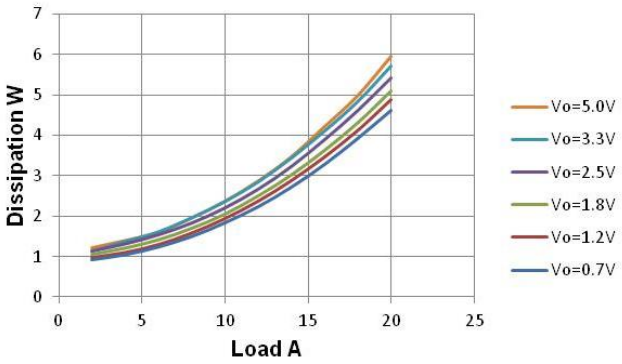


Figure 7. Efficiency vs. Input Voltage, Iout=20A, Fsw=500KHz

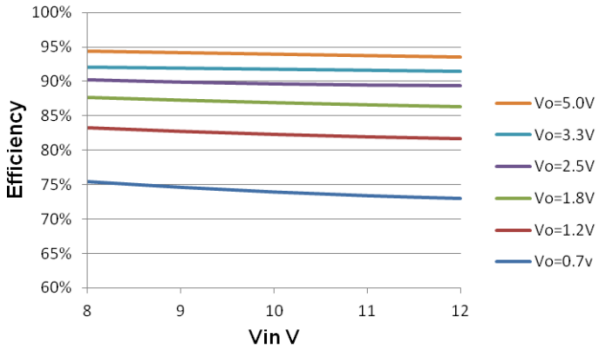


Figure 8. Efficiency vs Load, Vin=12V, Fsw=500KHz

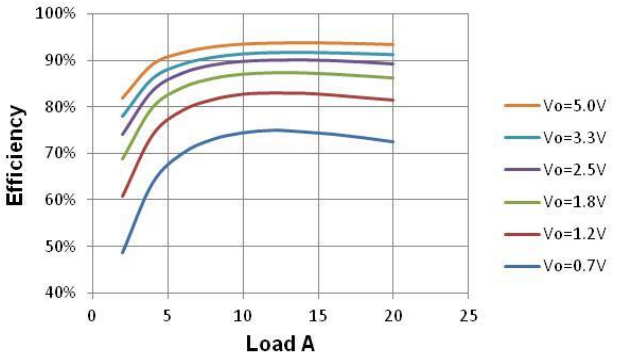


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Figure 9. Dissipation vs Load, Vin=12V, Fsw=500KHz

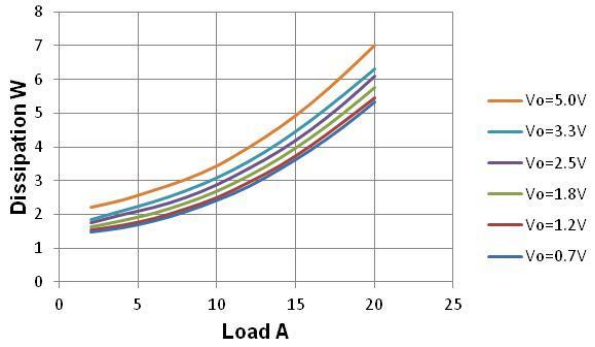


Figure 10. Efficiency vs Vin, Iout=20A, Fsw=1MHz

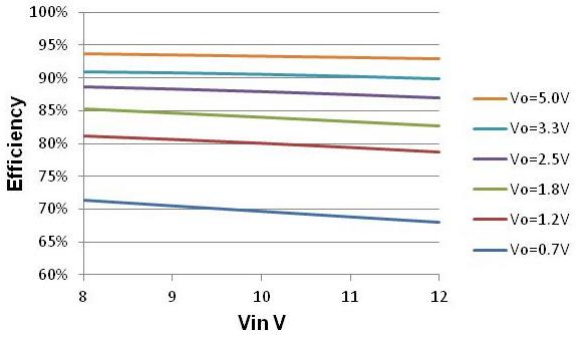


Figure 11. Efficiency vs Vout, Iout=20A, Fsw=500KHz

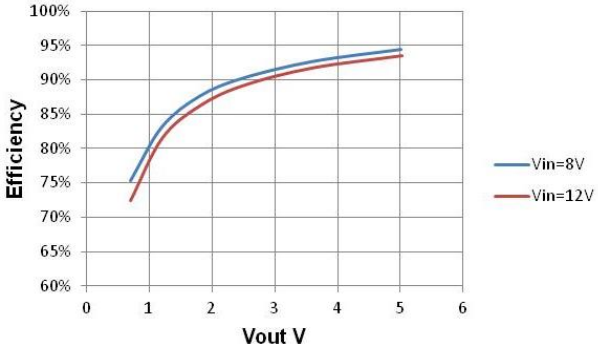
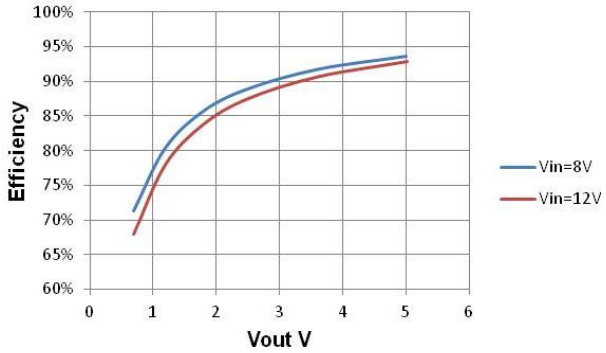


Figure 12. Efficiency vs Vout, Iout=20A, Fsw=1MHz



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6. PROGRAMMABLE FEATURES

Performance parameters of DP8120G dPOL converters are programmed by the system DPM over a self-clocking single wire bus as need. Each parameter is stored in FLASH memory in the DPM and loaded into volatile memory registers in the dPOL control chip detailed in Table 1. Setup registers 00h through 14h are programmed at the system power-up. When the input voltage is removed, the dPOL controller's default values are restored.

Table 1. DP8120G Memory Registers

CONFIGURATION REGISTERS		
Name	**Register**	**Address**
PC1	Protection Configuration 1	0x00
PC2	Protection Configuration 2	0x01
PC3	Protection Configuration 3	0x02
TC	Tracking Configuration	0x03
INT	Interleave and Frequency Configuration	0x04
DON	Turn-On Delay	0x05
DOF	Turn-Off Delay	0x06
VLC	Voltage Loop Configuration	0x07
CLS	Current Limit Set-point	0x08
DCL	Duty Cycle Limit	0x09
PC4	Protection Configuration 4	0x0A
V1H	Output Voltage Setpoint 1 (Low Byte)	0x0B
V1L	Output Voltage Setpoint 1 (High Byte)	0x0C
V2H	Output Voltage Setpoint 2 (Low Byte)	0x0D
V2L	Output Voltage Setpoint 2 (High Byte)	0x0E
V3H	Output Voltage Setpoint 3 (Low Byte)	0x0F
V3L	Output Voltage Setpoint 3 (High Byte)	0x10
CP	Controller Proportional Coefficient	0x11
CI	Controller Integral Coefficient	0x12
CD	Controller Derivative Coefficient	0x13
B1	Controller Derivative Roll-Off Coefficient	0x14
STATUS REGISTERS		
Name	**Register**	**Address**
RUN	Run enable / status	0x15
ST	Status	0x16
MONITORING REGISTERS		
Name	**Register**	**Address**
VOH	Output Voltage High Byte (Monitoring)	0x17
VOL	Output Voltage Low Byte (Monitoring)	0x27
IO	Output Current (Monitoring)	0x18
TMP	Temperature (Monitoring)	0x19

DP8120G converters can be programmed using the Graphical User Interface or directly via the I2C bus by using high and low level commands as described in the “DPM Programming Manual”.
DP8120G parameters can be reprogrammed at any time during the system operation and service except for the digital filter coefficients, the switching frequency and the duty cycle limit, that can only be changed when the dPOL output is turned off.

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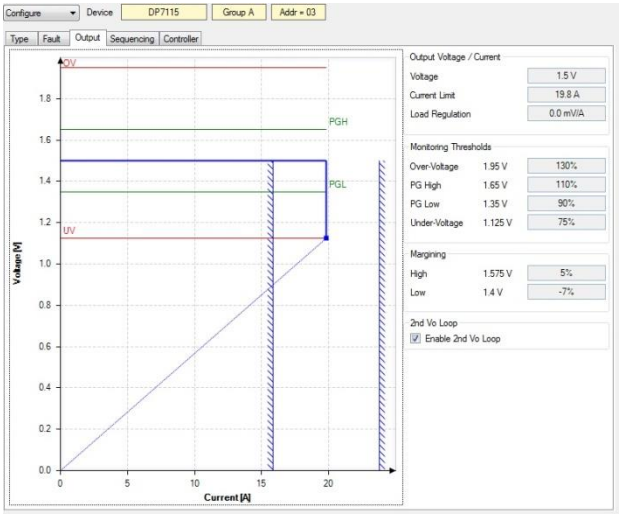
6.1. OUTPUT VOLTAGE

The output voltage can be programmed in the GUI Output Configuration window shown in the Figure 13 or directly via the I2C bus by writing into the VOS register shown in Figure 14.

Figure 13. Output Configuration Window



Note that the GUI shows the effect of setting PG, OV and UV limits as both values and graphical limit bars. Vertical hashed lines are error bars for the Overcurrent (OC) limit.

6.1.1. Output Voltage Setpoint

The output voltage programming range is from 0.7 V to 5.5 V. The resolution is constant across the range and is 2.5 mV. A Total of 3 registers are provided: one should be used for the normal setpoint voltage; the other two can be used to define a low/high margining voltage setpoint. Note that each register is 16bit wide and that the high byte needs always to be written / read first. The writing of the low byte triggers the refresh of the whole 16bit register (the high byte is written to a shadow register).
Unlike other configuration registers, the dPOL controller's VOS registers are dynamic. Changes to VOS values can be made while the output is enabled over the I2C bus through register bypass commands and the POL will change its output immediately.

Figure 14. Output Voltage Setpoint Register VOS

VOS: Output Voltage Set-Point
Address: 0x0B … 0x10

	Coefficient	Addr	Bits	Default
V1H	First Vo Setpoint High Byte	0x0B	8	
V1L	First Vo Setpoint Low Byte	0x0C	8	
V2H	Second Vo Setpoint High Byte	0x0D	8	
V2L	Second Vo Setpoint Low Byte	0x0E	8	
V3H	Third Vo Setpoint High Byte	0x0F	8	
V3L	Third Vo Setpoint Low Byte	0x10	8	

Mapping:	**Note:**
- 12 bit data word, left aligned - 1LSB = 2.5mV	- all registers are readable and writeable - always write and read the high byte first

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6.1.2. Output Voltage Margining

If the output voltage needs to be varied by a certain percentage, the margining function can be utilized. The margining can be programmed in the dPOL Configuration window or directly via the I2C bus using high level commands as described in the ”DM7300 Digital Power Manager Programming Manual”.
In order to properly margin dPOLs that are connected in parallel, the dPOLs must be members of one of the Parallel Buses. Refer to the GUI System Configuration Window shown in Figure 53.
Output Regulation Control
Load Regulation provides for dynamic output voltage change proportional to load current. This feature helps to improve step load response by changing the VI characteristic slope at the point of regulation. This can be programmed in the GUI Output Configuration window shown in Figure 13 or directly via the I2C bus. In the DP8120G Load Regulation can be set to one of eight values: 0, 0.37, 0.74, 1.11, 1.47, 1.84, 2.21, or 2.58 mv/A.

Figure 15. Optimal Voltage Positioning Concept

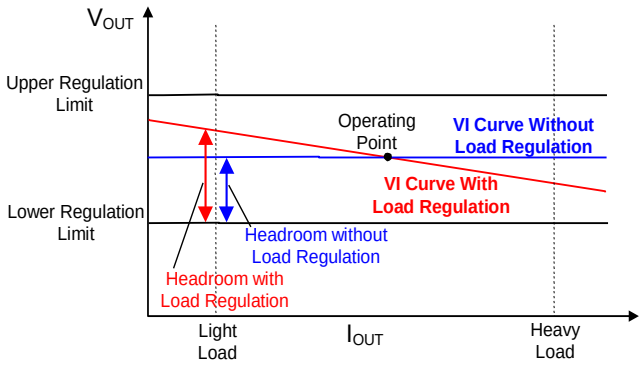


Figure 16 shows a DP8120G POL with 0 mv/A (load current) regulation. Alternating high and low output load currents causes large transients in Vout to appear with each change.

Figure 16 Transient Response with Regulation set to 0 mV/A

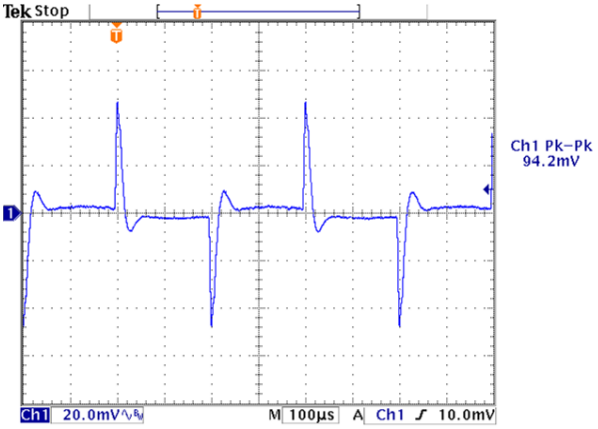
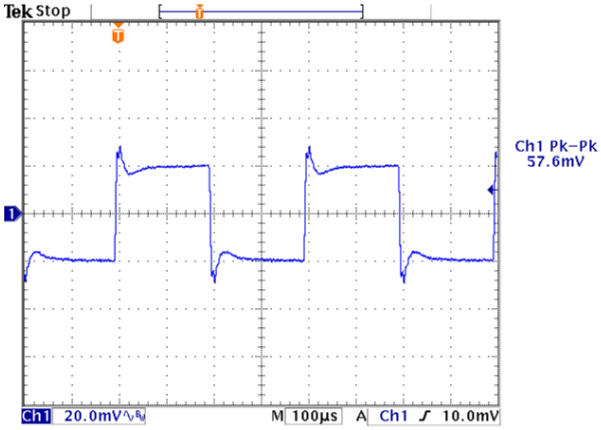


Figure 17 Transient response with non-zero Regulation.



As the Load Regulation parameter is increased, step offsets in output voltage begin to appear, as shown in Figure 17.

The Load Regulation parameter is an important part of Current Sharing. It is used to set one dPOL as a "master", by assigning a lower mV/A load regulation than all other dPOLs which share the load as "slaves". The dPOL with the lowest Regulation parameter sets the effective overall regulation. (See Current Sharing elsewhere in this document.)

6.2. SEQUENCING AND TRACKING

Turn-on delay, turn-off delay, and rising and falling output voltage slew rates can be programmed in the dPOL Configure Sequencing window shown in Figure 18 or directly via the I²C bus by writing into the DON, DOF, and TC registers, respectively. The registers are shown in Figure 19, Figure 21, and Figure 22.

Figure 18. dPOL Configure Sequencing Window

6.2.1. Turn-On Delay

Turn-on delay is defined as an interval from the application of the Turn-On command until the output voltage starts ramping up.

Figure 19. Turn-On Delay Register DON

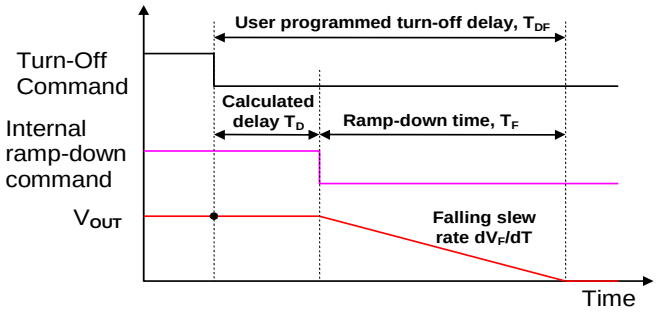
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DON7	DON6	DON5	DON4	DON3	DON2	DON1	DON0
Bit 7							Bit 0

Bit 7:0 **DON[7:0]**: Turn-on delay time
00h: corresponds to 0ms delay after turn-on command has occurred
…
FFh: corresponds to 255ms delay after turn-on command has occurred

6.2.2. Turn-Off Delay

Turn-off delay is defined as an interval from the application of the Turn-Off command until the output voltage reaches zero (if the falling slew rate is programmed) or until both high side and low side switches are turned off (if the slew rate is not programmed). Therefore, for the slew rate controlled turn-off the ramp-down time is included in the turn-off delay as shown in Figure 20.

Figure 20. Relationship between Turn-Off Delay and Falling Slew Rate



As it can be seen from the figure, the internally calculated delay T_D is determined by the equation below.

$$T_D = T_{DF} - \frac{V_{OUT}}{dV_F/dT},$$

For proper operation T_D shall be greater than zero. The appropriate value of the turn-off delay needs to be programmed to satisfy the condition.

If the falling slew rate control is not utilized, the turn-off delay only determines an interval from the application of the Turn-Off command until both high side and low side switches are turned off. In this case, the output voltage ramp-down process is determined by load parameters.

Figure 21. Turn-Off Delay Register DOF

DOF: Turn-Off Delay Configuration
Address: 0x06

U	U	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
---	---	**DOF5**	**DOF4**	**DOF3**	**DOF2**	**DOF1**	**DOF0**
Bit 7							Bit 0

Bit 7:6 **Unimplemented:** read as '0'

Bit 5:0 **DOF[5:0]**: Turn-Off delay in ms
0x00 = 0ms
0x01 = 1ms
…
0x0B = 11ms (default)
…
0x3F = 63ms

6.3. TURN-ON/OFF CONTROL

Once delays are accounted for, turn-on and turn-off characteristics are simply a function of slew rates, which are selectable.

6.3.1. Rising and Falling Slew Rates

Output voltage ramp up (and down) control is accomplished by programming the rising and falling slew rates of the output voltage, supported in the GUI as shown in Figure 18, which is implemented by the DPM through writing data to the TC register, Figure 22.

To achieve programmed slew rates, the output voltage is being changed in 10mV steps where duration of each step determines the slew rate. For example, ramping up a 1.0V output with a slew rate of 0.5V/ms will require 100 steps duration of 20µs each.

Duration of each voltage step is calculated by dividing the master clock frequency generated by the DPM. Since all dPOLs in the system are synchronized to the master clock, the matching of voltage slew rates of different outputs is very accurate as it can be seen in Figure 23 and Figure 28.

During the turn on process, a dPOL not only delivers current required by the load (I_{LOAD}), but also charges the load capacitance. The charging current can be determined from the equation below:

$$I_{CHG} = C_{LOAD} \times dV_R/dt$$

Where, C_{LOAD} is load capacitance, dV_R/dt is rising voltage slew rate, and I_{CHG} is charging current.

Figure 22. Tracking Configuration Register TC

TC: Tracking Configuration
Address: 0x03

U	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
---	**R2**	**R1**	**R0**	**SC**	**F2**	**F1**	**F0**
Bit 7							Bit 0

Bit 7 **Unimplemented**: read as '0'

R[2:0]: Vo rising slew rate
0 = 0.05 V/ms (default when in bus terminator mode)
1 = 0.1 V/ms (default)
2 = 0.2 V/ms
3 = 0.25 V/ms
4 = 0.5 V/ms
5 = 1.0 V/ms
6 = 2.0 V/ms
7 = Reserved

SC: Turn-off slew rate control
0 = disabled
1 = enabled (default)

F[2:0]: Vo falling slew rate
0 = -0.05 V/ms
1 = -0.1 V/ms
2 = -0.2 V/ms
3 = -0.25 V/ms (default when in bus terminator mode)
4 = -0.5 V/ms (default)
5 = -1.0 V/ms
6 = -2.0 V/ms
7 = Reserved

When selecting the rising slew rate, a user needs to ensure that

$$I_{LOAD} + I_{CHG} < I_{OCP}$$

Where I_{OCP} is the overcurrent protection threshold of the dPOL. If the condition is not met, then the overcurrent protection will be triggered during the turn-on process. To avoid this, dV_R/dt and the overcurrent protection threshold should be programmed to meet the condition above.

6.3.2. Delay and Slew Rate Combination

The effect of setting slew rates and turn on/off delays is illustrated in the following sets of figures.

Figure 23. Tracking Turn-On. Rising Slew Rate is programmed at 0.5V/ms for each output.

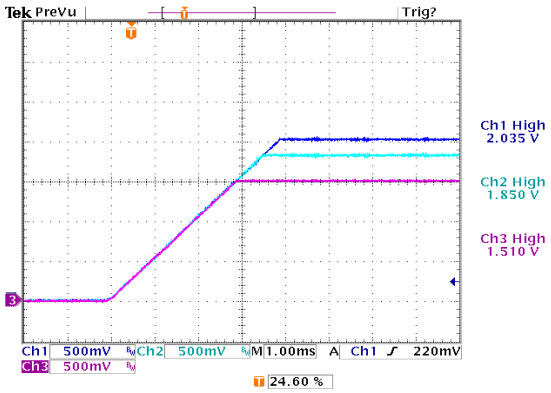


Figure 24. Turn-On with Different Rising Slew Rates. Rising Slew Rates are V1-1V/ms, V2-0.5V/ms, V3-0.2V/ms.

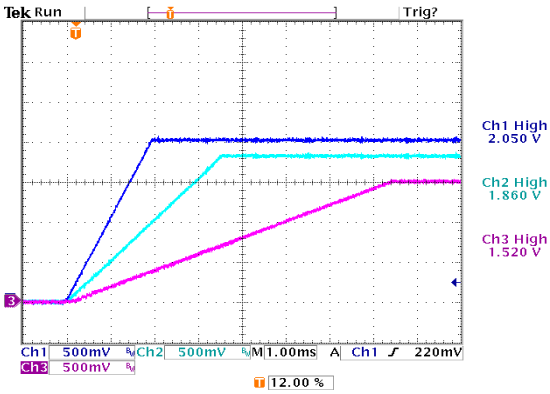


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Figure 25. Sequenced Turn-On. Rising Slew Rate is programmed at 1V/ms. V2 Delay is 2ms, V3 delay is 4ms.

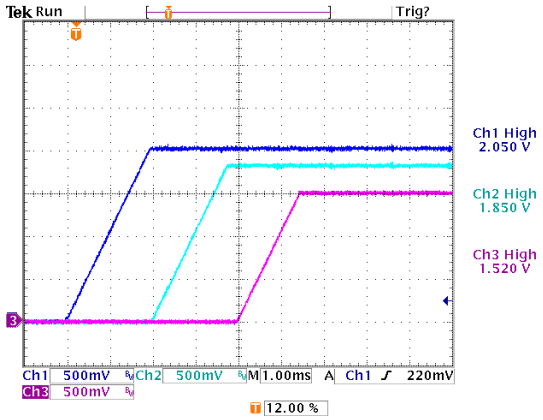
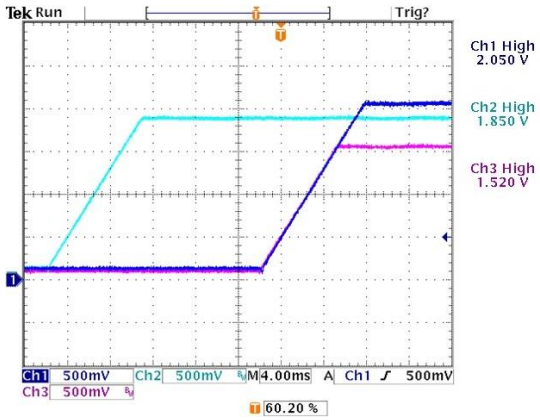


Figure 26. Two outputs delayed 5ms. All slew rates at 0.5V/ms.



6.3.3. Pre-Bias

In some applications, power may "leak" from a powered circuit to an unpowered bus, typically through ESD protection diodes. The d-pwer® controller in the dPOL holds off turn on its output until the desired ramp up point crosses the pre-bias point, as seen in Figure 27.

Figure 27. Turn On into Prebiased Load. V3 is Prebiased by V2 via a Diode.

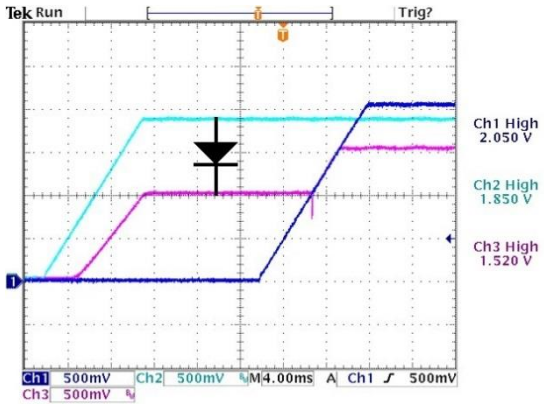


Figure 27 was captured with an actual system where a diode was added to pre-bias a 1.5V bus from a 1.85V bus in order to simulate the effect of current leakage through protection circuits of unpowered logic connected to powered logic outputs (a common source of pre-bias in power systems).

6.4. TURN-OFF CHARACTERISTICS

Turn of captures show that combining turn off delays and ramp rates. Note that while turnoff delays have a lower upper time limit as compared to turn on delays, all ramp down rates are available independently to turn on and off.

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Figure 28. Tracking Turn-Off. Falling Slew Rate is programmed at 0.5V/ms.

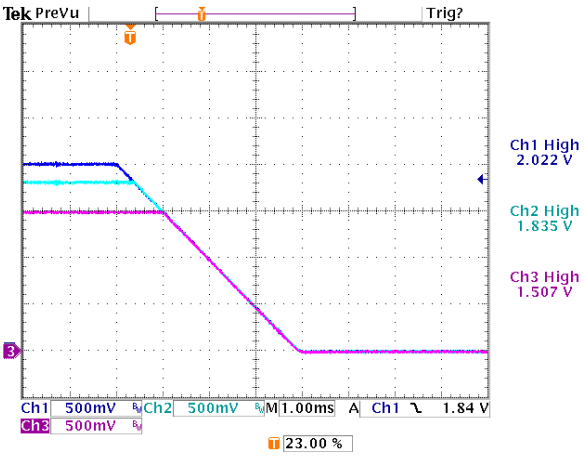
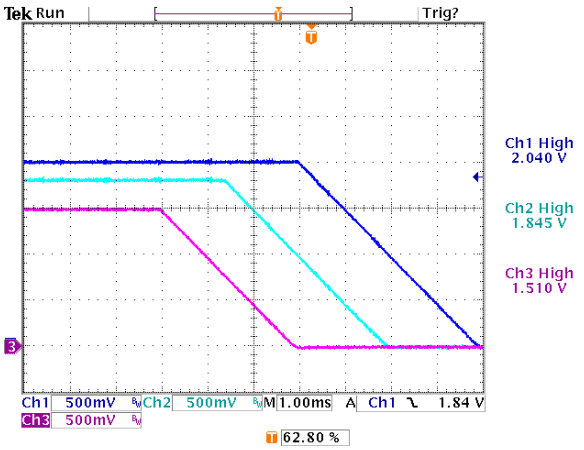


Figure 29. Turn-Off with Tracking and Sequencing. Falling Slew Rate is programmed at 0.5V/ms.



6.5. FAULTS, ERRORS AND WARNINGS

All dPOL series converters have a comprehensive set of programmable fault and error protection functions that can be classified into three groups based on their effect on system operation: warnings, faults, and errors. These are *warnings*, *errors* and *faults*. Warnings include Thermal (Overtemperature limit near) and Power Good (a warning in a negative sense.)

Faults in dP8xxx series POLs include overcurrent protection, overvoltage, overtemperature and tracking failure detection. Errors include only undervoltage. Control of responses to Faults and Errors are distributed between different dPOL registers and are configurable in the GUI.

Thresholds of overcurrent, over- and undervoltage detection, and Power Good limits can be programmed in the GUI Output Configuration window (Figure 13) or directly via the I²C bus by writing into the PC2 registers shown in Figure 30.

Figure 30. Protection Configuration Register PC2

PC2: Protection Configuration Register 2 [1)]
Address: 0x01

U	U	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
---	---	**PGHL**	**PGLL**	**OVPL1**	**OVPL0**	**UVPL1**	**UVPL0**
Bit 7							Bit 0

Bit7:6	**Unimplemented**: read as '0'
Bit 5	**PGHL**: Power Good High Level 1 = 105% of Vo 0 = 110% of Vo (default)
Bit 4	**PGLL**: Power Good Low Level 1 = 95% of Vo 0 = 90% of Vo (default)
Bit 3:2	**OVPL**: Over Voltage Protection Level 00 = 110% of Vo 01 = 120% of Vo 10 = 130% of Vo (default) 11 = 130% of Vo
Bit 1:0	**UVPL**: Under Voltage Protection Level 00 = 75% of Vo (default) 01 = 80% of Vo 10 = 85% of Vo 11 = 90% of Vo

[1)] This register can only be written when PWM is not active (RUN[RUN] is '0')

Note that the overvoltage and undervoltage protection thresholds and Power Good limits are defined as percentages of the output voltage. Therefore, the absolute levels of the thresholds change when the output voltage setpoint is changed either by output voltage adjustment or by margining.
Overcurrent limits are set either in the GUI POL Output configuration dialog or in the POL's CLS register as shown in Figure 31.
Note that the CLS register includes bits which control the Regulation option settings. When writing into this register be careful to not change Regulation by accident.

Figure 31. Current Limit Setpoint Register CLS

CLS: Current Limit Setting
Address: 0x08

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1
LR2	**LR1**	**LR0**	**TCE**	**CL3**	**CL2**	**CL1**	**CL0**
Bit 7							Bit 0

Bit 7:5	**LR[2:0]**: Load Regulation setting 0 = 0 V/A/Ω (default) 1 = 0.39 V/A/Ω 2 = 0.78 V/A/Ω 3 = 1.18 V/A/Ω 4 = 1.57 V/A/Ω 5 = 1.96 V/A/Ω 6 = 2.35 V/A/Ω 7 = 2.75 V/A/Ω
Bit 4	**TCE**: Temperature Compensation for Current Limitation Enable 0 = disabled 1 = enabled (default)
Bit 3:0	**CLS[3:0]**: Current Limit set-point when Vo Stationary or Falling 0x0 = 37% 0x1 = 47% … 0xB = 140% (default) values higher than 0xB are translated to 0xB (140%)

6.5.1. Warnings

This group includes Overtemperature Warning and Power Good Signal. Warnings do not turn off dPOLs but rather generate signals that can be transmitted to a host controller via the I^2C bus.

6.5.1.1. Overtemperature Warning

The Overtemperature Warning is generated when temperature of the controller exceeds 120°C. The Overtemperature Warning changes the TW bit of the status register ST. When the temperature falls below 117°C, the PT bit is cleared and the Overtemperature Warning is removed.

6.5.1.2. Power Good

Power Good (PG) is an open collector output that is pulled low, if the output voltage is outside of the Power Good window. The window is formed by the Power Good High threshold that is programmable at 105 or 110% of the output voltage and the Power Good Low threshold that can be programmed at 90 or 95% of the output voltage.
Power Good protection is only enabled after the output voltage reaches its steady state level. A programmable delay can be set between 0 and 150ms to delay the release of the PG pin after the voltage has reached the steady state level (see Figure 18). This allows using the PG pin to reset load circuits properly. The Power Good protection remains active during margining voltage transitions. The threshold will vary proportionally to the voltage change (see Figure 32).
The Power Good Warning pulls the PG pin low and changes the PG bit of the status register ST to 0. When the output voltage returns within the Power Good window, the PG pin is released high, the PG bit is cleared and the Power Good

Warning is removed. The Power Good pin can also be pulled low by an external circuit to initiate the Power Good Warning.
At turn-off the PG pin can be programmed to either be pulled low immediately following the turn-off command, or then when the voltage actually starts to ramp down (Reset vs. Power Good functionality in Figure 18).

NOTE: To retrieve status information, Status Monitoring in the GUI DPM Configure Devices window should be enabled (refer to Digital Power Manager Data Sheet). The DPM will retrieve the status information from each dPOL on a continuous basis.

6.5.2. Faults

This group includes overcurrent, overtemperature, undervoltage, and tracking protections. Triggering any protection in this group will turn off the dPOL.

6.5.2.1. Overcurrent Protection

Overcurrent protection is active whenever the output voltage of the dPOL exceeds the prebias voltage (if any). When the output current reaches the OC threshold, the POL control chip asserts an OC fault. The dPOL sets the OC bit in the register ST to 0. Both high side and low side switches of the dPOL are turned off instantly (fast turn-off).
Current sensing is across the dPOLs choke. To compensate for copper winding T_C, compensation is added to keep the OC threshold approximately constant at temperatures above room temperature. Note that the temperature compensation can be disabled in the dPOL Configure Output window or directly via the I^2C by writing into the CLS register. However, it is recommended to keep the temperature compensation enabled.

6.5.2.2. Undervoltage Protection

The undervoltage protection is only active during steady state operation of the dPOL to prevent nuisance tripping. If the output voltage decreases below the UV threshold and there is no OC fault, the UV fault signal is generated, the dPOL turns off, and the UV bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

6.5.2.3. Overtemperature Protection

Overtemperature protection is active whenever the dPOL is powered up. If temperature of the controller exceeds 120°C, the OT fault is generated, dPOL turns off, and the OT bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).
If non-latching OTP is programmed, the dPOL will restart as soon as the temperature of the controller decreases below the Overtemperature Warning threshold of 110°C.

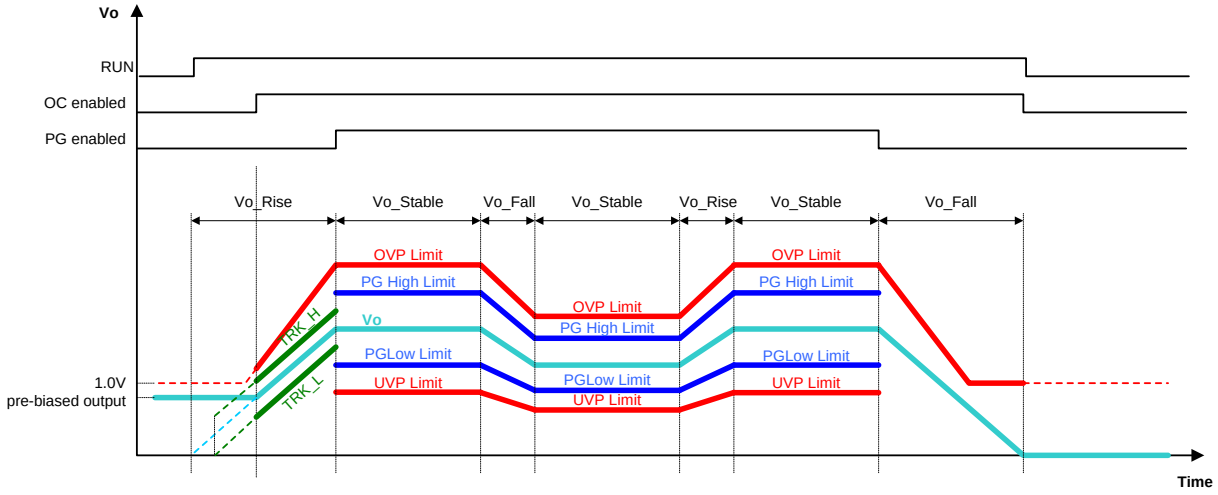
6.5.2.4. Tracking Protection

Ramp up and down operations are under control by the dPOL. Tracking protection, however, is active only when the output voltage is ramping up. The purpose of the protection is to ensure that the voltage differential between multiple rails being tracked does not exceed 250mV. This protection eliminates the need for external clamping diodes between different voltage rails which are frequently recommended by ASIC manufacturers.
When the tracking protection is enabled, the dPOL continuously compares actual value of the output voltage to its programmed value as defined by the output voltage and its rising slew rate. If absolute value of the difference exceeds 250mV, the tracking fault signal is generated, the dPOL turns off, and the TR bit in the register ST is changed to 0. Both high side and low side switches of the dPOL are turned off instantly (fast turn-off).
The tracking protection can be disabled, if it contradicts requirements of a particular system (for example turning into high capacitive load where rising slew rate is not important). It can be disabled in the dPOL Configure Fault window or directly via the I^2C bus by writing into the PC1 register.

6.5.3. Faults and Margining

As noted earlier, UV and OV protection settings are a percentage of Vout. As Vout ramps between nominal, low or high margin values, UVP and OVP limits adjust accordingly. This is illustrated in Figure 32. The middle plot of Vo (Vout) level is the result of a Low Margining command. Note that Tracking is not re-enabled during changes to Vout from margining commands.

Figure 32. Protection Enable Conditions



6.5.4. Errors

This protection group includes only overvoltage protection.

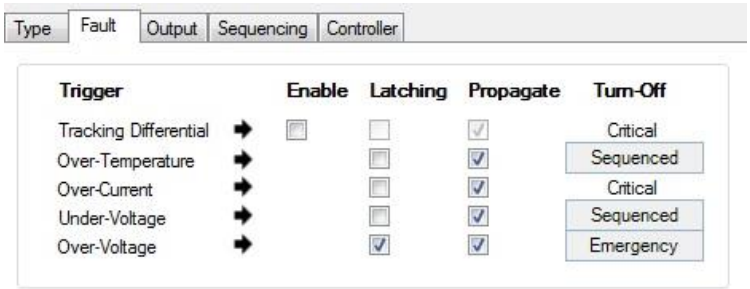
6.5.4.1. Overvoltage Protection

The overvoltage protection is active whenever the output voltage of the dPOL exceeds the pre-bias voltage (if any). If the output voltage exceeds the overvoltage protection threshold, the overvoltage error signal is generated, the dPOL turns off, and the OV bit in the register ST is changed to 0. The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads. The low side switch provides low impedance path to quickly dissipate energy stored in the output filter and achieve effective voltage limitation. The OV threshold can be programmed from 110% to 130% of the output voltage setpoint, but not lower than 0.5V. Also the OV threshold will always be at least 0.25V above the setpoint.

6.5.5. Fault and Error Latching

The user has the option of setting up any protection option as either latching/non-latching and propagating or non-propagating.
Propagation and Latching for each POL is set in the GUI (Figure 33 below) or directly via the I²C by writing into the PC1 register shown in Figure 34.

Figure 33. GUI dPOL Fault Propagation Option Window



If the non-latching protection is selected, a dPOL will attempt to restart every 130ms until the condition that triggered the protection is removed. When restarting, the output voltages follow tracking and sequencing settings.
If the latching type is selected, a dPOL will turn off and stay off. The dPOL can be turned on after 130ms, if the condition that caused the fault is removed and the respective bit in the ST register was cleared, or the Turn On command was recycled, or the input voltage was recycled.

Figure 34. Protection Configuration Register PC1

PC1: Protection Configuration Register 1
Address: 0x00

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
TRE	**PVE**	**TRC**	**OTC**	**OCC**	**UVC**	**OVC**	**PVC**
Bit 7							Bit 0

Bit 7 **TRE**: Tracking fault enable
1 = enabled
0 = disabled

Bit 6 **PVE**: Phase voltage error enable
1 = enabled
0 = disabled

Bit 5 **TRC**: Tracking Fault Protection Configuration
1 = latching
0 = non-latching

Bit 4 **OTC**: Over Temperature Protection Configuration
1 = latching
0 = non-latching

Bit 3 **OCC**: Over Current Protection Configuration
1 = latching
0 = non- latching

Bit 2 **UVC**: Under Voltage Protection Configuration
1 = latching
0 = non- latching

Bit 1 **OVC**: Over Voltage Protection Configuration
1 = latching
0 = non- latching

Bit 0 **PVC**: Phase Voltage Protection Configuration
1 = latching
0 = non- latching

6.5.6. Fault and Error Turn Off Control

In the GUI dPOL Fault dialog is a column of spin controls which set the Turn-Off style OT, UV and OV events. The choices are defined as:

Sequenced: Outputs shut down according to ramp down rate control settings. This is the method used when a dPOL is told to do a normal, controlled shut down.

Critical: Both high side and low side switches of the dPOL are turned off instantly.

Emergency: The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads.

6.5.7. Fault and Error Status

Status of dPOL protection logic is stored in the dPOL's ST register shown in Figure 35.
When Status monitoring is enabled for a group, the DPM will read this register and make the information available for uses such as GUI Monitor display.

Figure 35. Protection Status Register ST

ST: Status register
Address: 0x16

R-1	R-0	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]
TW	**PG**	**TR**	**OT**	**OC**	**UV**	**OV**	**PV**
Bit 7							Bit 0

Bit 7 **TW**: Temperature Warning
Bit 6 **PG**: Power Good Warning (high and low)
Bit 5 **TR**: Tracking Fault
Bit 4 **OT**: Over Temperature Fault
Bit 3 **OC**: Over Current Fault
Bit 2 **UV**: Under Voltage Fault
Bit 1 **OV**: Over Voltage Error
Bit 0 **PV**: Reserved
Note: an activated fault is encoded as '0'
1) Writing a '1' into a fault/error bit clears a latching fault/error

6.5.8. Fault and Error Propagation

The feature adds flexibility to the fault management scheme by giving users control over propagation of fault signals within and outside of the system. The propagation means that a fault in one dPOL can be programmed to turn off other dPOLs and devices in the system, even if they are not directly affected by the fault.

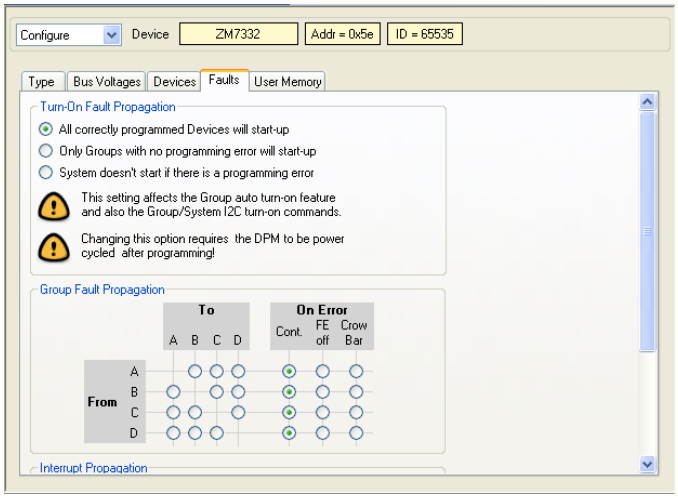
6.5.8.1. Fault Propagation

When propagation is enabled, a faulty dPOL propagates declaration of that even through pulling its OK pin low. This signals to the DPM and any other dPOL connected to that signal, that the dPOL has a Fault or Error condition. A low OK line initiates turn-off of other dPOLs connected to the same OK line with the same turn-off behavior as the faulty dPOL. The turn-off type is encoded into the OK line when it transitions from high to low.

6.5.8.2. Grouping of dPOLs

d-pwer® dPOLs can be arranged in groups of up to 4, 8, 16 or 32 dPOLs (depending upon the DPM model used). Membership in a group is set in the GUI in the **DPM / Configure / Devices** dialog, and implemented in hardware by connecting the OK pins of each dPOL in the group to the matching OK input on the DPM.
In order for a particular Fault or Error to propagate through the OK line to other groups, Propagation needs to be checked in the GUI dPOL **Configure / Fault** Management Window. shown in Figure 36.

Figure 36. DPM Configure Faults Window



Note that the turn-off type of the fault as it propagates through the DPM will remain unchanged. Propagation options for dPOLs can be read or set in the dPOL PC3 register shown in Figure 37.

Figure 37. Protection Configuration Register PC3

PC3: Protection Configuration Register 3
Address: 0x02

U	U	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
---	---	**TRP**	**OTP**	**OCP**	**UVP**	**OVP**	**PVP**
Bit 7							Bit 0

Bit 7:6	**Unimplemented**: Read as '0'
Bit 5	**TRP**: Tracking Protection Propagation 0 = disabled 1 = enabled
Bit 4	**OTP**: Over Temperature Protection Propagation 0 = disabled 1 = enabled
Bit 3	**OCP**: Over Current Protection Propagation 0 = disabled 1 = enabled
Bit 2	**UVP**: Under Voltage Protection Propagation 0 = disabled 1 = enabled
Bit 1	**OVP**: Over Voltage Protection Propagation 0 = disabled 1 = enabled
Bit 0	**PVP**: Reserved

6.5.9. Front End and Crowbar

As shown in the propagation dialog, if an error is propagated, the DPM can be configured to generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) or trigger crowbar protection to accelerate removal of the IBV voltage. (The two options are independent of inter-group propagation, and may require some external hardware to interface to the front end supply or crow-bar SCR device.)

6.5.10. Propagation Examples

Understanding Fault and Error propagation is easier with the following examples.
The First example is of non-propagation from a dPOL, as shown in Figure 38. An undervoltage error shuts down the Vo, but since propagation was not enabled, OK-A is not pulled down and Vo2 stays up.

Figure 38. No Group Fault Propagation

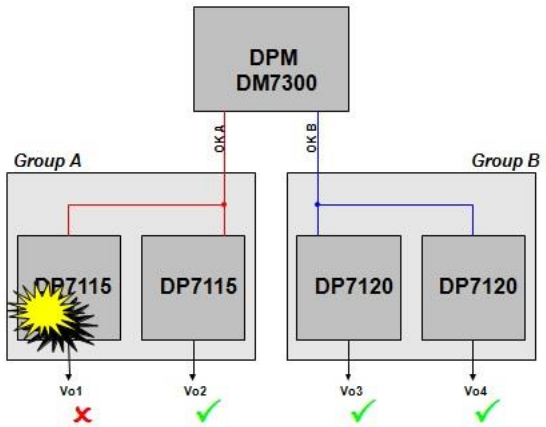


Figure 39. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching. Ch1 – Vo1, Ch2 – Vo2 (Group A), Ch3 Vo3 (Group B) Vo4 not shown.

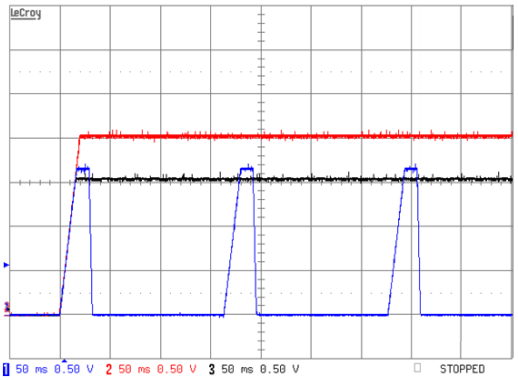


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Figure 39 shows a scope capture an actual system when undervoltage error detection is set to not propagate.

In this example, the dPOL connected to scope Ch 1 encounters the undervoltage fault after turn-on. Because fault propagation is not enabled for this POL, it alone turns off and generates the UV fault signal. Because a UV fault triggers the sequenced turn-off, the dPOL meets its turn-off delay and falling slew rate settings during the turn-off process as shown in the trace for Ch1. Since the UV fault is programmed to be non-latching, the dPOL will attempt to restart every 130 ms, repeating the process described above until the condition causing the undervoltage is removed. The 130ms hiccup interval is guaranteed regardless of the turn-off delay setting.

The next example is intra-group propagation, the dPOL propagates its fault or error events. Here fault propagation between POLs is enabled.

In Figure 40 the dPOL powering output Vo1 again encounters an undervoltage error. It pulls its OK line low. Since the dPOL powering output Vo2 (Ch3 in the picture) belongs to the same group (A in this case), pulling down OK-A tells that dPOL to execute a regular turn-off.

Figure 40. Intra Group Fault Propagation

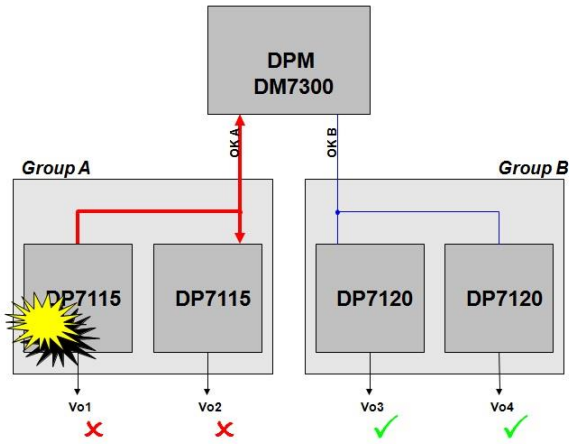
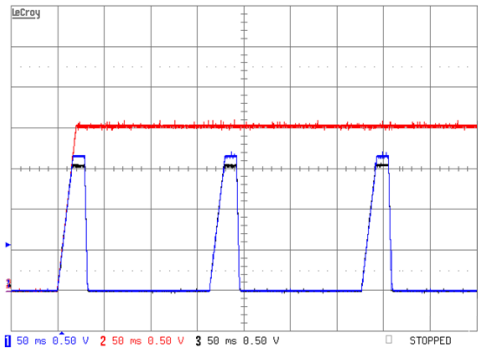


Figure 41. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching and Propagate From Group C to Group A. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)



Since both Vo1 and Vo2 have the same delay and slew rate settings they will continue to turn off and on synchronously every 130ms as shown in Figure 41 until the condition causing the undervoltage is removed.

Note that the dPOL powering the output Vo2 (Ch3) actually reaches its voltage set point before the error in Vo1 is detected.

The turn-off type of a POL fault/error as propagated by the faulty dPOL via the OK line is propagated through the DPM to other dPOLs connected to other Groups through its connection to their OK line or lines.

This behavior assures that all dPOLs configured to be affected through Group linkages will switch off with the same turn-off type.

6.5.11. Protection Summary

A summary of protection support, their parameters and features are shown in Table 2.

Table 2. Summary of Protection Parameters and Features

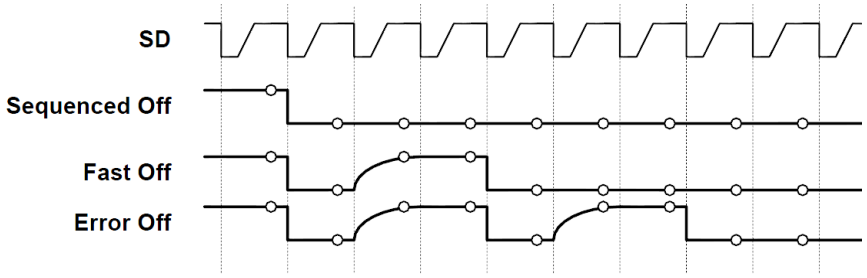
CODE	NAME	TYPE	WHEN ACTIVE	TURN OFF	LOW SIDE SWITCH	PROPAGATION	DISABLE
TW	Temperature Warning	Warning	Whenever V_{IN} is applied	No	N/A	Status Bit	No
PG	Power Good	Warning	During steady state	No	N/A	PG	No
TR	Tracking	Fault	During ramp up	Fast	Off	Critical	Yes
OT	Overtemperature	Fault	Whenever V_{IN} is applied	Regular	Off	Sequenced or Critical	No
OC	Overcurrent	Fault	When V_{OUT} exceeds prebias	Fast	Off	Critical	No
UV	Undervoltage	Fault	During steady state	Regular	Off	Sequenced or Critical	No
OV	Overvoltage	Error	When V_{OUT} exceeds prebias	Fast	On	Critical or Emergency	No

6.6. OK FAULT AND ERROR CODING

d-pwer® dPOLs have an additional functionality added to the OK line signal. The OK line is used to propagate and receive information from other devices in the power system belonging to the same group as to the kind of turn-off procedure a device has initiated because of a fault.

Figure 42 shows the three types of OK encoding. The bubbles show when the SD and OK line logic levels are sampled by dPOL and DPM logic.

Figure 42. OK Severity Encoding Waveforms



Note that the OK line state changes are always executed by dPOLs at the negative edge of the SD line.

The chart shows shut down response types as the user can select the kind of response desired for each type of Fault or Error (within the limits of choice provided for each type of Fault or Error) .All dPOL devices in the same Group are expected to trigger the same turn-off procedure in order to maintain overall tracking of output voltages in the system. And when fault propagation is set to go from one group to another, the encoding is passed along un-changed.

6.7. SWITCHING AND COMPENSATION

d-pwer® dPOLs utilize the digital PWM controller. The controller enables users to program most of the performance parameters, such as switching frequency, PWM duty cycle and limiting, interleave, and feedback loop compensation.

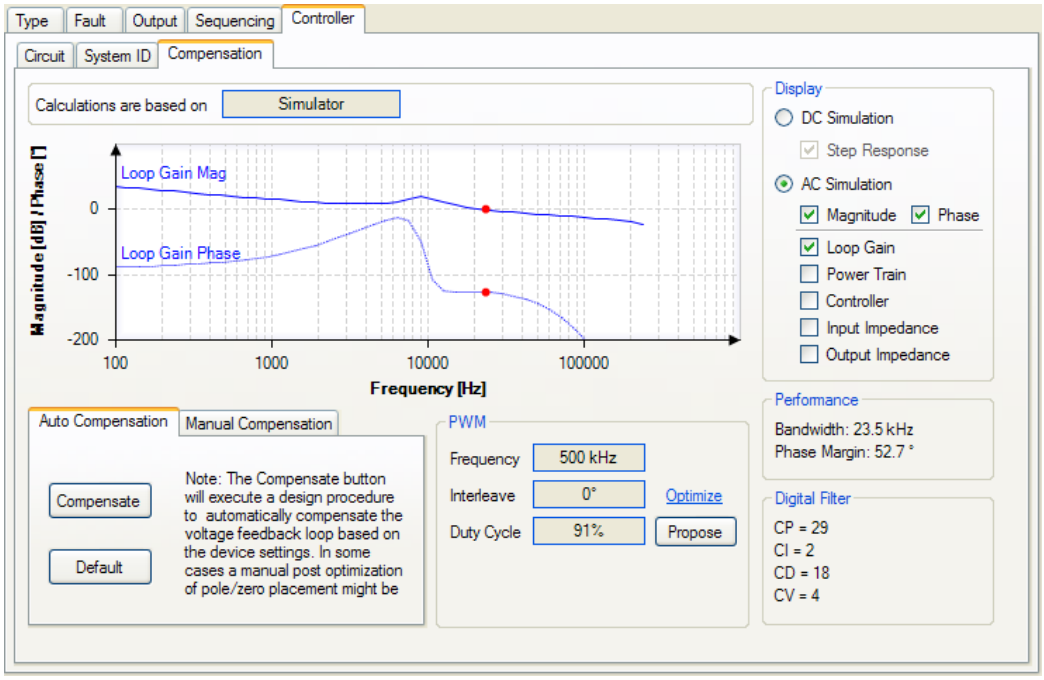
6.7.1. Switching Frequency

The switching frequency of the DP8120G can be programmed to either 500KHz or 1MHz in the GUI PWM Controller window shown in Figure 43 or directly via the I^2C bus by writing into the INT register shown in Figure 44.

Each dPOL is equipped with a PLL that locks to the 500 KHzSD signal which is generated by the DPM. This sets up for switching actions to be synchronous to the falling edge of SD by all dPOLs, which are thereby kept coordinated to each other.

Although synchronized to SD, switching frequency selection is independent for each dPOL, with the exception of shared load bus groups, where dPOLs attached to a shared load bus are forced to use the same frequency by the GUI.

Figure 43. PWM Controller Window



In some applications, switching at higher frequencies is desirable because it allows for better transient response. This tends to be true of applications where the output filter capacitance is low.

6.7.2. Interleave Selection

Within the same PWM dialog is the switching Interleave control. Interleave is defined as a phase delay between the synchronizing slope of the master clock on the SD pin and the start of each dPOL PWM cycle. This parameter can be programmed in the dPOL Controller Configure Compensation window or directly via the I²C bus by writing into the INT register in 22.5° steps.

Figure 44. Interleave Configuration Register INT

INT: Interleave Configuration
Address: 0x04

R	R	R/W-0	U	R/W-0	R/W-0	R/W-0	R/W-0
PHS1	**PHS0**	**FRQ**	**---**	**INT3**	**INT2**	**INT1**	**INT0**
Bit 7							Bit 0

Bit 7:6	**PHS[1:0]**: Phase selection 0 = Single phase (PWM0) 1 = Dual phase (PWM0 and PWM2) 2 = Triple phase (PWM0, PWM1 and PWM2) 3 = Quad phase (PWM0, PWM1, PWM2 and PMW3)
Bit 5	**FRQ**: PWM frequency selection 0 = 500 kHz (default) 1 = 1000 kHz
Bit 4	**Unimplemented**: Read as '0'
Bit 3:0	**INT[3:0]**: PWM interleave phase with respect to SD line 0x00 = 0° phase lag 0x01 = 22.5° phase lag 0x02 = 45° phase lag … 0x1F = 337.5° phase lag

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6.7.3. Interleave and Input Bus Noise

When a dPOL turns on its high side switch there is an inrush of current. If no interleave is programmed, inrush current spikes from all dPOLs in the system reflect back into the input source at the same time, adding together as shown in Figure 45.

Figure 45. Input Voltage Noise, No Interleave

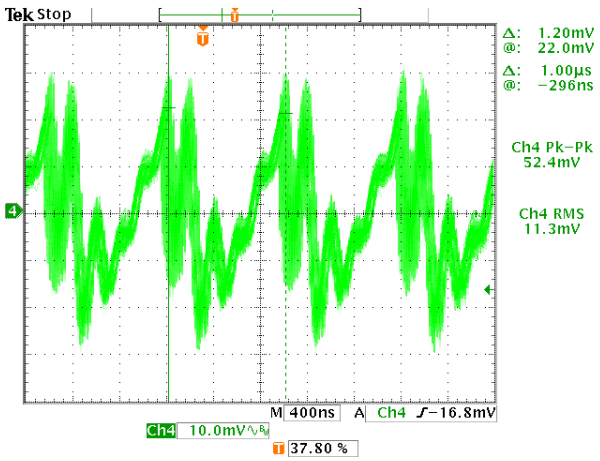


Figure 46. Input Voltage Noise with Interleave

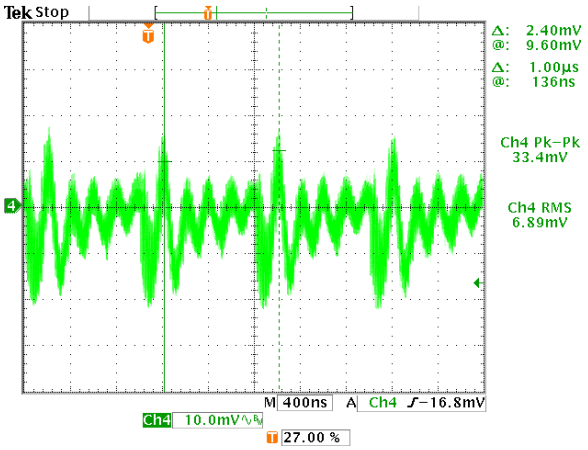


Figure 46 shows the input voltage noise of the three-output system with programmed interleave. Instead of all three dPOLs switching at the same time as in the previous example, the switching cycle of dPOLs V1, V2, and V3 start at 67.5°, 180°, and 303.75° of phase delay, respectively. Noise is spread evenly across the switching cycle resulting in more than 1.5 times reduction.

6.7.4. Interleave and Current Sharing Noise

Similar noise reduction can be achieved on the output of dPOLs connected in parallel. Figure 47 and Figure 48 show the output noise of two dPOLs connected in parallel without and with a 180° interleave, respectively. Resulting noise reduction is more than 2 times and is equivalent to doubling switching frequency or adding extra capacitance on the output of the dPOLs.

Figure 47. Output Voltage Noise, Full Load, No Interleave

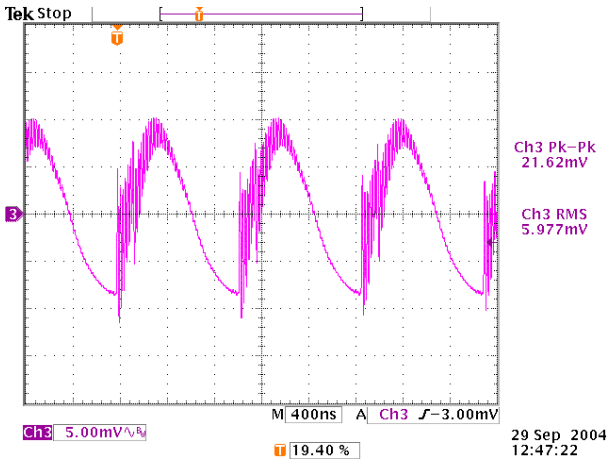
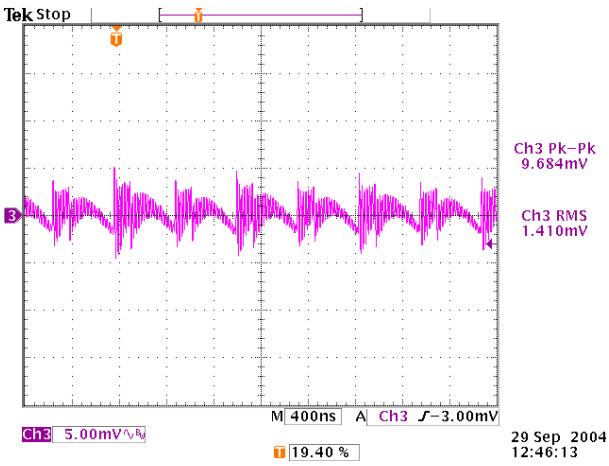


Figure 48. Output Voltage Noise, Full Load, 180° Interleave



6.7.5. Duty Cycle Limit

The DP8120G is a step-down converter therefore V_{OUT} is always less than V_{IN}. The relationship between the two parameters is characterized by the duty cycle and can be estimated from the following equation:

$$DC = \frac{V_{OUT}}{V_{IN.MIN}},$$

Where, DC is the duty cycle, V_{OUT} is the required maximum output voltage (including margining), $V_{IN.MIN}$ is the minimum input voltage.
The dPOL controller sets PWM duty cycle higher or lower than the above to compensate for drive train losses or to pull excess charge out of the output filter to keep the output voltage where it is supposed to be.
A side effect of PWM duty cycle is it also sets the rate of change of current into the output filter. A high limit helps deal with transients. However, if this is too high, an overcurrent alarm can be tripped. Thus DC limiting must be a compromise between supplying drive train losses and avoiding nuisance trips from transient load responses.
The duty cycle limit can be programmed in the GUI PWM Controller window Figure 43 or directly via the I²C bus by writing into the DCL register shown in Figure 49.

Figure 49. Duty Cycle Limit Register

DCL: Duty Cycle Limitation
Address: 0x09

R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	U	U
DCL5	**DCL4**	**DCL3**	**DCL2**	**DCL1**	**DCL0**	**---**	**---**
Bit 7							Bit 0

Bit 7:2	**DCL[5:0]**: Duty Cycle Limitation 0x00 = 0 0x01 = 1/64 0x02 = 2/64 … 0x1F = 63/64
Bit 1:0	**Unimplemented**: Read as '0'

Programming feedback loop compensation allows optimizing dPOL performance for various application conditions. For example, increase in bandwidth can significantly improve dynamic response.
The dPOL implements a programmable PID (Proportional, Integral, and Derivative) digital controller to shape the open loop transfer function for desired bandwidth, phase/gain margin.
Feedback loop compensation can be programmed in the GUI PWM Controller window by setting Kr (Proportional), Ti (Integral), Td (Derivative), and Tv (Derivative roll-off) parameters or directly writing into the respective registers (CP, CI, CD, B1). Note that the coefficient Kr and the timing parameters (Ti, Td, Tv) displayed in the GUI do not map directly to the register values. It is therefore strongly recommended to use only the GUI to set the compensation values.
The GUI offers 3 ways to compensate the feedback loop:

Auto-Compensation: The GUI will calculate compensation settings from either information entered as to output capacitors in the application circuit, or, if the SysID function has been run, the frequency response measured through the SysID function in the target dPOL. This method is usually sufficient, but is sensitive to accurate accounting of capacitor values and esr. The GUI displays the results of running Auto-Compensation as a set of graphs and compensation values.

Manual Compensation: The GUI supports manually adjusting feedback compensation parameters. As the parameters are changed the GUI recalculates expected frequency and phase performance.

System Identification (SysID) and Auto-Compensation: Hardware built into the dPOL controller that injects pseudo random bit sequence (PRBS) noise into PWM calculations and observes the response of the output voltage. The GUI collects this data and calculates actual system frequency response. Having frequency response data allows the Auto-Compensation function to have a better idea of actual output filter characteristics when it calculates feedback coefficients.

Using noise to plumb the output filter requires current values for compensation be good enough that injected signal can be extracted from system noise and the added noise does not trip a fault or error response. A moderately workable solution for compensation must be obtained by calculating from assumed system component values before invoking SysID.

6.8. TRANSIENT RESPONSE

The following figures show the deviation of the output voltage in response to alternating 25 and 75 % step loads applied at 2.5A/µs. The dPOL converter is switching at 500KHz and has 10 x 22µF ceramic capacitors connected across the output pins. Bandwidth of the feedback loop was optimized for slightly overdamped response.

Figure 50. Transient Response with Regulation set to 0.0 mV/A.

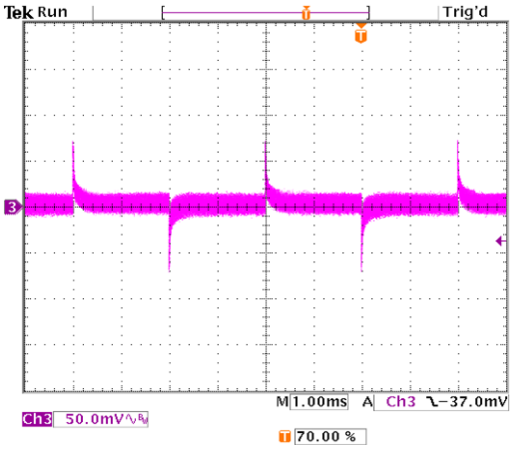
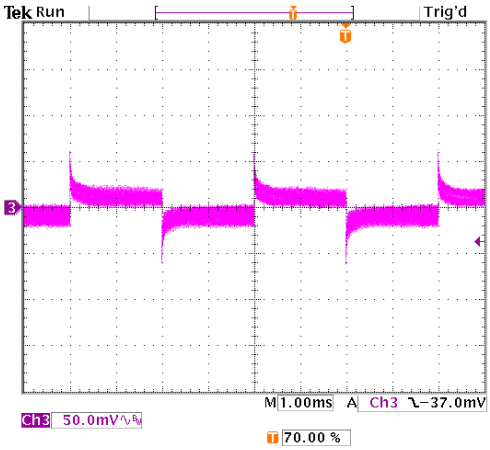


Figure 51. Transient Response with Regulation set to 0.74 mV/A



As noted earlier, increasing the Load Regulation parameter provides load dependant dynamic load positioning. This shows up in the following figure.

6.9. LOAD CURRENT SHARING

The DP7007 is equipped with a patented active digital current share function. Setting up for current sharing requires both hardware and software configuration actions.

To set up for the current sharing, interconnect the CS pins of the dPOLs that are to share the load in parallel. This pulse width modulated digital signal drives the output currents of all dPOLs to approximately the same level (the dominant, or master dPOL will tend to carry slightly more of the load than the others).

In addition to the CS interconnection, the DPM must be informed of the sharing configuration. This is done in the **DPM / Configure / Devices** window shown in Figure 53. Just to the right of each dPOL address, set the spin control to one of 10 possible sharing busses (the number is an accounting aid for firmware.)

The GUI automatically copies common parameters changed in one dPOL's setup information into all dPOLs connected to the parallel bus. Some parameters, such as load sharing, must be set independently.

6.9.1. CS and Regulation

Load Regulation is an important part of setting up two or more dPOLs to share load. The dPOL designated the "master" should have a lower Load Regulation setting than the other dPOL(s) connected to its sharing bus.

In operation, the negative CS duty cycle in each dPOL is proportional to the unit's load current. As the loading goes up, the negative period gets wider. A dPOL which sees CS duty greater than its internally calculated value will increase its output voltage to increase its load share.

Non-zero regulation, on the other hand, tends to lower output voltage as loading increases. It also tends to retard the calculated CS period. The effect of these two actions, regulation and CS tracking, cause the dPOL or dPOLS with higher regulation values to track the loading of the dPOL with a lower regulation value. The Load Regulation setting insures the master will carry a slightly higher share of the common load.

Load Regulation is set in the **Device / Configure / Output** dialog as noted earlier. Best sharing is done when the slave devices have two to three steps higher Load Regulation values. Less and sharing is slightly unstable (ripple noise increases), more regulation and sharing becomes much less equal. Note that the GUI does not automatically bump up regulation for dPOLs attached to the same regulation bus. This must be done by hand. Also, it is recommended that the dPOL closest to the biggest load element on the shared output bus be set up to act as the group's master.

6.9.2. CS and Interleave

Since shared busses tend to have relatively high currents, interleaving switching of shared bus dPOLs is generally desirable. The lowest noise generation is usually achieved when shared bus dPOL interleave phasing is set to approximately equally spaced intervals.

6.10. MONITORING

Along with status information, dPOL converters can monitor their own performance parameters such as output voltage, output current, and temperature.

The output voltage is measured at the output sense pins, output current is measured using the ESR of the output inductor and temperature is measured by the thermal sensor built into the controller IC. Output current readings are adjusted based on temperature readings to compensate for the change of ESR of the inductor with temperature.

A 12-Bit Analog to Digital Converter (ADC) converts the output voltage, output current, and temperature into a digital signal to be transmitted via the serial interface (12Bits for the Voltage, 8 Bits for the Current and Temperature).

Monitored parameters are stored in registers (VOM, IOM, and TMON) that are continuously updated in the DPM at a fixed refresh rate of 1sec. These monitoring values can be accessed via the I²C interface with high and low level commands as described in the “DPM Programming Manual”.

Shown in Figure 52 is a capture of the GUI System Monitor while operating the ZM7300 Evaluation board.

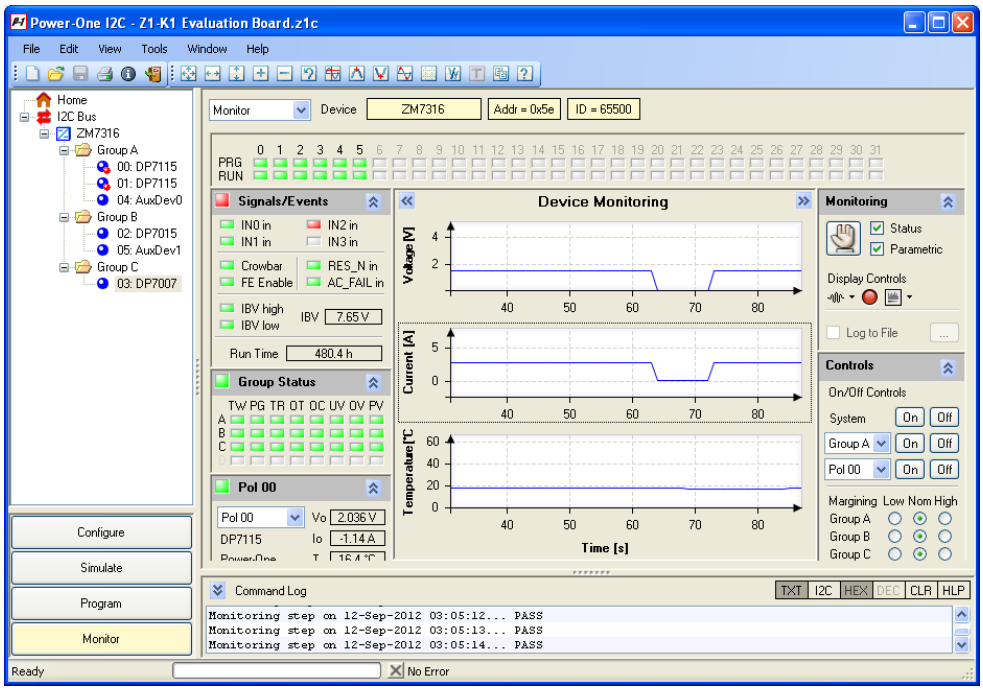
6.10.1. In System Monitoring

In system parametric and status monitoring is implemented through the I²C interface. The appropriate protocols are covered in the ZM7300 DPM Programming Manual. The GUI uses the published commands.

In writing software for I²C bus transactions, it is important to note that I²C responses are lower in priority in DPM operation than SD bus transactions. If an I²C transaction overlaps an SD bus transaction, the DPM will put the I²C bus on "hold" until it completes its SD activity. The GUI is aware of this and such delays are transparent.

When directly polling dPOLs for information, setting I²C bus timeouts too low can cause hangups where the DPM is waiting for the I²C master to complete a transaction and the master has timed out. To avoid such timeout related problems, set I²C interface timeout to greater than the time required for polling all dPOLs, or 150ms (whichever is greater). See the programming manual referenced above for the equation used to calculated worst case polling duration.

Figure 52. DPM Monitoring Window



7. ADDING DPOLS TO THE SYSTEM

dPOL converters are added to a d-pwer® system through the DPM Configuration/Devices dialog. Clicking on an empty address location brings up a menu which allows specifying which dPOL type is needed. Figure 53 below is an example of a typical d-pwer® system.

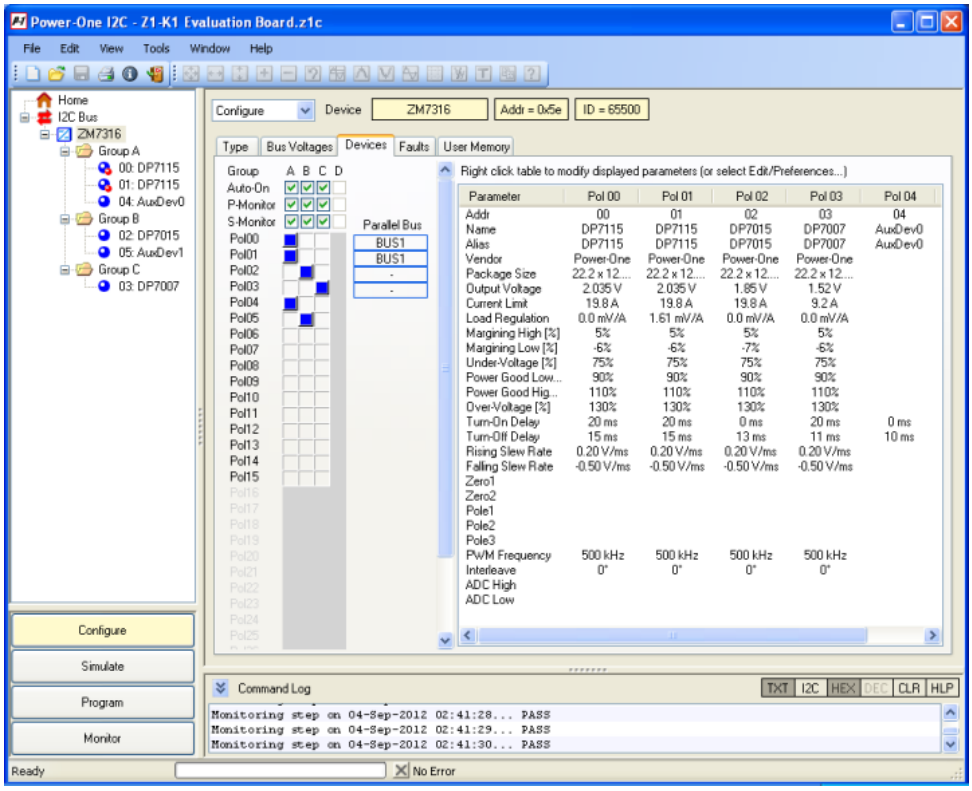
Note that Auto-On, P-Monitor and S-Monitor options are only configurable by Group, and not by individual dPOL configuration. These options affect only DPM behavior. Enabling them does not burden a dPOL.

Auto-On sets a group to turn on once all IBV power is available and dPOLs are configured.

P-Monitor enables periodic query of Vout, Iout and Temp values from each dPOL in the group where it is enabled (dPOLs will always measure these parameters in an ongoing basis even if Vout is not enabled.

S-Monitor enables periodic query of POL Status. While a DPM will always be able to detect a low OK condition, it requires this option enabled for Monitor function to query status registers.

Figure 53 Evaluation Board Configuration showing Current Share Bus Assignment



8. TESTING FAULT AND ERROR RESPONSE

Included in the architecture of d-pwer® dPOLs is a mechanism for simulating errors and faults. This allows the designer to test their response configuration without actually needing to induce the fault.

The Bel Power Solutions GUI supports this feature in the Monitor window when monitoring is active (See Figure 54). When monitoring is off, the Fault Injection control boxes are disabled and grayed out.

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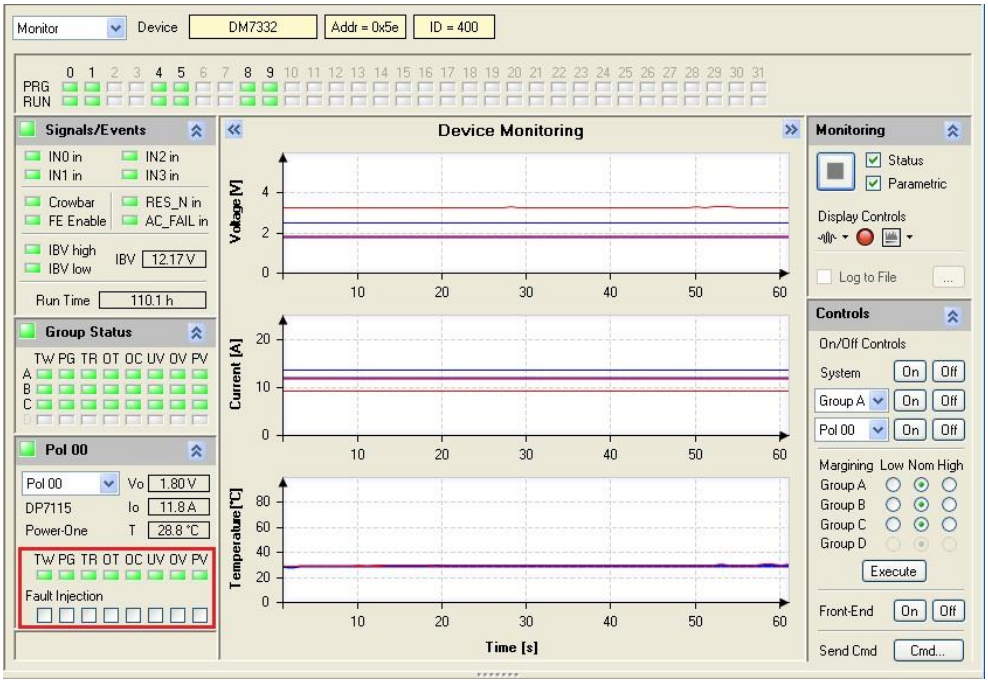
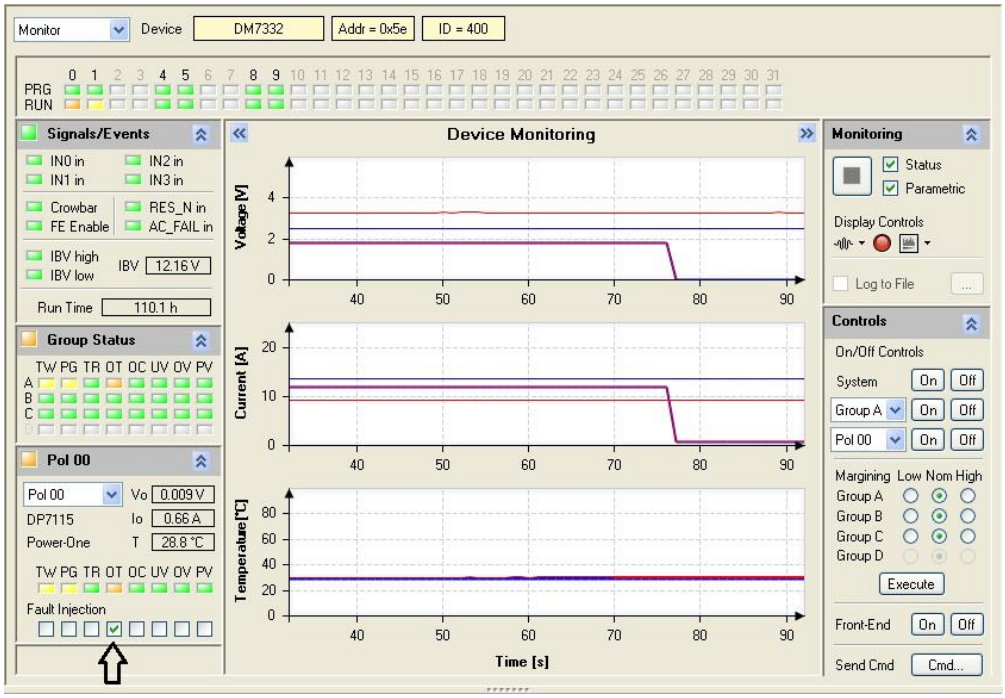
Figure 54. Fault Injection Controls In Monitor Window



Fault injection into a dPOL requires selecting that dPOL in the POL status dialog in the left column of the Monitoring dialog window. As long as the checkbox is checked, the fault trigger is present in the dPOL. An injected fault is handle by the dPOL in the same fashion as an actual fault. It therefore gets propagated to the other dPOLs / Groups and shuts down in the programmed way the dPOL/Group/System as programmed for that fault.

Figure 55. Example Overtemp Fault Injection in the GUI



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In Figure 55 we see the effects of injecting an Overtemp (OT) fault. Note that dPOL-0 shows an OT fault. dPOL-0 and -1 are in the same Group and fault propagation for the dPOL is to propagate to the group. dPOL -4 and above are in Groups B and C. Propagation is not enabled from Group A to B.

The OT fault shows up as an orange indicator in the dPOL and RUN status LEDs. Group LEDs show yellow, indicating all of the members of the group have shut down.

Fault recovery depends whether the fault is a latching or non-latching fault:

A non-latching fault is cleared by unchecking the checkbox (clears the fault trigger). The dPOL will re-start after the 130ms time out of non-latching faults (hiccup time) (Group and System follows restart).

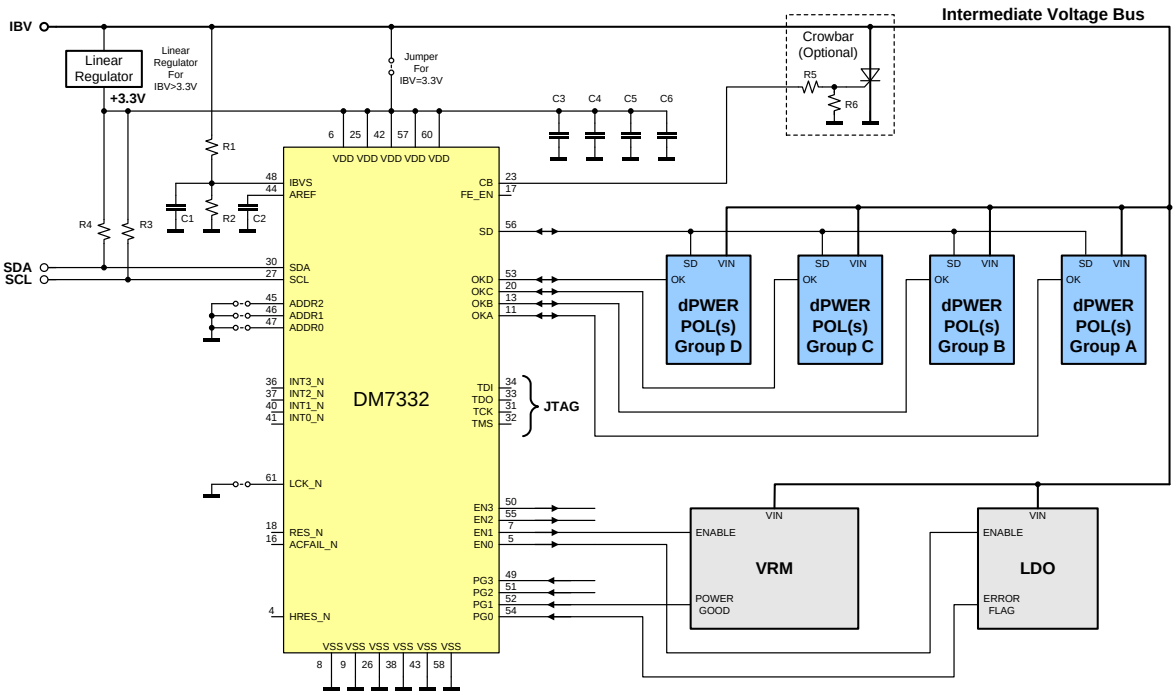
Latching faults clear in one of two ways. The first method is to clear the fault trigger (uncheck the checkbox) (note: the dPOL remains off since the fault is latching).

Alternately, a latched fault can be cleared by toggling the EN pin or by commanding the dPOL to turn-off and turn-off again via the GUI interface (obviously more convenient). Therefore, once the fault trigger is cleared, click the “Off” button of the dPOL or Group (clears the fault, status LEDs turn back to green) and then the “On” button of the dPOL or Group to re-enable it.

9. APPLICATION

Shown in Figure 56 is a block diagram of a multiple dPOL power system. The key interconnections needed between the DPM and the dPOLs are Intermediate Voltage Bus (IBV), SD, OK (A - D), and, between the first two dPOLs which share a bus load, their CS connections. Each dPOL has its own output bulk filter capacitors. This illustrates how simple a dPOL based system is to implement in hardware. SD provides synchronization of all dPOLs as well as communication. PG, not shown, is optional, though this is usually used with auxiliary power supplies that are not digitally controlled.

Figure 56. Multi-dPOL Power System Diagram



Shown in Figure 57 is a more detailed schematic of a typical application using a DM7300 series Digital Power Manager (DPM) and at least one DP8120G point-of-load converter (dPOL). Additional d-pwer® series dPOLs may be connected (Note SD and OK dashed lines "TO OTHER dPOLS"). As noted earlier, OK connections are determined by which group a given dPOL is assigned to in the user's application.

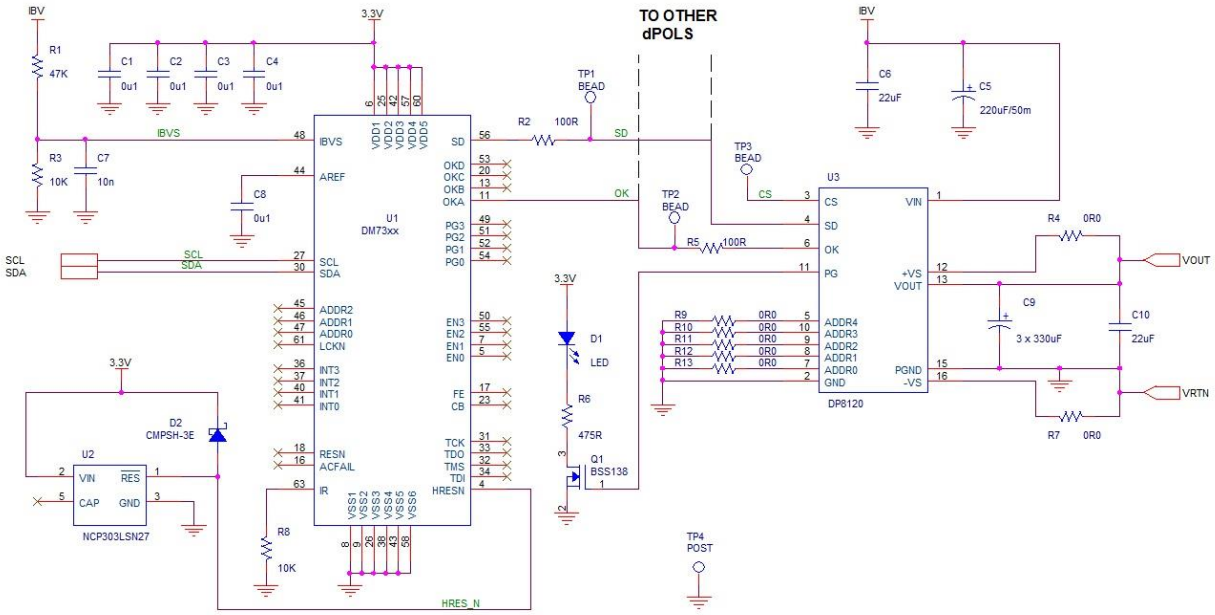
In this case the DP8120G is connected to OK-A. Shown connected to the dP8120G OK pin is an optional low value resistor helpful in some cases for fault isolation.

The type, value, and the number of output capacitors shown in the schematic are required to meet the specifications published in the data sheet. However, all d-pwer® dPOLs are fully operational with different configurations of output capacitors. The supervisory reset circuit in the above diagram, U2, is recommended for systems where the 3.3V supply to the DPM does not turn on faster than 0.5 V/ms.

The DPM does require some passive components which are located close to that part but not shown in the diagram above.

Note: The DP8120G is footprint compatible with the **ZY**8120—No change in PCB is needed to upgrade to d-pwer® parts. However, configuration data must be altered through the I²C GUI and programmed into the DPM. When upgrading to d-pwer®, *mixing ZY and DP series parts is not recommended. All parts must be upgraded*.

Figure 57. Typical Application with Digital Power Manager and I2C Interface



10. SAFETY

The DP8120G dPOL converters **do not provide isolation** from input to output. The input devices powering DP8120G must provide relevant isolation requirements according to all IEC60950 based standards. Nevertheless, if the system using the converter needs to receive safety agency approval, certain rules must be followed in the design of the system. In particular, all of the creepage and clearance requirements of the end-use safety requirements must be observed. These requirements are included in UL60950 - CSA60950-00 and EN60950, although specific applications may have other or additional requirements.

The DP8120G dPOL converters have no internal fuse. If required, the external fuse needs to be provided to protect the converter from catastrophic failure. Refer to the “Input Fuse Selection for DC/DC converters” application note on www.belpowersolutions.com for proper selection of the input fuse. Both input traces and the chassis ground trace (if applicable) must be capable of conducting a current of 1.5 times the value of the fuse without opening. The fuse must not be placed in the grounded input line.

Abnormal and component failure tests were conducted with the dPOL input protected by a fast-acting 65 V, 15 A, fuse. If a fuse rated greater than 15A is used, additional testing may be required.

In order for the output of the DP8120G dPOL converter to be considered as SELV (Safety Extra Low Voltage), according to all IEC60950 based standards, the input to the dPOL needs to be supplied by an isolated secondary source providing a SELV also.

11. ENVIRONMENTAL

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Ambient Temperature Range		-40		85	°C
Storage Temperature (Ts)		-55		125	°C
MTBF	Calculated Per Telcordia Technologies SR-332	6.24			MHrs
Peak Reflow Temperature	DP8120G		245	260	°C
Lead Plating	DP8120G		100% Matte Tin		
Moisture Sensitivity Level	DP8120G		3		

12. MECHANICAL DRAWINGS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Dimensions	Width	40.35	40.6	40.85	mm
	Height	24.75	25	25.25	
	Depth		10.4		
Weight			15		g

Figure 58. Mechanical Drawing

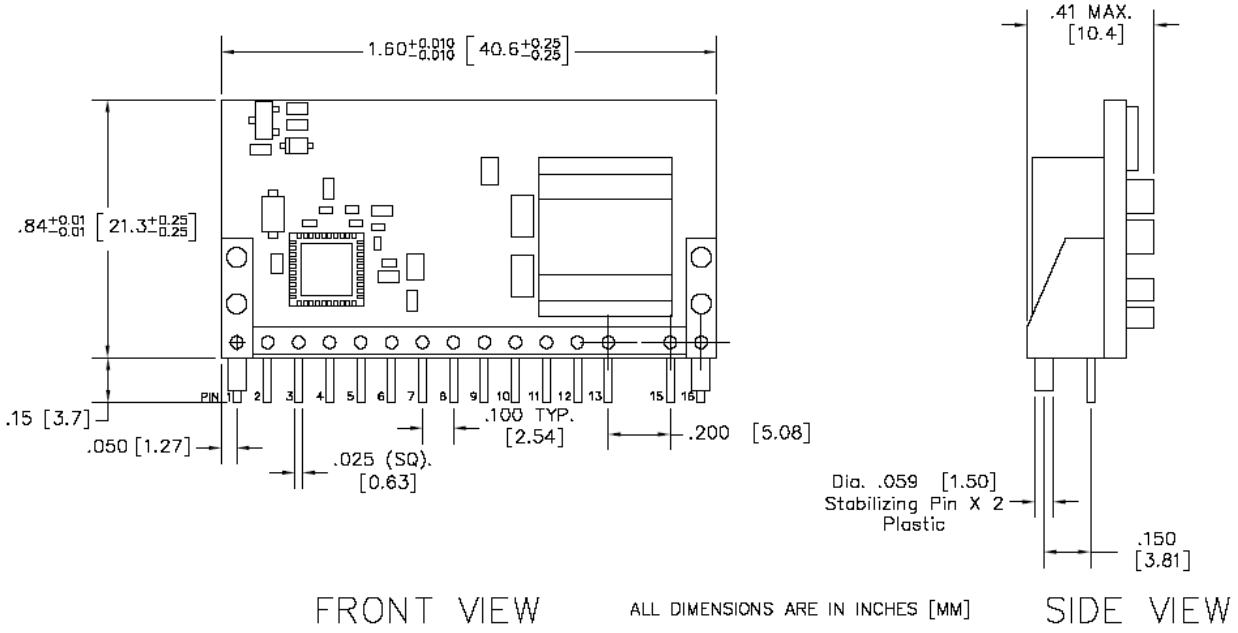


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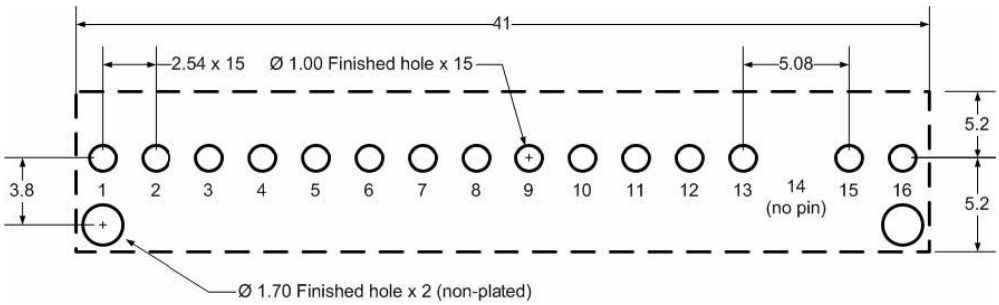
Figure 59. Pinout Diagram (Bottom View)



Note: I²C is a trademark of Philips Corporation.

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