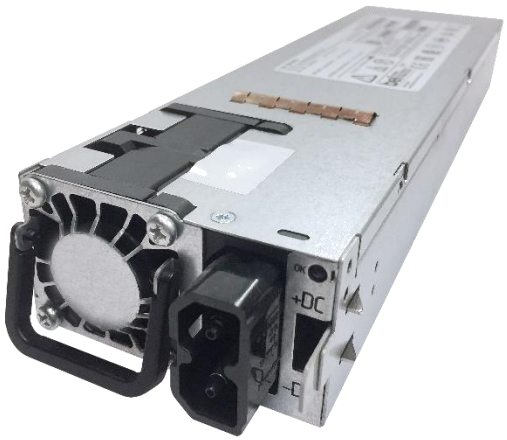
PET2000-12-074xD

DC-DC Front-End Power Supply

The PET2000-12-074xD is a 2000 Watt DC to DC power supply that converts -40 to -72 VDC voltage into an isolated main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PET2000-12-074xD utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards.



RoHS Compliant

Key Features & Benefits

- Best-in-class, “Platinum” equivalent efficiency
- Wide input voltage range: -40 to -72 VDC
- Always-On 12 V / 3 A / 36 W standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High density design: 42.1 W/in^3
- Small form factor: 265 x 73.5 x 40.0 mm (10.43 x 2.89 x 1.57 in)
- Power Management Bus communication protocol for control, programming and monitoring
- Status LED with fault signaling

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

1. ORDERING INFORMATION

PET	2000	-	12	-	074	x	D	x
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**	**DC Inlet**
PET Front-Ends	2000 W		12 V		74 mm	N: Normal [1] R: Reverse [2]	D: DC	- - Black, 6 AWG (C10-747100) * **K** - Black, 4 AWG (C10-747442) **Y** - Grey, 6 AWG (C10-638974)

[1] "N" Normal Airflow (NAF) from Output connector to Input DC Inlet.
[2] "R" Reverse Airflow (RAF) from Input DC Inlet to Output connector.
* Default option – no suffix needed.
Input plug with wire: Amphenol # CR-302001-257

2. OVERVIEW

The PET2000-12-074xD DC-DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates state-of-the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency.
With a wide input DC voltage range the PET2000-12-074xD maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

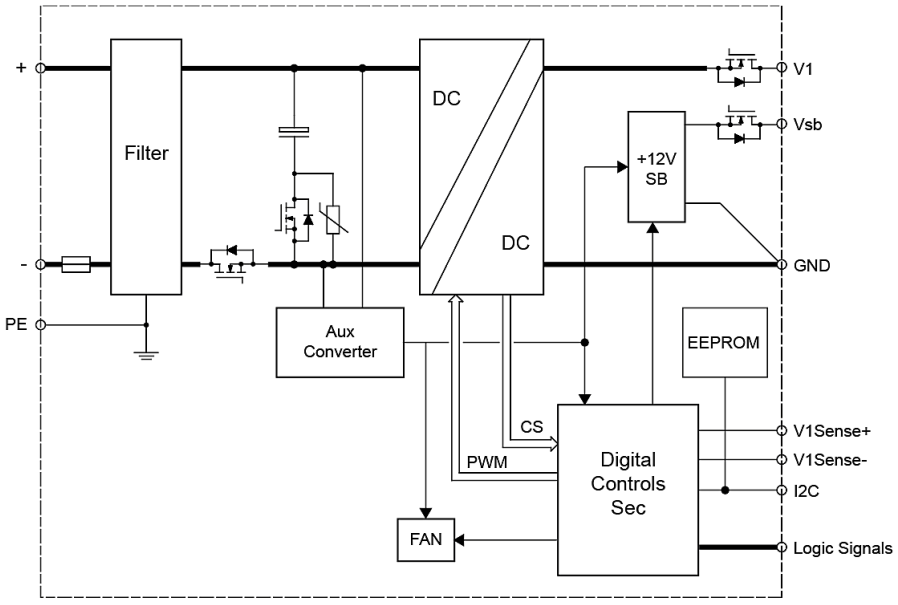


Figure 1. Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Vi max	Maximum Input Voltage	Continuous		-72	VDC

4. INPUT

General Condition: T_A = -5…40 °C (PET2000-12-074RD), T_A = -5…55 °C (PET2000-12-074ND), unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi start	Minimum Operating Input Voltage	Stand-by output available, DSP running	-32			VDC
Vi nom	Nominal Input Voltage			-53		VDC
Vi	Input Voltage	Normal operation (from Vi min to Vi max)	-40		-72	VDC
Ii	Input Current	Vi > Vi min				A
Ii pk	Inrush Current Limitation	From Vi min to Vi max, T_A = 25°C, turn on		40	55	A
Vi on	Turn-On Standby Input Voltage	Ramping up		-31.5		VDC
Vi on	Turn-On Input Voltage	Ramping up	-41		-42	VDC
Vi off	Turn-Off Input Voltage	Ramping down	-38.0		-39.5	VDC
η	Efficiency	Vi = -53 VDC; 20% load		93		%
		Vi = -53 VDC; 50% load		95		%
		Vi = -53 VDC; 100% load		93		%
Thold_V1	Hold-Up Time V1	T_A = 25°C, Vi = -48 VDC; $I_{1\ nom}$, $I_{SB\ nom}$, C_{ext} = 2200 µF	5	6		ms
Thold_Vsb	Hold-Up Time Vsb	T_A = 25°C, Vi = -48 VDC; $I_{1\ nom}$, $I_{SB\ nom}$, C_{ext} = 2200 µF	6			ms

4.1 INPUT FUSE

A fast-acting 80 A input fuse in the negative voltage path inside the power supply protect against severe defects. The fuse is not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the value of input DC voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again. If the input voltage stays below the input undervoltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

5. OUTPUT

General Condition: T_A = -5…40 °C (PET2000-12-074RD), T_A = -5…55 °C (PET2000-12-074ND), unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%$V_{1\ nom}$
$dV_{1\ tot}$	Total Static Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, T_A = 0 to 40°C	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power [1]	$V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 55°C (PET2000-12-074ND) $V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 40°C (PET2000-12-074RD)		2000		W
$I_{1\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 55°C (PET2000-12-074ND) $V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 40°C (PET2000-12-074RD)	0.0		167	ADC
$I_{1\ peak}$	Peak Output Current	$V_{i\ min}$ to $V_{i\ max}$,	0.0	177.5		ADC
$V_{1\ pp}$	Output Ripple Voltage [2]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, C_{ext} ≥ 1 mF/Low ESR			120	mVpp
$dV_{1\ load}$	Load Regulation	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$		-160		mV
$dV_{1\ line}$	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0.5 · $I_{1\ nom}$	-20	0	20	mV
$dV_{1\ temp}$	Thermal Drift	$V_{i\ nom\ HL}$, 0.5 · $I_{1\ nom}$			-0.5	mV/°C
$dI_{1\ share}$	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-4		+4	ADC
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ peak}$ at 180 A		9.4		VDC
$dV_{1\ lt}$	Load Transient Response	ΔI_1 = 40% $I_{1\ nom}$, I_1 = 10 … 100% $I_{1\ nom}$, C_{ext} = 0 mF,			0.6	VDC
t_{rec}	Recovery Time	dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom}$		0.5	1	ms
$V_{1\ dyn}$	Dynamic Load Regulation	ΔI_1 = 40% $I_{1\ nom}$, starting anywhere from 10% to 60%, f = 50 … 5000 Hz, Duty cycle = 10 … 90%, C_{ext} = 2 …30mF, di/dt =1A/µs, 25°C	11.4		12.6	V
$t_{V1\ on\ delay}$	Delay time from DC applied	V1 in regulation Vi = 0V to $V_{i\ min}$, $V_{i\ nom}$, $V_{i\ max}$			3	sec
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$, C_{ext} < 10 mF		10	200	ms
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$			13.2	V
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{1\ nom}$			0.25	V
$C_{V1\ load}$	Capacitive Loading		0		20	mF
OVP	Over voltage Trip	$V_{i\ min}$ to $V_{i\ max}$,	13.6		15.0	V
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	I_{SB} = *1.25A (50% of* I_{SBnom}, 25°C, (PET2000-12-074ND)) I_{SB} = *1.50A (50% of* I_{SBnom}, 25°C, (PET2000-12-074RD))		12.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-2		+2	%V_{SBnom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-5		+5	%V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 75°C (PET2000-12-074ND) $V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 55°C (PET2000-12-074RD)		30 36		W W
$P_{SB\ peak}$	Peak Output Power	$V_{i\ min}$ to $V_{i\ max}$		40		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 75°C (PET2000-12-074ND) $V_{i\ min}$ to $V_{i\ max}$, T_A = -5 to 55°C (PET2000-12-074RD)	0 0		2.5 3.0	ADC ADC
$I_{SB\ peak}$	Peak Output Current	$V_{i\ min}$ to $V_{i\ max}$	3.2	3.5	4.5	ADC
$V_{SB\ pp}$	Output Ripple Voltage [2]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, C_{ext} = 0 mF $V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, C_{ext} ≥ 2 mF/Low ESR			150 120	mVpp mVpp
$dV_{SB\ load}$	Load Regulation	$V_{i\ nom\ HL}$, 0 to 100% $I_{SB\ nom}$		-300		mV
$dV_{SB\ line}$	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$, I_{SB} = *0 A*	-20	4	20	mV

[1] See also chapter TEMPERATURE AND FAN CONTROL
[2] Measured with a 10 µF low ESR capacitor in parallel with a 0.1 µF ceramic capacitor at the point of measurement

$dV_{SB\ temp}$	Thermal Drift	$V_{i\ nom\ HL}$, $I_{SB} = 0\ A$			-0.5	mV/°C
$dI_{SB\ share}$	Current Sharing	Deviation from $I_{SB\ tot}$ / N, $I_{SB} = 0.5 \cdot I_{SB\ nom}$	-1		+1	ADC
$dV_{SB\ lt}$	Load Transient Response	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 0 … 100% $I_{SB\ nom}$,		0.2	0.3	VDC
t_{rec}	Recovery Time	dI_{SB}/dt = 1A/µs, recovery within 1% of $V_{SB\ nom}$		1	2	ms
$V_{SB\ dyn}$	Dynamic Load Regulation	ΔI_{SB} = 1 A, I_{SB} = 0 … $I_{SB\ nom}$, f = 50 ... 5000 Hz, Duty cycle = 10 ... 90%, C_{ext} = 0 ... 5 mF	10.8		13.2	V
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$, C_{ext} < 1 mF	5	10	20	ms
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			13.2	V
$C_{VSB\ load}$	Capacitive Loading		0		3000	µF

6. EFFICIENCY

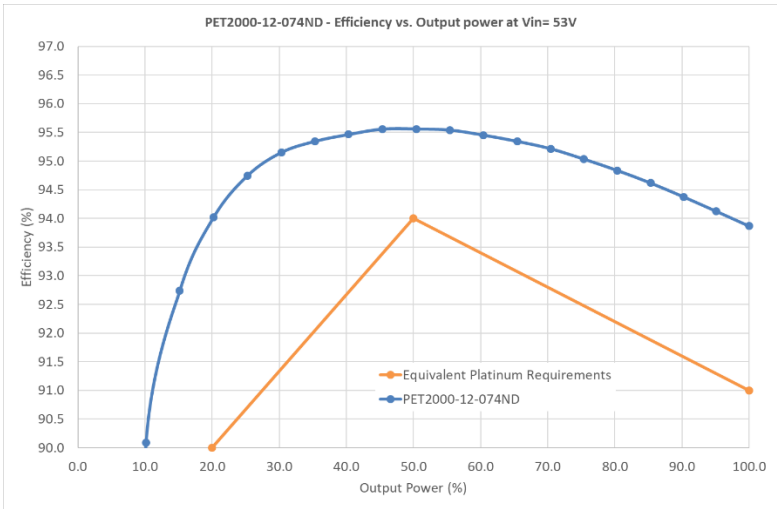


Figure 2. Efficiency vs. Output Power (fan losses not included)

7. OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 3*. Alternatively, separated ground signals can be used as shown in *Figure 4*. In this case the two ground planes should be connected together at the power supplies ground pins.

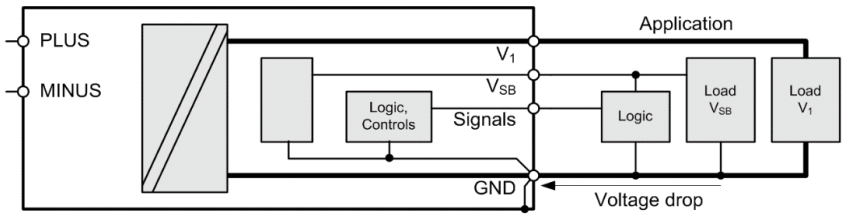


Figure 3. Common low impedance ground plane

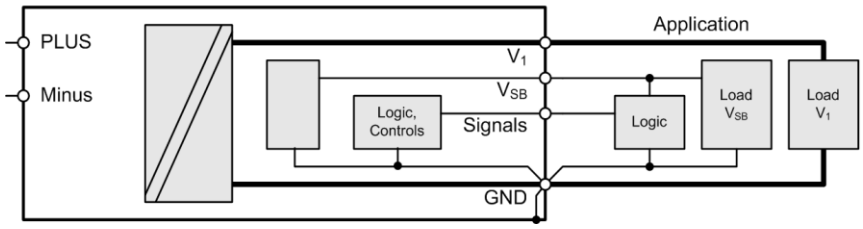


Figure 4. Separated power and signal ground

Due the unit has no Input Earth Connector Terminal on the front of the unit it is mandatory to have a reliable system output GND to Earth connection.

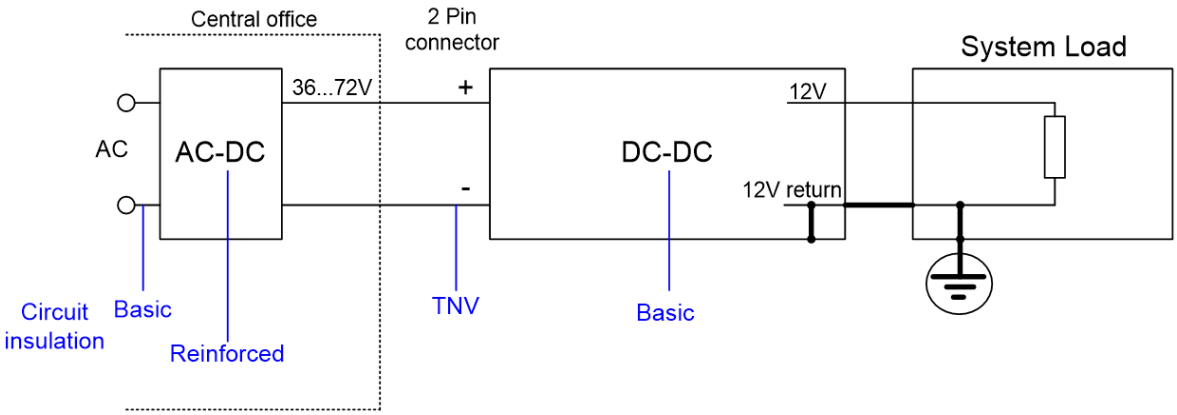


Figure 5. Block diagram with reliable System Earth connection

8. PROTECTION

General Condition: T_A = 0…40 °C (PET2000-12-074RD), T_A = 0…55 °C (PET2000-12-074ND), unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (L)	Not use accessible, fast acting		80		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.6	14.3	14.5	VDC
$t_{V1\ OV}$	OV Trip Time V_1				1	ms
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage V_1 Protection, Automatic retry each 1s	13.6	14.3	14.5	VDC
$t_{VSB\ OV}$	OV Trip Time V_{SB}				1	ms
$I_{V1\ OC\ Slow}$	OC Limit V_1	Over Current Limitation, Latch-off, $V_{i\ min}$ to $V_{i\ max}$	169		175	ADC
		Over Current Limitation, Latch-off time		20		s
$I_{V1\ OC\ Fast}$	Fast OC Limit V_1	Fast Over Current Limit. Latch-off, $V_{i\ min}$ to $V_{i\ max}$	176			ADC
$t_{V1\ OC\ Fast}$	Fast OC Trip time V_1	Fast Over Current Limitation, Latch-off time	50		60	ms
$I_{V1\ SC}$	Max Short Circuit Current V_1	V_1 < 3 V, time until I_{V1} is limited to < $I_{V1\ SC}$			180	A
$t_{V1\ SC}$	Short Circuit Regulation Time	Over Current Limitation, Constant-Current Type			2	ms
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limit., time until I_{VSB} is limited to $I_{VSB\ OC}$			6	A
$t_{VSB\ OC}$	OC Trip time V_{SB}	Automatic shut-down			1	ms
T_{SD}	Over Temperature on Heat Sinks			115		°C
OVP	Over voltage trip	$V_{i\ min}$ to $V_{i\ max}$	13.6		15.0	V

8.1 OVERVOLTAGE PROTECTION

The PET2000-12-074xD front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC supply or by toggling the PSON_L input. The standby output will continuously try to restart with a 1 s interval after OV condition has occurred.

8.2 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H will change if the output voltage exceeds regulation band. The main output will latch off if the main output voltage V_1 falls below 10 V (typically in an overload condition) for more than 55 ms. The latch can be unlocked by disconnecting the supply from the DC supply or by toggling the PSON_L input.
If the standby output leaves its regulation bandwidth for more than 2 ms then the main output is disabled to protect the system.

8.3 CURRENT LIMITATION

MAIN OUTPUT

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If output current exceeds $I_{V1\ OC\ Fast}$ it will reduce output voltage in order to keep output current at $I_{V1\ OC\ Fast}$. If the output voltage drops below ~10.0 VDC for more than 55 ms, the output will latch off (standby remains on).
The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input. The main output current limitation thresholds depend on the actual input applied to the power supply.

STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0 V (no hiccup mode / latch off). The current limitation of the standby output is independent of the DC input voltage.
Running in current limitation causes the output voltage to fall, this will trigger under voltage protection and disables the main output.

9. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to chapter I2C / POWER MANAGEMENT BUS COMMUNICATION and document URP.00234 (PET2000-12-074 Power Management Bus Communication Manual).

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input Voltage	$V_{i\ min\ LL} \leq V_i \leq V_{i\ max}$	-2		+2	VDC
$I_{i\ mon}$	Input Current	I_i > 5.8 A	-5		+5	%
$P_{i\ mon}$	True Input Power	P_i > 400 W	-5		+5	%
		200 W <P_i < 400 W	25		25	W
$V_{1\ mon}$	V_1 Voltage		-0.2		+0.2	VDC
$I_{1\ mon}$	V_1 Current	I_1 > 50A	-2		+2	%
		16.7 A < I_1 ≤ 50 A	-2		+2	ADC
$P_{1\ nom}$	V_1 Output Power	P_i > 400 W	-5		+5	%
		200 W < P_i ≤ 400 W	-15		+15	W
$V_{SB\ mon}$	V_{SB} Voltage		-0.25		+0.25	VDC
$I_{SB\ mon}$	V_{SB} Current		-0.2		+0.2	ADC
$T_{A\ mon}$	Inlet Temperature	$T_{A\ min} \leq T_A \leq T_{A\ max}$	-5	2	+5	°C

10. SIGNALING AND CONTROL

10.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_H / HOTSTANDBYEN_H						
V_{IL}	Input Low Level Voltage	PSON_L: Main output enabled HOTSTANDBYEN_H: Hot Standby mode not allowed	-0.2		0.8	V
V_{IH}	Input High Level Voltage	PSON_L: Main output disabled HOTSTANDBYEN_H: Hot Standby mode allowed	2		3.5	V
$I_{IL,H}$	Maximum Input Sink or Source Current	V_I = -0.2 V to +3.5 V	-1		1	mA
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3 V			10		kΩ
R_{LOW}	Maximum external Pull down Resistance to GND to obtain Low Level				1	kΩ
R_{HIGH}	Minimum external Pull down Resistance to GND to obtain High Level		50			kΩ
PWOK_H						
V_{OL}	Output Low Level Voltage	V_1 or V_{SB} out of regulation, V_{Isink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	V_1 and V_{SB} in regulation, I_{source} < 0.5 mA	2.4		3.5	V
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3 V			1		kΩ
I_{OL}	Maximum Sink Current	V_O < 0.4 V			4	mA

10.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the GND rail.
With open sense inputs the main output voltage will rise by 270 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

10.3 CURRENT SHARE

The PET front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.
The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.
The standby output uses a passive current share method (droop output voltage characteristic).

10.4 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source.

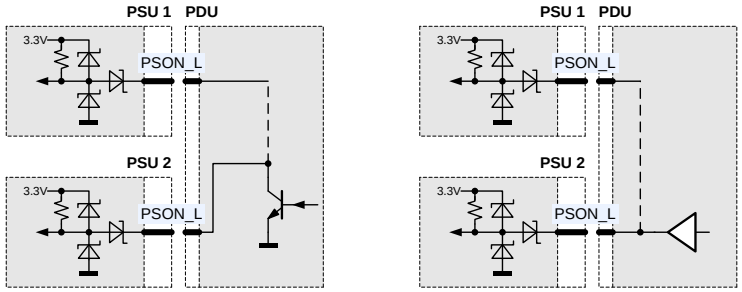


Figure 6. PSON_L connection

10.5 PWOK_H OUTPUT

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both VSB and V1 outputs are within regulation. This pin is active-low.

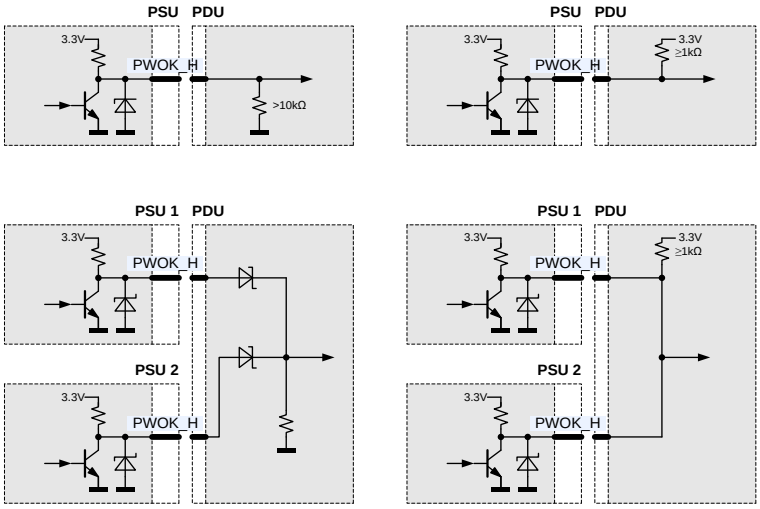


Figure 7. PWOK_H connection

10.6 PRESENT_L OUTPUT

The PRESENT_L pin is wired through a 100 Ohms resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

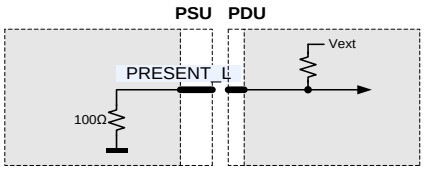


Figure 8. PRESENT_L connection

10.7 SIGNAL TIMING

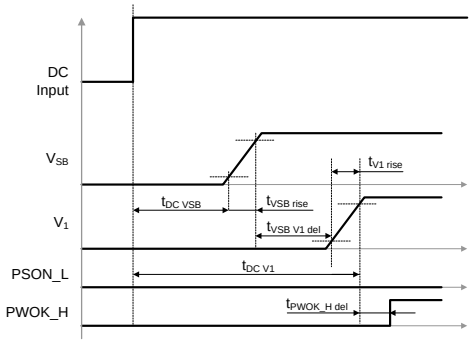


Figure 9. DC turn-on timing

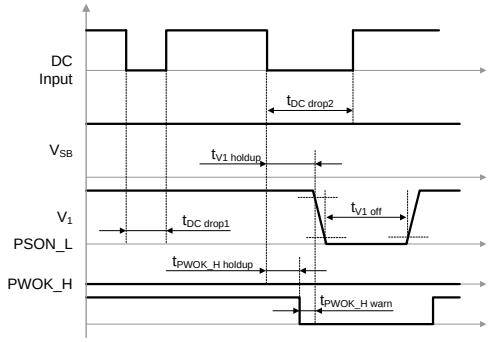


Figure 10. DC short dips

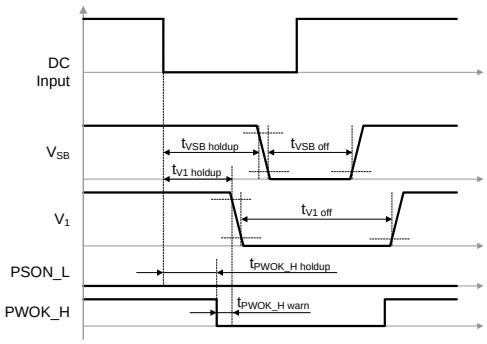


Figure 11. DC long dips

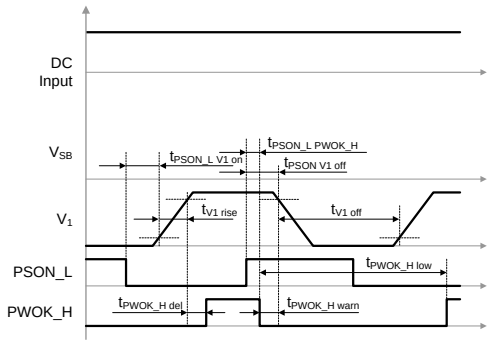


Figure 12. PSON_L turn-on/off timing

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$t_{DC\ VSB}$	DC Line to 90% V_{SB}				3	s
$t_{DC\ V1}$	DC Line to 90% V_1	PSON_L = Low			5 [3]	s
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	PSON_L = Low	50		1000	ms
$t_{V1\ rise}$	V_1 rise time	See chapter OUTPUT				
$t_{VSB\ rise}$	V_{SB} rise time	See chapter OUTPUT				
$t_{DC\ drop1}$	DC drop from Vi = -48 VDC, without V_1 leaving regulation	I_1 = 150A, $I_{SB\ nom}$	5	5.5		ms
$t_{DC\ drop2}$	DC drop without V_{SB} leaving regulation	$I_{1\ nom}$, $I_{SB\ nom}$	6			ms
$t_{V1\ holdup}$	Loss of DC to V_1 leaving regulation	See chapter INPUT				
$t_{VSB\ holdup}$	Loss of DC to V_{SB} leaving regulation	See chapter INPUT				
$t_{PWOK\_H\ del}$	Outputs in regulation to PWOK_H asserted		5		400	ms
$t_{PWOK\_H\ warn}$	Warning time from de-assertion of PWOK_H to V_1 leaving regulation		0			ms
$t_{PWOK\_H\ holdup}$	Loss of DC to PWOK_H de-asserted		2			ms
$t_{PWOK\_H\ low}$	Time PWOK_H is kept low after being de-asserted		100			ms
$t_{PSON\_L\ V1\ on}$	Delay PSON_L active to V_1 in regulation		5		400	ms
$t_{PSON\_L\ V1\ off}$	Delay PSON_L de-asserted to V_1 disabled			50		ms
$t_{PSON\_L\ PWOK\_H}$	Delay PSON_L de-asserted to PWOK_H de-asserted				4	ms
$t_{V1\ off}$	Time V_1 is kept off after leaving regulation			1		s
$t_{VSB\ off}$	Time V_{SB} is kept off after leaving regulation			1		s

[3] At repeated ON-OFF cycles the start-up times can be increased by 1 s

10.8 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and amber, and indicates DC input and DC output power presence and warning or fault conditions. *Table 1* below lists the different LED status.

OPERATING CONDITION [4]	LED SIGNALING
No Vi or DC Line in UV condition, V_{SB} not present from paralleled power supplies	Off
PSON_L High	Blinking Green 1 Hz
No DC or DC Line in UV condition, V_{SB} present from paralleled power supplies V_1 or V_{SB} out of regulation Over temperature shutdown Output over voltage shutdown (V_1 or V_{SB}) Output over current shutdown (V_1 or V_{SB}) Fan error (>55%)	Solid Amber
Over temperature warning Minor fan regulation error (>45%, <45%)	Blinking Amber 1 Hz
Firmware boot loading in process	Blinking Green 2 Hz
Outputs V_1 and V_{SB} in regulation	Solid Green

Table 1. LED Status

[4] The order of the criteria in the table corresponds to the testing precedence in the controller

11. I2C / POWER MANAGEMENT BUS COMMUNICATION

The PET front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 2* and further characterized through:

- The SDA/SCL IOs use 3.3 V logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

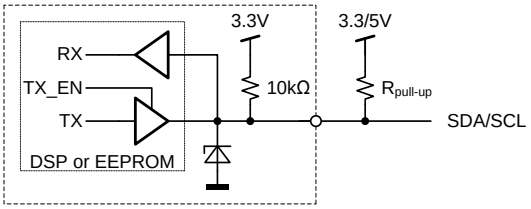


Figure 13. Physical Layer of Communication Interface

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life VSB output (provided e.g. by the redundant unit). If only V1 is provided, communication is not possible.

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 2. I²C / SMBus Specification

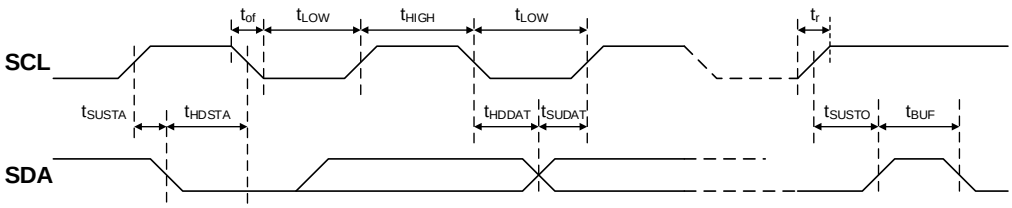


Figure 14. I²C / SMBus Timing

ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pins A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A0/A1 and A2 pin to be in High Level if left open.
A fixed addressing offset exists between the Controller and the EEPROM.

A2 [2]	A1	A0	I2C Address [1]	
			Controller	EEPROM
0	0	0	0xB0	0xA0
0	0	1	0xB2	0xA2
0	1	0	0xB4	0xA4
0	1	1	0xB6	0xA6
1	0	0	0xB8	0xA8
1	0	1	0xBA	0xAA
1	1	0	0xBC	0xAC
1	1	1	0xBE	0xAE

[1] The LSB of the address byte is the R/W bit.
[2] A2 is used on the standard model only.
On special models (e.g. PET2000-12-074ND020) the connector PIN is used for IN_OK functionality. These models have only two addressing pins A0 and A1. A2 is set to 0 inside firmware by default.

Table 3. Address and Protocol Encoding

11.1 SMBALERT_L OUTPUT

The SMBALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

The SMBAlert signal is asserted simultaneously with the LED turning to solid amber or blinking amber.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
SMB_ALERT_L						
V_{ext}	Maximum External Pull up Voltage				12	V
I_{OH}	Maximum High Level Leakage Current	No Failure or Warning condition, V_O = 12 V			10	µA
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4 mA	0		0.4	V
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3 V			None		
I_{OL}	Maximum Sink Current	V_O < 0.4 V			4	mA

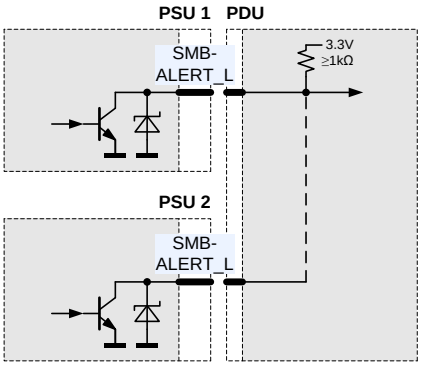


Figure 15. SMBALERT_L connection

11.2 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 16*) and can be accessed under different addresses, see ADDRESS SELECTION. The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3.3 V.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

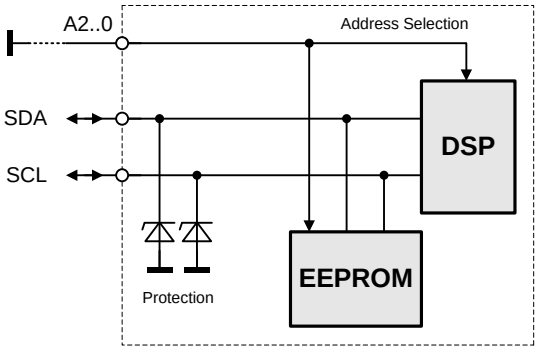


Figure 16. I²C Bus to DSP and EEPROM

11.3 EEPROM PROTOCOL

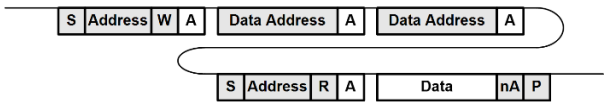
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the “SMBus 1.1 Write Byte Protocol”. After the device address with the write bit cleared, the Two Byte Data Address is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the “SMBus 1.1 Read Byte Protocol”. After the device address with the write bit cleared the two byte data address is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



11.4 POWER MANAGEMENT BUS PROTOCOL

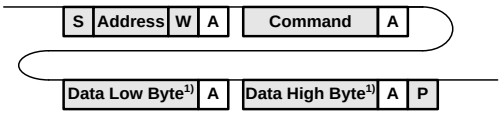
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PET2000-12-074ND supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

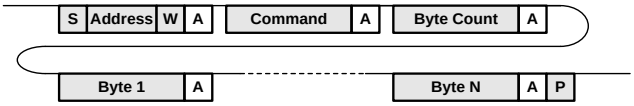
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



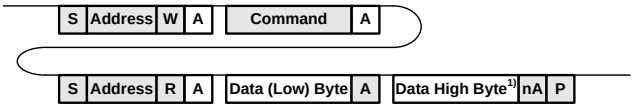
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET2000-12-074NA / PET2000-12-074ND Power Management Bus Communication Manual URP.00234 for further information.



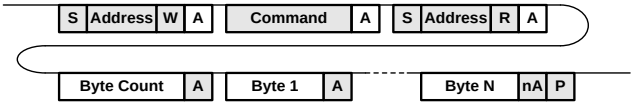
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.
See PET2000-12-074NA/ PET2000-12-074ND Power Management Bus Communication Manual URP.00234 for further information.



11.5 GRAPHICAL USER INTERFACE

The Bel Power Solutions provides with its "I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET2000-12-074xD Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the YTM.00046 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.
Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.
The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings.
This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

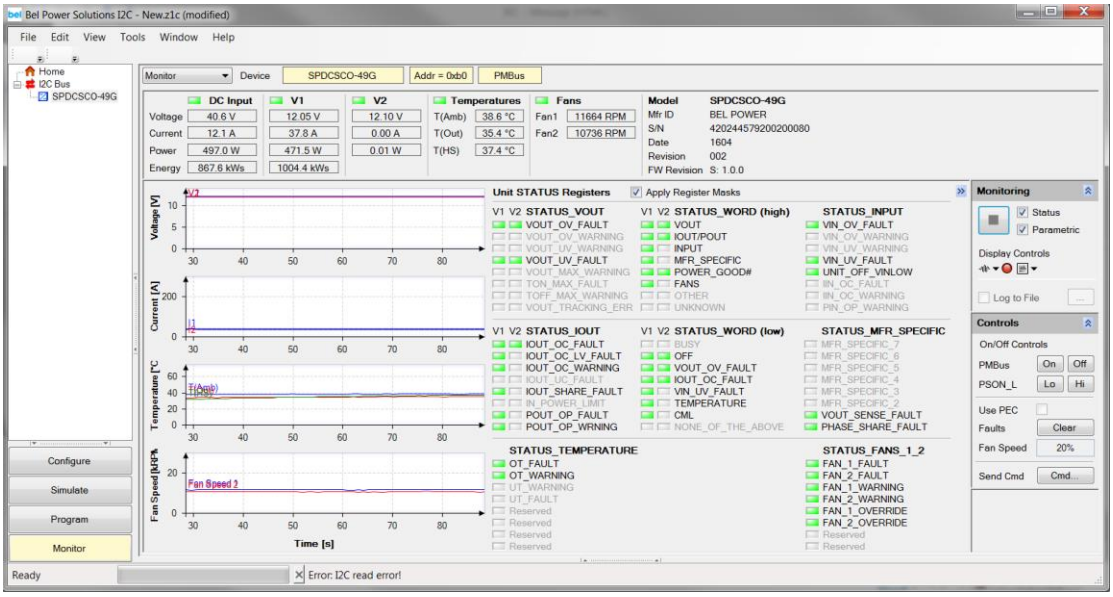


Figure 17. Monitoring dialog of the I²C Utility

12. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET2000-12-074ND is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the DC-inlet. The PET2000-12-074RD is provided with a front to rear airflow, which means the air enters through the DC-input of the supply and leaves at the DC-output. The PET2000-12-074xD power supply has been designed for horizontal operation.

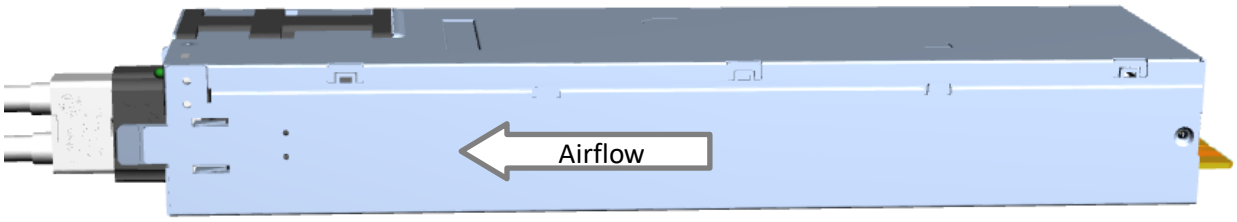


Figure 18. Airflow direction PET2000-12-074ND

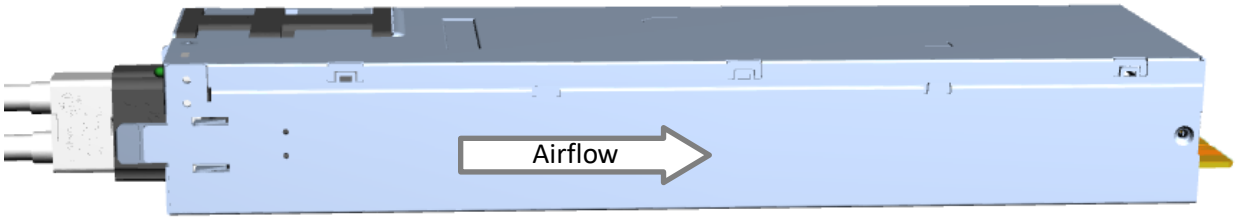


Figure 19. Airflow direction PET2000-12-074RD

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature. *Figure 20* illustrates the programmed fan curves.

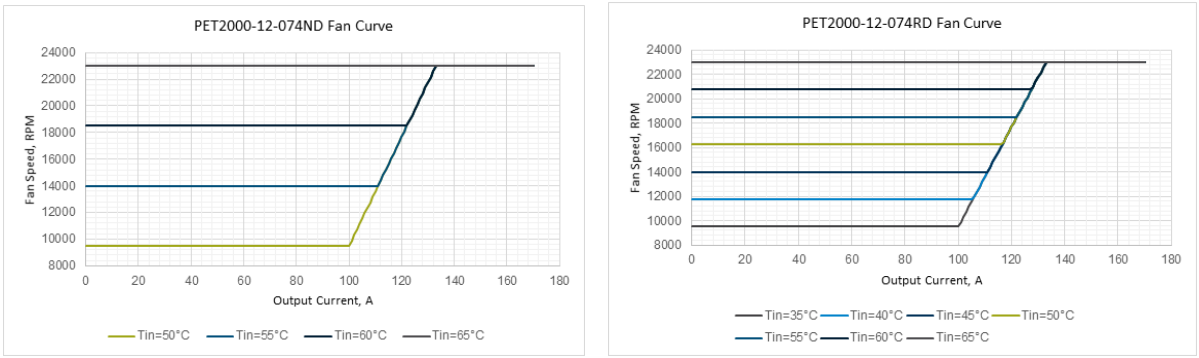


Figure 20. Fan speed vs. main output load

The PET2000-12-074xD provides access via I²C to the measured temperatures of sensors within the power supply, see *Table 4*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V_1 (or V_{SB} if auxiliary converter is affected) will be disabled. At the same time, the warning or fault condition is signalized accordingly through LED, PWOK_H and SMBALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet Air Temperature	PET2000-12-074ND Sensor located on control board close to DC end of power supply (card edge connector)	0x8D	77°C	80°C
	PET2000-12-074RD Sensor located next to the fan of power supply		67°C	70°C
Synchronous Rectifier	Sensor located on secondary side of DC/DC stage	0xD6	95°C	105°C
Primary Heat Sink	Sensor located next to the heat sink	0x8E	95°C	105°C

Table 4. Temperature sensor location and thresholds

13. MAXIMUM OUTPUT POWER VERSUS INLET TEMPERATURE FOR SAFETY COMPLIANCY

For safety compliant operation the power supply needs to be operating inside the specified operating conditions.
The PET2000-12-074xD modules have different power derating behavior which are mainly dependent on the air flow direction and the ambient conditions.

PET2000-12-074ND

Above 55°C the maximum output power is reduced with rising temperature. *Figure 21* illustrates these maximum current and power levels.

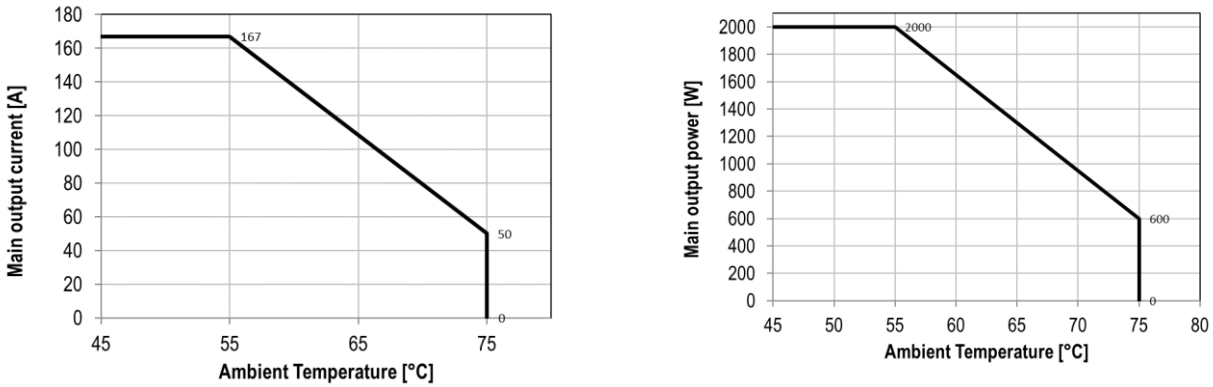


Figure 21. Maximum current and power levels PET2000-12-074ND

PET2000-12-074RD

Above 40°C the maximum output power is reduced with rising temperature. *Figure 22* illustrates these maximum current and power levels.

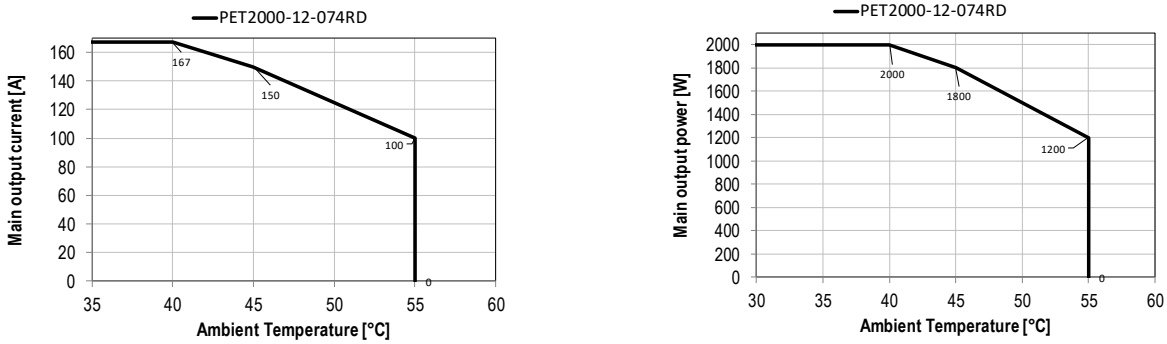


Figure 22. Maximum current and power levels PET2000-12-074RD

14. ELECTROMAGNETIC COMPATIBILITY

14.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LED, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1µs Pulse Modulation, 10 kHz ... 2 GHz	A
Burst	IEC / EN 61000-4-4, Level 3 DC input port ±2 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 ; NEBS GR-1089-CORE Issue 6 Common mode: ±1 kV (2 Ohm) Differential mode : ±1 kV (2 Ohm)	A
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A

14.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55032 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class A - 6 dB
Radiated Emission	EN 55032 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class A - 6 dB
Acoustical Noise	Distance at bystander position, 25°C, 50% Load	65 dBA

15. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	UL 60950-1 2nd Edition CAN/CSA-C22.2 No. 60950-1-07 2nd Edition IEC 60950-1: 2005 EN 62368-1: 2014 EN 60950-1: 2006 NEMKO EAC CQC GB4943.1-2011 TP TC 004/2011	Approved
Isolation Strength	Input plus to chassis; 1414V for 1 minute	Basic
	Input minus to chassis; 1414V for 1 minute	Basic
	Output to chassis	None (Direct connection)
Creepage / Clearance	Primary to chassis (PE)	>2 mm
	Primary to secondary	

16. ENVIRONMENTAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
TA	Ambient Temperature	Up to 1'000m ASL, PET2000-12-074ND Up to 1'000m ASL, PET2000-12-074RD Linear derating from 1'000 to 3048 m ASL PET2000-12-074ND PET2000-12-074RD	-5 -5		+55 +40 +45 +30	°C °C °C °C
TAext	Extended Temp. Range	PET2000-12-074ND PET2000-12-074RD			70 55	°C °C
TS	Storage Temperature	Non-operational	-20		+70	°C
	Altitude	Operational, above Sea Level Non-operational, above Sea Level	- -		3'048 10'600	m m
	Shock, operational Shock, non-operational	Half sine, 11ms, 10 shocks per direction, 6 directions			1 30	g peak g peak
	Vibration, sinusoidal, operational Vibration, sinusoidal, non-operational	IEC/EN 60068-2-6, sweep 5 to 500 to 5 Hz, 1 octave/min, 5 sweep per axis			1 4	g peak g peak
	Vibration, random, operational	7.7grms 30min, 3 axes operational			7.7	Grms
	Vibration, random, non-operational	IEC/EN 60068-2-64, 5 to 500 Hz, 1 hour per axis			0.025	g^2/Hz

17. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time to failure	According Bellcore TR-TSY-000332, Issue 3 T_A = 25°C, V_i = -48 VDC, 0.5 · $I_{1\ nom}$, $I_{SB\ nom}$	683			kh
	Expected life time	T_A = 25°C, V_i = -48 VDC, 0.7 · $I_{1\ nom}$, $I_{SB\ nom}$ T_A = 55°C, V_i = -48 VDC, $I_{1\ nom}$, $I_{SB\ nom}$	7 2			years

18. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions *	Width		73.5		mm
		Heigth		40.0		mm
		Depth		265.0		mm
m	Weight			1.2		kg

* Dimensions in mm, tolerances acc. ISO 2768 ()-H, unless otherwise stated: 0.5-30: ±0.2; 30-120: ±0.3; 120-400: ±0.5

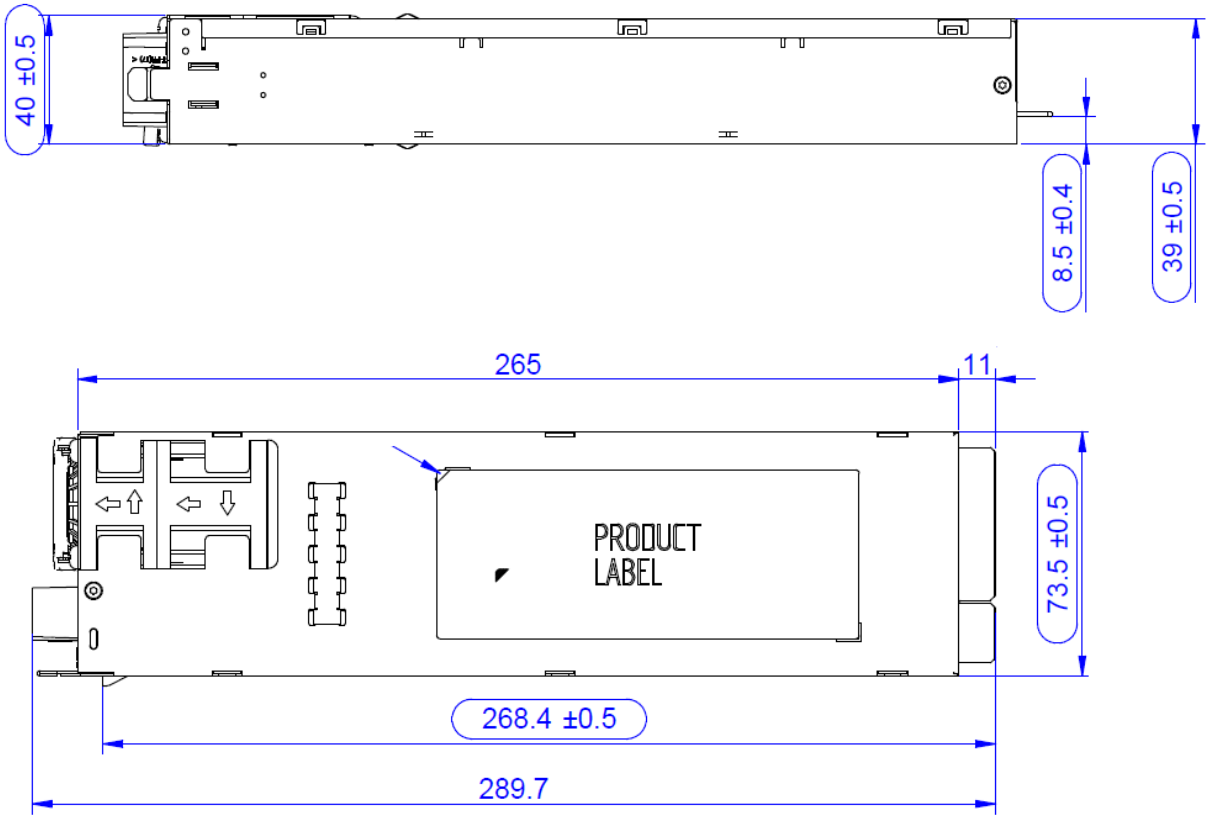


Figure 23. Top and side view with the connector added

Figure 24. Front view

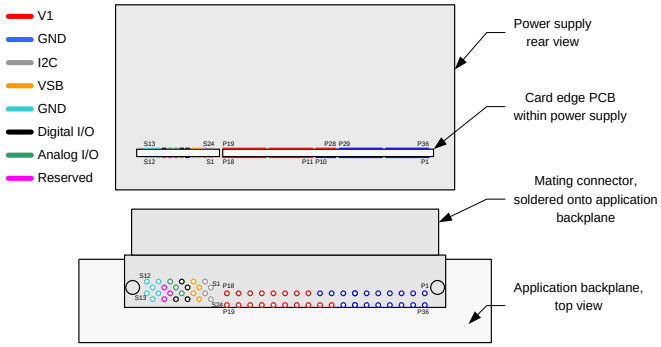


Figure 25. Rear view

A screw added on the PET2000-12-074xD side prevents the unit from being inserted into system with standard INTEL connector. Systems using PET2000-12-074xD must have a slot of ø6 mm x 14 mm implemented to allow the unit to be inserted. The maximum size of the screw head is ø6mm and height 2.12 mm.

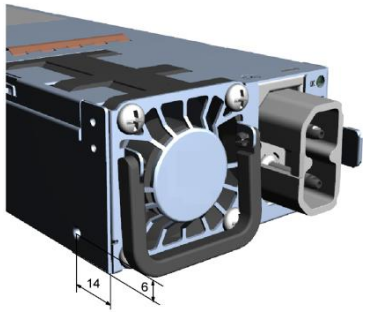


Figure 26. Polarizing screw

19. CONNECTORS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
DC inlet	Receptacle: Amphenol # C10-730138-000, 3.6 mm Plug: Amphenol # C10-747100-000, for 6 AWG (black) Amphenol # C10-638974-000, for 6 AWG (gray) Amphenol # C10-747442-000, for 4 AWG (black) Input wire harness (with black plug): Amphenol # CR-302001-257				
DC diameter requirement	Wire size	6		4	AWG
Output connector	25-Pin PCB card edge				
Mating output connector	Manufacturer: FCI Electronics Manufacturer P/N: 10130248-005LF or 10139371-1824CLF (see *Figure 28* for options) BEL P/N: ZES.00678 Refer to Table 20 and Table 21 respectively for the pin assignment, as the FCI pin definition of the 2 connectors are different				

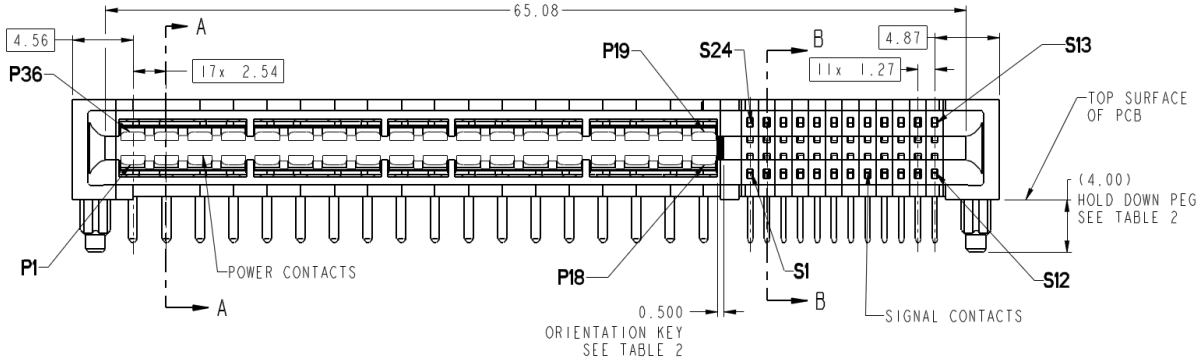


Figure 27. 10130248-005LF Rear view

Pin definition for mating output connector 10130248-005LF (refer to Figure 27)

PIN	SIGNAL NAME	DESCRIPTION
P1 ~ P10 P29 ~ P36	GND GND	Power and signal ground (return)
P11 ~ P18 P19 ~ P28	V1 V1	+12 VDC main output
S1 S2	A0 A1	I²C address selection input
S3, S4, S21, S22	VSB	+12 V Standby positive output
S5	NC	Not used
S6	ISHARE	Analog current share bus
S7	Reserved	For future use, keep open circuit
S8	PRESENT_L	Power supply seated, active-low
S9	A2 or IN_OK	I2C address selection input (on standard models) or Input voltage OK signal output, active-high (e.g. For PET2000-12-074ND0200)
S10 ~ S15	GND	Power and signal ground (return)
S16	PWOK_H	Power OK signal output, active-high
S17	V1_SENSE	Main output positive sense
S18	V1_SENSE_R	Main output negative sense
S19	SMB_ALERT_L	SMB Alert signal output, active-low
S20	PSON_L	Power supply on input, active-low
S23	SCL	I²C clock signal line
S24	SDA	I²C data signal line

Table 5. Output connector pin assignment for 10130248-005LF

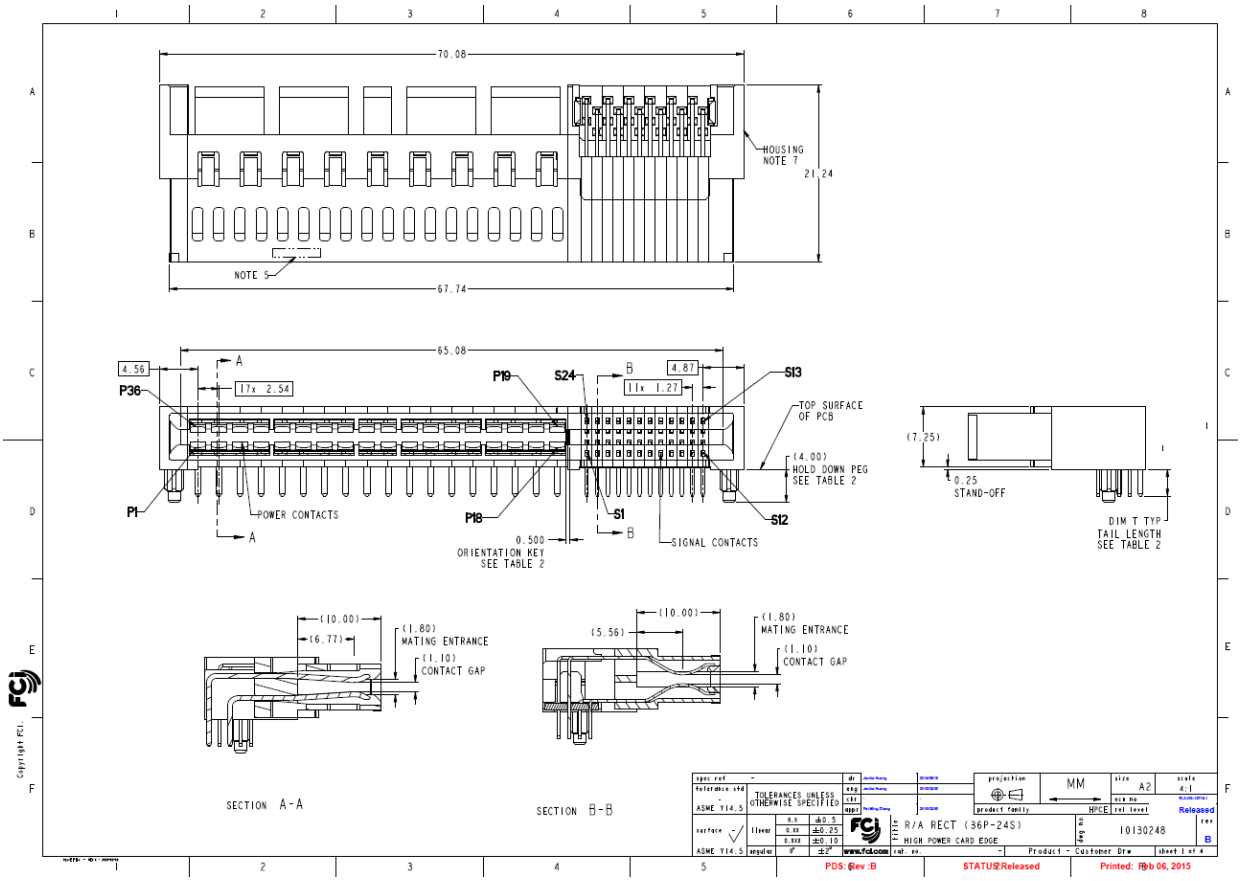


Figure 28. Mating connector drawing page 1

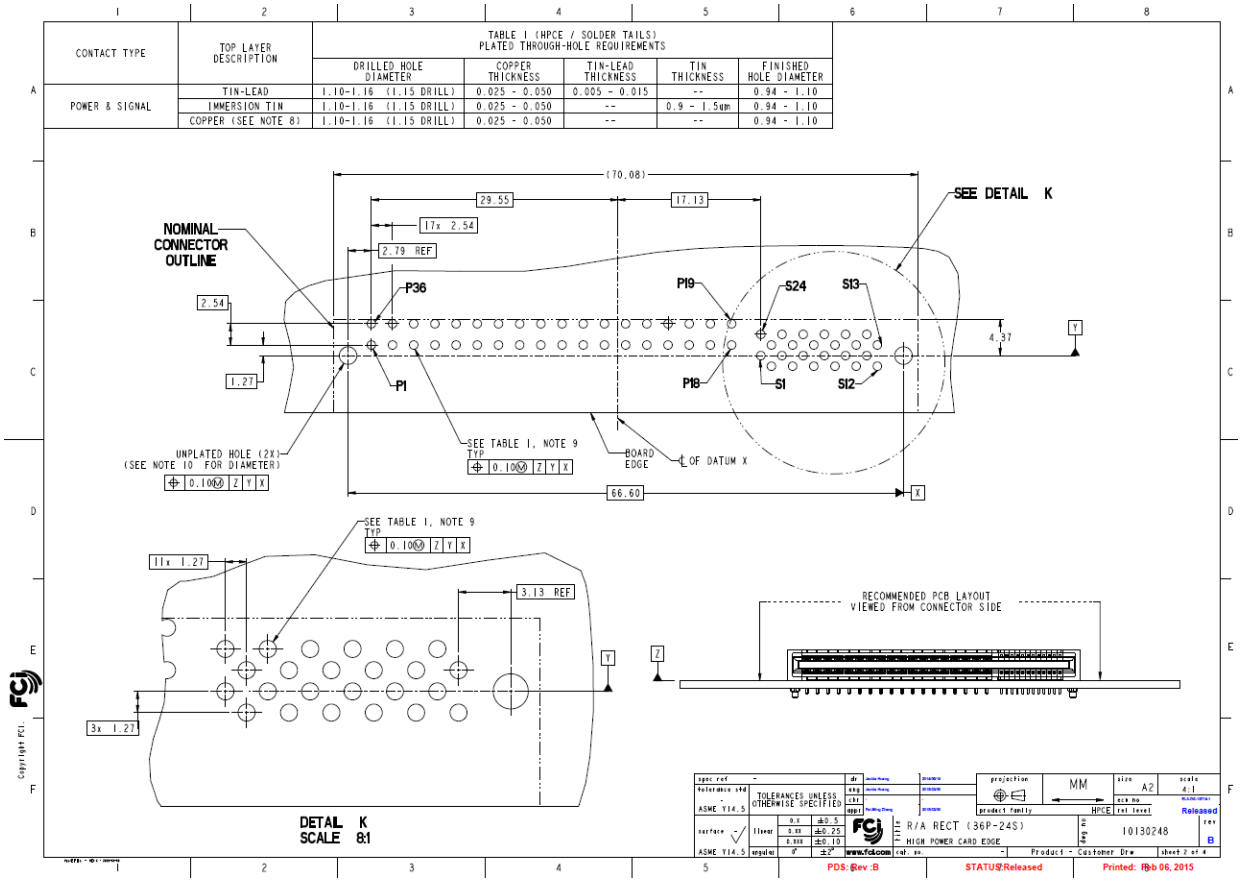
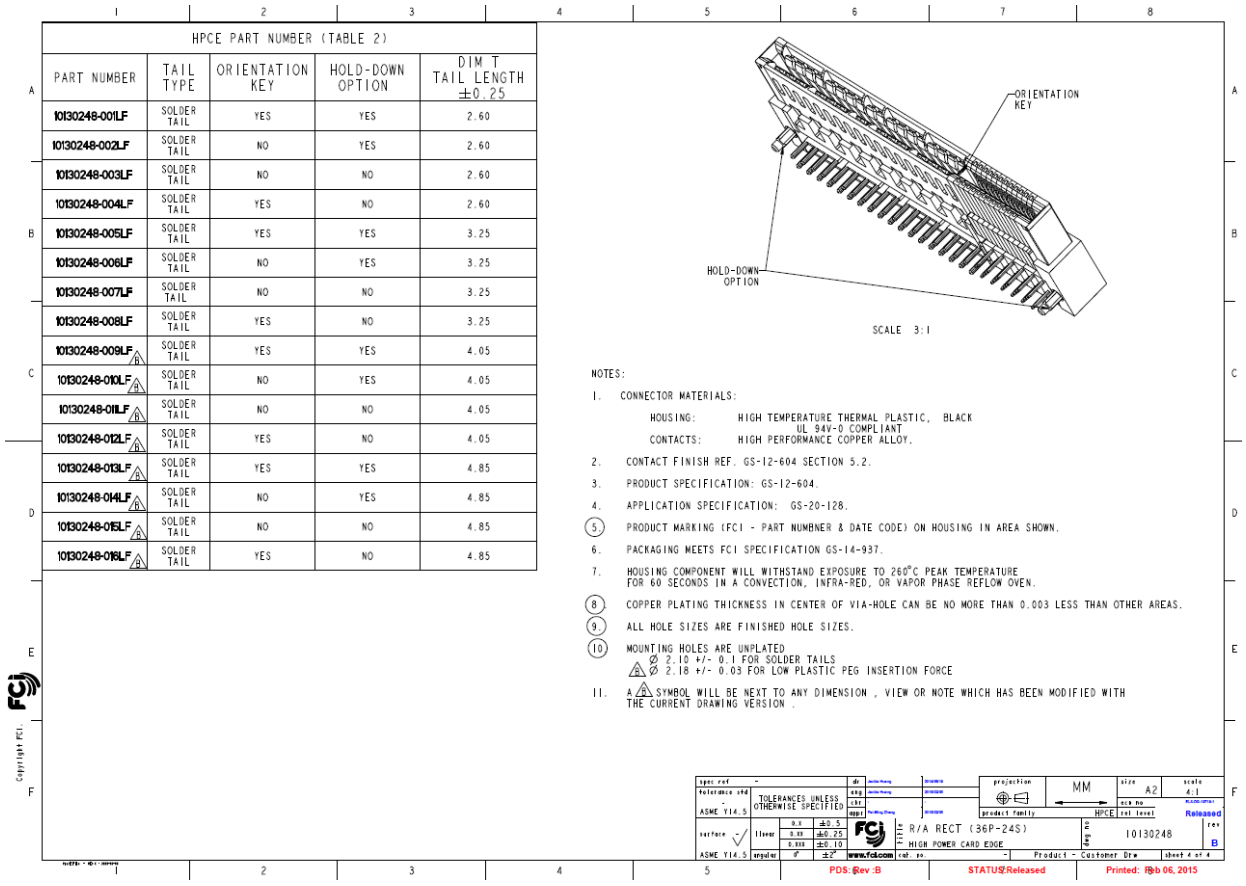


Figure 29. Mating connector drawing page 2



HPCE PART NUMBER (TABLE 2)

PART NUMBER	TAIL TYPE	ORIENTATION KEY	HOLD-DOWN OPTION	DIM T TAIL LENGTH ±0.25
10130248-001LF	SOLDER TAIL	YES	YES	2.60
10130248-002LF	SOLDER TAIL	NO	YES	2.60
10130248-003LF	SOLDER TAIL	NO	NO	2.60
10130248-004LF	SOLDER TAIL	YES	NO	2.60
10130248-005LF	SOLDER TAIL	YES	YES	3.25
10130248-006LF	SOLDER TAIL	NO	YES	3.25
10130248-007LF	SOLDER TAIL	NO	NO	3.25
10130248-008LF	SOLDER TAIL	YES	NO	3.25
10130248-009LF (A)	SOLDER TAIL	YES	YES	4.05
10130248-010LF (A)	SOLDER TAIL	NO	YES	4.05
10130248-011LF (A)	SOLDER TAIL	NO	NO	4.05
10130248-012LF (A)	SOLDER TAIL	YES	NO	4.05
10130248-013LF (A)	SOLDER TAIL	YES	YES	4.85
10130248-014LF (A)	SOLDER TAIL	NO	YES	4.85
10130248-015LF (A)	SOLDER TAIL	NO	NO	4.85
10130248-016LF (A)	SOLDER TAIL	YES	NO	4.85

NOTES:

1. CONNECTOR MATERIALS:
   HOUSING: HIGH TEMPERATURE THERMAL PLASTIC, BLACK UL 94V-0 COMPLIANT
   CONTACTS: HIGH PERFORMANCE COPPER ALLOY.
2. CONTACT FINISH REF. GS-12-604 SECTION 5.2.
3. PRODUCT SPECIFICATION: GS-12-604.
4. APPLICATION SPECIFICATION: GS-20-128.
5. PRODUCT MARKING (FCI - PART NUMBNER & DATE CODE) ON HOUSING IN AREA SHOWN.
6. PACKAGING MEETS FCI SPECIFICATION GS-14-937.
7. HOUSING COMPONENT WILL WITHSTAND EXPOSURE TO 260°C PEAK TEMPERATURE FOR 60 SECONDS IN A CONVECTION, INFRA-RED, OR VAPOR PHASE REFLOW OVEN.
8. COPPER PLATING THICKNESS IN CENTER OF VIA-HOLE CAN BE NO MORE THAN 0.003 LESS THAN OTHER AREAS.
9. ALL HOLE SIZES ARE FINISHED HOLE SIZES.
10. MOUNTING HOLES ARE UNPLATED.
    Ø 2.10 +/- 0.1 FOR SOLDER TAILS
    (A) Ø 2.18 +/- 0.03 FOR LOW PLASTIC PEG INSERTION FORCE
11. A (A) SYMBOL WILL BE NEXT TO ANY DIMENSION , VIEW OR NOTE WHICH HAS BEEN MODIFIED WITH THE CURRENT DRAWING VERSION .

Figure 30. Mating connector drawing page 3

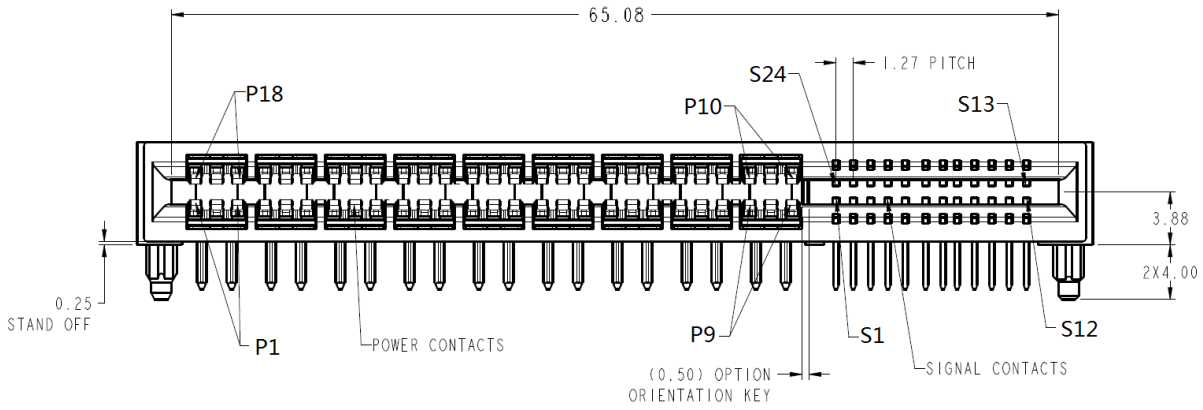


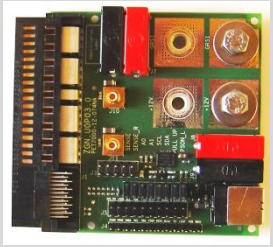
Figure 31. 10139371-1824CLF Rear view

Pin definition for mating output connector 10139371-1824CLF (refer to Figure 31)

PIN	SIGNAL NAME	DESCRIPTION
P1 ~ P5 P15 ~ P18	GND GND	Power and signal ground (return)
P6 ~ P9 P10 ~ P14	V1 V1	+12 VDC main output
S1 S2	A0 A1	I²C address selection input
S3, S4, S21, S22	VSB	+12 V Standby positive output
S5	NC	Not used
S6	ISHARE	Analog current share bus
S7	Reserved	For future use, keep open circuit
S8	PRESENT_L	Power supply seated, active-low
S9	A2 or IN_OK	I2C address selection input (on standard models) or Input voltage OK signal output, active-high (e.g. For PET2000-12-074ND0200)
S10 ~ S15	GND	Power and signal ground (return)
S16	PWOK_H	Power OK signal output, active-high
S17	V1_SENSE	Main output positive sense
S18	V1_SENSE_R	Main output negative sense
S19	SMB_ALERT_L	SMB Alert signal output, active-low
S20	PSON_L	Power supply on input, active-low
S23	SCL	I²C clock signal line
S24	SDA	I²C data signal line

Table 6. Output connector pin assignment for 10139371-1824CLF

20. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor Front-End power supplies (and other I²C units)	ZS-00130	belfuse.com/power-solutions
	**Evaluation Board** Connector board to operate PET2000-12-074NA and PET2000-12-074ND. Includes an on-board USB to I²C converter (use *I²C Utility* as desktop software).	YTM.00046	belfuse.com/power-solutions

21. REVISION HISTORY

DATE	REVISION	ISSUE	PREPARED BY	APPROVED BY	ECO/MCO REFERENCE NO
2019/10/30	AH		r.kaelin	j.schumann	C96708

For more information on these products consult: tech.support@psbel.com

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