# SLDN-20D1A

## Non-Isolated DC-DC Converter


The SLDN-20D1A modules are non-isolated DC-DC converters that can deliver up to 20 A of output current. These modules operate over a wide range of input voltage (Vin = 3-14.4 VDC) and provide a precisely regulated output voltage from 0.6 to 5.5 VDC, programmable via an external resistor and power management bus control.

Features include a digital interface using the power management bus protocol, remote on/off, adjustable output voltage, over current and over temperature protection. The power management bus interface supports a range of commands to both control and monitor the module.

The module also includes the Tunable Loop$^{TM}$ feature that allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

### Key Features & Benefits

- 3 – 14.4 VDC Input
- 0.45 – 5.5 VDC / 20 A Outputs
- Power Good Signal
- Remote On/Off
- Over Temperature Protection
- Cost Efficient Open Frame Design
- Ability to Sink and Source Current
- DOSA Based
- Output Voltage Programmable from 0.6 to 2.0 VDC via External Resistor
- Tunable Loop$^{TM}$ to Optimize Dynamic Output Voltage Response
- Flexible Output Voltage Sequencing EZ-SEQUENCE
- Fixed Switching Frequency with Capability of External Synchronization
- Output Over Current Protection (non-latching)
- Small Size: 20.32 x 11.43 x 8.5 mm (0.8 x 0.45 x 0.334 inch)
- Approved to UL/CSA 60950-1

TUNABLE LOOP™
A LINEAGE POWER TRADEMARK

RoHS Compliant

### Applications

- Distributed Power Architectures
- Servers and Storage Applications
- Intermediate Bus Voltage Applications
- Networking Equipment
- Telecommunications Equipment
- Industrial Equipment

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## 1. MODEL SELECTION

| MODEL NUMBER | OUTPUT VOLTAGE | INPUT VOLTAGE | MAX. OUTPUT CURRENT | MAX. OUTPUT POWER | TYPICAL EFFICIENCY |
|---|---|---|---|---|---|
| SLDN-20D1A0G<br>SLDN-20D1A0R<br>SLDN-20D1ALG<br>SLDN-20D1ALR | 0.45 - 5.5 VDC | 3 - 14.4 VDC | 20 A | 110 W | 95.2% |

### PART NUMBER EXPLANATION

| S | LDN | - | 20 | D | 1A | x | y |
|---|---|---|---|---|---|---|---|
| Mounting Type | Series Code | | Output Current | Input Voltage Range | Sequencing or not | Active Logic | Package |
| Surface Mount | SLDN Series | | 20 A | 3 - 14.4 V | with Sequencing | 0 – Active High<br>L – Active Low | G – Tray Package<br>R – Tape & Reel Package |

## 2. ABSOLUTE MAXIMUM RATINGS

| PARAMETER | DESCRIPTION | MIN | TYP | UNITS |
|---|---|---|---|---|
| Continuous Input Voltage | | -0.3 | 15 | V |
| Voltage on SEQ , SYNC, VS+ | | - | 7 | V |
| Voltage on CLK,DATA, SMBALERT Terminal | | - | 3.6 | V |
| Operating Ambient Temperature | See Thermal Considerations section | -40 | 85 | °C |
| Storage Temperature | | -55 | 125 | °C |
| Altitude | | - | 2000 | m |

**NOTE:** Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

## 3. INPUT SPECIFICATIONS

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Operating Input Voltage | | 3 | - | 14.4 | V |
| Input Current | VIN = 3 to 14 V, IO = IO, max | - | - | 19 | A |
| Input Current (no load) | VO,set = 0.6 VDC; VIN = 12 VDC, IO = 0, module enabled | - | 69 | - | mA |
| | VO,set = 5 VDC; VIN = 12 VDC, IO = 0, module enabled | - | 134 | - | mA |
| Input Stand-by Current | VIN = 12 V, module disabled | - | 16.5 | - | mA |
| Input Reflected Ripple Current (pk-pk) | 1. 5 Hz to 20 MHz, 1 µH source impedance; VIN =0 to 14 V, IO = IO, max<br>2. See Test Configurations | - | 50 | - | mA |
| $I^2t$ Inrush Current Transient | | - | - | 1 | $A^2s$ |
| Input Ripple Rejection (120 Hz) | | - | -64 | - | dB |

**NOTE:** Unless otherwise indicated, specifications apply over entire operating input voltage range, resistive load, and temperature conditions.

## 4. OUTPUT SPECIFICATIONS

| PARAMETER | | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Voltage Set Point | | with 0.1% tolerance for external resistor used to set output voltage | | -1.0 | - | +1.0 | %Vo,set |
| Output Voltage | | Over entire operating input voltage range, resistive load, and temperature conditions until end of life | | -3.0 | - | +3.0 | %Vo,set |
| Power Management Bus Adjustable Output Voltage Range | | | | -25 | 0 | +25 | %Vo,set |
| Power Management Bus Output Voltage Adjustment Step Size | | | | - | 0.4 | - | %Vo,set |
| Adjustment Range | | 1. Selected by an external resistor<br>2. Some output voltages may not be possible depending on the input voltage – see Feature Descriptions Section | | 0.6 | - | 5.5 | V |
| Remote Sense Range | | | | - | - | 0.5 | V |
| Line Regulation | | Vo ≥ 2.5 V | $V_{IN}=V_{IN, min}$ to $V_{IN, max}$ | ±0.17 | ±0.27 | 0.4 | %Vo,set |
| | | Vo < 2.5 V | | - | - | 5 | mV |
| Load Regulation | | Vo ≥ 2.5 V | Io = Io, min to Io, max | - | - | 10 | mV |
| | | Vo < 2.5 V | | - | - | 10 | |
| Temperature Regulation | | Tref = TA, min to TA, max | | - | - | 0.4 | %Vo,set |
| Output Current | | In either sink or source mode | | 0 | - | 20 | mV |
| Output Ripple and Noise (pk-pk) | | 5 Hz to 20 MHz BW, VIN=VIN, nom and $I_O = I_{O, min}$ to $I_{O, max}$, Co = 0.1 µF // 22 µF ceramic capacitors) | | - | 50 | 100 | mV |
| Output Ripple and Noise (rms) | | | | - | 20 | 38 | mV |
| Output Short-Circuit Current | | Vo ≤ 250 mV, Hiccup Mode | | 1.4 | 2.5 | 3.6 | Arms |
| Turn-On Delay and Rise Times (VIN=VIN, nom, IO=IO, max , VO to within ±1% of steady state.) | | Case 1: On/Off input is enabled and then input power is applied (delay from instant at which VIN = VIN, min until Vo = 10% of Vo, set) | | 1.0 | 1.1 | 1.7 | ms |
| | | Case 2: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until Vo = 10% of Vo, set) | | 600 | 700 | 1800 | µs |
| Output Voltage Rise Time | | Time for Vo to rise from 10% of Vo, set to 90% of Vo, set. | | 1.2 | 1.5 | 2.7 | ms |
| Output Capacitance | ESR ≥ 1 mΩ | Without the Tunable Loop™ | | 2x47 | - | 2x47 | µF |
| | ESR ≥ 0.15 mΩ | With the Tunable Loop™ | | 2x47 | - | 1000 | |
| | ESR ≥ 10 mΩ | With the Tunable Loop™ | | 2x47 | - | 10000 | |
| Output Current Limit Inception | | Current limit does not operate in sink mode | | 110 | 130 | 150 | % Io,max |

**NOTE**:
1. Unless otherwise indicated, specifications apply over entire operating input voltage range, resistive load, and temperature conditions.
2. External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

## 5. GENERAL SPECIFICATIONS

| PARAMETER | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Efficiency | Vo=0.6 V | Vin = 12 VDC, TA = 25°C<br>Io = Io, max ,<br>Vo = Vo,set | 76.0 | 79.1 | - | % |
| | Vo=1.2 V | | 84.3 | 87.1 | - | |
| | Vo=1.8 V | | 87.2 | 90.4 | - | |
| | Vo=2.5 V | | 90.3 | 92.6 | - | |
| | Vo=3.3 V | | 91.4 | 93.8 | - | |
| | Vo=5.0 V | | 92.8 | 95.2 | - | |
| Switching Frequency | | | 475 | 500 | 525 | kHz |
| Synchronization Frequency Range | | | 425 | - | 600 | kHz |
| High-Level Input Voltage | | | 2.0 | - | - | V |
| Low-Level Input Voltage | | | - | - | 0.4 | V |
| Input Current, SYNC | | | - | - | 100 | nA |
| Minimum Pulse Width, SYNC | | | 100 | - | - | ns |
| Maximum SYNC Rise Time | | | 100 | - | - | ns |
| Power Management Bus Over Temperature Warning Threshold | | | 120 | 130 | 140 | °C |
| Power Management Bus Adjustable Input Under Voltage Lockout Thresholds | | | 2.5 | - | 14 | V |
| Resolution of Adjustable Input Under Voltage Threshold | | | - | - | 500 | mV |
| Over Temperature Protection | | Tref-Q1 | 123 | 133 | 143 | °C |
| | | Tref-Q4 | 121 | 131 | 141 | |
| Tracking Accuracy | Power-Up: 2 V/ms | Vin, min to Vin, max; Io, min to Io, max, VSEQ < Vo | - | - | 100 | mV |
| | Power-Down: 2 V/ms | | - | - | 100 | |
| PGOOD (Power Good) | Overvoltage threshold for PGOOD ON | Signal Interface Open Drain, Vsupply ≤ 5 VDC | 103 | 108 | 113 | %Vo, set |
| | Overvoltage threshold for PGOOD OFF | | 100 | 105 | 110 | %Vo, set |
| | Undervoltage threshold for PGOOD ON | | 105 | 110 | 115 | %Vo, set |
| | Undervoltage threshold for PGOOD OFF | | 85 | 90 | 95 | %Vo, set |
| | Pulldown resistance of PGOOD pin | | - | - | 50 | Ω |
| | Sink current capability into PGOOD pin | | - | - | 5 | mA |
| Weight | | | 4.086 | 4.54 | 4.994 | g |
| Input Under-voltage Lockout | Turn-on Threshold | | 2.7 | - | 2.95 | V |
| | Turn-off Threshold | | 2.4 | - | 2.75 | |
| | Hysteresis | | 0.05 | - | 0.4 | |
| MTBF | | Calculated MTBF ($I_O$ = 0.8 $I_O$, max, TA = 40°C) Telecordia Issue 2 Method 1 Case 3 | | 15,455,614 | | hours |
| Dimensions (L × W × H) | | | | 0. 800 x 0.450 x 0.334 | | inch |
| | | | | 20.32 x 11.43 x 8.50 | | mm |

**NOTE**: Unless otherwise indicated, specifications apply over entire operating input voltage range, resistive load, and temperature conditions.

## 6. DIGITAL INTERFACE SPECIFICATIONS

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **POWER MANAGEMENT BUS SIGNAL INTERFACE CHARACTERISTICS** | | | | | |
| Input High Voltage (CLK, DATA) | | 2.1 | - | 3.6 | V |
| Input Low Voltage (CLK, DATA) | | - | - | 0.8 | V |
| Input High Level Current (CLK, DATA) | | -10 | - | 10 | µA |
| Input Low Level Current (CLK, DATA) | | -10 | - | 10 | µA |
| Output Low Voltage (CLK, DATA, SMBALERT#) | $I_{out}$ = 2 mA | - | - | 0.4 | V |
| Output High Level Open Drain Leakage Current (DATA, SMBALERT#) | $V_{out}$ = 3.6 V | 0 | - | 10 | µA |
| Pin Capacitance | | - | 0.7 | - | pF |
| Data Hold Time | Receive Mode | 0 | - | - | ns |
| | Transmit Mode | 300 | - | - | |
| Data Setup Time | | 250 | - | - | ns |
| Power Management Bus Operating Frequency Range | | 10 | - | 400 | kHz |
| **MEASUREMENT SYSTEM CHARACTERISTICS** | | | | | |
| Read delay time | | 153 | 192 | 231 | µs |
| Output current measurement range | | 0 | - | 26 | A |
| Output current measurement resolution | | 62.5 | - | - | mA |
| Output current measurement gain accuracy | | - | - | ±5 | % |
| Output current measurement offset | | - | - | 0.1 | A |
| VOUT measurement range | | 0 | - | 5.5 | V |
| VOUT measurement resolution | | - | 15.625 | - | mV |
| VOUT measurement gain accuracy | | -15 | - | 5 | % |
| VOUT measurement offset | | -3 | - | 3 | % |
| VIN measurement range | | 0 | - | 14.4 | V |
| VIN measurement resolution | | - | 32.5 | - | mV |
| VIN measurement gain accuracy | | -15 | - | 5 | % |
| VIN measurement offset | | -5.5 | -2 | 1.4 | LSB |

**NOTE**: Unless otherwise indicated, specifications apply over entire operating input voltage range, resistive load, and temperature conditions. See Feature Descriptions for additional information.


Asia-Pacific
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+353 61 225 977
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+1 408 785 5200

## 7. EFFICIENCY DATA

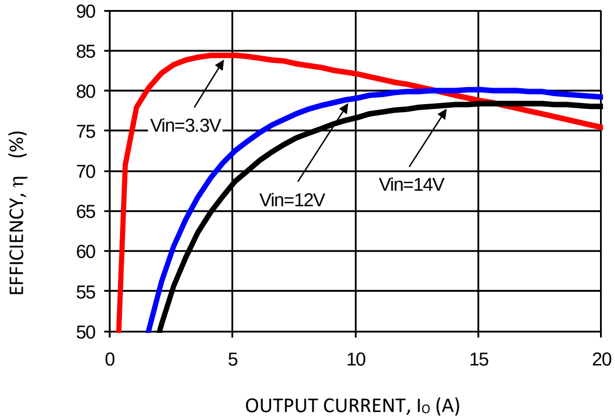



*Figure 1. Vo = 0.6 V*

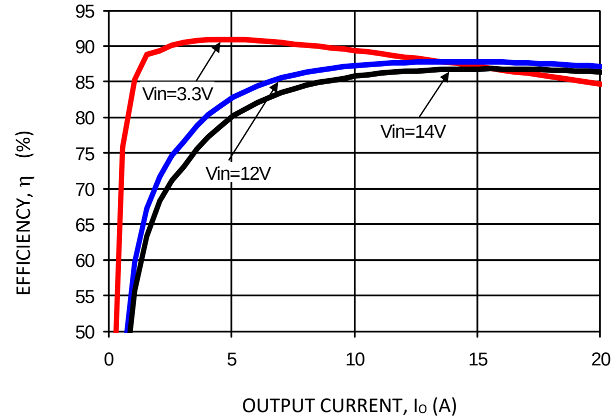



*Figure 2. Vo = 1.2 V*

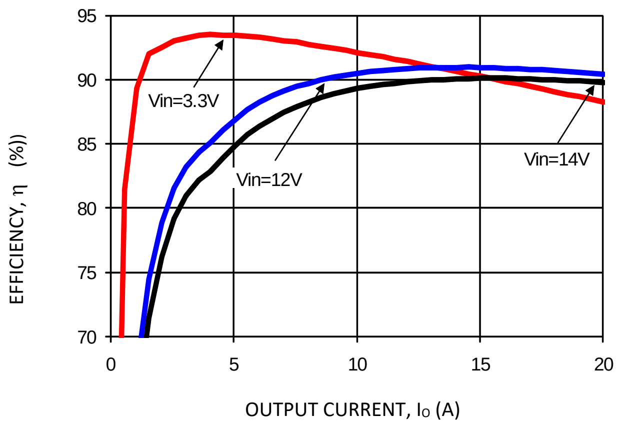



*Figure 3. Vo =1.8 V*

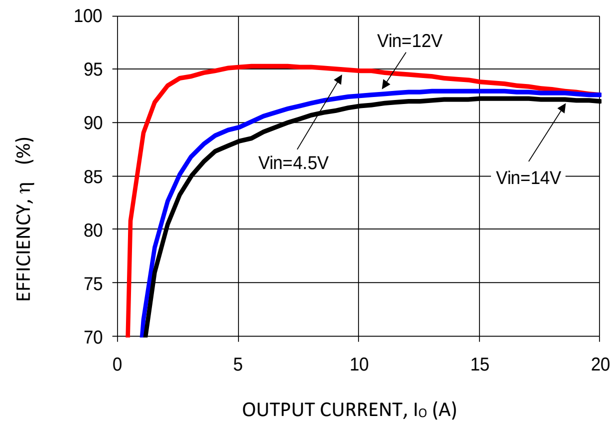



*Figure 4. Vo = 2.5 V*

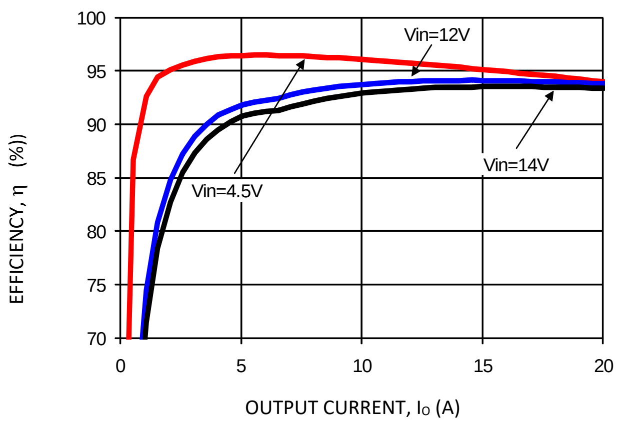



*Figure 5. Vo = 3.3 V*

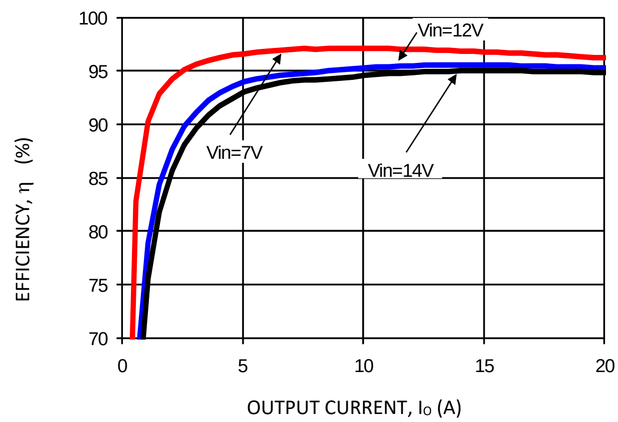



*Figure 6. Vo = 5.0 V*

## 8. THERMAL DERATING CURVES

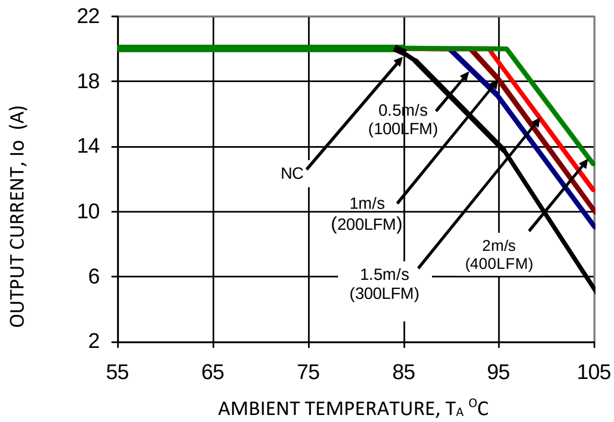



*Figure 7. Vo = 0.6 V*

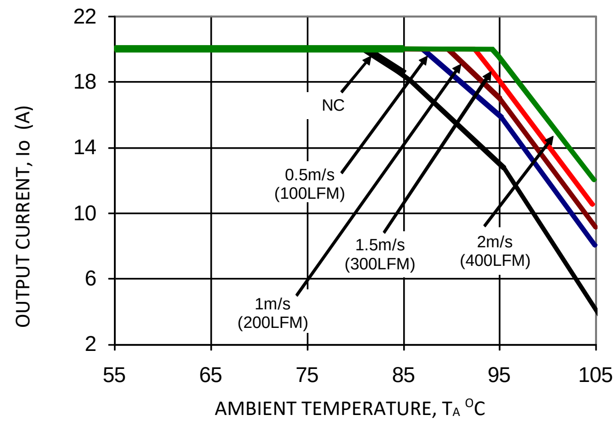



*Figure 8. Vo = 1.2 V*

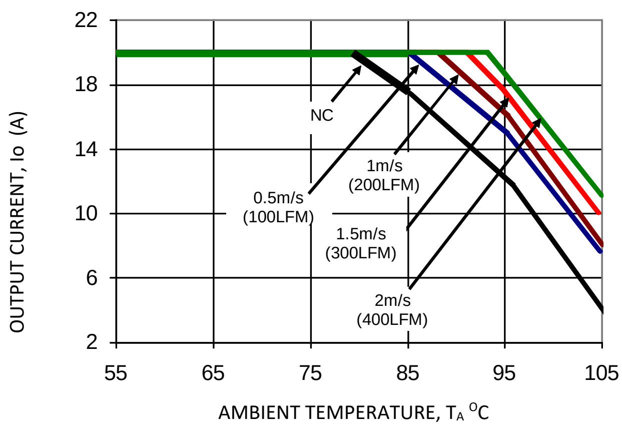



*Figure 9. Vo = 1.8 V*

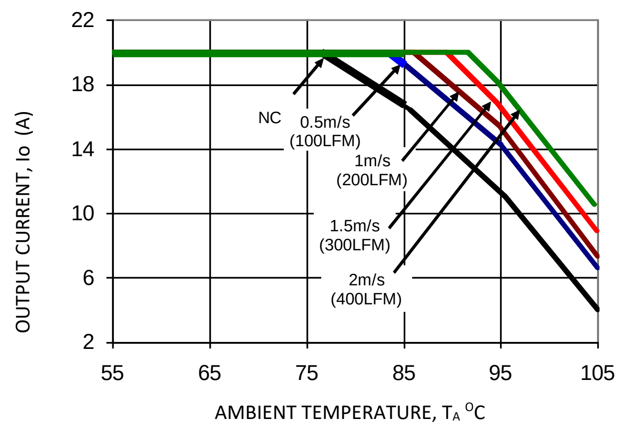



*Figure 10. Vo = 2.5 V*

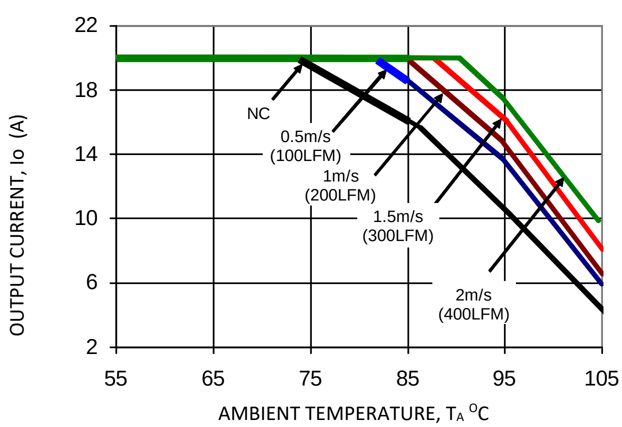



*Figure 11. Vo = 3.3 V*

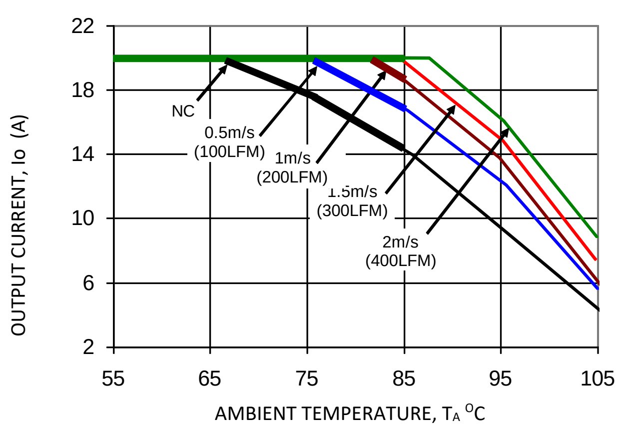



*Figure 12. Vo = 5.0 V*

## 9. OUTPUT RIPPLE AND NOISE WAVEFORMS

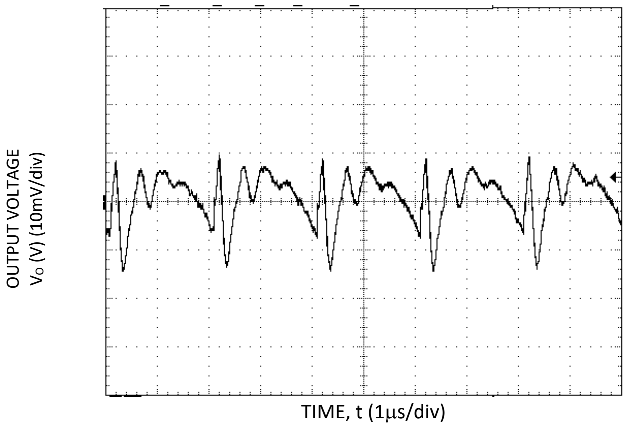



*Figure 13. Vo = 0.6 V, Io = Io, max*

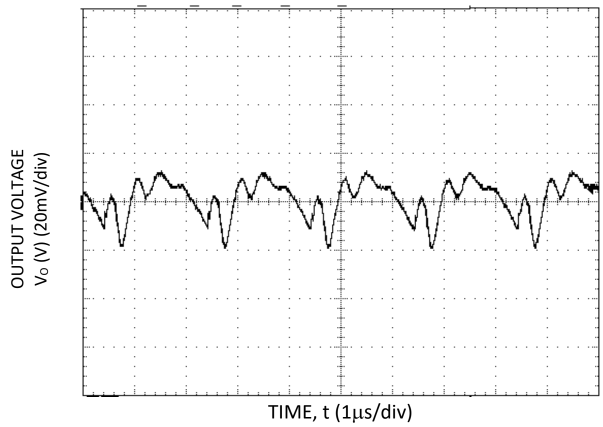



*Figure 14. Vo = 1.2 V, Io = Io, max*

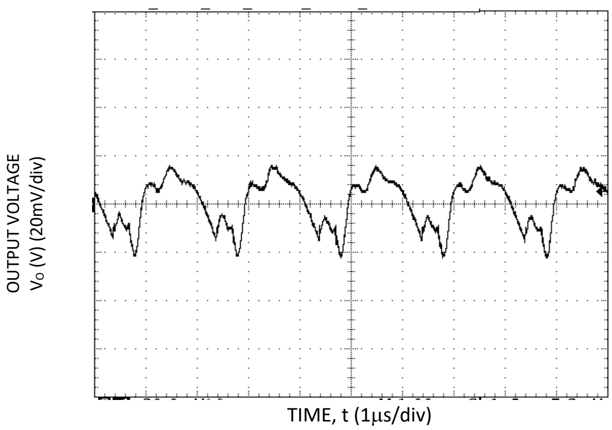



*Figure 15. Vo = 1.8 V, Io = Io, max*

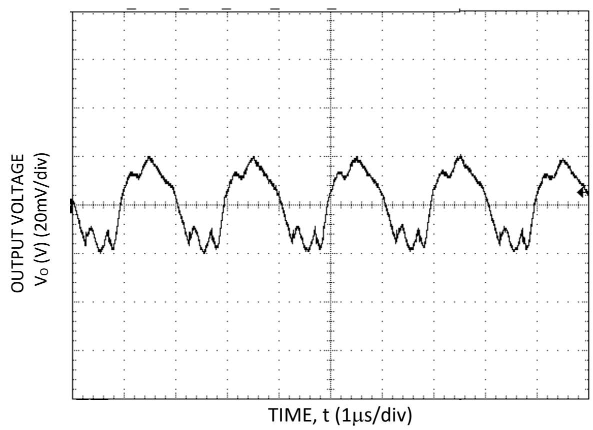



*Figure 16. Vo = 2.5 V, Io = Io, max*

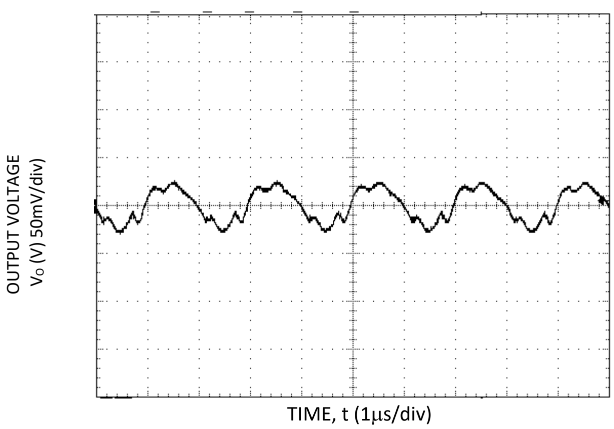



*Figure 17. Vo = 3.3 V, Io = Io, max*

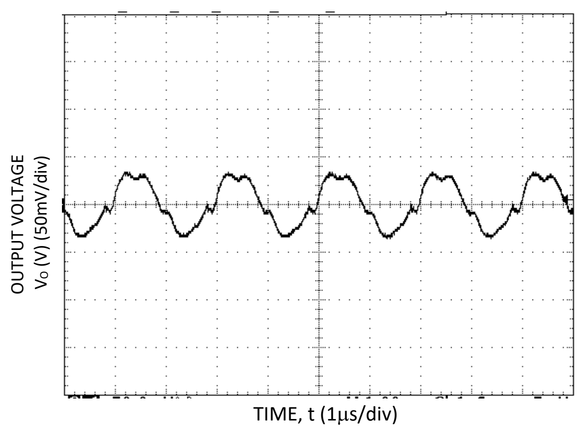



*Figure 18. Vo = 5.0 V, Io = Io, max*

## 10. TRANSIENT RESPONSE

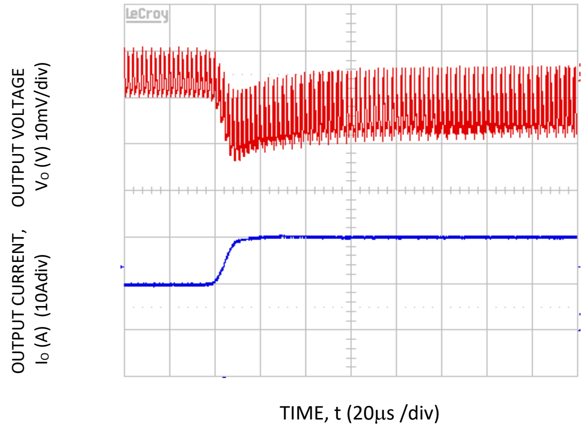



*Figure 19. Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout = 1x 47 µF + 11x 330 µF CTune = 47 nF, RTune = 178 ohms. Vo = 0.6 V*

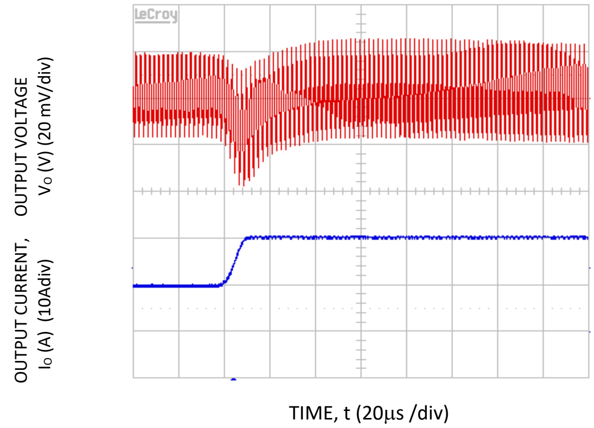



*Figure 20. Transient Response to Dynamic Load Change from 50% to 100% at 12 Vin, Cout = 1x 47 µF + 5x 330 µF, CTune = 10 nF & RTune = 178 ohms. Vo = 1.2 V*

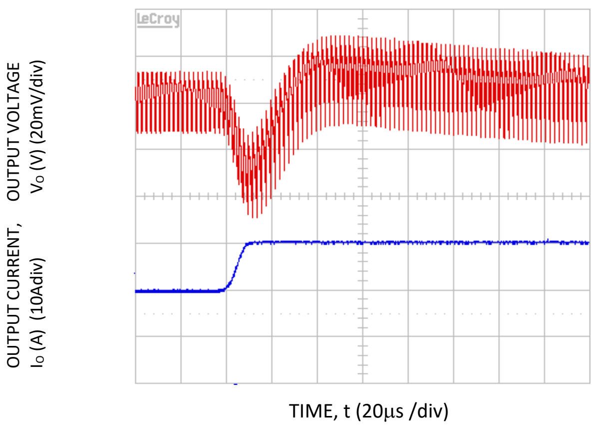



*Figure 21. Transient Response to Dynamic Load Change from 50% to 100% at 12 Vin, Cout = 2x 47 µF + 3x 330 µF, CTune = 5600 pF & RTune = 220 ohms . Vo = 1.8 V*

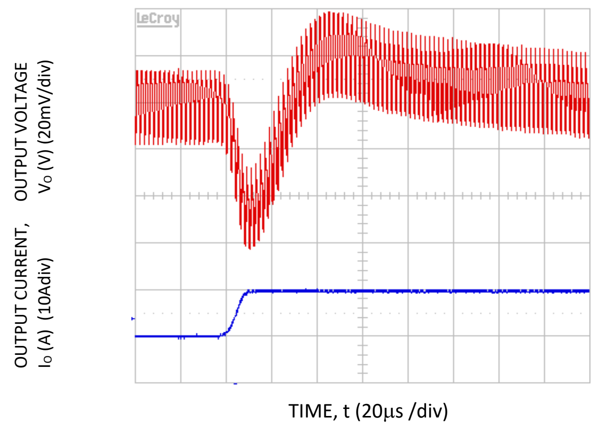



*Figure 22. Transient Response to Dynamic Load Change from 50% to 100% at 12 Vin, Cout = 2x 47 µF + 2x 330 µF, CTune = 3300 pF & RTune = 220 ohms . Vo = 2.5 V*

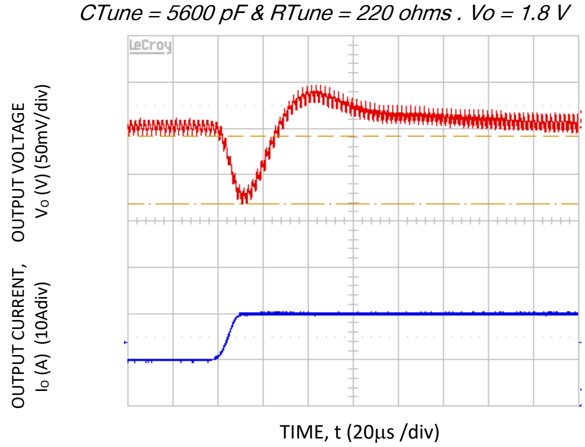



*Figure 23. Transient Response to Dynamic Load Change from 50% to 100% at 12 Vin, Cout = 5x 47 µF +1x 330 µF, CTune = 2200 pF & RTune = 220 ohms. Vo = 3.3 V*

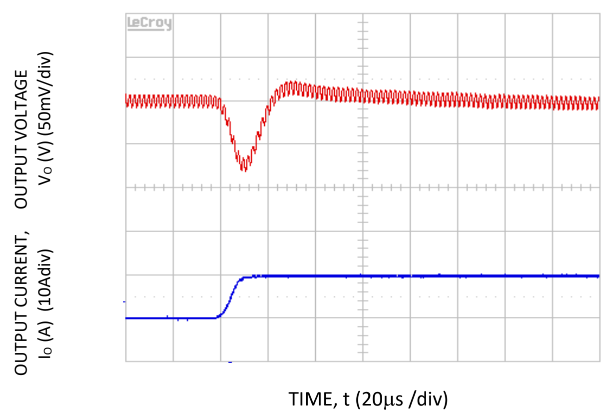



*Figure 24. Transient Response to Dynamic Load Change from 50% to 100% at 12 Vin, Cout = 8x 47 µF, CTune = 1500 pF & RTune = 220 ohms. Vo = 5.0 V*



## 11. STARTUP TIME

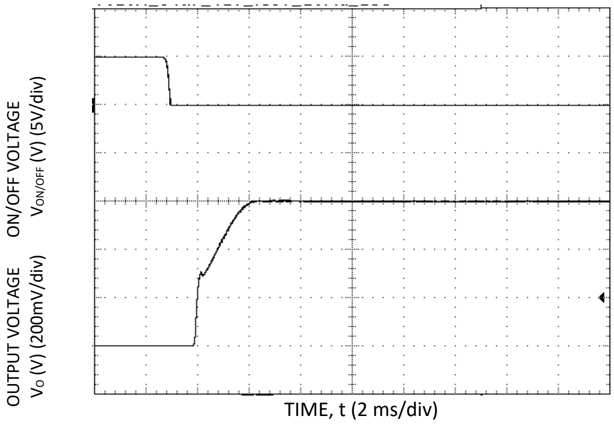



*Figure 25. Start-up Using On/Off Voltage (Io = Io,max), Vo = 0.6 V*

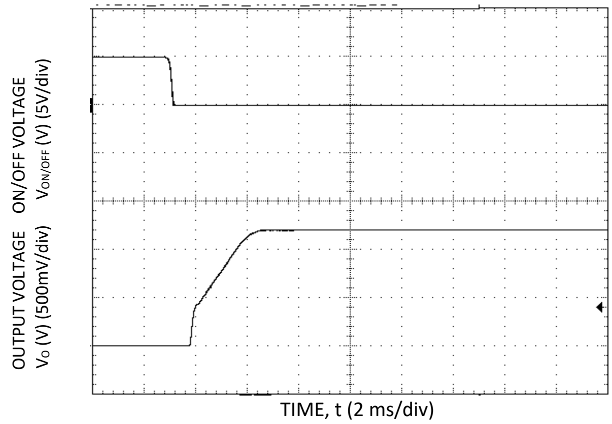



*Figure 26. Start-up Using On/Off Voltage (Io = Io,max), Vo = 1.2 V*

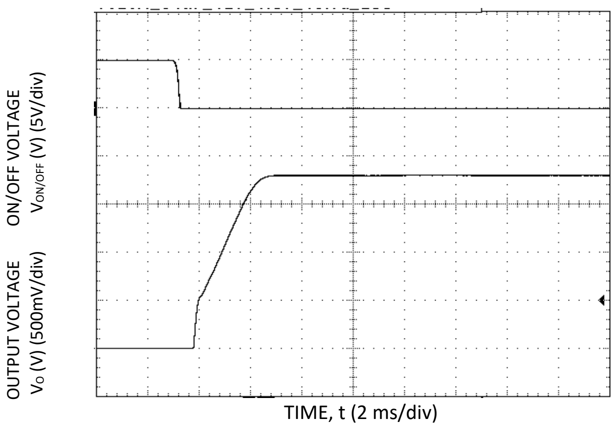



*Figure 27. Start-up Using On/Off Voltage (Io = Io,max), Vo = 1.8 V*

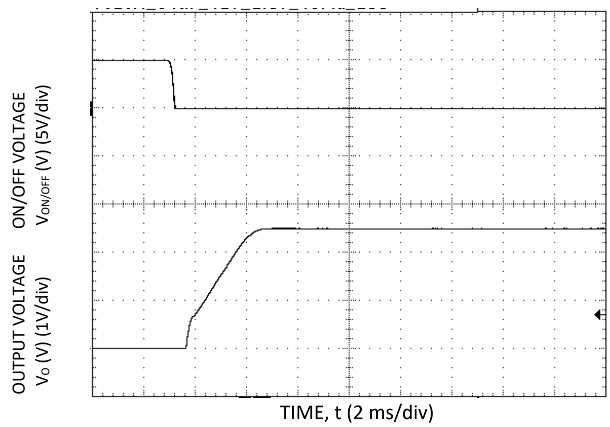



*Figure 28. Start-up Using On/Off Voltage (Io = Io,max), Vo = 2.5 V*

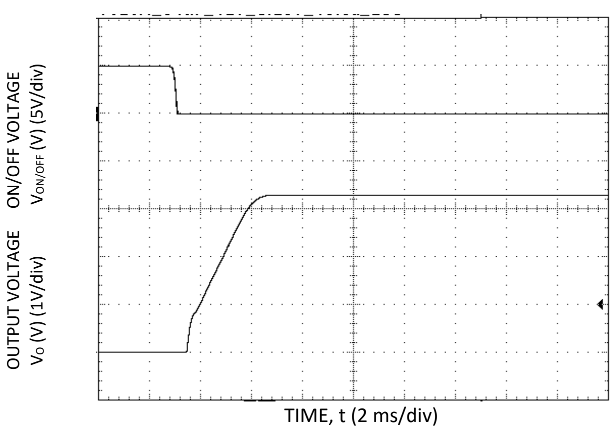



*Figure 29. Start-up Using On/Off Voltage (Io = Io,max), Vo = 3.3 V*

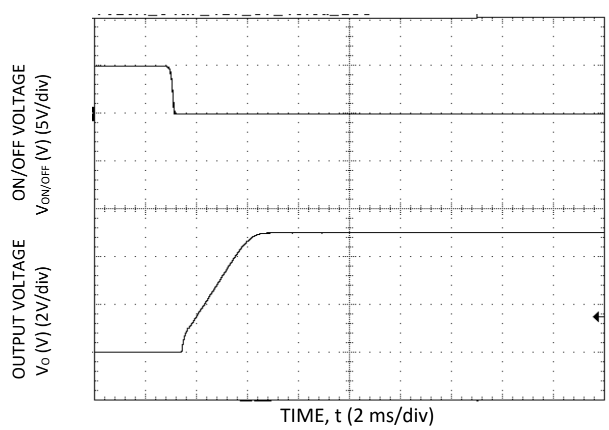



*Figure 30. Start-up Using On/Off Voltage (Io = Io,max), Vo = 5.0 V*

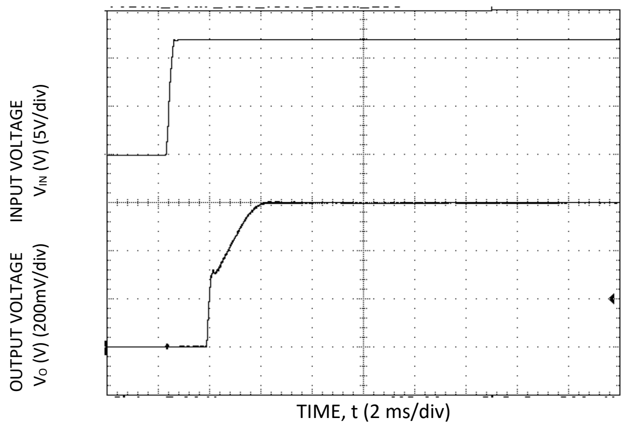



*Figure 31. Start-up Using Input Voltage (VIN = 12V, Io = Io,max ), Vo = 0.60 V*

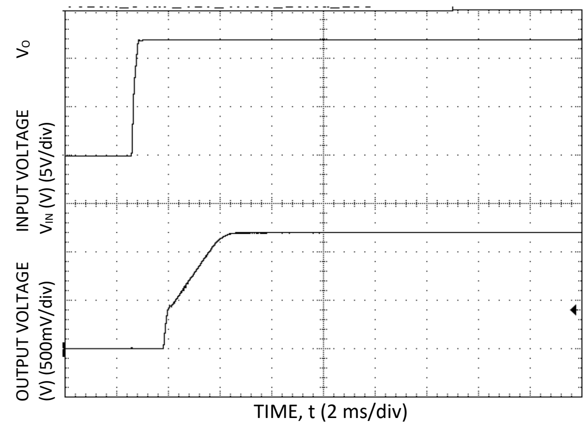



*Figure 32. Start-up Using Input Voltage (VIN = 12V, Io = Io,max ), Vo = 1.2 V*

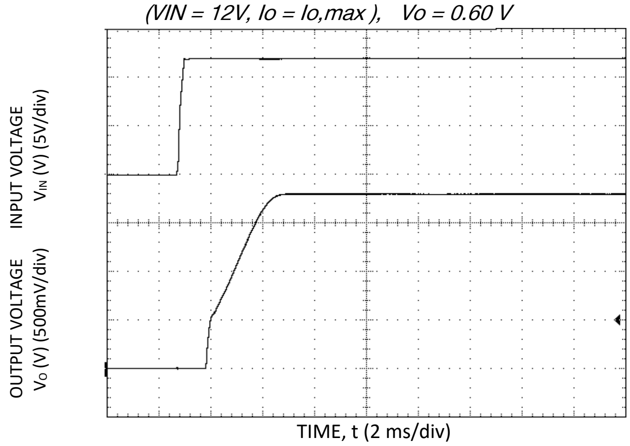



*Figure 33. Start-up Using Input Voltage (VIN = 12V, Io = Io,max ), Vo = 1.8 V*

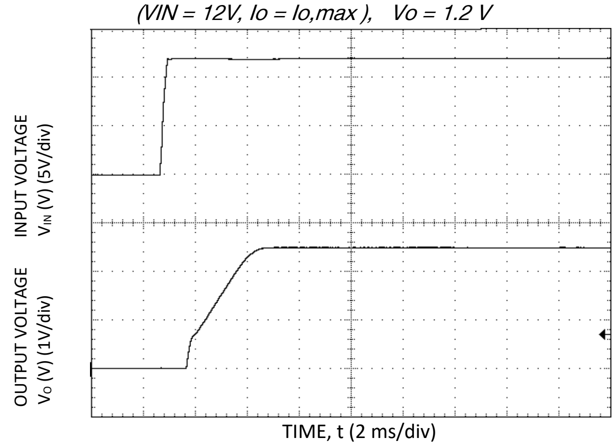



*Figure 34. Start-up Using Input Voltage (VIN = 12V, Io = Io,max ), Vo = 2.5 V*

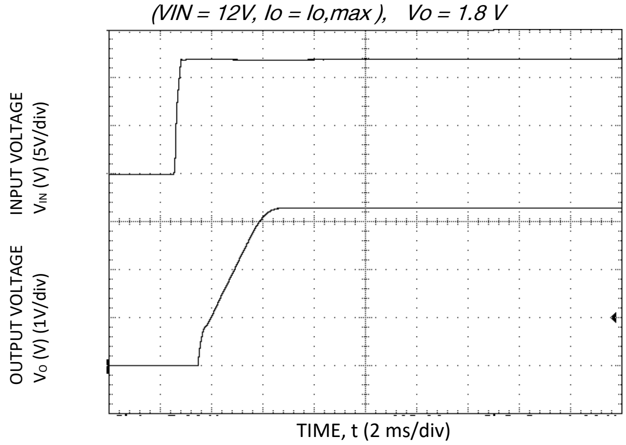



*Figure 35. Start-up Using Input Voltage (VIN = 12V, Io = Io,max ), Vo = 3.3 V*

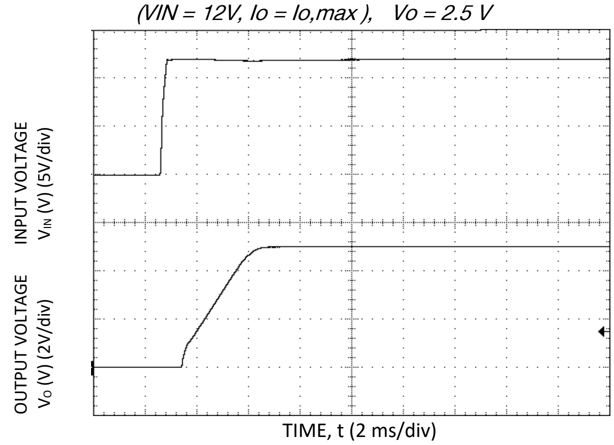



*Figure 36. Start-up Using Input Voltage (VIN = 12V, Io = Io,max ), Vo = 5.0 V*

## 12. DESIGN CONSIDERATIONS

### INPUT FILTERING

The SLDN-20D1A module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.
To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 37 shows the input ripple voltage for various output voltages at 20A of load current with 2x22 μF or 3x22 μF ceramic capacitors and an input of 12V.

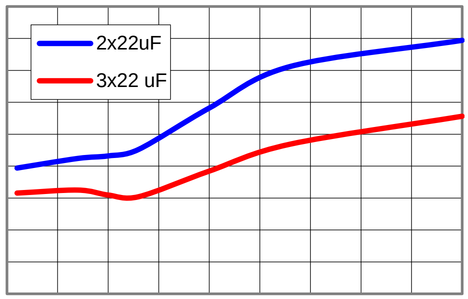



*Figure 37. Output Voltage (VDC)*

**NOTE**: Input ripple voltage for various output voltages with various external ceramic capacitors at the input (40A load). Input voltage is 12V. Scope Bandwidth limited to 20 MHz.

### OUTPUT FILTERING

These modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1 μF ceramic and 2x47 μF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figure 38 provides output ripple information for different external capacitance values at various Vo and a full load current of 20A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop$^{TM}$ feature described later in this data sheet.

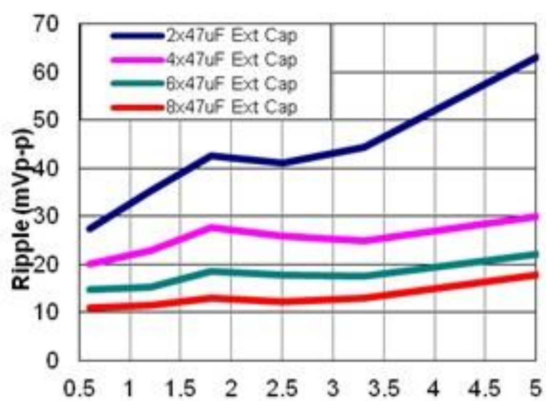



*Figure 38.*

**NOTE:** Output ripple voltage for various output voltages with external 2x47 µF, 4x47 µF or 6x47 µF ceramic capacitors at the output (20A load). Input voltage is 12V.

### SAFETY CONSIDERATIONS

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1 2nd, CSA C22.2 No. 60950-1-07.
For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.
The SLDN-20D1A series were tested using an external fast-acting fuse rated at 30 A, 100 VDC in the ungrounded input.

## 13. ANALOG FEATURE DESCRIPTIONS

### REMOTE ON/OFF

| PARAMETER | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Signal Low (Unit On) | Active Low | The remote on/off pin open, Unit on. | -0.2 | - | 0.6 | V |
| Signal High (Unit Off) | | | 2.0 | - | VIn,max | |
| Signal Low (Unit Off) | Active High | The remote on/off pin open, Unit on. | -0.2 | - | 0.6 | V |
| Signal High (Unit On) | | | 2.0 | - | VIn,max | |

For negative logic On/Off modules, the circuit configuration is shown in Figure. 9.
The SLDN-20D1A module can be turned ON and OFF either by using the ON/OFF pin (Analog interface) or through the Power Management Bus interface (Digital). The module can be configured in a number of ways through the Power Management Bus interface to react to the two ON/OFF inputs:

- Module ON/OFF can be controlled only through the analog interface (digital interface ON/OFF commands are ignored)
- Module ON/OFF can be controlled only through the Power Management Bus interface (analog interface is ignored)
- Module ON/OFF can be controlled by either the analog or digital interface.

The default state of the module (as shipped from the factory) is to be controlled by the analog interface only. If the digital interface is to be enabled, or the module is to be controlled only through the digital interface, this change must be made through the Power Management Bus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

### ANALOG ON/OFF

The SLDN-20D1A modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix “0” – see Ordering Information), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (device code suffix “L” – see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.
For positive logic modules, the circuit configuration for using the On/Off pin is shown in Figure 39. When the external transistor Q2 is in the OFF state, the internal transistor Q7 is turned OFF, which keeps Q6 OFF and Q5 OFF. This allows the internal PWM #Enable signal to be pulled up by the internal 3.3V, thus turning the module ON. When transistor Q2 is turned ON, the On/Off pin is pulled low, which turns Q7, Q6 and Q5 ON and the internal PWM #Enable signal is pulled low and the module is OFF. A suggested value for Rpullup is 20kΩ.
For negative logic On/Off modules, the circuit configuration is shown in Fig. 40. The On/Off pin should be pulled high with an external pull-up resistor (suggested value for the 3V to 14V input range is 20Kohms). When transistor Q2 is in the OFF state, the On/Off pin is pulled high, transistor Q3 is turned ON. This turns Q6 ON, followed by Q5 turning ON which pulls the internal ENABLE low and the module is OFF. To turn the module ON, Q2 is turned ON pulling the On/Off pin low, turning transistor Q3 OFF, which keeps Q6 and Q5 OFF resulting in the PWM Enable pin going high.

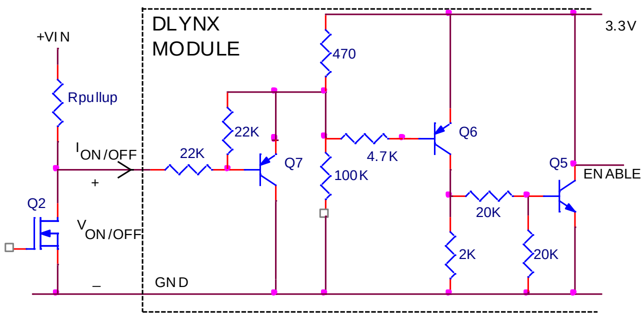



*Figure 39. Circuit configuration for using positive On/Off logic*

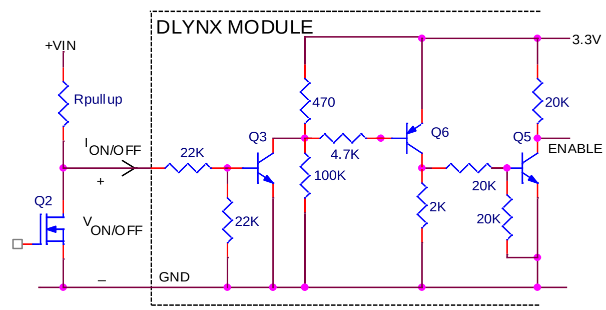



*Figure 40. Circuit configuration for using positive On/Off logic*

### DIGITAL ON/OFF

Please see the Digital Feature Descriptions section.

## 14. MONOTONIC START-UP AND SHUTDOWN

The SLDN-20D1A module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

## 15. STARTUP INTO PRE-BIASED OUTPUT

The SLDN-20D1A module can start into a pre-biased output as long as the pre-bias voltage is 0.5V less than the set output voltage.

## 16. ANALOG OUTPUT VOLTAGE PROGRAMMING

The output voltage of the module is programmable to any voltage from 0.6DC to 5.5VDC by connecting a resistor between the Trim and SIG_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig. 41. The Upper Limit curve shows that for output voltages lower than 1V, the input voltage must be lower than the maximum of 14.4V. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 3V.

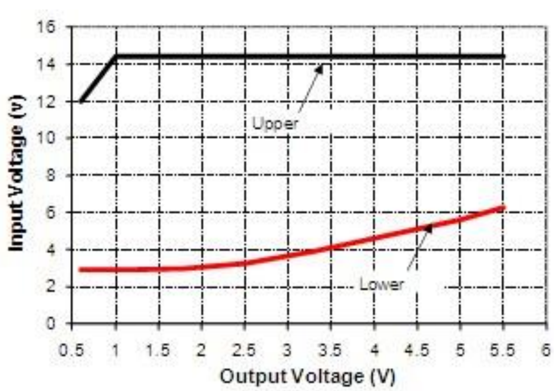



*Figure 41.*

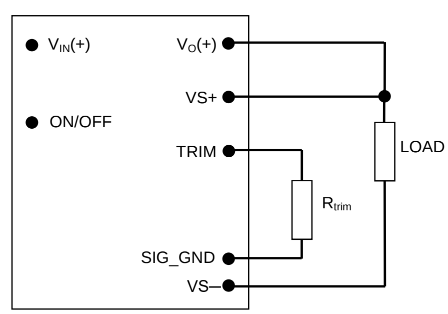



*Figure 42.*

**NOTE**: Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

**CAUTION** – Do not connect SIG_GND to GND elsewhere in the layout.
Circuit configuration for programming output voltage using an external resistor.

Without an external resistor between Trim and SIG_GND pins, the output of the module will be 0.6 VDC.To calculate the value of the trim resistor, Rtrim for a desired output voltage, should be as per the following equation:

$$Rtrim = \left[\frac{12}{(Vo - 0.6)}\right] k\Omega$$

Rtrim is the external resistor in kΩ
*Vo* is the desired output voltage.

Table 1 provides Rtrim values required for some common output voltages.

| VO, set (V) | RTRIM (KΩ) |
|---|---|
| 0.6 | Open |
| 0.9 | 40 |
| 1.0 | 30 |
| 1.2 | 20 |
| 1.5 | 13.33 |
| 1.8 | 10 |
| 2.5 | 6.316 |
| 3.3 | 4.444 |
| 5.0 | 2.727 |

*Table 1.*

## 17. DIGITAL OUTPUT VOLTAGE ADJUSTMENT

Please see the Digital Feature Descriptions section.

## 18. REMOTE SENSE

The SLDN-20D1A power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the VOUT and GND pins of the module should not exceed 0.5V.

## 19. ANALOG VOLTAGE MARGINING

Output voltage margining can be implemented in the module by connecting a resistor, Rmargin-up, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, Rmargin-down, from the Trim pin to output pin for margining-down. Figure 43 shows the circuit configuration for output voltage margining. Please consult your local Bel Power technical representative for additional details.

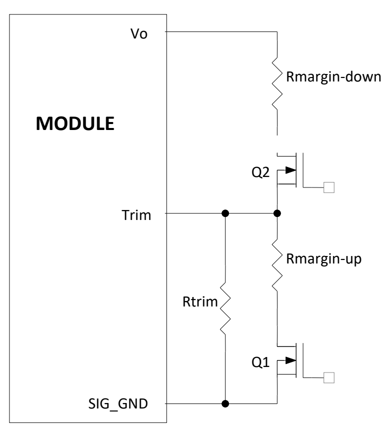


*Figure 43. Circuit Configuration for margining Output voltage*

## 20. DIGITAL OUTPUT VOLTAGE MARGINING

Please see the Digital Feature Descriptions section.

## 21. OUTPUT VOLTAGE SEQUENCING

The SLDN-20D1A module includes a sequencing feature, EZ-SEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.
The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig. 44. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.
For SLDN-20D1A modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.

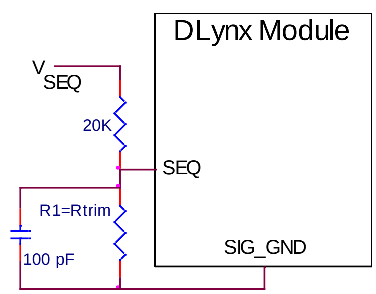



*Figure 44. Circuit showing connection of the sequencing signal to the SEQ pin*

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.
To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage ust be maintained until the tracking and output voltages reach ground potential.
Note that in all digital Bel series of modules, the Power Management Bus Output Undervoltage Fault will be tripped when sequencing is employed. This will be detected using the STATUS_WORD and STATUS_VOUT Power Management Bus commands. In addition, the SMBALERT# signal will be asserted low as occurs for all faults and warnings. To avoid the module shutting down due to the Output Undervoltage Fault, the module must be set to continue operation without interruption as the response to this fault (see the description of the Power Management Bus command VOUT_UV_FAULT_RESPONSE for additional information).

## 22. OVERCURRENT PROTECTION

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

## 23. DIGITAL ADJUSTABLE OVERCURRENT WARNING

Please see the Digital Feature Descriptions section.

## 24. OVERTEMPERATURE PROTECTION

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of 128°C ~ 130°C is exceeded at the thermal reference point Tref .Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

## 25. INPUT UNDERVOLTAGE LOCKOUT

Please see the Digital Feature Descriptions section.

## 26. DIGITAL TEMPERATURE STATUS VIA POWER MANAGEMENT BUS

Please see the Digital Feature Descriptions section.

## 27. DIGITALLY ADJUSTABLE OUTPUT OVER AND UNDER VOLTAGE PROTECTION

Please see the Digital Feature Descriptions section.

## 28. INPUT UNDERVOLTAGE LOCKOUT

At input voltages below the input undervoltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the undervoltage lockout turn-on threshold.

## 29. DIGITALLY ADJUSTABLE INPUT UNDERVOLTAGE LOCKOUT

Please see the Digital Feature Descriptions section.

## 30. DIGITALLY ADJUSTABLE POWER GOOD THRESHOLDS

Please see the Digital Feature Descriptions section.

## 31. MEASURING OUTPUT CURRENT, OUTPUT VOLTAGE AND INPUT VOLTAGE

Please see the Digital Feature Descriptions section.

## 32. DUAL LAYOUT

Identical dimensions and pin layout of Analog and Digital modules permit migration from one to the other without needing to change the layout. In both cases the trim resistor is connected between trim and signal ground. The output of the analog module cannot be trimmed down to 0.45V.

## 33. POWER GOOD

The SLDN-20D1A module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going ±10% outside the setpoint value. The PGOOD terminal can be connected through a pullup resistor (suggested value 100KΩ) to a source of 5VDC or lower.

## 34. TUNABLE LOOP™

The SLDN-20D1A has a feature that optimizes transient response of the module called Tunable Loop™.
External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise (see Figure 38) and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to Become unstable.
The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the VS+ and TRIM pins of the module, as shown in Fig. 45. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

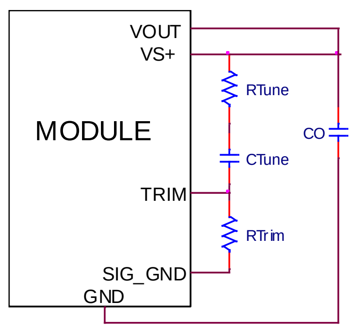



*Figure 45. Circuit diagram showing connection of $R_{TUNE}$ and $C_{TUNE}$ to tune the control loop of the module.*

Recommended values of $R_{TUNE}$ and $C_{TUNE}$ for different output capacitor combinations are given in Tables 2 and 3. Table 3 shows the recommended values of $R_{TUNE}$ and $C_{TUNE}$ for different values of ceramic output capacitors up to 1000μF that might be needed for an application to meet output ripple and noise requirements. Selecting $R_{TUNE}$ and $C_{TUNE}$ according to Table 3 will ensure stable operation of the module. In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of $R_{TUNE}$ and $C_{TUNE}$ in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 10A to 20A step change (50% of full load), with an input voltage of 12V.

Please contact your Bel Power technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values.

| Co | 2x 47 μF | 4x 47 μF | 6x 47 μF | 10x 47 μF | 20x 47 μF |
|---|---|---|---|---|---|
| $R_{TUNE}$ | 330 Ω | 330 Ω | 270 Ω | 330 Ω | 180 Ω |
| $C_{TUNE}$ | 47 pF | 560 pF | 1200 pF | 2200 pF | 4700 pF |

*Table 2.*

General recommended values of of $R_{TUNE}$ and $C_{TUNE}$ for Vin=12V and various external ceramic capacitor combinations.

| Vo | 5 V | 3.3 V | 2.5 V | 1.8 V | 1.2 V | 0.6 V |
|---|---|---|---|---|---|---|
| Co | 8x 47 µF | 5x 47 µF + 1x 330 µF Polymer | 2x 47 µF + 2x 330 µF Polymer | 2x 47 µF + 3x 330 µF Polymer | 1x 47 µF + 5x 330 µF Polymer | 1x 47 µF +11x 330 µF Polymer |
| $R_{TUNE}$ | 220 Ω | 220 Ω | 220 Ω | 220 Ω | 180 Ω | 180 Ω |
| $C_{TUNE}$ | 1500 pF | 2200 pF | 3300 pF | 5600 pF | 10 nF | 47 nF |
| ΔV | 100 mV | 64 mV | 49 mV | 36 mV | 24 mV | 12 mV |

*Table 3.*

Recommended values of $R_{TUNE}$ and $C_{TUNE}$ to obtain transient deviation of 2% of Vout for a 10A step load with Vin=12V.

**NOTE**: The capacitors used in the Tunable Loop tables are 47 µF/3 mΩ ESR ceramic and 330 µF/12 mΩ ESR polymer capacitors.

# 35. DIGITAL FEATURE DESCRIPTIONS

## POWER MANAGEMENT BUS INTERFACE CAPABILITY

The SLDN-20D1A modules have a Power Management Bus interface that supports both communication and control. The Power Management Bus Power Management Protocol Specification can be obtained from www.Power Management Bus.org. The modules support a subset of version 1.1 of the specification (see Table 6 for a list of the specific commands supported). Most module parameters can be programmed using Power Management Bus and stored as defaults for later use.

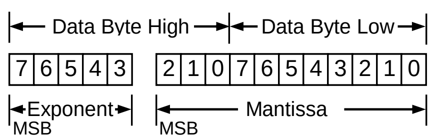
The module also supports the SMBALERT response protocol whereby the module can alert the bus master if it wants to talk. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The module has non-volatile memory that is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory, only those specifically identified as capable of being stored can be saved (see Table 6 for which command parameters can be saved to non-volatile storage).

The module has non-volatile memory that is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory, only those specifically identified as capable of being stored can be saved (see Table 6 for which command parameters can be saved to non-volatile storage).

## POWER MANAGEMENT BUS DATA FORMAT

For commands that set thresholds, voltages or report such quantities, the module supports the “Linear” data format among the three data formats supported by Power Management Bus. The Linear Data Format is a two byte value with an 11-bit, two’s complement mantissa and a 5-bit, two’s complement exponent. The format of the two data bytes is shown below:




**NOTE**: The value is of the number is then given by

Value = Mantissa x 2 $^{Exponent}$

## POWER MANAGEMENT BUS ADDRESSING

The SLDN-20D1A module can be addressed through the Power Management Bus using a device address. The module has 64 possible addresses (0 to 63 in decimal) which can be set using resistors connected from the ADDR0 and ADDR1 pins to GND. Note that some of these addresses (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 12, 40, 44, 45, 55 in decimal) are reserved according to the SMBus specifications and may not be useable. The address is set in the form of two octal (0 to 7) digits, with each pin setting one digit. The ADDR1 pin sets the high order digit and ADDR0 sets the low order digit. The resistor values suggested for each digit are shown in Table 4 (1% tolerance resistors are recommended). Note that if either address resistor value is outside the range specified in Table 4, the module will respond to address 127.

| DIGIT | RESISTOR VALUE (KΩ) |
|---|---|
| 0 | 10 |
| 1 | 15.4 |
| 2 | 23.7 |
| 3 | 36.5 |
| 4 | 54.9 |
| 5 | 84.5 |
| 6 | 130 |
| 7 | 200 |

*Table 4.*

The user must know which I2C addresses are reserved in a system for special functions and set the address of the module to avoid interfering with other system operations. Both 100kHz and 400kHz bus speeds are supported by the module. Connection for the Power Management Bus interface should follow the High Power DC specifications given in section 3.1.3 in the SMBus specification V2.0 for the 400kHz bus speed or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

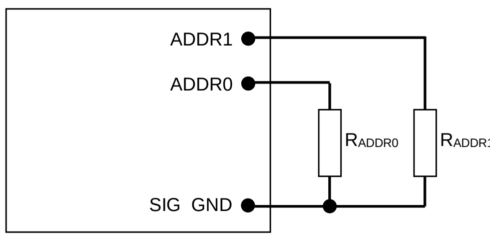



*Figure 46. Circuit showing connection of resistors used to set the Power Management Bus address of the module.*

## POWER MANAGEMENT BUS ENABLED ON/OFF

The module can also be turned on and off via the Power Management Bus interface. The OPERATION command is used to actually turn the module on and off via the Power Management Bus, while the ON_OFF_CONFIG command configures the combination of analog ON/OFF pin input and Power Management Bus commands needed to turn the module on and off. Bit [7] in the OPERATION command data byte enables the module, with the following functions:

0 : Output is disabled

1 : Output is enabled

This module uses the lower five bits of the ON_OFF_CONFIG data byte to set various ON/OFF options as follows:

| BIT POSITION | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| ACCESS | r/w | r/w | r/w | r/w | r |
| FUNCTION | PU | CMD | CPR | POL | CPA |
| DEFAULT VALUE | **1** | **0** | **1** | **1** | **1** |

PU: Sets the default to either operate any time input power is present or for the ON/OFF to be controlled by the analog ON/OFF input and the Power Management Bus OPERATION command. This bit is used together with the CP, CMD and ON bits to determine startup.

| BIT VALUE | ACTION |
|---|---|
| 0 | Module powers up any time power is present regardless of state of the analog ON/OFF pin |
| 1 | Module does not power up until commanded by the analog ON/OFF pin and the OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register. |

CMD: The CMD bit controls how the device responds to the OPERATION command.

| BIT VALUE | ACTION |
|---|---|
| 0 | Module ignores the ON bit in the OPERATION command |
| 1 | Module responds to the ON bit in the OPERATION command |

CPR: Sets the response of the analog ON/OFF pin. This bit is used together with the CMD, PU and ON bits to determine startup.

| BIT VALUE | ACTION |
|---|---|
| 0 | Module ignores the analog ON/OFF pin, i.e. ON/OFF is only controlled through the POWER MANAGEMENT BUS via the OPERATION command |
| 1 | Module requires the analog ON/OFF pin to be asserted to start the unit |

## POWER MANAGEMENT BUS ADJUSTABLE SOFT START RISE TIME

The soft start rise time can be adjusted in the module via Power Management Bus. When setting this parameter, make sure that the charging current for output capacitors can be delivered by the module in addition to any load current to avoid nuisance tripping of the overcurrent protection circuitry during startup. The TON_RISE command sets the rise time in ms, and allows choosing soft start times between 600µs and 9ms, with possible values listed in Table 5. Note that the exponent is fixed at -4 (decimal) and the upper two bits of the mantissa are also fixed at 0.

| RISE TIME | EXPONENT | MANTISSA |
|---|---|---|
| 600µs | 11100 | 00000001010 |
| 900µs | 11100 | 00000001110 |
| 1.2ms | 11100 | 00000010011 |
| 1.8ms | 11100 | 00000011101 |
| 2.7ms | 11100 | 00000101011 |
| 4.2ms | 11100 | 00001000011 |
| 6.0ms | 11100 | 00001100000 |
| 9.0ms | 11100 | 00010010000 |

*Table 5.*

## OUTPUT VOLTAGE ADJUSTMENT USING THE POWER MANAGEMENT BUS

The VOUT_SCALE_LOOP parameter is important for a number of Power Management Bus commands related to output voltage trimming, margining, over/under voltage protection and the PGOOD thresholds. The output voltage of the module is set as the combination of the voltage divider formed by RTrim and a 20kΩ upper divider resistor inside the module, and the internal reference voltage of the module. The reference voltage VREF is nominally set at 600mV, and the output regulation voltage is then given by

$$V_{OUT} = \left[\frac{20000 + RTrim}{RTrim}\right] \times V_{REF}$$

Hence the module output voltage is dependent on the value of RTrim which is connected external to the module. The information on the output voltage divider ratio is conveyed to the module through the VOUT_SCALE_LOOP parameter which is calculated as follows:

$$VOUT\_SCALE\_LOOP = \frac{RTrim}{20000 + RTrim}$$

The VOUT_SCALE_LOOP parameter is specified using the "Linear" format and two bytes. The upper five bits [7:3] of the high byte are used to set the exponent which is fixed at –9 (decimal). The remaining three bits of the high byte [2:0] and the eight bits of the lower byte are used for the mantissa. The default value of the mantissa is 00100000000 corresponding to 256 (decimal), corresponding to a divider ratio of 0.5. The maximum value of the mantissa is 512 corresponding to a divider ratio of 1. Note that the resolution of the VOUT_SCALE_LOOP command is 0.2%.

When Power Management Bus commands are used to trim or margin the output voltage, the value of VREF is what is changed inside the module, which in turn changes the regulated output voltage of the module.

The nominal output voltage of the module can be adjusted with a minimum step size of 0.4% over a ±25% range from nominal using the VOUT_TRIM command over the Power Management Bus.. The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value using the "Linear" mode with the exponent fixed at –10 (decimal). The value of the offset voltage is given by

$$V_{OUT(offset)} = VOUT\_TRIM \times 2^{-10}$$

This offset voltage is added to the voltage set through the divider ratio and nominal VREF to produce the trimmed output voltage. The valid range in two's complement for this command is –4000h to 3FFFh. The high order two bits of the high byte must both be either 0 or 1. If a value outside of the +/-25% adjustment range is given with this command, the module will set it's output voltage to the nominal value (as if VOUT_TRIM had been set to 0), assert SMBALRT#, set the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

## OUTPUT VOLTAGE MARGINING USING THE POWER MANAGEMENT BUS

The module can also have its output voltage margined via Power Management Bus commands. The command VOUT_MARGIN_HIGH sets the margin high voltage, while the command VOUT_MARGIN_LOW sets the margin low voltage. Both the VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW commands use the "Linear" mode with the exponent fixed at –10 (decimal). Two bytes are used for the mantissa with the upper bit [7] of the high byte fixed at 0. The actual margined output voltage is a combination of the VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW and the VOUT_TRIM values as shown below.

$$V_{OUT(MH)} = (VOUT\_MARGIN\_HIGH + VOUT\_TRIM) \times 2^{-10}$$

$$V_{OUT(ML)} = (VOUT\_MARGIN\_LOW + VOUT\_TRIM) \times 2^{-10}$$

Note that the sum of the margin and trim voltages cannot be outside the ±25% window around the nominal output voltage. The data associated with VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The module is commanded to go to the margined high or low voltages using the OPERATION command. Bits [5:2] are used to enable margining as follows:

00XX : Margin Off

0101 : Margin Low (Ignore Fault)



0110 : Margin Low (Act on Fault)

1001 : Margin High (Ignore Fault)

1010 : Margin High (Act on Fault)

## POWER MANAGEMENT BUS ADJUSTABLE OVERCURRENT WARNING

The SLDN-20D1A module can provide an overcurrent warning via the Power Management Bus. The threshold for the overcurrent warning can be set using the parameter IOUT_OC_WARN_LIMIT. This command uses the "Linear" data format with a two byte data word where the upper five bits [7:3] of the high byte represent the exponent and the remaining three bits of the high byte [2:0] and the eight bits in the low byte represent the mantissa. The exponent is fixed at –1 (decimal). The upper five bits of the mantissa are fixed at 0 while the lower six bits are programmable with a default value of 24A. The resolution of this warning limit is 500mA. The value of the IOUT_OC_WARN_LIMIT can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

## TEMPERATURE STATUS VIA POWER MANAGEMENT BUS

The SLDN-20D1A module can provide information related to temperature of the module through the STATUS_TEMPERATURE command. The command returns information about whether the pre-set over temperature fault threshold and/or the warning threshold have been exceeded.

## POWER MANAGEMENT BUS ADJUSTABLE OUTPUT OVER AND UNDER VOLTAGE PROTECTION

The SLDN-20D1A module has output over and under voltage protection capability. The Power Management Bus command VOUT_OV_FAULT_LIMIT is used to set the output over voltage threshold from four possible values: 108%, 110%, 112% or 115% of the commanded output voltage. The command VOUT_UV_FAULT_LIMIT sets the threshold that causes an output under voltage fault and can also be selected from four possible values: 92%, 90%, 88% or 85%. The default values are 112% and 88% of commanded output voltage. Both commands use two data bytes formatted as two's complement binary integers. The "Linear" mode is used with the exponent fixed to –10 (decimal) and the effective over or under voltage trip points given by:

$$V_{OUT(OV\_REQ)} = (VOUT\_OV\_FAULT\_LIMIT) \times 2^{-10}$$
$$V_{OUT(UV\_REQ)} = (VOUT\_UV\_FAULT\_LIMIT) \times 2^{-10}$$

Values within the supported range for over and undervoltage detection thresholds will be set to the nearest fixed percentage. Note that the correct value for VOUT_SCALE_LOOP must be set in the module for the correct over or under voltage trip points to be calculated.

In addition to adjustable output voltage protection, the 12A Digital module can also be programmed for the response to the fault. The VOUT_OV_FAULT RESPONSE and VOUT_UV_FAULT_RESPONSE commands specify the response to the fault. Both these commands use a single data byte with the possible options as shown below.

Continue operation without interruption (Bits [7:6] = 00, Bits [5:3] = xxx).

Continue for four switching cycles and then shut down if the fault is still present, followed by no restart or continuous restart (Bits [7:6] = 01, Bits [5:3] = 000 means no restart, Bits [5:3] = 111 means continuous restart).

Immediate shut down followed by no restart or continuous restart (Bits [7:6] = 10, Bits [5:3] = 000 means no restart, Bits [5:3] = 111 means continuous restart).

Module output is disabled when the fault is present and the output is enabled when the fault no longer exists (Bits [7:6] = 11, Bits [5:3] = xxx).

Note that separate response choices are possible for output over voltage or under voltage faults.

## POWER MANAGEMENT BUS ADJUSTABLE INPUT UNDERVOLTAGE LOCKOUT

The SLDN-20D1A module allows adjustment of the input under voltage lockout and hysteresis. The command VIN_ON allows setting the input voltage turn on threshold, while the VIN_OFF command sets the input voltage turn off threshold. For the VIN_ON command, possible values are 2.75V, and 3V to 14V in 0.5V steps. For the VIN_OFF command, possible values are 2.5V to 14V in 0.5V steps. If other values are entered for either command, they will be mapped to the closest of the allowed values.

Both the VIN_ON and VIN_OFF commands use the "Linear" format with two data bytes. The upper five bits represent the exponent (fixed at -2) and the remaining 11 bits represent the mantissa. For the mantissa, the four most significant bits are fixed at 0.

## POWER GOOD

The SLDN-20D1A module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going outside the specified thresholds. The PGOOD thresholds are user selectable via the Power Management Bus (the default values are as shown in the Feature Specifications Section). Each threshold is set up symmetrically above and below the nominal value. The POWER_GOOD_ON command sets the output voltage level above which PGOOD is asserted (lower threshold). For example, with a 1.2V nominal output voltage, the POWER_GOOD_ON threshold can set the lower threshold to 1.14 or 1.1V. Doing this will automatically set the upper thresholds to 1.26 or 1.3V.

The POWER_GOOD_OFF command sets the level below which the PGOOD command is de-asserted. This command also sets two thresholds symmetrically placed around the nominal output voltage. Normally, the POWER_GOOD_ON threshold is set higher than the POWER_GOOD_OFF threshold.

Both POWER_GOOD_ON and POWER_GOOD_OFF commands use the "Linear" format with the exponent fixed at –10 (decimal). The two thresholds are given by

$$V_{OUT(PGOOD\_ON)} = (POWER\_GOOD\_ON) \times 2^{-10}$$

$$V_{OUT(PGOOD\_OFF)} = (POWER\_GOOD\_OFF) \times 2^{-10}$$

Both commands use two data bytes with bit [7] of the high byte fixed at 0, while the remaining bits are r/w and used to set the mantissa using two's complement representation. Both commands also use the  The VOUT_SCALE_LOOP parameter so it must be set correctly. The default value of POWER_GOOD_ON is set at 1.1035V and that of the POWER_GOOD_OFF is set at 1.08V. The values associated with these commands can be stored in non-volatile memory using the STORE_DEFAULT_ALL command.

The PGOOD terminal can be connected through a pullup resistor (suggested value 100KΩ) to a source of 5VDC or lower.

## MEASUREMENT OF OUTPUT CURRENT, OUTPUT VOLTAGE AND INPUT VOLTAGE

The SLDN-20D1A module is capable of measuring key module parameters such as output current and voltage and input voltage and providing this information through the Power Management Bus interface. Roughly every 200µs, the module makes 16 measurements each of output current, voltage and input voltage. Average values of each of these measurements are then calculated and placed in the appropriate registers. These values in the registers can then be read using the Power Management Bus interface.

## MEASURING OUTPUT CURRENT USING THE POWER MANAGEMENT BUS

The module measures current by using the inductor winding resistance as a current sense element. The inductor winding resistance is then the current gain factor used to scale the measured voltage into a current reading. This gain factor is the argument of the IOUT_CAL_GAIN command, and consists of two bytes in the linear data format. The exponent uses the upper five bits [7:3] of the high data byte in two-s complement format and is fixed at –15 (decimal). The remaining 11 bits in two's complement binary format represent the mantissa. During manufacture, each module is calibrated by measuring and storing the current gain factor into non-volatile storage.

The current measurement accuracy is also improved by each module being calibrated during manufacture with the offset in the current reading. The IOUT_CAL_OFFSET command is used to store and read the current offset. The argument for this command consists of two bytes composed of a 5-bit exponent (fixed at -4d) and a 11-bit mantissa. This command has a resolution of 62.5mA and a range of -4000mA to +3937.5mA.

The READ_IOUT command provides module average output current information. This command only supports positive or current sourced from the module. If the converter is sinking current a reading of 0 is provided. The READ_IOUT command returns two bytes of data in the linear data format. The exponent uses the upper five bits [7:3] of the high data byte in two-s complement format and is fixed at –4 (decimal). The remaining 11 bits in two's complement binary format represent the mantissa with the 11th bit fixed at 0 since only positive numbers are considered valid.

Note that the current reading provided by the module is not corrected for temperature. The temperature corrected current reading for module temperature TModule can be estimated using the following equation

$$I_{\mathrm{OUT,CORR}} = \frac{I_{READ\_OUT}}{1+[(T_{IND}-30)\times 0.00393]}$$

where IOUT_CORR is the temperature corrected value of the current measurement, IREAD_OUT is the module current measurement value, TIND is the temperature of the inductor winding on the module. Since it may be difficult to measure TIND, it may be approximated by an estimate of the module temperature.

## MEASURING OUTPUT VOLTAGE USING THE POWER MANAGEMENT BUS

The SLDN-20D1A module can provide output voltage information using the READ_VOUT command. The command returns two bytes of data all representing the mantissa while the exponent is fixed at -10 (decimal).

During manufacture of the module, offset and gain correction values are written into the non-volatile memory of the module. The command VOUT_CAL_OFFSET can be used to read and/or write the offset (two bytes consisting of a 16-bit mantissa in two's complement format) while the exponent is always fixed at -10 (decimal). The allowed range for this offset correction is -125 to 124mV. The command VOUT_CAL_GAIN can be used to read and/or write the gain correction - two bytes consisting of a five-bit exponent (fixed at -8) and a 11-bit mantissa. The range of this correction factor is -0.125 to +0.121, with a resolution of 0.004. The corrected output voltage reading is then given by:

$$\begin{aligned} &V_{OUT}(Final) = \\ &[V_{OUT}(Initial)\times(1+VOUT\_CAL\_GAIN)] \\ &+VOUT\_CAL\_OFFSET \end{aligned}$$

## MEASURING INPUT VOLTAGE USING THE POWER MANAGEMENT BUS

The SLDN-20D1A module can provide output voltage information using the READ_VIN command. The command returns two bytes of data in the linear format. The upper five bits [7:3] of the high data form the two's complement representation of the mantissa which is fixed at –5 (decimal). The remaining 11 bits are used for two's complement representation of the mantissa, with the 11th bit fixed at zero since only positive numbers are valid.

During module manufacture, offset and gain correction values are written into the non-volatile memory of the module. The command VIN_CAL_OFFSET can be used to read and/or write the offset - two bytes consisting of a five-bit exponent (fixed at -5) and a11-bit mantissa in two's complement format. The allowed range for this offset correction is -2to 1.968V, and the resolution is 32mV. The command VIN_CAL_GAIN can be used to read and/or write the gain correction - two bytes consisting of a five-bit exponent (fixed at -8) and a 11-bit mantissa. The range of this correction factor is -0.125 to +0.121, with a resolution of 0.004. The corrected output voltage reading is then given by:

$$\begin{aligned} &V_{IN}(Final) = \\ &[V_{IN}(Initial) \times (1 + VIN\_CAL\_GAIN)] \\ &+ VIN\_CAL\_OFFSET \end{aligned}$$

## READING THE STATUS OF THE MODULE USING THE POWER MANAGEMENT BUS

The SLDN-20D1A module supports a number of status information commands implemented in Power Management Bus. However, not all features are supported in these commands. A 1 in the bit position indicates the fault that is flagged.

STATUS_BYTE : Returns one byte of information with a summary of the most critical device faults.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7 | X | 0 |
| 6 | OFF | 0 |
| 5 | VOUT Overvoltage | 0 |
| 4 | IOUT Overcurrent | 0 |
| 3 | VIN Undervoltage | 0 |
| 2 | Temperature | 0 |
| 1 | CML (Comm. Memory Fault) | 0 |
| 0 | None of the above | 0 |

*Table 6.*

STATUS_WORD: Returns two bytes of information with a summary of the module's fault/warning conditions.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7 | X | 0 |
| 6 | OFF | 0 |
| 5 | VOUT Overvoltage | 0 |
| 4 | IOUT Overcurrent | 0 |
| 3 | VIN Undervoltage | 0 |
| 2 | Temperature | 0 |
| 1 | CML (Comm. Memory Fault) | 0 |
| 0 | None of the above | 0 |

*Table 7. LOW BYTE*

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|

| | | |
|---|---|---|
| 7 | VOUT fault or warning | 0 |
| 6 | IOUT fault or warning | 0 |
| 5 | X | 0 |
| 4 | X | 0 |
| 3 | POWER_GOOD# (is negated) | 0 |
| 2 | X | 0 |
| 1 | X | 0 |
| 0 | X | 0 |

*Table 8. HIGH BYTE*

STATUS_VOUT : Returns one byte of information relating to the status of the module's output voltage related faults.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7 | VOUT OV Fault | 0 |
| 6 | X | 0 |
| 5 | X | 0 |
| 4 | VOUT UV Fault | 0 |
| 3 | X | 0 |
| 2 | X | 0 |
| 1 | X | 0 |
| 0 | X | 0 |

*Table 9.*

STATUS_IOUT : Returns one byte of information relating to the status of the module's output voltage related faults.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7 | IOUT OC Fault | 0 |
| 6 | X | 0 |
| 5 | IOUT OC Warning | 0 |
| 4 | X | 0 |
| 3 | X | 0 |
| 2 | X | 0 |
| 1 | X | 0 |
| 0 | X | 0 |

*Table 10.*

STATUS_TEMPERATURE: Returns one byte of information relating to the status of the module's temperature related faults.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7 | OT Fault | 0 |
| 6 | OT Warning | 0 |
| 5 | X | 0 |
| 4 | X | 0 |
| 3 | X | 0 |
| 2 | X | 0 |
| 1 | X | 0 |
| 0 | X | 0 |

*Table 11.*

STATUS_CML : Returns one byte of information relating to the status of the module's communication related faults.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7 | Invalid/Unsupported Command | 0 |
| 6 | Invalid/Unsupported Command | 0 |
| 5 | Packet Error Check Failed | 0 |
| 4 | X | 0 |
| 3 | X | 0 |
| 2 | X | 0 |
| 1 | Other Communication Fault | 0 |
| 0 | X | 0 |

*Table 12.*

MFR_VIN_MIN : Returns minimum input voltage as two data bytes of information in Linear format (upper five bits are exponent – fixed at -2, and lower 11 bits are mantissa in two's complement format – fixed at 12)

MFR_VOUT_MIN : Returns minimum output voltage as two data bytes of information in Linear format (upper five bits are exponent – fixed at -10, and lower 11 bits are mantissa in two's complement format – fixed at 614)

MFR_SPECIFIC_00 : Returns information related to the type of module and revision number. Bits [7:2] in the Low Byte indicate the module type (000010 corresponds to the SLDN-20D1A series of module), while bits [7:3] indicate the revision number of the module.

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7:2 | Module Name | 000110 |
| 1:0 | Reserved | 10 |

*Table 13. LOW BYTE*

| BIT POSITION | FLAG | DEFAULT VALUE |
|---|---|---|
| 7:3 | Module Revision Number | None |
| 2:0 | Reserved | 000 |

*Table 14. HIGH BYTE*

## SUMMARY OF SUPPORTED POWER MANAGEMENT BUS COMMANDS

Please refer to the Power Management Bus 1.1 specification for more details of these commands

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>01</td><td>OPERATION</td><td>Turn Module on or off. Also used to margin the output voltage
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r/w</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td>On</td><td>X</td><td colspan="4">Margin</td><td>X</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td></tr>
</table></td><td></td></tr>
<tr><td>02</td><td>ON_OFF_CONFIG</td><td>Configures the ON/OFF functionality as a combination of analog ON/OFF pin and PMBus commands
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td></tr>
<tr><th>Function</th><td>X</td><td>X</td><td>X</td><td>pu</td><td>cmd</td><td>cpr</td><td>pol</td><td>cpa</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>YES</td></tr>
<tr><td>03</td><td>CLEAR_FAULTS</td><td>Clear any fault bits that may have been set, also releases the SMBALERT# signal if the device has been asserting it.</td><td></td></tr>
</table>

<table>
<tr><td>10</td><td>WRITE_PROTECT</td><td>Used to control writing to the module via PMBus. Copies the current register setting in the module whose command code matches the value in the data byte into non-volatile memory (EEPROM) on the module
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r/w</td><td>r/w</td><td>r/w</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><th>Function</th><td>bit7</td><td>bit6</td><td>bit5</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
</table>
Bit5: 0 – Enables all writes as permitted in bit6 or bit7<br>1 – Disables all writes except the WRITE_PROTECT, OPERATION and ON_OFF_CONFIG (bit 6 and bit7 must be 0)<br>Bit 6: 0 – Enables all writes as permitted in bit5 or bit7<br>1 – Disables all writes except for the WRITE_PROTECT and OPERATION commands (bit5 and bit7 must be 0)<br>Bit7: 0 – Enables all writes as permitted in bit5 or bit6<br>1 – Disables all writes except for the WRITE_PROTECT command (bit5 and bit6 must be 0)</td><td>YES</td></tr>
<tr><td>11</td><td>STORE_DEFAULT_ALL</td><td>Copies all current register settings in the module into non-volatile memory (EEPROM) on the module. Takes about 50ms for the command to execute.</td><td></td></tr>
<tr><td>12</td><td>RESTORE_DEFAULT_ALL</td><td>Restores all current register settings in the module from values in the module non-volatile memory (EEPROM)</td><td></td></tr>
<tr><td>13</td><td>STORE_DEFAULT_CODE</td><td>Copies the current register setting in the module whose command code matches the value in the data byte into non-volatile memory (EEPROM) on the module
<table>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td></tr>
<tr><th>Function</th><td colspan="8">Command code</td></tr>
</table></td><td></td></tr>
<tr><td>14</td><td>RESTORE_DEFAULT_CODE</td><td>Restores the current register setting in the module whose command code matches the value in the data byte from the value in the module non-volatile memory (EEPROM)
<table>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td></tr>
<tr><th>Function</th><td colspan="8">Command code</td></tr>
</table></td><td></td></tr>
</table>

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>20</td><td>VOUT_MODE</td><td>The module has MODE set to Linear and Exponent set to -10. These values cannot be changed
<table>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="3">Mode</td><td colspan="5">Exponent</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>22</td><td>VOUT_TRIM</td><td>Apply a fixed offset voltage to the output voltage command value
<table>
<tr><th>Format</th><td colspan="8">Linear, two's complement binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r/w</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><th>Function</th><td colspan="8">High Byte</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><th>Function</th><td colspan="8">Low Byte</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
</table>

| | | | |
|---|---|---|---|
| 25 | VOUT_MARGIN_HIGH | Sets the target voltage for margining the output high | YES |

| Format | Linear, two’s complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Low Byte | | | | | | | |
| Default Value | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

| | | | |
|---|---|---|---|
| 26 | VOUT_MARGIN_LOW | Sets the target voltage for margining the output low | YES |

| Format | Linear, two’s complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Low Byte | | | | | | | |
| Default Value | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |

| | | | |
|---|---|---|---|
| 29 | VOUT_SCALE_LOOP | Sets the scaling of the output voltage – equal to the feedback resistor divider ratio | YES |

| Format | Linear, two’s complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | |
| Default Value | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Mantissa | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 35 | VIN_ON | Sets the value of input voltage at which the module turns on | YES |

| Format | Linear, two’s complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | Exponent | | | | | Mantissa | | |
| Default Value | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Mantissa | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

| | | | |
|---|---|---|---|
| 36 | VIN_OFF | Sets the value of input voltage at which the module turns off | YES |

| Format | Linear, two’s complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | Exponent | | | | | Mantissa | | |
| Default Value | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Mantissa | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Default Value** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| | | | |
|---|---|---|---|
| 38 | IOUT_CAL_GAIN | Returns the value of the gain correction term used to correct the measured output current | YES |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Format** | Linear, two's complement binary | | | | | | | |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r/w |
| **Function** | Exponent | | | | | Mantissa | | |
| **Default Value** | 1 | 0 | 0 | 0 | 1 | 0 | 0 | V |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| **Function** | Mantissa | | | | | | | |
| **Default Value** | V: Variable based on factory calibration | | | | | | | |

| | | | |
|---|---|---|---|
| 39 | IOUT_CAL_OFFSET | Returns the value of the offset correction term used to correct the measured output current | YES |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Format** | Linear, two's complement binary | | | | | | | |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r/w | r | r |
| **Function** | Exponent | | | | | Mantissa | | |
| **Default Value** | 1 | 1 | 1 | 0 | 0 | V | 0 | 0 |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r/w | r/w | r/w | r/w | r/w | r/w |
| **Function** | Mantissa | | | | | | | |
| **Default Value** | 0 | 0 | V: Variable based on factory calibration | | | | | |

| | | | |
|---|---|---|---|
| 40 | VOUT_OV_FAULT_LIMIT | Sets the voltage level for an output overvoltage fault. Exponent is fixed at -10. Suggested value shown for 1.2Vo. Should be changed for different output voltage. Values can be 108%, 110%, 112% or 115% of output voltage | YES |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Format** | Linear, two's complement binary | | | | | | | |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| **Function** | High Byte | | | | | | | |
| **Default Value** | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| **Function** | Low Byte | | | | | | | |
| **Default Value** | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 41 | VOUT_OV_FAULT_RESPONSE | Instructs the module on what action to take in response to a output overvoltage fault | YES |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Format** | Unsigned Binary | | | | | | | |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r/w | r/w | r/w | r/w | r/w | r | r | r |
| **Function** | RSP [1] | RSP [0] | RS[2] | RS[1] | RS[0] | X | X | X |
| **Default Value** | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

<table>
<tr><td>44</td><td>VOUT_UV_FAULT_LIMIT</td><td>Sets the voltage level for an output undervoltage fault. Exponent is fixed at -10. Suggested value shown for 1.2Vo. Should be changed for different output voltage. Values can be 92%, 90%, 88% or 85% of output voltage
<table>
<tr><th>Format</th><td colspan="8">Linear, two's complement binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><th>Function</th><td colspan="8">High Byte</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><th>Function</th><td colspan="8">Low Byte</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
</table></td><td>YES</td></tr>
<tr><td>45</td><td>VOUT_UV_FAULT_RESPONSE</td><td>Instructs the module on what action to take in response to a output undervoltage fault
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td>RSP [1]</td><td>RSP [0]</td><td>RS[2]</td><td>RS[1]</td><td>RS[0]</td><td>X</td><td>X</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>46</td><td>IOUT_OC_FAULT_LIMIT</td><td>Sets the output overcurrent fault level in A (cannot be changed)
<table>
<tr><th>Format</th><td colspan="8">Linear, two's complement binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><th>Default Value</th><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>R</td></tr>
<tr><th>Function</th><td colspan="8">Mantissa</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>4A</td><td>IOUT_OC_WARN_LIMIT</td><td>Sets the output overcurrent warning level in A
<table>
<tr><th>Format</th><td colspan="8">Linear, two's complement binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><th>Default Value</th><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><th>Function</th><td colspan="8">Mantissa</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
</table>

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 5E | POWER_GOOD_ON | Sets the output voltage level at which the PGOOD pin is asserted high | YES |

| Format | Linear, two's complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Low Byte | | | | | | | |
| Default Value | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 5F | POWER_GOOD_OFF | Sets the output voltage level at which the PGOOD pin is de-asserted low | YES |

| Format | Linear, two's complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Low Byte | | | | | | | |
| Default Value | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 61 | TON_RISE | Sets the rise time of the output voltage during startup | YES |

| Format | Linear, two's complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r/w |
| Function | Exponent | | | | | Mantissa | | |
| Default Value | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Mantissa | | | | | | | |
| Default Value | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 78 | STATUS_BYTE | Returns one byte of information with a summary of the most critical module faults | |

| Format | Unsigned Binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Flag | X | OFF | VOUT_OV | IOUT_OC | VIN_UV | TEMP | CML | OTHER |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|
| 79 | STATUS_WORD | Returns two bytes of information with a summary of the module's fault/warning conditions | |

| Format | Unsigned binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Flag | VOUT | IOUT_OC | X | X | PGOOD | X | X | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Flag | X | OFF | VOUT_OV | IOUT_OC | VIN_UV | TEMP | CML | OTHER |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|

<table>
<tr><td>7A</td><td>STATUS_VOUT</td><td>Returns one byte of information with the status of the module’s output voltage related faults
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Flag</th><td>VOUT_OV</td><td>X</td><td>X</td><td>VOUT_UV</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>7B</td><td>STATUS_IOUT</td><td>Returns one byte of information with the status of the module’s output current related faults
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Flag</th><td>IOUT_OC</td><td>X</td><td>IOUT_OC_WARN</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>7D</td><td>STATUS_TEMPERATURE</td><td>Returns one byte of information with the status of the module’s temperature related faults
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Flag</th><td>OT_FAULT</td><td>OT_WARN</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>7E</td><td>STATUS_CML</td><td>Returns one byte of information with the status of the module’s communication related faults
<table>
<tr><th>Format</th><td colspan="8">Unsigned Binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Flag</th><td>Invalid Command</td><td>Invalid Data</td><td>PEC Fail</td><td>X</td><td>X</td><td>X</td><td>Other Comm Fault</td><td>X</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>88</td><td>READ_VIN</td><td>Returns the value of the input voltage applied to the module
<table>
<tr><th>Format</th><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><th>Default Value</th><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="8">Mantissa</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>8B</td><td>READ_VOUT</td><td>Returns the value of the output voltage of the module
<table>
<tr><th>Format</th><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="8">Mantissa</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><th>Function</th><td colspan="8">Mantissa</td></tr>
<tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
</table>

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|

| | | | |
|---|---|---|---|
| 8C | READ_IOUT | Returns the value of the output current of the module | |

| Format | Linear, two's complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Exponent | | | | | Mantissa | | |
| **Default Value** | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Mantissa | | | | | | | |
| **Default Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | |
|---|---|---|---|
| 98 | PMBUS_REVISION | Returns one byte indicating the module is compliant to PMBus Spec. 1.1 (read only) | YES |

| Format | Unsigned Binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Default Value** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

| | | | |
|---|---|---|---|
| A0 | MFR_VIN_MIN | Returns the minimum input voltage the module is specified to operate at (read only) | YES |

| Format | Linear, two's complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Exponent | | | | | Mantissa | | |
| **Default Value** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Mantissa | | | | | | | |
| **Default Value** | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

| | | | |
|---|---|---|---|
| A4 | MFR_VOUT_MIN | Returns the minimum output voltage possible from the module (read only) | YES |

| Format | Linear, two's complement binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Exponent | | | | | Mantissa | | |
| **Default Value** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Mantissa | | | | | | | |
| **Default Value** | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

| | | | |
|---|---|---|---|
| D0 | MFR_SPECIFIC_00 | Returns module name information (read only) | YES |

| Format | Unsigned Binary | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Reserved | | | | | | | |
| **Default Value** | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Access** | r | r | r | r | r | r | r | r |
| **Function** | Module Name | | | | | | Reserved | |
| **Default Value** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| Hex Code | Command | Brief Description | Non-Volatile Memory Storage |
|---|---|---|---|

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D4 | VOUT_CAL_OFFSET | Applies an offset to the READ_VOUT command results to calibrate out offset errors in module measurements of the output voltage (between -125mV and +124mV) | | | | | | | | | YES |
| | | **Format** | Linear, two's complement binary | | | | | | | | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r/w | r | r | r | r | r | r | r | |
| | | **Function** | Mantissa | | | | | | | | |
| | | **Default Value** | V | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w | |
| | | **Function** | Mantissa | | | | | | | | |
| | | **Default Value** | V | V | V | V | V | V | V | V | |
| D5 | VOUT_CAL_GAIN | Applies a gain correction to the READ_VOUT command results to calibrate out gain errors in module measurements of the output voltage (between -0.125 and 0.121) | | | | | | | | | YES |
| | | **Format** | Linear, two's complement binary | | | | | | | | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r | r | r | r | r/w | r | r | |
| | | **Function** | Exponent | | | | | Mantissa | | | |
| | | **Default Value** | 1 | 1 | 0 | 0 | 0 | 0 | 0 | V | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r | r | r/w | r/w | r/w | r/w | r/w | |
| | | **Function** | Mantissa | | | | | | | | |
| | | **Default Value** | V | V | V | V | V | V | V | V | |
| D6 | VIN_CAL_OFFSET | Applies an offset correction to the READ_VIN command results to calibrate out offset errors in module measurements of the input voltage (between -2V and +1.968V) | | | | | | | | | YES |
| | | **Format** | Linear, two's complement binary | | | | | | | | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r | r | r | r | r | r/w | r | |
| | | **Function** | Exponent | | | | | Mantissa | | | |
| | | **Default Value** | 1 | 1 | 0 | 1 | V | 0 | 0 | V | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r | r/w | r/w | r/w | r/w | r/w | r/w | |
| | | **Function** | Mantissa | | | | | | | | |
| | | **Default Value** | 0 | 0 | V | V | V | V | V | V | |
| D7 | VIN_CAL_GAIN | Applies a gain correction to the READ_VIN command results to calibrate out gain errors in module measurements of the input voltage (between -0.125 and 0.121) | | | | | | | | | YES |
| | | **Format** | Linear, two's complement binary | | | | | | | | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r | r | r | r | r/w | r | r | |
| | | **Function** | Exponent | | | | | Mantissa | | | |
| | | **Default Value** | 1 | 1 | 0 | 0 | V | 0 | 0 | V | |
| | | **Bit Position** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | **Access** | r | r | r | r/w | r/w | r/w | r/w | r/w | |
| | | **Function** | Mantissa | | | | | | | | |
| | | **Default Value** | 0 | 0 | 0 | V | V | V | V | V | |

## 36. THERMAL CONSIDERATIONS

The SLDN-20D1A power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 47. The preferred airflow direction for the module is in Figure 48.

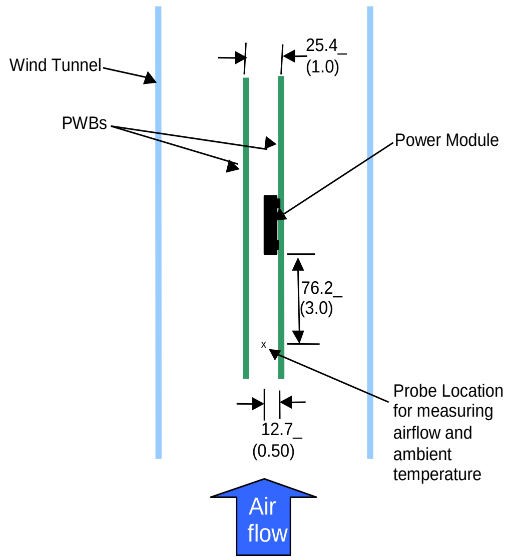



*Figure 47. Thermal Test Setup*

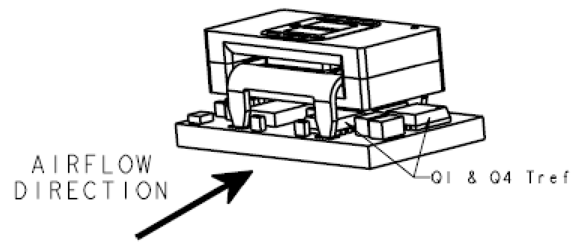



*Figure 48. Preferred airflow direction and location of hot-spot of the module(Tref).*

The thermal reference points, Tref used in the specifications are also shown in Figure 49. For reliable operation the temperatures at these points should not exceed 120 °C. The output power of the module should not exceed the rated power of the module (Vo,set x Io,max).

Please refer to the Application Note "Thermal Characterization Process For Open-Frame Board-Mounted Power Modules" for a detailed discussion of thermal aspects including maximum device temperatures.

## 37. SHOCK AND VIBRATION

The ruggedized (-D version) of the modules are designed to withstand elevated levels of shock and vibration to be able to operate in harsh environments. The ruggedized modules have been successfully tested to the following conditions:

Non-operating random vibration:

Random vibration tests conducted at 25C, 10 to 2000Hz, for 30 minutes each level, starting from 30Grms (Z axis) and up to 50Grms (Z axis). The units were then subjected to two more tests of 50Grms at 30 minutes each for a total of 90 minutes.

Operating shock to 40G per Mil Std. 810F, Method 516.4 Procedure I:

The modules were tested in opposing directions along each of three orthogonal axes, with waveform and amplitude of the shock impulse characteristics as follows:

All shocks were half sine pulses, 11 milliseconds (ms) in duration in all 3 axes.

UnIts were tested to the Functional Shock Test of MIL-STD-810, Method 516.4, Procedure I - Figure 516.4-4. A shock magnitude of 40G was utilized. The operational units were subjected to three shocks in each direction along three axes for a total of eighteen shocks.

**Operating vibration per Mil Std 810F, Method 514.5 Procedure I:**

The ruggedized (-D version) modules are designed and tested to vibration levels as outlined in MIL-STD-810F, Method 514.5, and Procedure 1, using the Power Spectral Density (PSD) profiles as shown in Table 1 and Table 2 for all axes. Full compliance with performance specifications was required during the performance test. No damage was allowed to the module and full compliance to performance specifications was required when the endurance environment was removed. The module was tested per MIL-STD-810, Method 514.5, Procedure I, for functional (performance) and endurance random vibration using the performance and endurance levels shown in Table 4 and Table 5 for all axes. The performance test has been split, with one half accomplished before the endurance test and one half after the endurance test (in each axis). The duration of the performance test was at least 16 minutes total per axis and at least 120 minutes total per axis for the endurance test. The endurance test period was 2 hours minimum per axis.

| FREQUENCY (Hz) | PSD LEVEL (G2/Hz) | FREQUENCY (Hz) | PSD LEVEL (G2/Hz) | FREQUENCY (Hz) | PSD LEVEL (G2/Hz) |
|---|---|---|---|---|---|
| 10 | 1.14E-03 | 170 | 2.54E-03 | 690 | 1.03E-03 |
| 30 | 5.96E-03 | 230 | 3.70E-03 | 800 | 7.29E-03 |
| 40 | 9.53E-04 | 290 | 7.99E-04 | 890 | 1.00E-03 |
| 50 | 2.08E-03 | 340 | 1.12E-02 | 1070 | 2.67E-03 |
| 90 | 2.08E-03 | 370 | 1.12E-02 | 1240 | 1.08E-03 |
| 110 | 7.05E-04 | 430 | 8.84E-04 | 1550 | 2.54E-03 |
| 130 | 5.00E-03 | 490 | 1.54E-03 | 1780 | 2.88E-03 |
| 140 | 8.20E-04 | 560 | 5.62E-04 | 2000 | 5.62E-04 |

*Table 15. Performance Vibration Qualification - All Axes*

| FREQUENCY (Hz) | PSD LEVEL (G2/Hz) | FREQUENCY (Hz) | PSD LEVEL (G2/Hz) | FREQUENCY (Hz) | PSD LEVEL (G2/Hz) |
|---|---|---|---|---|---|
| 10 | 0.00803 | 170 | 0.01795 | 690 | 0.00727 |
| 30 | 0.04216 | 230 | 0.02616 | 800 | 0.05155 |
| 40 | 0.00674 | 290 | 0.00565 | 890 | 0.00709 |
| 50 | 0.01468 | 340 | 0.07901 | 1070 | 0.01887 |
| 90 | 0.01468 | 370 | 0.07901 | 1240 | 0.00764 |
| 110 | 0.00498 | 430 | 0.00625 | 1550 | 0.01795 |
| 130 | 0.03536 | 490 | 0.01086 | 1780 | 0.02035 |
| 140 | 0.0058 | 560 | 0.00398 | 2000 | 0.00398 |

*Table 16. Endurance Vibration Qualification - All Axes*

## 38. EXAMPLE APPLICATION CIRCUIT

**Requirements:**

| | |
|---|---|
| Vin: | 12V |
| Vout: | 1.8V |
| Iout: | 15A max., worst case load transient is from 10A to 15A |
| ΔVout: | 1.5% of Vout (27mV) for worst case load transient |
| Vin, ripple | 1.5% of Vin (180mV, p-p) |

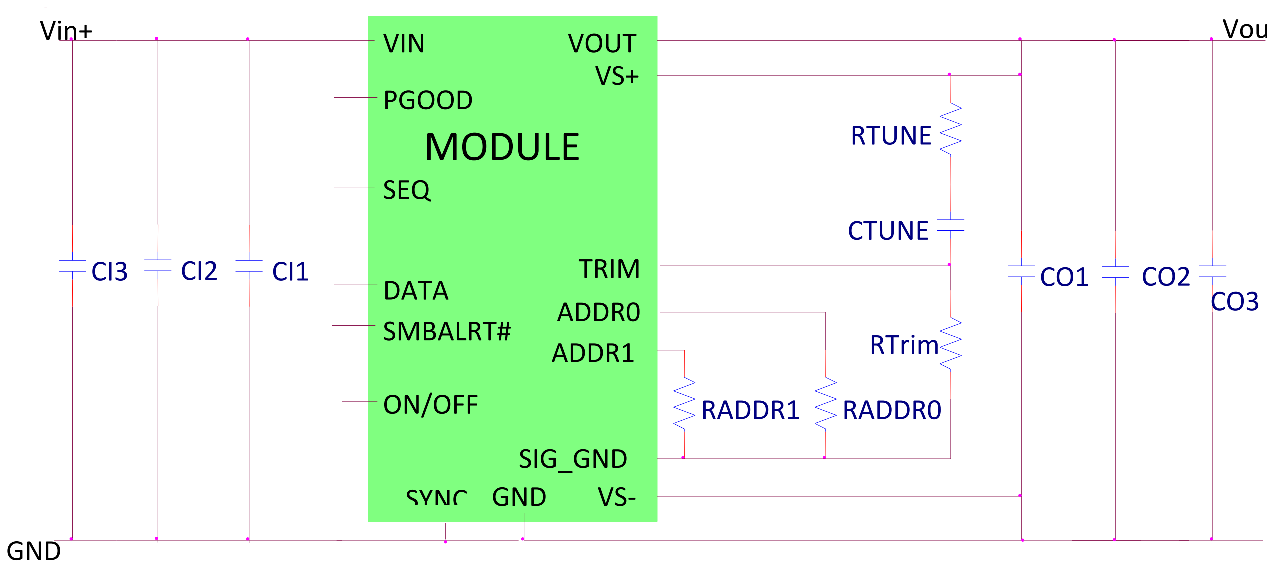



*Figure 49.*

| | |
|---|---|
| CI1 | Decoupling cap - 1x0.047µF/16V ceramic capacitor (e.g. Murata LLL185R71C473MA01) |
| CI2 | 3x22µF/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20) |
| CI3 | 47µF/16V bulk electrolytic |
| CO1 | Decoupling cap - 1x0.047µF/16V ceramic capacitor (e.g. Murata LLL185R71C473MA01) |
| CO2 | N.A. |
| CO3 | 3 x 330µF/6.3V Polymer (e.g. Sanyo Poscap) |
| CTune | 4700pF ceramic capacitor (can be 1206, 0805 or 0603 size) |
| RTune | 330 ohms SMT resistor (can be 1206, 0805 or 0603 size) |
| RTrim | 10kΩ SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%) |

**Note:** The DATA, CLK and SMBALRT pins do not have any pull-up resistors inside the module. Typically, the SMBus master controller will have the pull-up resistors as well as provide the driving source for these signals.

## 39. MECHANICAL OUTLINE

### OUTLINE

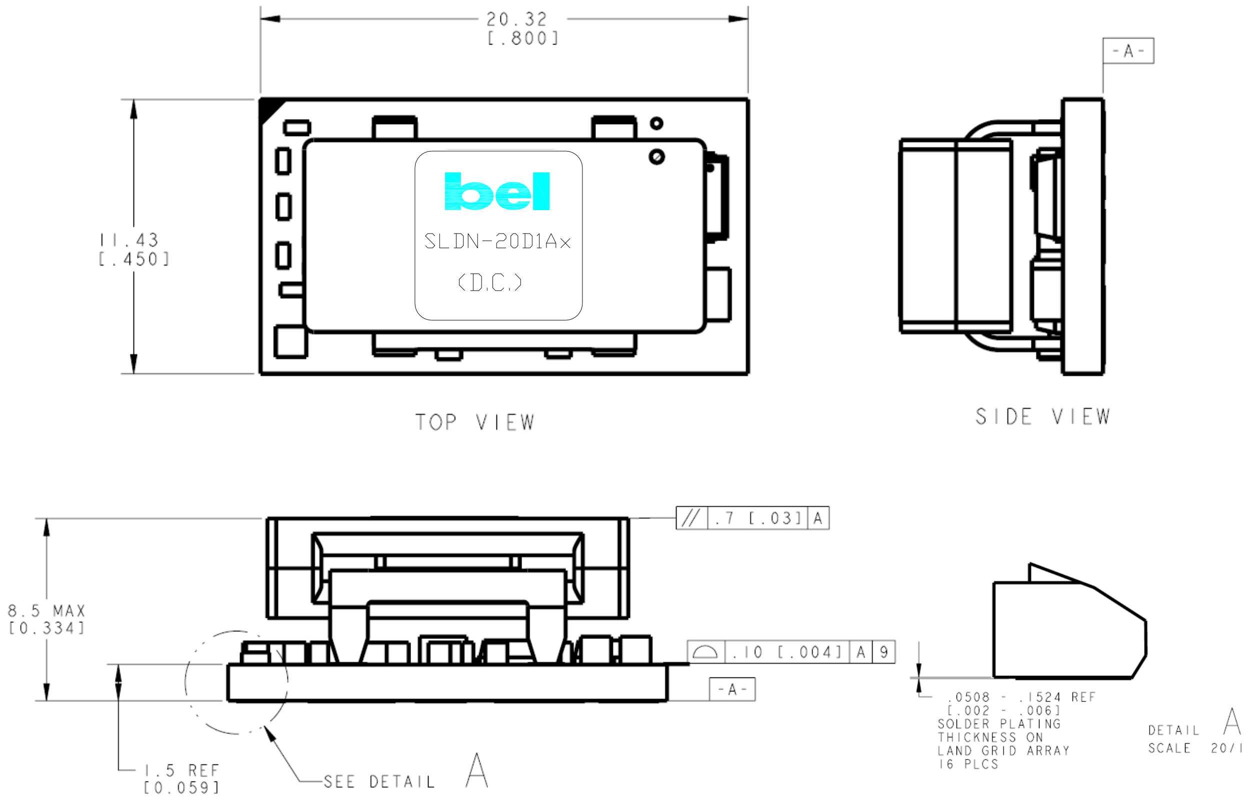



*Figure 50. Outline*

### PIN CONNECTIONS

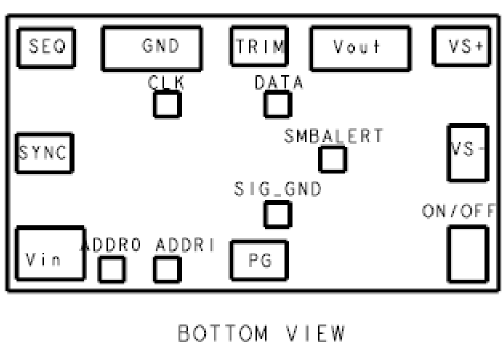



*Figure 51. Pins*

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | ON/OFF | 10 | SYNC [1] |
| 2 | VIN | 11 | CLK |
| 3 | SEQ | 12 | DATA |
| 4 | GND | 13 | SMBALERT |
| 5 | TRIM | 14 | SIG_GND |
| 6 | VOUT | 15 | ADDR1 |
| 7 | VS+ | 16 | ADDR0 |
| 8 | VS- | | |
| 9 | PG | | |

[1] If unused, connect to Ground.

## RECOMMENDED PAD LAYOUT

Dimensions are in millimeter [inch].

Tolerances: x.x mm ± 0.5 mm [0.02 inch] [unless otherwise indicated]

x.xx mm ± 0.25 mm [ 0.010 inch]

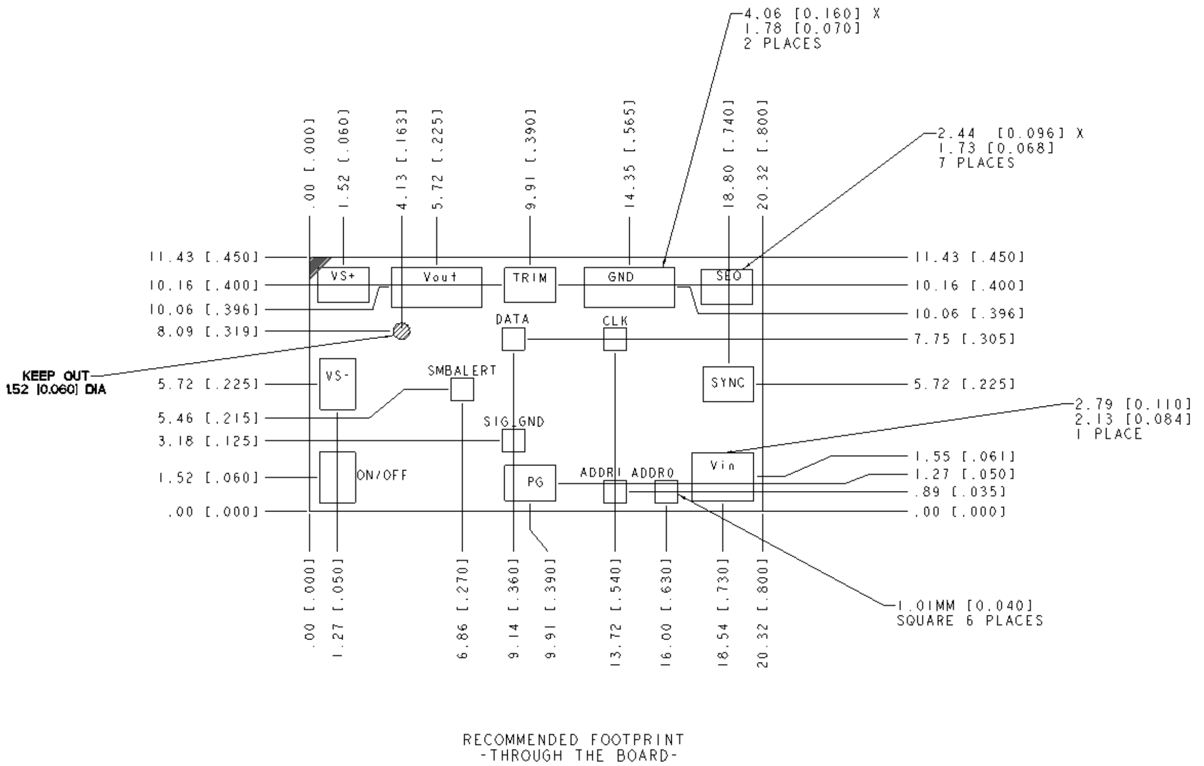



*Figure 52.*

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | ON/OFF | 10 | SYNC [2] |
| 2 | VIN | 11 | CLK |
| 3 | SEQ | 12 | DATA |
| 4 | GND | 13 | SMBALERT |
| 5 | TRIM | 14 | SIG_GND |
| 6 | VOUT | 15 | ADDR1 |
| 7 | VS+ | 16 | ADDR0 |
| 8 | VS- | | |
| 9 | PG | | |

[2] If unused, connect to Ground

## 40. PACKAGING DETAILS

The SLDN-20D1A modules are supplied in tape & reel as standard.
All Dimensions are in millimeters [inches]

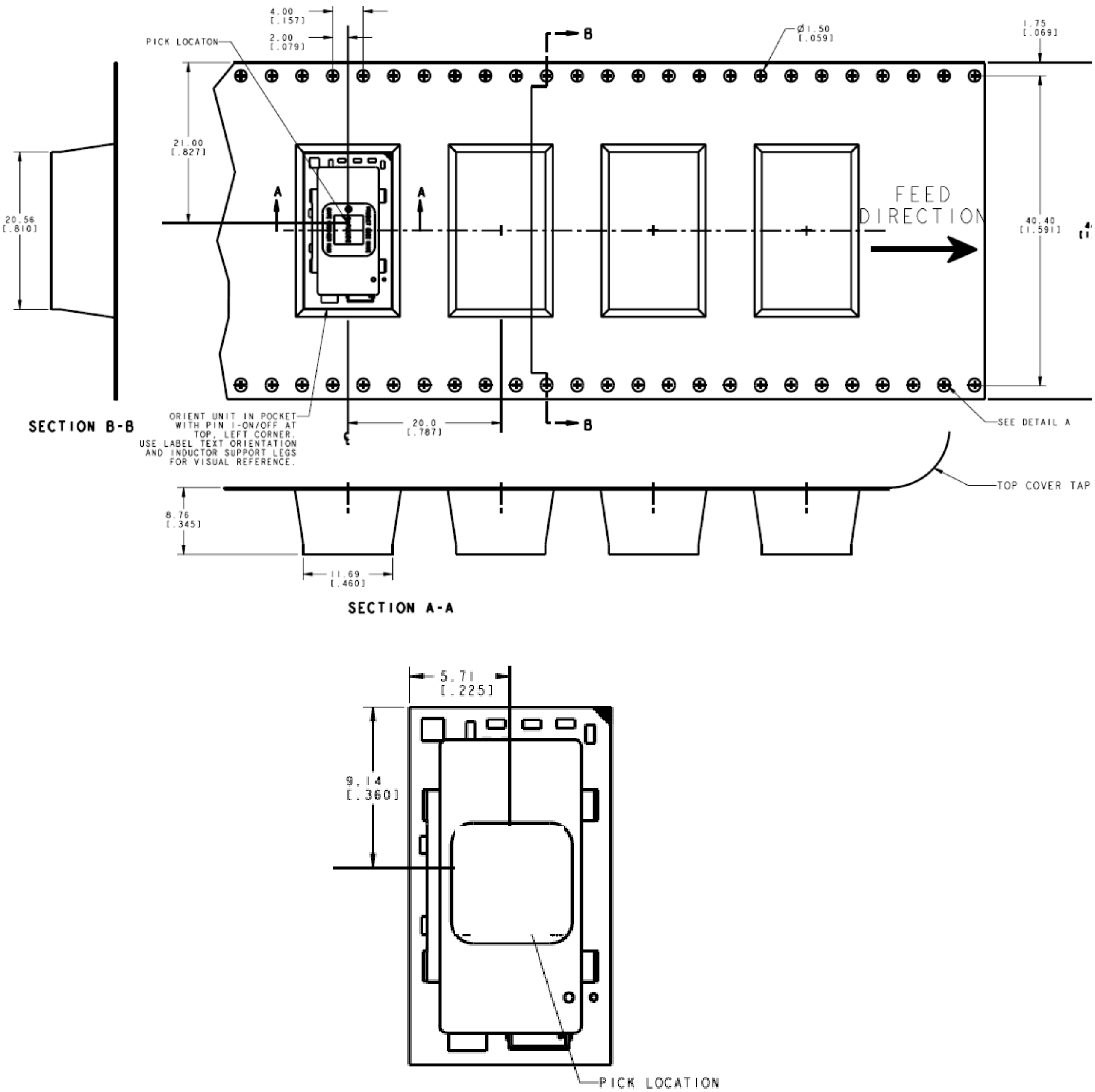



*Figure 53.*

**Reel Dimensions:**

| | |
|---|---|
| Outside Dimensions: | 330.2 mm [13.00 inch] |
| Inside Dimensions: | 177.8 mm [7.00 inch] |
| Tape Width: | 44.00 mm [1.732 inch] |

# 41. SURFACE MOUNT INFORMATION

## PICK AND PLACE

The SLDN-20D1A modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300oC. The label also carries product information such as product code, serial number and the location of manufacture.

## NOZZLE RECOMMENDATIONS

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3 mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

## BOTTOM SIDE / FIRST SIDE ASSEMBLY

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

## LEAD FREE SOLDERING

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

## PB-FREE REFLOW PROFILE

Power Systems will comply with J-STD-020 Rev. C (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Figure below. Soldering outside of the recommended profile requires testing to verify results and performance.

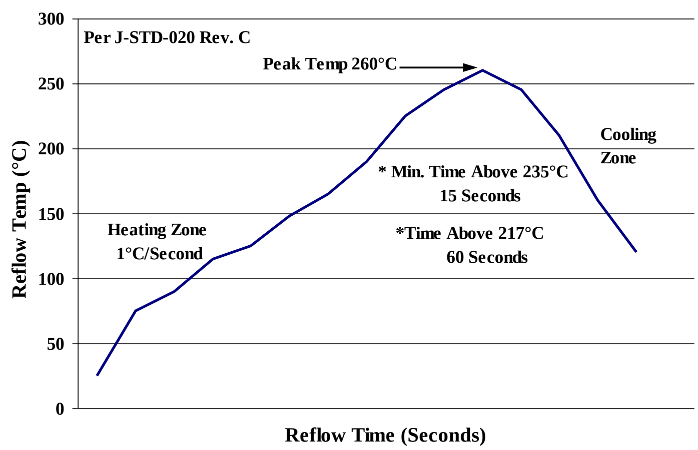



*Figure 54. Recommended linear reflow profile using Sn/Ag/Cu solder.*

## MSL RATING

The SLDN-20D1A modules have a MSL rating of 2A.

## STORAGE AND HANDLING

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of ≤ 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

## POST SOLDER CLEANING AND DRYING CONSIDERATIONS

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).

## 42. REVISION HISTORY

| DATE | REVISION | CHANGES DETAIL | APPROVAL |
|---|---|---|---|
| 2012-03-20 | A | First release | HL.Lu |
| 2012-05-09 | B | Adding patent info | HL.Lu |
| 2015-7-10 | C | Update part selection, absolute maximum Ratings, output specifications, general specifications, digital interface specification, safety considerations, analog voltage margining, overtemperature protection, output voltage adjustment using the power management bus, power management bus adjustable overcurrent warning, measuring output current using the power management bus, reading the statues of the module using the power management bus, summary of supported power management bus commands, example application circuit, packaging details, MSL Rating. | XF.Jiang |
| 2021-06-22 | AD | Add object ID. Delete safety considerations about VDE information. | XF.Jiang |

**For more information on these products consult: tech.support@psbel.com**



Bel Power Digital Non-Isolated DC-DC products use technology licensed from Power-One, protected by US patents: US20040246754, US2004090219A1, US2004093533A1, US2004123164A1, US2004123167A1, US2004178780A1, US2004179382A1, US20050200344, US20050223252, US2005289373A1, US20060061214, US2006015616A1, US20060174145, US20070226526, US20070234095, US20070240000, US20080052551, US20080072080, US20080186006, US6741099, US6788036, US6936999, US6949916, US7000125, US7049798, US7068021, US7080265, US7249267, US7266709, US7315156, US7372682, US7373527, US7394445, US7456617, US7459892, US7493504, US7526660. Outside the US the Power-One licensed technology is protected by patents: AU3287379AA, AU3287437AA, AU3290643AA, AU3291357AA, CN10371856C, CN1045261OC, CN10458656C, CN10459360C, CN10465848C, CN11069332A, CN11124619A, CN11346682A, CN1685299A, CN1685459A, CN1685582A, CN1685583A, CN1698023A, CN1802619A, EP1561156A1, EP1561268A2, EP1576710A1, EP1576711A1, EP1604254A4, EP1604264A4, EP1714369A2, EP1745536A4, EP1769382A4, EP1899789A2, EP1984801A2, W004044718A1, W004045042A3, W004045042C1, W004062061 A1, W004062062A1, W004070780A3, W004084390A3, W004084391A3, W005079227A3, W005081771A3, W006019569A3, W02007001584A3, W02007094935A3

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