# SQL48T20033

## Eighth-Brick DC-DC Converter

RoHS Compliant

The new high performance 20 A SQL48T20033 DC-DC converter provides a high efficiency single output, in a 1/8th brick package that is only 62% the size of the industry-standard quarter-brick. Specifically designed for operation in systems that have limited airflow and increased ambient temperatures, the SQL48T20033 converter utilizes the same pin-out and Input / Output functionality of the industry-standard quarter-bricks. In addition, a heat spreader feature is available (-xxxBx suffix) that provides an effective thermal interface for coldplate and heat sinking options.

The SQL48T20033 converter thermal performance is accomplished through the use of patent-pending circuits, packaging, and processing techniques to achieve ultra-high efficiency, excellent thermal management, and a low-body profile.

Low-body profile and the preclusion of heat sinks minimize impedance to system airflow, thus enhancing cooling for both upstream and downstream devices. The use of 100% automation for assembly, coupled with advanced electronic circuits and thermal design, results in a product with extremely high reliability.

Operating from a wide-range 36-75 V input, the SQL48T20033 converter provides a fully regulated 3.3 V output voltage. The outputs can be trimmed from –20% to +10% of the nominal output voltage, thus providing outstanding design flexibility. Employing a standard power pin-out, the SQL48T20033 converter is an ideal drop-in replacement for existing high current quarter-brick designs. Inclusion of this converter in a new design can result in significant board space and cost savings. The designer can expect reliability improvement over other available converters because of the SQL48T20033's optimized thermal efficiency.



## Key Features & Benefits

- 36-75 VDC Input; 3.3 VDC @ 20 A Output with no derating up to 70°C (@ 48 Vin, ≥ 100 LFM)
- Withstands 100 V input transient for 100ms
- Fixed-frequency operation
- On-board input differential LC-filter
- Start-up into pre-biased load
- No minimum load required
- Fully protected (OTP, OCP, OVP, UVLO)
- Remote output sense
- Positive or negative logic ON/OFF option
- Output voltage trim range: +10%/–20% with Industry Standard trim equations
- Low height of 0.375" (9.5 mm)
- Approved to the latest edition of the following standards: UL/CSA60950-1, IEC60950-1 and EN60950-1.
- All materials meet UL94, V-0 flammability rating
- RoHS lead-free solder and lead-solder-exempted products are available

**Applications:** Telecommunications, Data communications / processing, LAN/WAN, Servers, Workstations

## 1. ELECTRICAL SPECIFICATIONS

Conditions: $T_A$ = 25 °C, Airflow = 300 LFM (1.5 m/s), Vin = 48 VDC, unless otherwise specified.

| PARAMETER | CONDITIONS / DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| ***Absolute Maximum Ratings*** | | | | | |
| Input Voltage | Continuous | -0.3 | | 80 | VDC |
| | Transient (100ms) | | | 100 | VDC |
| Operating Temperature [1] | Ambient ($T_A$) | -40 | | 85 | °C |
| | Component ($T_C$) | -40 | | 120 | °C |
| (See Derating Curves) | Baseplate ($T_B$) | -40 | | 105 | °C |
| Storage Temperature | | -55 | | 125 | °C |
| ***Isolation Characteristics*** | | | | | |
| I/O Isolation | | 2,250 | | | VDC |
| Isolation Capacitance | | | 270 | | pF |
| Isolation Resistance | | 10 | | | MΩ |
| Input to Baseplate | | 1,500 | | | VDC |
| Output to Baseplate | | 1,500 | | | VDC |
| ***Feature Characteristics*** | | | | | |
| Switching Frequency | | | 445 | | kHz |
| Output Voltage Trim Range [2] | Industry-std. equations[3] | -20 | | +10 | % |
| Remote Sense Compensation [2, 4] | Percent of $V_{OUT}$(NOM) | | | +10 | % |
| Output Overvoltage Protection | Non-latching | 120 | | 140 | % |
| Over Temperature Shutdown | Non-latching | | 125 | | °C |
| Auto-Restart Period | Applies to all protection features | | 200 | | ms |
| Turn-On Time from Vin | Time from UVLO to Vo = 90%$V_{OUT}$(NOM) Resistive Load | | 5 | 20 | ms |
| Turn-On Time from ON/OFF Control | Time from ON to Vo = 90% $V_{OUT}$(NOM) Resistive Load | | 5 | 20 | ms |
| ON/OFF Control (Positive Logic option) | Converter Off (logic low) | -20 | | 0.8 | VDC |
| | Converter On (logic high) | 2.4 | | 20 | VDC |
| ON/OFF Control (Negative Logic option) | Converter Off (logic high) | 2.4 | | 20 | VDC |
| | Converter On (logic low) | -20 | | 0.8 | VDC |
| ***Input Characteristics*** | | | | | |
| Operating Input Voltage Range | | 36 | 48 | 75 | VDC |
| Input Undervoltage Lockout | Turn-on Threshold | 31.5 | 33.5 | 35.5 | VDC |
| | Turn-off Threshold | 30 | 32 | 34 | VDC |
| Lockout Hysteresis Voltage | | 1.0 | | 2.0 | VDC |



[1] Reference Figure H for component ($T_C$ and $T_B$) locations.

[2] Vout can be increased up to 10% via the sense leads or up to 10% via the trim function. However, the total output voltage trim-up should not exceed 10% of $V_{OUT}$(NOM).

[3] Trim equations are defined within this document's "Operations" section.

[4] When using remote sense a minimum of 100uF ceramic capacitance should be mounted between Vout(+) and Vout(-) close to pin 8 and pin 4.

| | | | | | | |
|---|---|---|---|---|---|---|
| Maximum Input Current | 3.3 Vout, Full Load @ 36 VDC In | | | | 2.1 | ADC |
| Input Standby Current | Vin = 48V, converter disabled | | | 5 | | mADC |
| Input No Load Current (No load on the output) | Vin = 48V, converter enabled | | | 45 | | mADC |
| Input Reflected-Ripple Current, **ic** | Vin = 48 V, 20 MHz bandwidth, Full Load (resistive) (See Fig. J) | | | 200 | 400 | $mA_{PK-PK}$ |
| | | | | | 150 | $mA_{RMS}$ |
| Input Reflected-Ripple Current, **is** | | | | | 30 | $mA_{PK-PK}$ |
| | | | | | 5 | $mA_{RMS}$ |
| Input Voltage Ripple Rejection | @ 120 Hz | | | 60 | | dB |
| ***Output Characteristics*** | | | | | | |
| Output Voltage Setpoint | $V_{IN}$ = 48 V, $I_{OUT}$ = 0 Amps, $T_A$ = 25°C | | 3.25 | 3.3 | 3.35 | VDC |
| Output Regulation | Over Line: $I_{OUT}$ = 20Amps, $T_A$ = 25°C | | | ±2 | ±17 | mV |
| | Over Load: $V_{IN}$=48V, , $T_A$=25°C | | | ±2 | ±17 | mV |
| Output Voltage Range | Over line, load and temperature | | 3.2 | | 3.4 | VDC |
| Output Ripple and Noise – 20 MHz bandwidth | $I_{OUT}$ = 20 Amps, $C_{EXT}$ =10 µF tantalum + 1 µF ceramic | | | 30 | 100 | $mV_{PK-PK}$ |
| | | | | 15 | 30 | $V_{RMS}$ |
| External Load Capacitance[1] | Plus Full Load (resistive) | $C_{EXT}$ | 0 | | 10,000 | µF |
| | | ESR | 1 | | | mOhm |
| Output Current Range | | | 0 | | 20 | ADC |
| Current Limit Inception | Non-latching | | 22 | 26 | 30 | ADC |
| Short-Circuit Current Pk: | Non-latching Short = 10 mΩ | | | 30 | | Amps |
| RMS: | | | | 5 | 10 | $A_{RMS}$ |
| ***Dynamic Response*** | | | | | | |
| Load Change 50%-75%-50% of $I_{OUT}$ Max | di/dt = 0.1 A/µs, $C_{EXT}$ = 10µF tantalum + 1µF ceramic | | | ±50 | | mV |
| | di/dt = 1.0 A/µs, $C_{EXT}$ = 470µF POS + 1µF ceramic | | | ±100 | | mV |
| Settling Time to 1% of $V_{OUT}$ | | | | 20 | | µs |
| ***Efficiency*** | | | | | | |
| @ 100% Load | 48V IN, $T_A$ = 25°C, 300LFM (1.5 m/s) | | | 91 | | % |
| @ 50% Load | | | | 90 | | % |
| ***Environmental*** | | | | | | |
| Operating Humidity | RH (Non-condensing) | | | | 95 | % |
| Storage Humidity | RH (Non-condensing) | | | | 95 | % |
| ***Mechanical*** | | | | | | |
| Weight | No Baseplate | | | 21.4 | | g |
| | With Baseplate | | | 32.9 | | g |
| ***Reliability*** | | | | | | |
| MTBF | Telcordia SR-332, Method I Case 1 50% electrical stress, 40°C components | | 23.6 | | | MHrs |
| ***EMI and Regulatory Compliance*** | | | | | | |
| Conducted Emissions | CISPR 22 B with external EMI filter network | | | | | |
| Safely Agency Approvals | UL60950-1/CSA60950-1, EN60950-1 and IEC60950-1 | | | | | |





# 2. OPERATIONS

## 2.1 INPUT AND OUTPUT IMPEDANCE

These power converters have been designed to be stable with no external capacitors when used in low inductance input and output circuits. In many applications, the inductance associated with the distribution from the power source to the input of the converter can affect the stability of the converter. The addition of a 33 µF electrolytic capacitor with an ESR <1 Ω across the input helps to ensure stability of the converter. In applications where decoupling capacitance is distributed at the load, the power converter will exhibit stable operation with up to the maximum admissible external load capacitance up to 10,000 µF and ESR > 1mΩ.

## 2.2 ON/OFF (Pin 2)

The ON/OFF pin is used to turn the power converter on or off remotely via a system signal. There are two remote control options available, positive and negative logic, with both referenced to Vin(-). A typical connection is shown in Fig. A.

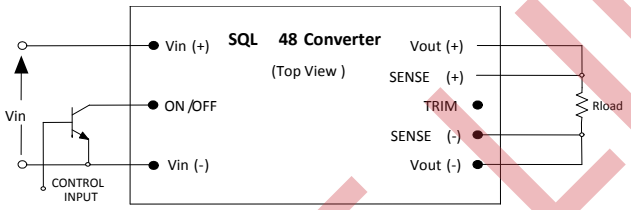



*Figure A. Circuit configuration for ON/OFF function.*

The positive logic version turns on when the ON/OFF pin is at logic high and turns off when at logic low. The converter is on when the ON/OFF pin is left open. See the Electrical Specifications for logic high/low definitions.
The negative logic version turns on when the pin is at logic low and turns off when the pin is at logic high. The ON/OFF pin can be hard wired directly to Vin(-) to enable automatic power up of the converter without the need of an external control signal.
The ON/OFF pin is internally pulled up to 5 VDC through a resistor. A properly de-bounced mechanical switch, open-collector transistor, or FET can be used to drive the input of the ON/OFF pin. The device must be capable of sinking up to 0.2 mA at a low level voltage of ≤ 0.8 V. An external voltage source (±20 V maximum) may be connected directly to the ON/OFF input, in which case it must be capable of sourcing or sinking up to 1 mA depending on the signal polarity. See the Startup Information section for system timing waveforms associated with use of the ON/OFF pin.

## 2.3 REMOTE SENSE

The remote sense feature of the converter compensates for voltage drops occurring between the output pins of the converter and the load. The SENSE(-) (Pin 5) and SENSE(+) ( Pin 7) pins should be connected at the load or at the point where regulation is required (see Fig. B). When using remote sense a minimum of 100uF ceramic capacitance should be mounted between Vout(+) and Vout(-) close to the pin 8 and pin 4.

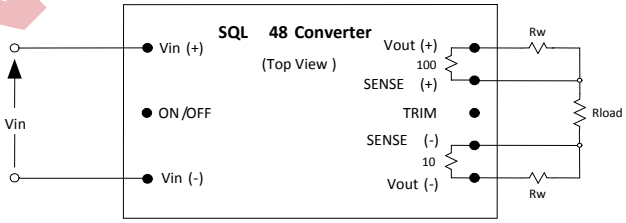



*Figure B. Remote sense circuit configuration.*

**CAUTION**
**If remote sensing is not utilized, the SENSE(-) pin must be connected to the Vout(-) pin, and the SENSE(+) pin must be connected to the Vout(+) pin to ensure the converter will regulate at the specified output voltage. If these connections are not made, the converter will deliver an output voltage that is slightly higher than the specified data sheet value.**

Because the sense leads carry minimal current, large traces on the end-user board are not required. However, sense traces should be run side by side and located close to a ground plane to minimize system noise and ensure optimum performance.
The converter's output overvoltage protection (OVP) circuitry senses the voltage across Vout(+) and Vout(-), and not across the sense lines, so the resistance (and resulting voltage drop) between the output pins of the converter and the load should be minimized to prevent unwanted triggering of the OVP.
When utilizing the remote sense feature, care must be taken not to exceed the maximum allowable output power capability of the converter, which is equal to the product of the nominal output voltage and the allowable output current for the given conditions.
When using remote sense, the output voltage at the converter can be increased by as much as 10% above the nominal rating in order to maintain the required voltage across the load. Therefore, the designer must, if necessary, decrease the maximum current (originally obtained from the derating curves) by the same percentage to ensure the converter's actual output power remains at or below the maximum allowable output power.

## 2.4 OUTPUT VOLTAGE ADJUST / TRIM

The output voltage can be adjusted up 10% or down 20% relative to the rated output voltage by the addition of an externally connected resistor. For output voltage 3.3V, trim-up to 10% is guaranteed at Vin ≥ 40V, and to 8% at Vin ≥ 36V.
The TRIM pin should be left open if trimming is not being used. To minimize noise pickup, a 0.1 µF capacitor is connected internally between the TRIM and SENSE(-) pins.
To increase the output voltage (Fig. C) a trim resistor,
$R_{T-INCR}$, should be connected between the TRIM (Pin 6) and SENSE(+) (Pin 7), with a value of

$$R_{T-INCR} = \frac{5.11(100+\Delta)V_{O-NOM} - 626}{1.225\Delta} - 10.22 \quad [k\Omega],$$

where,

$R_{T-INCR}$ = Required value of trim-up resistor kΩ]

$V_{O-NOM}$ = Nominal value of output voltage [V]

$$\Delta = \left| \frac{(V_{O-REQ} - V_{O-NOM})}{V_{O-NOM}} \right| X\ 100 \quad [\%]$$

$V_{O-REQ}$ = Desired (trimmed) output voltage [V].
When trimming up, care must be taken not to exceed the converter's maximum allowable output power. See the previous section for a complete discussion of this requirement.

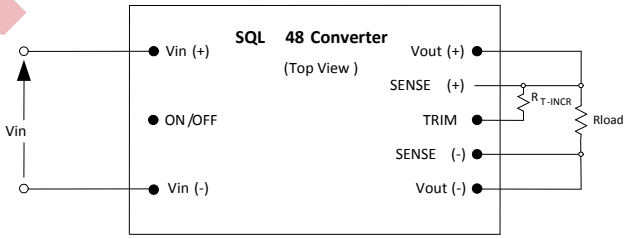



*Figure C. Configuration for increasing output voltage.*

To decrease the output voltage (Fig. D), a trim resistor, $R_{T-DECR}$, should be connected between the TRIM (Pin 6) and SENSE(-) (Pin 5), with a value of:





$$R_{T\text{-}DECR} = \frac{511}{|\Delta|} - 10.22 \quad [k\Omega]$$

where,

$R_{T\text{-}DECR}$ = Required value of trim-down resistor [kΩ] and $\Delta$ is defined above.

**Note:**

The above equations for calculation of trim resistor values match those typically used in conventional industry-standard quarter-bricks, eighth-bricks and sixteenth-brick models.

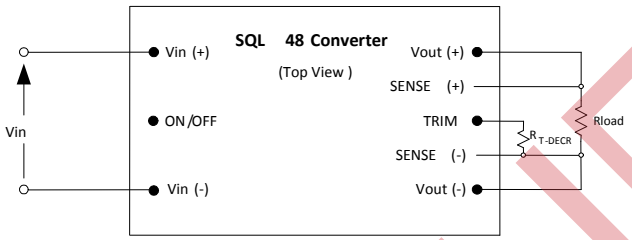



*Figure D. Configuration for decreasing output voltage.*

Trimming/sensing beyond 110% of the rated output voltage is not an acceptable design practice, as this condition could cause unwanted triggering of the output overvoltage protection (OVP) circuit. The designer should ensure that the difference between the voltages across the converter's output pins and its sense pins does not exceed 10% of $V_{OUT}$(nom), or:

$$[V_{OUT}(+) - V_{OUT}(-)] - [V_{SENSE}(+) - V_{SENSE}(-)] \leq V_{O\text{-}NOM} \times 10\% \quad [V]$$

This equation is applicable for any condition of output sensing and/or output trim.

# 3. PROTECTION FEATURES

## 3.1 INPUT UNDERVOLTAGE LOCKOUT (UVLO)

Input undervoltage lockout is standard with this converter. The converter will shut down when the input voltage drops below a pre-determined voltage.
The input voltage must be typically 34 V for the converter to turn on. Once the converter has been turned on, it will shut off when the input voltage drops typically below 32 V. This feature is beneficial in preventing deep discharging of batteries used in telecom applications.

## 3.2 OUTPUT PROTECTIONS

All output circuit protection features are non-latching and operate in a “hiccup” mode. After an output protection event occurs, the converter will be turned off, and held off for approximately 200 ms after which, the protection circuit will reset and the converter will attempt to restart. If the fault is still present, the converter will repeat the above action. Once the fault is removed, the converter will start normally

## 3.3 OUTPUT OVERCURRENT PROTECTION (OCP)

The converter is protected against overcurrent or short circuit conditions. Upon sensing an overcurrent condition, the converter will shut down.
Once this occurs, it will enter hiccup mode and attempt to restart approximately every 200 ms with an approximate duty cycle of 9% for overcurrent and 3% for short circuit. The attempted restart will continue indefinitely until the overload or short circuit condition is removed.
Once the output current is brought back into its specified range, the converter automatically exits the hiccup mode and resumes normal operation.

## 3.4 OUTPUT OVERVOLTAGE PROTECTION (OVP)

The converter will shut down if the output voltage across Vout(+) and Vout(-) exceeds the threshold of the OVP circuitry. The OVP circuitry contains its own reference, independent of the output voltage regulation loop. Once the converter has shut down, it will attempt to restart every 200 ms until the OVP condition is removed.

## 3.5 OVERTEMPERATURE PROTECTION (OTP)

The converter will shut down under an overtemperature condition to protect itself from overheating caused by operation outside the thermal derating curves, or operation in abnormal conditions such as system fan failure. The converter will automatically restart after it has cooled to a safe operating temperature.

## 3.6 SAFETY REQUIREMENTS

The converters are safety approved to UL/CSA609501, EN60950-1, and IEC60950-1. Basic Insulation is provided between input and output.
The converters have no internal fuse. To comply with safety agencies requirements, an input line fuse must be used external to the converter. A 5-A fuse is recommended for use with this product. The SQL converter is UL approved for a maximum fuse rating of 15 A.

## 3.7 ELECTROMAGNETIC COMPATIBILITY (EMC)

EMC requirements must be met at the end-product system level, as no specific standards dedicated to EMC characteristics of board mounted component dcdc converters exist. However, Power-One tests its converters to several system level standards, primary of which is the more stringent EN55022, Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement.
An effective internal LC differential filter significantly reduces input reflected ripple current, and improves EMC.
With the addition of a simple external filter, the SQL48T20033 converter will pass the requirements of Class B conducted emissions per EN55022 and FCC requirements. Refer to Figures 17 – 18 for typical performance with external filter.





## 3.8 STARTUP INFORMATION (USING NEGATIVE ON/OFF)

**Scenario #1: Initial Startup From Bulk Supply**
ON/OFF function enabled, converter started via application of $V_{IN}$. See Fig. E.

| Time | Comments |
|---|---|
| $t_0$ | ON/OFF pin is ON; system front-end power is toggled on, $V_{IN}$ to converter begins to rise. |
| $t_1$ | $V_{IN}$ crosses undervoltage Lockout protection circuit threshold; converter enabled. |
| $t_2$ | Converter begins to respond to turn-on command (converter turn-on delay). |
| $t_3$ | Converter $V_{OUT}$ reaches 100% of nominal value. |

For this example, the total converter startup time ($t_3$- $t_1$) is typically 4 ms.

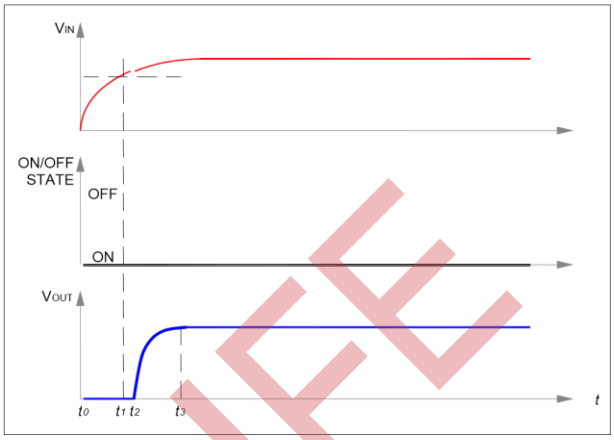



*Figure E. Startup scenario #1.*

**Scenario #2: Initial Startup Using ON/OFF Pin** With $V_{IN}$ previously powered, converter started via ON/OFF pin. See Fig. F.

| Time | Comments |
|---|---|
| $t_0$ | $V_{INPUT}$ at nominal value. |
| $t_1$ | Arbitrary time when ON/OFF pin is enabled (converter enabled). |
| $t_2$ | End of converter turn-on delay. |
| $t_3$ | Converter $V_{OUT}$ reaches 100% of nominal value. |

For this example, the total converter startup time ($t_3$- $t_1$) is typically 5 ms.

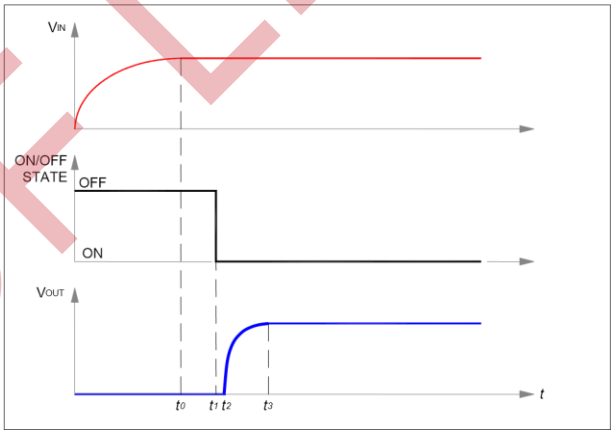



*Figure F. Startup scenario #2.*

**Scenario #3: Turn-off and Restart Using ON/OFF Pin** With $V_{IN}$ previously powered, converter is disabled and then enabled via ON/OFF pin. See Fig. G.

| Time | Comments |
|---|---|
| $t_0$ | $V_{IN}$ and $V_{OUT}$ are at nominal values; ON/OFF pin ON. |
| $t_1$ | ON/OFF pin arbitrarily disabled; converter output falls to zero; turn-on inhibit delay period (200 ms typical) is initiated, and ON/OFF pin action is internally inhibited. |
| $t_2$ | ON/OFF pin is externally re-enabled. **If ($t_2$- $t_1$) ≤ 200 ms**, external action of ON/OFF pin is locked out by startup inhibit timer. **If ($t_2$- $t_1$) > 200 ms**, ON/OFF pin action is internally enabled. |
| $t_3$ | Turn-on inhibit delay period ends. If ON/OFF pin is ON, converter begins turn-on; if off, converter awaits ON/OFF pin ON signal; see Figure F. $t_4$ End of converter turn-on delay. |
| $t_5$ | Converter $V_{OUT}$ reaches 100% of nominal value. |

For the condition, **($t_2$- $t_1$) ≤ 200 ms**, the total converter startup time ($t_5$- $t_1$) is typically 205 ms. For **($t_2$- $t_1$) > 200 ms**, startup will be typically 5 ms after release of ON/OFF pin.

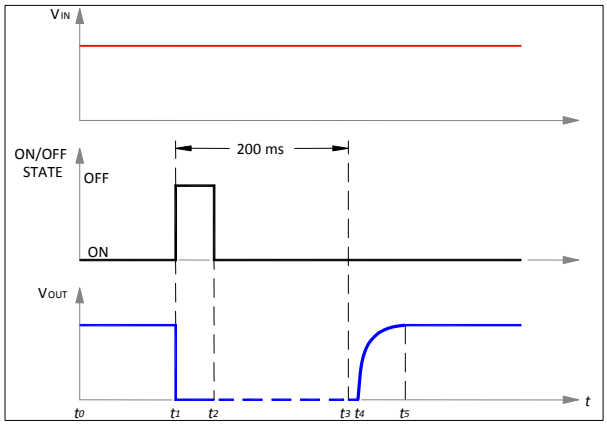



*Figure G. Startup scenario #3.*

# 4. CHARACTERIZATION

## 4.1 GENERAL INFORMATION

The converter has been characterized for many operational aspects, to include thermal derating (maximum load current as a function of ambient temperature and airflow), efficiency, startup and shutdown parameters, output ripple and noise, transient response to load step-change, overcurrent, and short circuit.
The following pages contain specific plots or waveforms associated with the converter. Additional comments for specific data are provided below.

## 4.2 TEST CONDITIONS

All data presented were taken with the converter soldered to a test board, specifically a 0.060" thick printed wiring board (PWB) with four layers. The top and bottom layers were not metalized. The two inner layers, comprised of two-ounce copper, were used to provide traces for connectivity to the converter.
The lack of metallization on the outer layers as well as the limited thermal connection ensured that heat transfer from the converter to the PWB was minimized. This provides a worst-case but consistent scenario for thermal derating purposes.
All measurements requiring airflow were made in the vertical and/or horizontal wind tunnel using Infrared(IR) thermography and thermocouples for thermometry.
Ensuring components on the converter do not exceed their ratings is important to maintaining high reliability. If one anticipates operating the converter at or close to the maximum loads specified in the derating curves, it is prudent to check actual operating temperatures in the application. Thermographic imaging is preferable; if this capability is not available, then thermocouples may be used. The use of AWG #36 gauge thermocouples is recommended to ensure measurement accuracy. Careful routing of the thermocouple leads will further minimize measurement error. Refer to Figure H for the optimum measuring thermocouple location.

## 4.3 THERMAL DERATING

**AIR COOLED**
Load current vs. ambient temperature and airflow rates are given in Figures 1 - 3. Ambient temperature was varied between 25°C and 85°C, with airflow rates from 30 to 500LFM (0.15 to 2.5m/s).
For each set of conditions, the maximum load current was defined as the lowest of:

(i) The output current at which any FET junction temperature does not exceed a maximum temperature of 120°C as indicated by the thermal measurement, or
(ii) The output current at which the temperature at the thermocouple locations $T_C$ do not exceed 120°C. (Fig. H)
(iii) The nominal rating of the converter (20A).

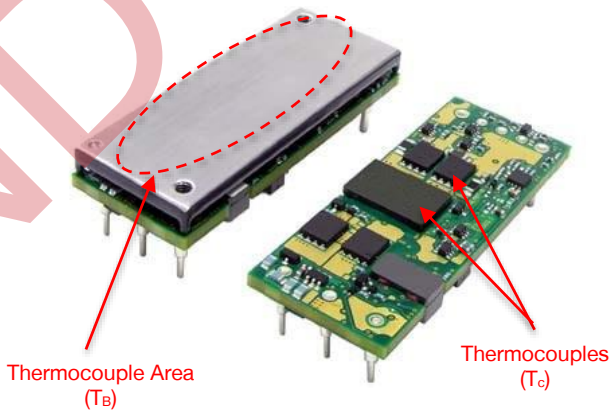



*Fig. H: Location of the thermocouple for thermal testing.*

**BASEPLATE w/ COLDPLATE**
The maximum load current rating vs. baseplate temperature is provided in Figure 4. The baseplate temperature ($T_B$) was maintained ≤ 105°C, with an airflow rate of ≤ 30LFM (≤ 0.15m/s) and ambient temperature ≤ 85°C. Thermocouple measurements (in Fig. H) were recorded with $T_C$ ≤ 120°C. The user should design for $T_B$ ≤ 105°C.





## 4.4 EFFICIENCY

Efficiency vs. load current is showing in Figure 5 for ambient temperature ($T_A$) of 25ºC, airflow rate of 300LFM (1.5m/s) with vertical mounting and input voltages of 36V, 48V, 65V and 75V. Also, a plot of efficiency vs. load current, as a function of ambient temperature with Vin = 48V, airflow rate of 200 LFM (1 m/s) with vertical mounting is shown in Figure. 6.

## 4.5 POWER DISSIPATION

Power dissipation vs. load current is showing in Figure 7 for $T_A$=25ºC, airflow rate of 300LFM (1.5m/s) with vertical mounting and input voltages of 36V, 48V, 65V and 75V. Also, a plot of power dissipation vs. load current, as a function of ambient temperature with Vin = 48V, airflow rate of 200 LFM (1m/s) with vertical mounting is shown in Figure. 8.

## 4.6 STARTUP

Output voltage waveforms, during the turn-on transient using the ON/OFF pin for full rated load currents (resistive load) are shown with and without external load capacitance in Figure 9 and Figure 10.

## 4.7 RIPPLE AND NOISE

Figure 13 shows the output voltage ripple waveform, measured at full rated load current with a 10µF tantalum and a 1µF ceramic capacitor across the output. Note that all output voltage waveforms are measured across the 1µF ceramic capacitor.

The input reflected-ripple current waveforms are obtained using the test setup shown in Fig. J. The corresponding waveforms are shown in Figure 14, and Figure 15.

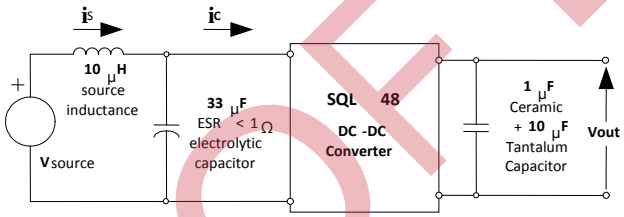



*Fig. J: Test setup for measuring input reflected ripple currents, ic and is.*

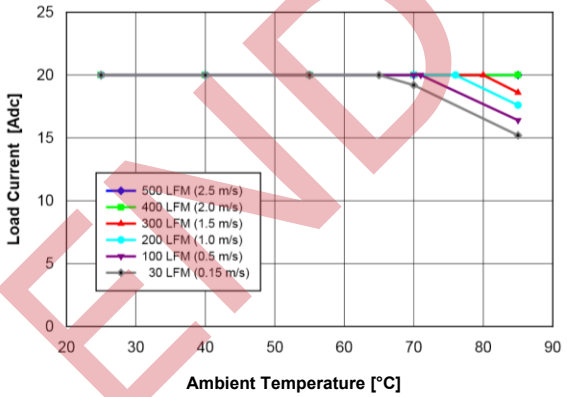



*Figure 1. Available load current vs. ambient air temperature and airflow rates for SQL48T20033 converter mounted vertically with air flowing from pin 3 to pin 1, Tc temperatures ≤ 120 °C, Vin = 48 V.*

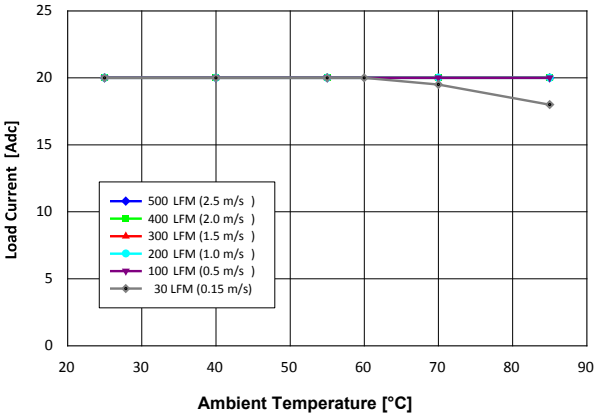



*Figure 2. Power derating of SQL48T20033 converter with baseplate option and 0.25" tall horizontal-fin heatsink. (Conditions: same as Figure 1)*

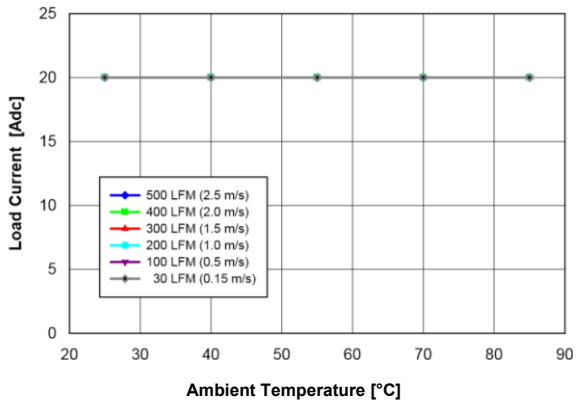



*Figure 3. Power derating of SQL48T20033 converter with baseplate option and 0.91" tall horizontal-fin heatsink. (Conditions: same as Figure 1) No thermal derating required.*

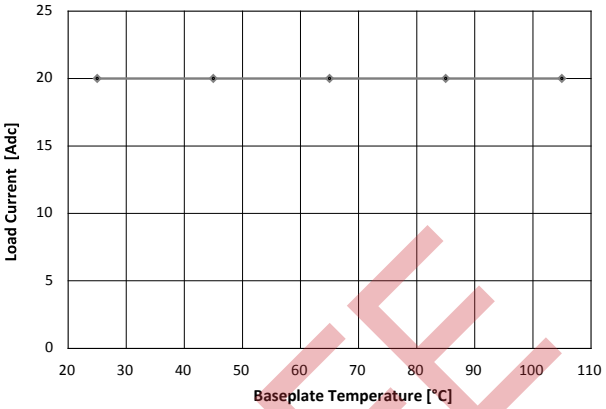



*Figure 4. Coldplate cooling: Power derating of SQL48T20033-xxxBx converter with baseplate option and coldplate cooling. No thermal derating required. (Conditions: Air velocity ≤ 30LFM (≤ 0.15m/s), Vin = 48 V, TB ≤ 105°C)*

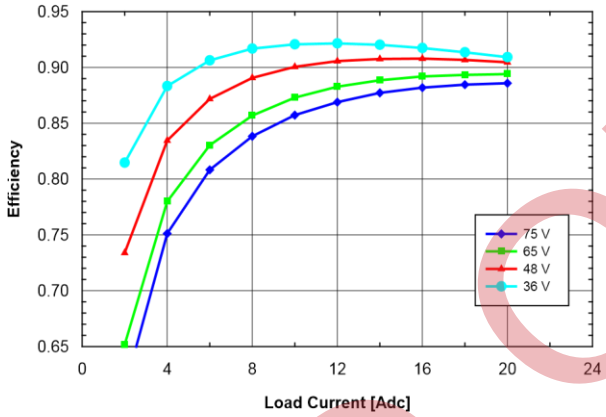



*Figure 5. Efficiency vs. load current and input voltage converter mounted vertically with air flowing from pin 3 to pin 1 at 300 LFM (1.5 m/s) and TA = 25°C.*

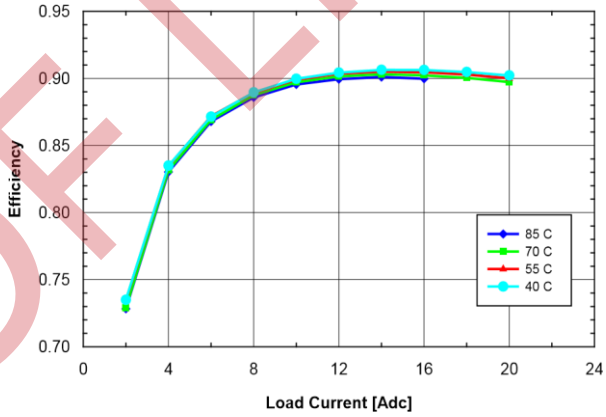



*Figure 6. Efficiency vs. load current and ambient temperature for converter mounted vertically with Vin = 48 V and air flowing from pin 3 to pin 1 at a rate of 200 LFM (1.0 m/s).*

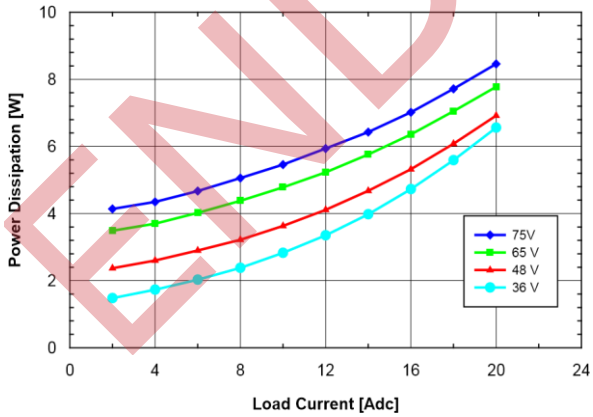



*Figure 7. Power dissipation vs. load current and input voltage converter mounted vertically with air flowing from pin 3 to pin 1 at 300 LFM (1.5 m/s) and $T_A$ = 25°C.*

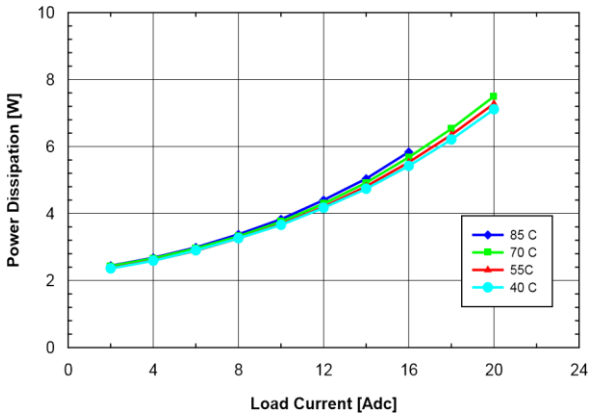



*Figure 8. Power dissipation vs. load current and ambient temperature for converter mounted vertically with Vin = 48V and air flowing from pin 3 to pin 1 at a rate of 200 LFM (1.0m/s).*





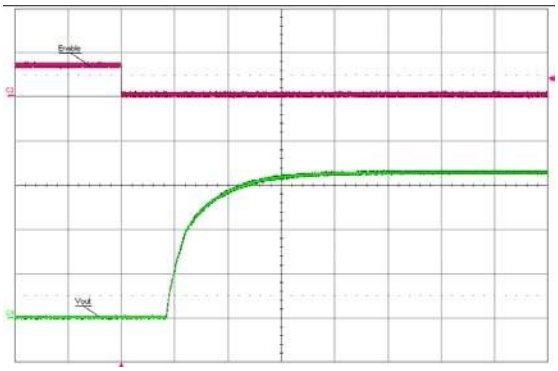


*Figure 9. Turn-on waveform at full rated load current (resistive) with 10,000 uF output capacitor at Vin=48V, triggered via ON/OFF pin. Top trace: ON/OFF signal (5V/div.). Bottom trace: Output voltage (1V/div.). Time scale: 2 ms/div.*

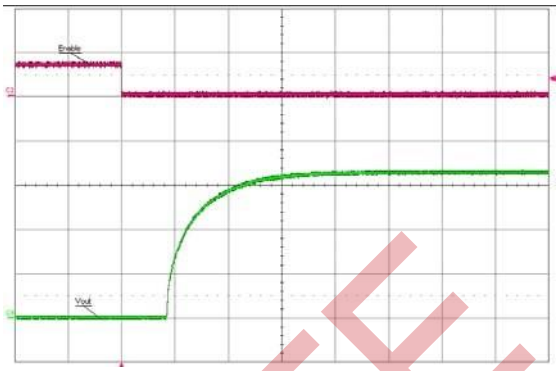


*Figure 10. Turn-on waveform at full rated load current (resistive) with 10uF tant. + 1uF cer. output capacitor at Vin=48V, triggered via ON/OFF pin. Top trace: ON/OFF signal (5V/div.). Bottom trace: Output voltage (1V/div.). Time scale: 2 ms/div.*

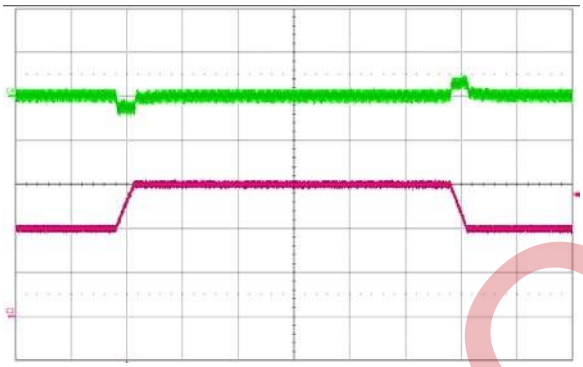


*Figure 11. Output voltage response to load current step change (10A – 15A – 10A) at Vin = 48 V. Top trace: output voltage (50mV/div.) Bottom: load current (5 A/div.). Current slew rate: 0.1 A/µs. Time scale: 200 µs /div. Co = 10µF tantalum + 1µF ceramic*

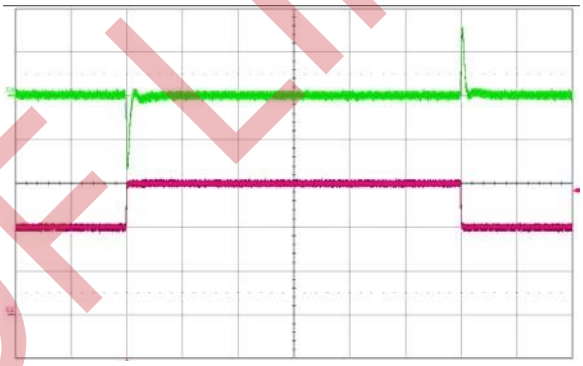


*Figure 12. Output voltage response to load current step change (10A – 15A – 10A) at Vin = 48 V. Top trace: output voltage (50mV/div.) Bottom: load current (5 A/div.). Current slew rate: 1 A/µs. Time scale: 200 µs /div. Co = 470µF POS + 1µF ceramic*

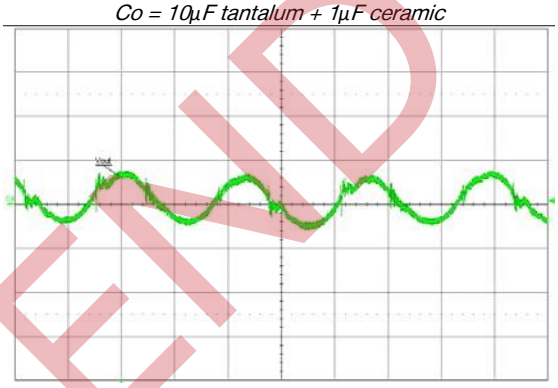


*Figure 13. Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with Co = 10µF tantalum + 1µF ceramic and Vin = 48V. Time scale: 1µs/div.*

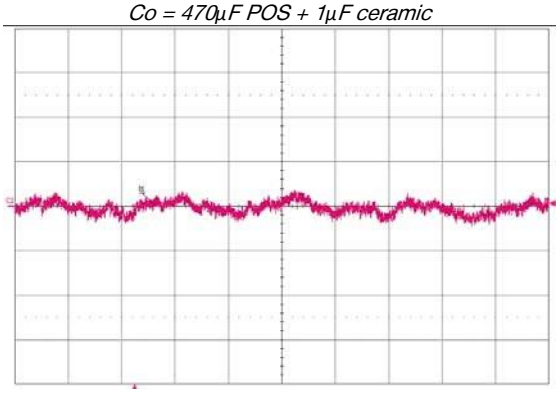


*Figure 14. Input reflected-ripple current, is (10 mA/div.), measured through 10 µH at the source at full rated load current and Vin = 48 V. Refer to Fig. J for test setup. Time scale: 1µs/div.*

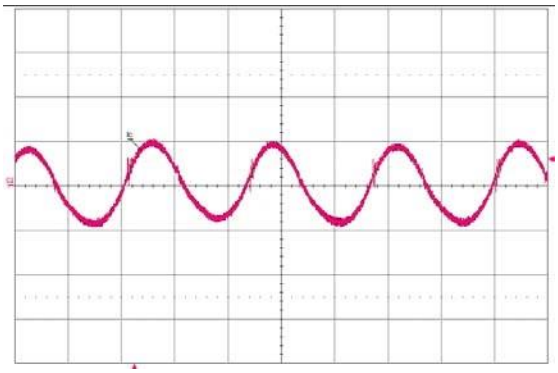


*Figure 15. Input reflected ripple-current, ic (100 mA/div.), measured at input terminals at full rated load current and Vin = 48 V. Refer to Fig. J for test setup. Time scale: 1 µs/div.*

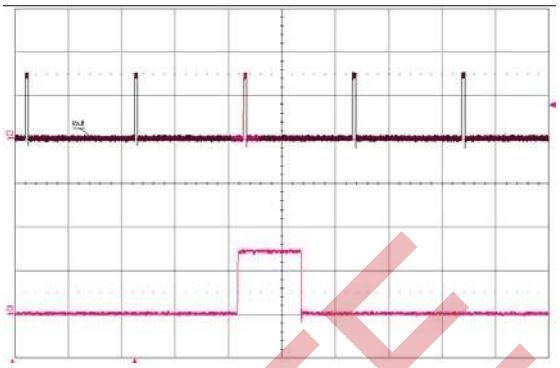
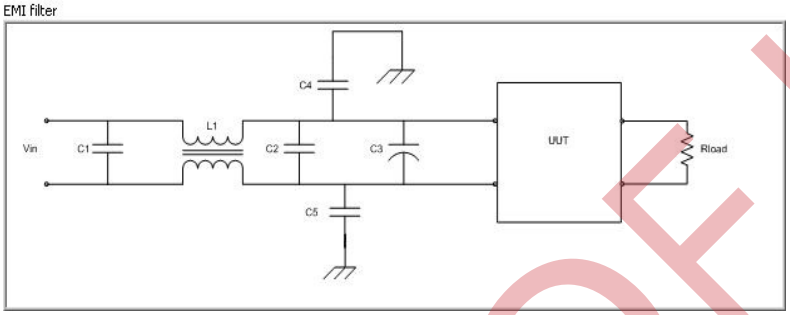


*Figure 16. Load current (top trace, 20 A/div., 100 ms/div.) into a 10 mΩ short circuit during restart, at Vin = 48 V. Bottom trace (20 A/div., 5 ms/div.) is an expansion of the on-time portion of the top trace.*




| COMP. DES. | DESCRIPTION |
|---|---|
| C1 | 3 x 1uF, 100V Ceramic Capacitor |
| C3 | 33uF, 100V Electrolytic Capacitor |
| L1 | F4810 Bel Power Solutions Input Filter |
| C4, C5 | 2200pF Ceramic Capacitor |
| C2 | Not Assembled |

*Figure 17. Typical input EMI filter circuit to attenuate conducted emissions.*

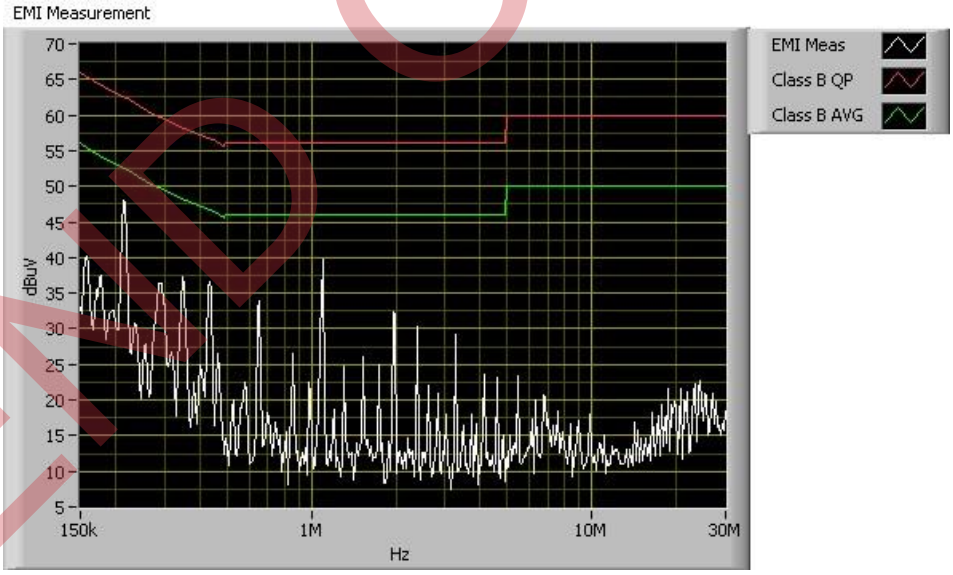


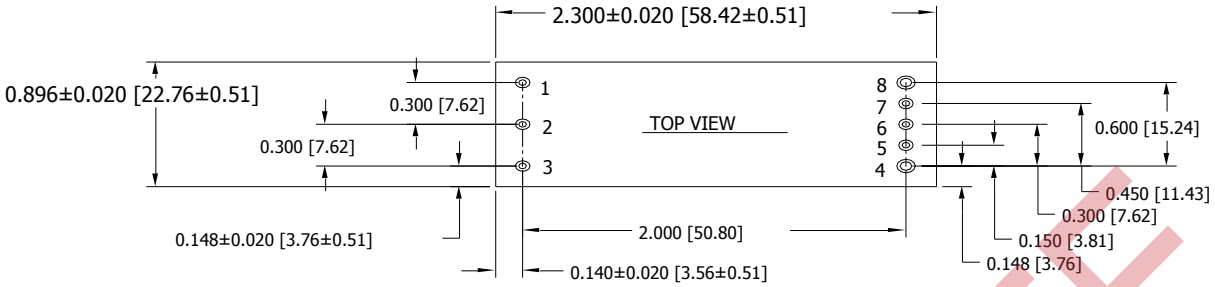

*Figure 18. Input conducted emissions measurement (Typ.) of SQL48T20033*
*Conditions: VIN = 48VDC, IOUT = 20 AMPS*



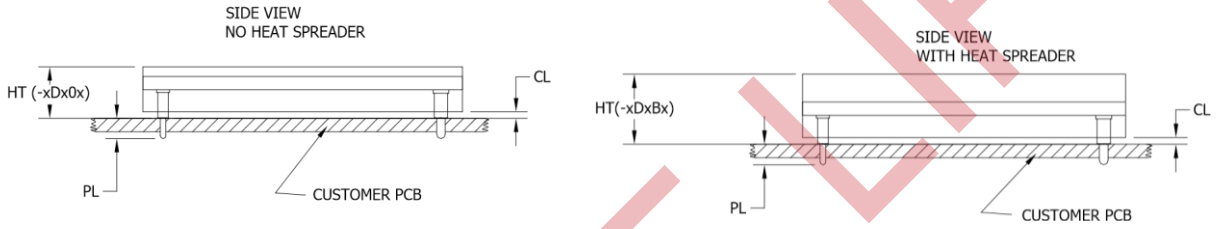


## 5. MECHANICAL PARAMETERS




***SQL48T Pinout (Through-Hole)***




**SQL48T Platform Notes**

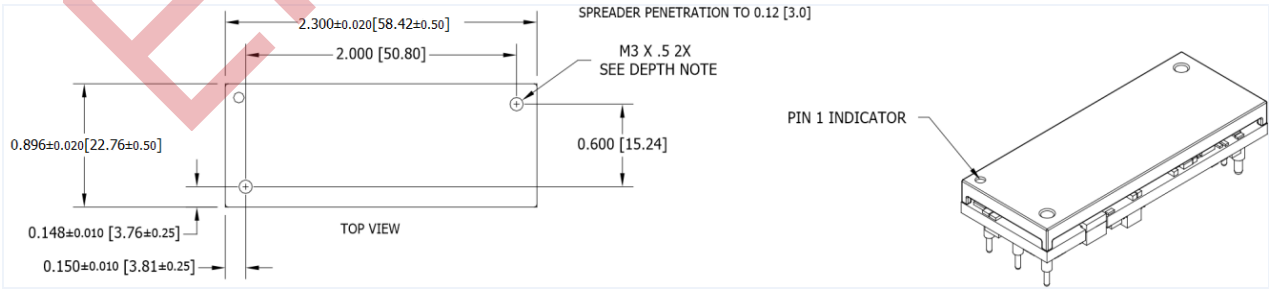
- All dimensions are in inches [mm]
- Pins 1-3, 5-7 are Ø 0.040” [1.02] with Ø 0.076” [1.93] shoulder
- Pins 4 and 8 are Ø 0.062” [1.57] with are Ø 0.096” [2.44] shoulder
- Pin Material: Brass Alloy 360
- Pin Finish: Tin over Nickel

| | Height [HT] | Minimum Clearance [CL] | Special Features |
|---|---|---|---|
| D | 0.375” [9.53] max | 0.040” [1.02] | 0 |
| | 0.500”+/-0.020 [12.70+/-0.51] | 0.040” [1.02] | B |

| Pin Option | PL Pin Length |
|---|---|
| | ±0.005 [±0.13] |
| A | 0.188 [4.78] |
| B | 0.145 [3.68] |

| PAD/PIN CONNECTIONS | |
|---|---|
| Pad/Pin # | Function |
| 1 | Vin (+) |
| 2 | ON/OFF |
| 3 | Vin (-) |
| 4 | Vout (-) |
| 5 | SENSE(-) |
| 6 | TRIM |
| 7 | SENSE(+) |
| 8 | Vout (+) |

**HEAT SPREADER INTERFACE INFORMATION**



## 6. ORDERING INFORMATION

| Product Series | Input Voltage | Mounting Scheme | Rated Current | Output Voltage | | ON/OFF Logic | Maximum Height [HT] | Pin Length [PL] | Special Features | RoHS |
|---|---|---|---|---|---|---|---|---|---|---|
| **SQL** | **48** | **T** | **20** | **033** | **-** | **N** | **D** | **A** | **B** | **G** |
| 1/8th Brick Format | 36-75 V | T ⇒ Throughhole | 20 ⇒ 20 ADC | 033 ⇒ 3.3V | | N ⇒ Negative<br>P ⇒ Positive | D ⇒ 0.375" for -xxx0x<br>for -xxxBx0.520" | Through hole<br>A ⇒ 0.188"<br>B ⇒ 0.145" | 0 ⇒ 2250 VDC isolation<br>B ⇒ Baseplate option + '0' above | No Suffix ⇒ RoHS lead-solder-exemption compliant<br>G ⇒ RoHS compliant for all six substances |

The example above describes P/N SQL48T20033-NDABG: 36-75V input, through-hole, 20 A @ 3.3 V output, negative ON/OFF logic, maximum height of 0.52", 0.188" pin length, 2250 VDC isolation, integral heat spreader (Baseplate) and RoHS compliant for all 6 substances. Consult factory for availability of other options.



**For more information on these products consult: tech.support@psbel.com**

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