



# TET3200-12-069xA

## AC-DC / HVDC Front-End Power Supplies

The TET3200 Series is a 3200 Watt AC-DC power-factor-corrected (PFC) or DC/DC power supply that converts standard AC mains power or high voltage DC bus voltages into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The TET3200-12-069xA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



### Key Features & Benefits

- Best-in-class, Titanium efficiency
- Universal input voltage range: 90 - 300 VAC
- AC input with power factor correction
- DC input voltage range: 180 - 410 VDC
- Hot-plug capable
- Parallel operation with active current sharing thru analog bus
- Full digital controls for improved performance
- High density design: 33.8 W/in<sup>3</sup>
- Small form factor: 555 x 69 x 40.5 mm (21.85 x 2.72 x 1.60 in)
- I2C communication interface with Power Management Bus protocol for monitoring, control, and firmware update via bootloader
- Overtemperature, output overvoltage and overcurrent protection
- RoHS Compliant
- 2 Status LEDs: AC OK and DC OK with fault signaling
- Safety approved to UL/CSA 62368-1, IEC/EN 62368-1 & IEC/EN 60950-1
- Three US patents (US 6,970,366 B2; US 8,503,199 B1; US9,166,498 B2) and three US patents pending



### Applications

- High Performance Servers
- Routers
- Networking Switches



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## 1. ORDERING INFORMATION

TET	3200	-	12	-	069	x	A	Option Code
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input	
TET Front-End	3200 W		12 V		69 mm	N: Normal R: Reverse <sup>1)</sup>	A: AC	Blank: Standard model

<sup>1)</sup> Front to Rear

## 2. OVERVIEW

The TET3200-12-069RA is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonant-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range and minimal linear derating of output power with respect to ambient temperature, the TET3200-12-069RA maximizes power availability in demanding server, switch, and router applications. The power supply is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on +12V standby output provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LEDs. In addition, the power supply can be monitored and controlled (i.e. fan speed setpoint) via I2C communication interface with Power Management Bus protocol. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The same I2C bus supports the bootloader to allow field update of the firmware in the DSP controllers.

Cooling is managed by a fan, controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C buses.

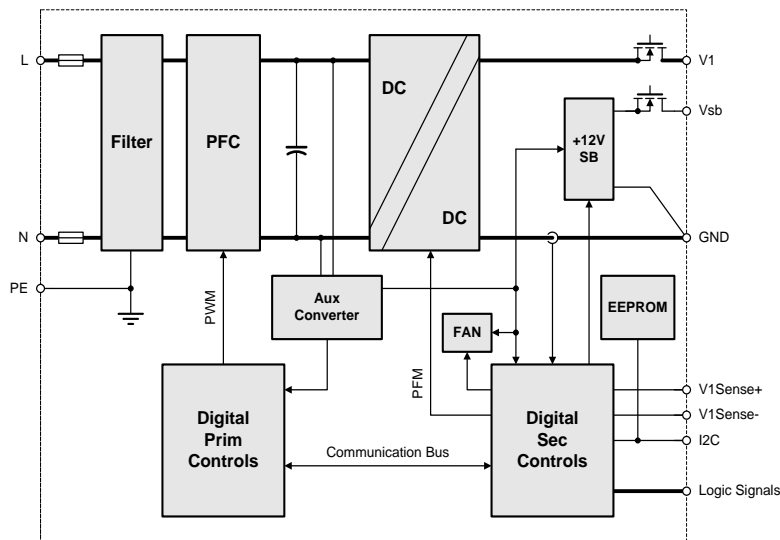


Figure 1. TET3200-12-069RA Block Diagram

## 3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the supply.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
$V_i$ maxc	Maximum Input	Continuous	300	VAC

## 4. INPUT

General Condition:  $T_A = 0 \dots +50 \text{ }^\circ\text{C}$ , unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT	
$V_{i,nom}$	AC Nominal Input Voltage	100	230	277	VAC	
$V_i$	AC Input Voltage Ranges	Normal operating ( $V_{i,min}$ to $V_{i,max}$ )		300	VAC	
$V_{i,nom,DC}$	DC Nominal Input Voltage <sup>2)</sup>	240		380	VDC	
$V_{i,DC}$	DC Input Voltage Ranges	Normal operating ( $V_{i,min}$ to $V_{i,max}$ )		410	VDC	
$V_{i,derated}$	Derated Input Voltage Range	See <i>Figure 20</i> and <i>Figure 33</i>		180	VAC	
$I_{i,max}$	Max Input Current	$V_i > 200 \text{ VAC}$ , $> 100 \text{ VAC}$		17	$A_{rms}$	
$I_{i,p}$	Inrush Current Limitation	$V_{i,min}$ to $V_{i,max}$ , $T_{NTC} = 25^\circ\text{C}$ ( <i>Figure 5</i> )		35	$A_p$	
$F_i$	Input Frequency	47	50/60	63	Hz	
$PF$	Power Factor	$V_{i,nom}$ , 50Hz, $> 0.2 I_{i,nom}$		0.96	0.99	W/VA
$V_{i,on}$	Turn-on Input Voltage <sup>3)</sup>	Ramping up		80	87	VAC
$V_{i,off}$	Turn-off Input Voltage <sup>3)</sup>	Ramping down		75	85	VAC
$\eta$	Efficiency Without Fan	$V_i = 230 \text{ VAC}$ , $0.1 \cdot k_{nom}$ , $V_{X,nom}$ , $T_A = 25^\circ\text{C}$		94.34		
		$V_i = 230 \text{ VAC}$ , $0.2 \cdot k_{nom}$ , $V_{X,nom}$ , $T_A = 25^\circ\text{C}$		95.41		
		$V_i = 230 \text{ VAC}$ , $0.5 \cdot k_{nom}$ , $V_{X,nom}$ , $T_A = 25^\circ\text{C}$		95.05		
		$V_i = 230 \text{ VAC}$ , $k_{nom}$ , $V_{X,nom}$ , $T_A = 25^\circ\text{C}$		93.89		
$T_{hold}$	Hold-up Time	After last AC zero point, $V_i > 10.8\text{V}$ , $V_{SB}$ within regulation, $V_i = 230 \text{ VAC}$ , $P_{X,nom}$		12	16	ms

<sup>2)</sup> In HVDC input application, LIVE pin has to be connected to "+" and NEUTRAL has to be connected to "-", Otherwise PSU will have no output

<sup>3)</sup> The Front-End is provided with a typical hysteresis of 3 V during turn-on and turn-off within the ranges.

### 4.1 INPUT FUSE

Quick-acting 25 A input fuses (7 × 32.7 in mm) in series with both the L- and N-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

### 4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 4.3  $\mu\text{F}$ , resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations below 5 sec interval time at maximum input, high temperature condition, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

### 4.3 INPUT UNDER-VOLTAGE

If the RMS value of input voltage (either AC or DC) stays below the input undervoltage lockout threshold  $V_{i,on}$ , the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

### 4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) (see *Figure 4*) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform. At DC input voltage the PFC is still in operation, but the input current will be DC in this case.



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### 4.5 EFFICIENCY

The high efficiency (see *Figure 2*) is achieved by using state-of-the-art GaN power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions. *Figure 3* shows efficiency when input voltage is supplied from a high voltage DC source.

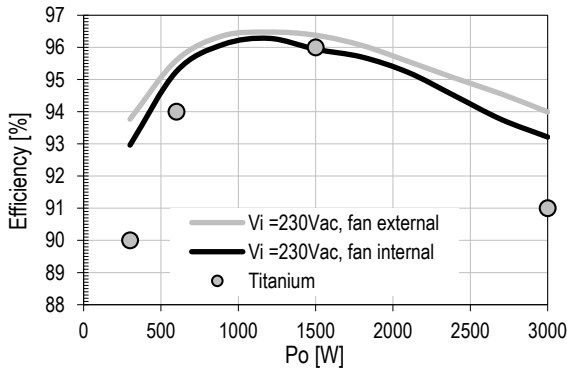


Figure 2. AC Input Efficiency vs. Load current

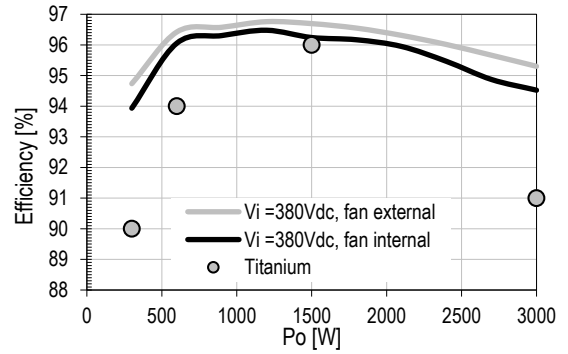


Figure 3. DC Input Efficiency vs. Load

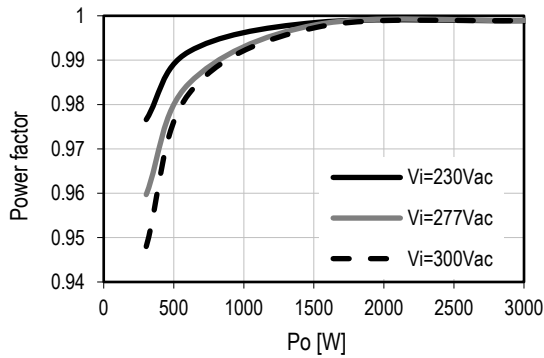


Figure 4. Power Factor vs. Load

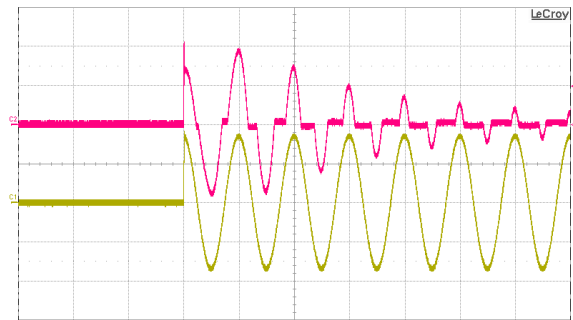


Figure 5. Inrush Current,  $V_{in} = 300\text{Vac}$ ,  $90^\circ$  phase angle  
 CH1:  $V_{in}$  (250V/div), CH2:  $i_{in}$  (10A/div), 20 ms/div

## 5. OUTPUT

General Condition:  $T_A = 0...+45\text{ }^\circ\text{C}$ , unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
<b>Main Output <math>V_I</math></b>					
$V_{I\text{ nom}}$	Nominal Output Voltage		12.3		VDC
$V_{I\text{ set}}$	Output Setpoint Accuracy	$0.5 \cdot I_{\text{ nom}}, T_{\text{ amb}} = 25\text{ }^\circ\text{C}$		+0.5	% $V_{I\text{ nom}}$
$dV_{I\text{ tot}}$	Total Regulation	$V_{I\text{ min}}$ to $V_{I\text{ max}}, 0$ to 100% $I_{\text{ nom}}, T_{a\text{ min}}$ to $T_{a\text{ max}}$		+2	% $V_{I\text{ nom}}$
$P_{I\text{ nomll}}$	Nominal Output Power	$V_I = 12.3\text{ VDC}, V_{\text{ in}} < 180\text{ VAC}$	See Figure 33		W
$I_{I\text{ nomll}}$	Nominal Output Current	$V_I = 12.3\text{ VDC}, V_{\text{ in}} < 180\text{ VAC}$	See Figure 20		A
$P_{I\text{ nom}}$	Nominal Output Power	$V_I = 12.3\text{ VDC}, V_{\text{ in}} > 180\text{ VAC}$	3200		W
$I_{I\text{ nom}}$	Nominal Output Current	$V_I = 12.3\text{ VDC}, V_{\text{ in}} > 180\text{ VAC}$	260		A
$I_{I\text{ ol}}$	Short Time Over Load Current	$V_I = 12.3\text{ VDC}, V_{\text{ in}} > 180\text{ VAC}$ $T_{a\text{ min}}$ to $T_{a\text{ max}},$ maximum duration 20 ms (See Section 5.2)		292	A
$V_{I\text{ pp}}$	Output Ripple Voltage	$V_{I\text{ nom}}, I_{\text{ nom}}, 20\text{ MHz BW}$ (See Section 5.1)	70	120	mVpp
$dV_{I\text{ Load}}$	Load Regulation	$V_I = V_{I\text{ nom}}, 0 - 100\% I_{\text{ nom}}$	180		mV
$dV_{I\text{ Line}}$	Line Regulation	$V_I = V_{I\text{ min}}... V_{I\text{ max}}$	0		mV
$dI_{\text{ share}}$	Current Sharing	$(I_x - I_y) / I_{\text{ tot}}, I > 25\% I_{\text{ nom}}$	-5	+5	%
$dV_{I\text{ dyn}}$	Dynamic Load Regulation	$\Delta I = 50\% I_{\text{ nom}}, I = 5 \dots 100\% I_{\text{ nom}},$ $dI/dt = 1\text{ A}/\mu\text{s},$ recovery within 1% of $V_{I\text{ nom}}$	-0.6	0.6	V
$T_{\text{ rec}}$	Recovery Time		0.5	1	ms
$t_{\text{ AC } V_I}$	Start-up Time from AC	$V_I = 10.8\text{ VDC}$ (see Figure 7)	2.7	3	sec
$t_{V_I\text{ rise}}$	Rise Time	$V_I = 10...90\% V_{I\text{ nom}}$ (see Figure 8)		20	ms
$C_{\text{ Load}}$	Capacitive Loading	$T_a = 25\text{ }^\circ\text{C}$		30,000	$\mu\text{F}$
<b>Standby Output <math>V_{SB}</math></b>					
$V_{SB\text{ nom}}$	Nominal Output Voltage		12		VDC
$V_{SB\text{ set}}$	Output Setpoint Accuracy	$0.5 \cdot I_{SB\text{ nom}}, T_{\text{ amb}} = 25\text{ }^\circ\text{C}$		+1	% $V_{SB\text{ nom}}$
$dV_{SB\text{ tot}}$	Total Regulation	$V_{I\text{ min}}$ to $V_{I\text{ max}}, 0$ to 100% $I_{SB\text{ nom}}, T_{a\text{ min}}$ to $T_{a\text{ max}}$		+3	% $V_{SB\text{ nom}}$
$P_{SB\text{ nom}}$	Nominal Output Power	$V_{SB} = 12\text{ VDC}$	36		W
$I_{SB\text{ nom}}$	Nominal Output Current	$V_{SB} = 12\text{ VDC}$	3		A
$V_{SB\text{ pp}}$	Output Ripple Voltage	$V_{SB\text{ nom}}, I_{SB\text{ nom}}, 20\text{ MHz BW}$ (See Section 5.1)	60	120	mVpp
$dV_{SB}$	Droop	$0 - 100\% I_{SB\text{ nom}}$	200		mV
$dV_{SB\text{ dyn}}$	Dynamic Load Regulation	$\Delta I_{SB} = 50\% I_{SB\text{ nom}}, I_{SB} = 5 \dots 100\% I_{SB\text{ nom}},$ $dI/dt = 1\text{ A}/\mu\text{s},$ recovery within 1% of $V_{I\text{ nom}}$	-0.6	0.6	V
$T_{\text{ rec}}$	Recovery Time			0.5	ms
$t_{\text{ AC } V_{SB}}$	Start-up Time from AC	$V_{SB} = 90\% V_{SB\text{ nom}}$ (see Figure 7)	2.5	3	sec
$t_{V_{SB}\text{ rise}}$	Rise Time	$V_{SB} = 10...90\% V_{SB\text{ nom}}$ (see Figure 9)		20	ms
$C_{\text{ Load}}$	Capacitive Loading	$T_{\text{ amb}} = 25\text{ }^\circ\text{C}$		1,500	$\mu\text{F}$

## 5.1 OUTPUT VOLTAGE RIPPLE

Ripple and noise shall be measured using the following methods:

- Outputs bypassed at the point of measurement with a parallel combination of 10  $\mu\text{F}$  tantalum capacitor in parallel with 0.1  $\mu\text{F}$  ceramic capacitors, referring the setup in *Figure 6*.
- The ripple voltage is measured with 20 MHz BWL.

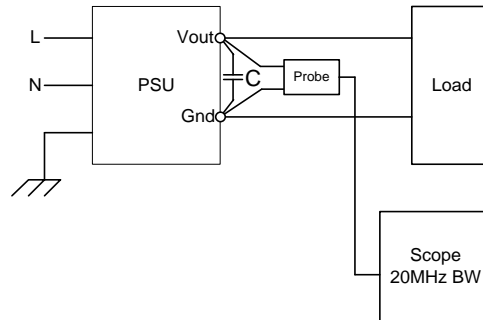


Figure 6. Output Ripple Test Setup

## 5.2 SHORT TIME OVERLOAD

The main output has the capability to allow output power up to 3600 W for a maximum duration of 20ms. This allows the system to consume extended power for short time dynamic processes.

## 5.3 OUTPUT ISOLATION

Main and standby output and all signals are isolated from the chassis and protective earth connection, although the applied voltage must not exceed 100 V<sub>peak</sub> to prevent any damage of the supply.

In order to prevent any potential difference in outputs or signals within the application these 3 grounds must be directly interconnected at system level. See also section 14 for pins to be interconnected.

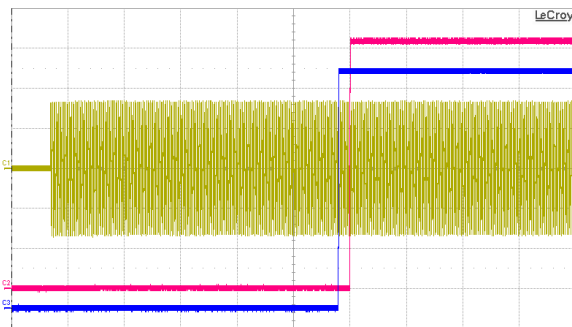


Figure 7. Turn-On AC Line 230 VAC, full load (500 ms/div)  
CH1: Vin (200V/div); CH2: V1 (2V/div); CH3: VSB (2V/div)

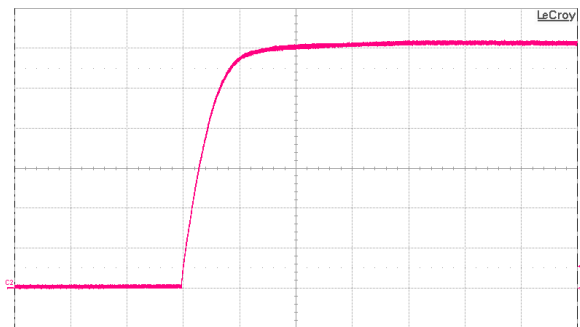


Figure 8. Turn-On AC Line 230 VAC, full load (1 ms/div)  
CH2: V1 (2 V/div)

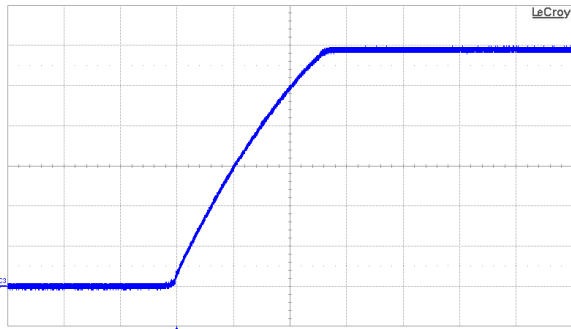


Figure 9. On AC Line 230 VAC, full load (2 ms/div)  
CH3: VSB (2 V/div)

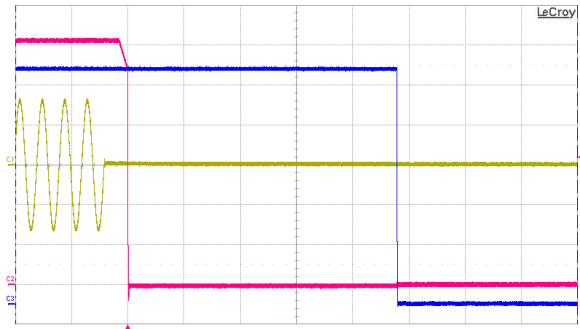


Figure 10. Turn-Off AC Line 230 VAC, full load (50 ms/div)  
CH1: Vin (200V/div); CH2: V1 (2V/div); CH3: VSB (2V/div)

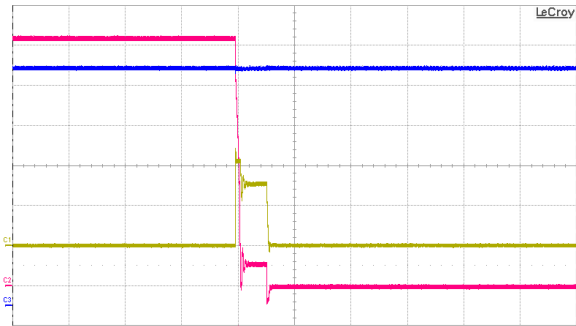


Figure 11. Short Circuit on V1 (20ms/div)  
CH1: I1 (200 A/div); CH2: V1 (2V/div); CH3: VSB (2V/div)

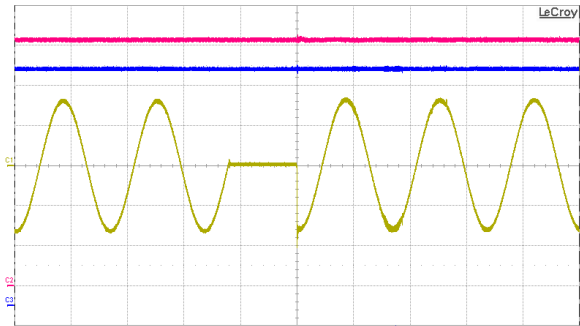


Figure 12. AC Drop Out 12ms, 80% full load (10ms/div)  
CH1: Vin (200V/div); CH2: V1 (2V/div); CH3: VSB (2V/div)

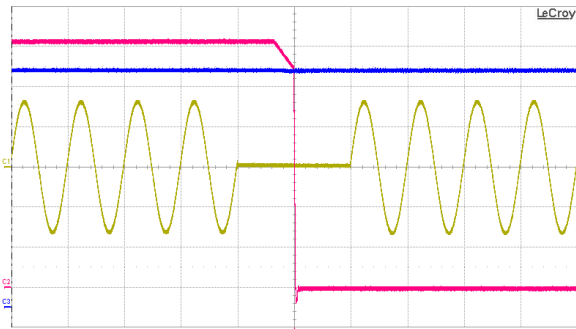


Figure 13. AC Drop Out 40 ms, full load (20 ms/div)  
CH1: Vin (200 V/div); CH2: V1 (2 V/div); CH3: VSB (2 V/div)

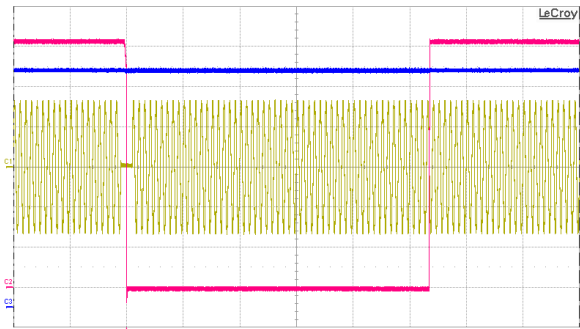


Figure 14. AC Drop Out 40 ms, full load (200 ms/div),  
CH1: Vin (200 V/div); CH2: V1 (2 V/div); CH3: VSB (2 V/div)

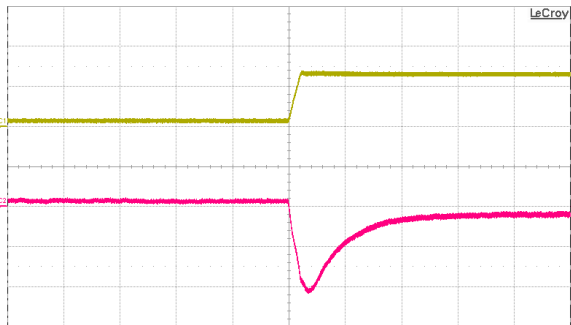


Figure 15. Load Transient V1, 12 to 134 A (500  $\mu$ s/div)  
CH1: I1 (100 A/div); CH2: V1 (200 mV/div)

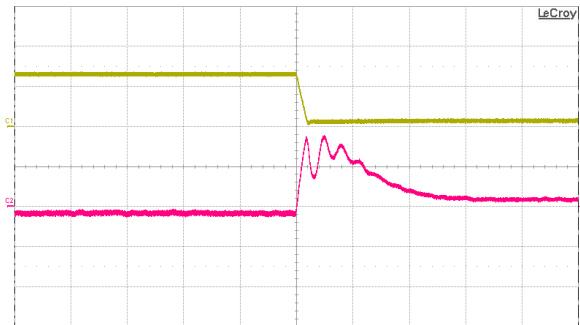


Figure 16. Load Transient V1, 134 to 12 A (500  $\mu$ s/div)  
CH1: I1 (100 A/div); CH2: V1 (200 mV/div)

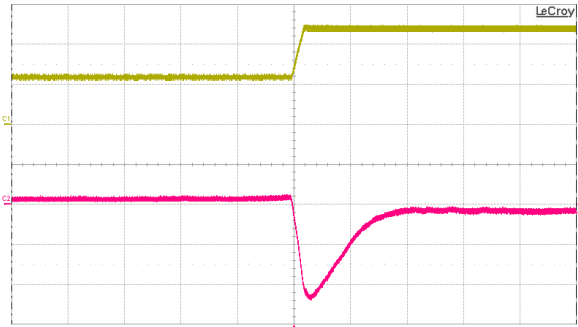


Figure 17. Load Transient  $V_1$ , 122 to 244 A (500  $\mu$ s/div)  
CH1: I1 (100 A/div); CH2:  $V_1$  (200 mV/div)

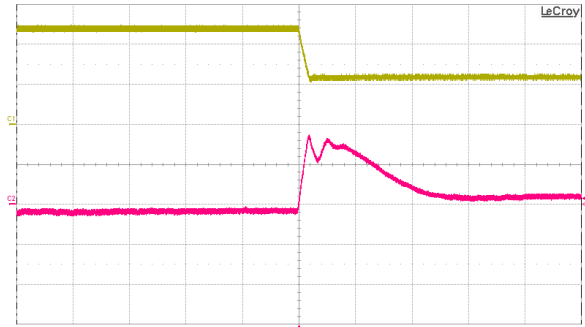


Figure 18. Load Transient  $V_1$ , 244 to 122 A (500  $\mu$ s/div)  
CH1: I1 (100 A/div); CH2:  $V_1$  (200 mV/div)

## 6. PROTECTION

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$F$	Input Fuses (L+N)	Not user accessible, quick-acting (F)			A
$V_1$ OV	OV Threshold $V_1$	13.6	14.2	14.8	VDC
$t_{OV V1}$	OV Latch Off Time $V_1$			1	ms
$V_{SB}$ OV	OV Threshold $V_{SB}$	13.3	13.9	14.5	VDC
$t_{OV VSB}$	OV Latch Off Time $V_{SB}$			1	ms
$I_1$ lim	Current Limitation $I_1$	See Figure 20 $V_1 < 180$ VAC, $T_a < 45^\circ\text{C}$ $V_1 < 180$ VAC, $T_a = 60^\circ\text{C}$ <sup>4)</sup> $V_1 > 180$ VAC, $T_a < 45^\circ\text{C}$ $V_1 > 180$ VAC, $T_a = 60^\circ\text{C}$ <sup>4)</sup>			A
$t_{V1}$ lim	Current Limit Blanking Time	20	25	30	ms
$I_1$ ol lim	Current Limit During Short Time Overload $I_1$	292	300	308	A
$I_1$ SC	Max Short Circuit Current $I_1$	$V_1 < 3$ V			350 <sup>5)</sup> A
$t_{V1 SC off}$	Short Circuit Latch Off Time	Time to latch off when in short circuit			10 ms
$V_{SB}$ lim	Current Limitation $V_{SB}$	3.45		4.05	A
$V_{SB}$ lim	Current Limit Blanking Time	Time to hit hiccup when in over current			1 ms
$T_{SD}$	Over Temperature on Critical Points	Inlet ambient temperature PFC heatsink temperature DC-DC primary heatsink temperature OR-ing Mosfet temperature			60 85 105 115 °C

<sup>4)</sup> See Figure 20 for linear derating  $> 45^\circ\text{C}$

<sup>5)</sup> Limit set doesn't include effects of main output capacitive discharge.

### 6.1 OVERVOLTAGE PROTECTION

The PSU provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition.

### 6.2 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK\_L pin signal if the output voltage exceeds  $\pm 7\%$  of its nominal voltage.

Output undervoltage protection is provided on both outputs. When either  $V_1$  or  $V_{SB}$  falls below 93% of its nominal voltage, the output is inhibited.



### 6.3 CURRENT LIMITATION

#### MAIN OUTPUT

Two different over current protection features are implemented on the main output.

A static over current protection will shut down the output, if the output current does exceed  $I_{V1\ lim}$  for more than 20ms. If the output current is increased slowly this protection will shut down the supply.

The main output current limitation level  $I_{V1\ lim}$  will decrease if the ambient (inlet) temperature increases beyond 45 °C (see *Figure 20*).

The 2<sup>nd</sup> protection is a substantially rectangular output characteristic controlled by a software feedback loop. This protects the power supply and system during the 20 ms blanking time of the static over current protection. If the output current is rising fast and reaches  $I_{V1\ ol\ lim}$ , the supply will immediately reduce its output voltage to prevent the output current from exceeding  $I_{V1\ ol\ lim}$ . When the output current is reduced below  $I_{V1\ ol\ lim}$ , the output voltage will return to its nominal value.

When the main output over current, the  $V_1$  will shut down for 10sec and restart automatically. The supply will auto-restart from a fault up to 5 times, after that it will latch off. The latch and restart counter can be cleared by recycling the input voltage or the PSON\_L input. A failure on the Main output will shut down only the Main output, while Standby continues to operate.

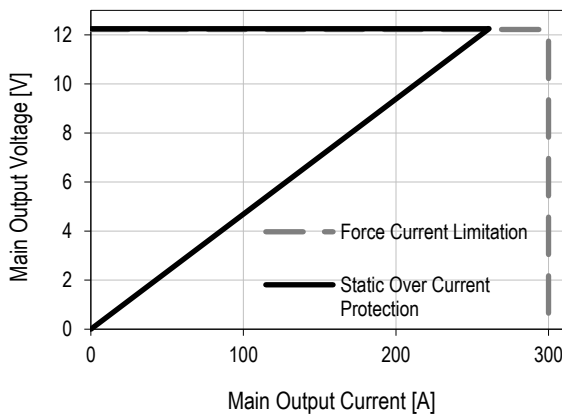


Figure 19. Current Limitation on  $V_1$  ( $V_i = 230VAC$ )

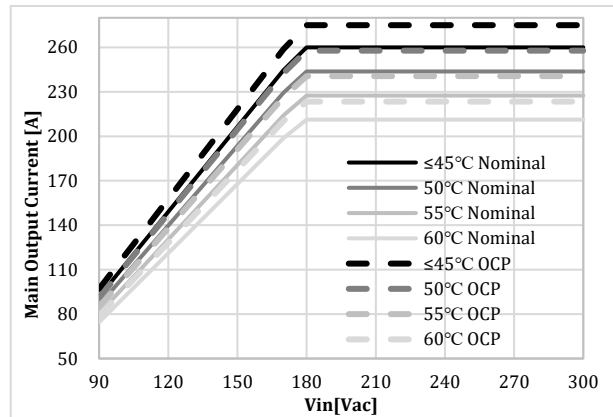


Figure 20. Derating on  $V_1$  vs  $T_a$  &  $V_{in}$

Vin(Vac)	≤45C	≤45C	≤50C	≤50C	≤55C	≤55C	≤60C	≤60C
	Iout_Nom (A)	Iout_OC P(A)	Iout_No m(A)	Iout_OC P(A)	Iout_No m(A)	Iout_OCP(A)	Iout_Nom(A)	Iout_OCP(A)
90	92	97	86	91	80	85	75	79
100	111	117	104	110	97	103	90	95
110	130	137	122	129	114	120	106	112
120	149	158	140	148	130	138	121	128
130	168	178	158	167	147	156	137	145
140	187	198	176	186	164	173	152	161
150	206	218	194	205	181	191	168	177
160	226	239	211	224	197	209	183	194
170	245	259	229	243	214	226	199	210
180	260	275	244	258	228	241	211	223
190	260	275	244	258	228	241	211	223
200	260	275	244	258	228	241	211	223
210	260	275	244	258	228	241	211	223
220	260	275	244	258	228	241	211	223
230	260	275	244	258	228	241	211	223
240	260	275	244	258	228	241	211	223
250-300	260	275	244	258	228	241	211	223

Main Output Nominal Output Current  $I_{1\ noml}$  & Current Limitation  $I_{V1\ lim}$  vs Inlet Temperature (degC) &  $V_{in}(Vac)$



## STANDBY OUTPUT

On the standby output a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds  $I_{SB\ lim}$ . After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

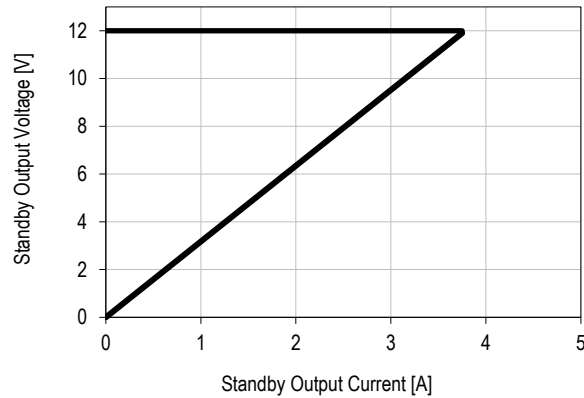


Figure 21. Current Limitation on  $V_{SB}$

## 7. MONITORING

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{mon}$	Input RMS Voltage $V_{min} \leq V \leq V_{max}$	-2.5		+2.5	%
$I_{mon}$	Input RMS Current $I > 6 A_{rms}$ $I \leq 6 A_{rms}$	-5 -0.3		+5 +0.3	% $A_{rms}$
$P_{mon}$	True Input Power $P > 700 W$ $P \leq 700 W$	-5 -35		+5 +35	% W
$V_{1\ mon}$	$V_1$ Voltage	-2		+2	%
$I_{1\ mon}$	$V_1$ Current $I_1 > 30 A$ $I_1 \leq 30 A$	-2 -1		+2 +1	% A
$P_{o\ nom}$	Total Output Power $P_o > 200 W$ $P_o \leq 200 W$	-5 -10		+5 +10	% W
$V_{SB\ mon}$	Standby Voltage	-2		+2	%
$I_{SB\ mon}$	Standby Current $I_{SB} \leq I_{SB\ nom}$	-0.2		+0.2	A

## 8. SIGNALING AND CONTROL

### 8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
<b>PSKILL / PSON_L inputs</b>					
$V_{IL}$	Input low level voltage	-0.2		0.5	V
$V_{IH}$	Input high level voltage	2.0		3.6	V
$I_{L, H}$	Maximum input sink or source current	0		1	mA
$R_{puPSKILL}$	Internal pull up resistor on PSKILL		10		k $\Omega$
$R_{puPSON\_L}$	Internal pull up resistor on PSON_L		10		k $\Omega$
<b>PWOK_L output</b>					
$V_{OL}$	Output low level voltage	$I_{sink} < 4 \text{ mA}$	-0.2	0.4	V
$V_{puPWOK\_L}$	External pull up voltage			12	V
$R_{puPWOK\_L}$	Recommended external pull up resistor on PWOK_L at $V_{puPWOK\_L} = 3.3 \text{ V}$		10		k $\Omega$
<i>Low level output</i>	All outputs are turned on and within regulation				
<i>High level output</i>	In standby mode or $V_I/V_{SB}$ have triggered a fault condition				
<b>INOK_L output</b>					
$V_{OL}$	Output low level voltage	$I_{sink} < 4 \text{ mA}$	-0.2	0.4	V
$V_{puINOK\_L}$	External pull up voltage			12	V
$R_{puINOK\_L}$	Recommended external pull up resistor on INOK_L at $V_{puINOK\_L} = 3.3 \text{ V}$		10		k $\Omega$
<i>Low level output</i>	Input voltage is within range for PSU to operate				
<i>High level output</i>	Input voltage is not within range for PSU to operate				
<b>SMB_ALERT_L output</b>					
$V_{OL}$	Output low level voltage	$I_{sink} < 4 \text{ mA}$	-0.2	0.4	V
$V_{puSMB\_ALERT\_L}$	External pull up voltage			12	V
$R_{puSMB\_ALERT\_L}$	Recommended external pull up resistor on SMB_ALERT_L at $V_{puSMB\_ALERT\_L} = 3.3 \text{ V}$		10		k $\Omega$
<i>Low level output</i>	PSU in warning or failure condition				
<i>High level output</i>	PSU is ok				

### 8.2 INTERFACING WITH SIGNALS

A 15V zener diode is added on all signal pins versus signal ground SGND to protect internal circuits from negative and high positive voltage. Signal pins of several supplies running in parallel can be interconnected directly. A supply having no input power will not affect the signals of the paralleled supplies.

ISHARE pins must be interconnected without any additional components. This in-/output also has a 15 V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

### 8.3 FRONT LEDS

The front-end has 2 front LEDs showing the status of the supply. LED number one is green and indicates AC power is on or off, while LED number two is bi-colored: green and yellow and indicates DC power presence or fault situations. For the position of the LEDs see *Table 1* lists the different LED status.

OPERATING CONDITION	LED SIGNALING
<b>AC LED</b>	
AC Line Within Range	Solid Green
AC Line UV Condition	Off
<b>DC LED<sup>6)</sup></b>	
Normal Operation	Solid Green
PSON_L High	Blinking Yellow (1:1)
$V_I$ or $V_{SB}$ Out Of Regulation	Solid Yellow
Over Temperature Shutdown	
Output Over Voltage Shutdown ( $V_I$ or $V_{SB}$ )	
Output Under Voltage Shutdown ( $V_I$ or $V_{SB}$ )	
Output Over Current Shutdown ( $V_I$ or $V_{SB}$ )	Blinking Yellow/Green (2:1)
Over Temperature Warning	
Minor Fan Regulation Error (>5%, <15%)	Blinking Yellow/Green (1:1)

<sup>6)</sup> The order of the criteria in the table corresponds to the testing precedence in the controller.

Table 1. LED Status

### 8.4 PRESENT\_L

The PRESENT\_L is normally a trailing pin within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum sink current on PRESENT\_L pin should not exceed 10 mA.

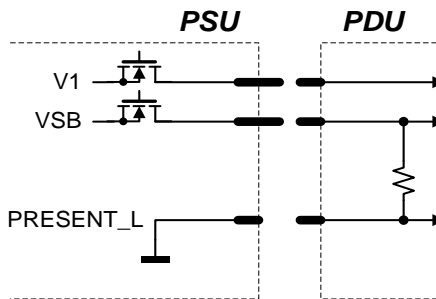


Figure 22. PRESENT\_L Signal Pin

### 8.5 PSKILL INPUT

The PSKILL input is an active-high and normally a trailing pin in the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL input state.

### 8.6 AC TURN-ON / DROP-OUTS / INOK\_L

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON\_L signal is pulled low and the AC line is within range. The INOK\_L is an open collector output that requires an external pull-up to a maximum of 12V indicating whether the input is within the range the power supply can use and turn on. The INOK\_L signal is active-low. The timing diagram is shown in *Figure 23* and referenced in *Table 2*.

OPERATING CONDITION	MIN	MAX	UNIT
$t_{AC\ VSB}$ AC Line to 90% $V_{SB}$		3	sec
$t_{AC\ V1}$ AC Line to 90% $V_1$		3	sec
$t_{INOK\_L\ on1}$ INOK_L signal on delay (start-up)		1800	ms
$t_{INOK\_L\ on2}$ INOK_L signal on delay (dips)	0	100	ms
$t_{V1\ holdup}$ Effective $V_1$ holdup time	12	300	ms
$t_{VSB\ holdup}$ Effective $V_{SB}$ holdup time	40	300	ms
$t_{INOK\_L\ V1}$ INOK_L to $V_1$ holdup	7		ms
$t_{INOK\_L\ VSB}$ INOK_L to $V_{SB}$ holdup	27		ms
$t_{V1\ off}$ Minimum $V_1$ off time	1000		ms
$t_{VSB\ off}$ Minimum $V_{SB}$ off time	1000		ms
$t_{V1\ dropout}$ Minimum $V_1$ dropout time ( $0.8 \cdot I_{1\ nom}$ )	12		ms
$t_{VSB\ dropout}$ Minimum $V_{SB}$ dropout time	40		ms

Table 2. AC Turn-on / Dip Timing

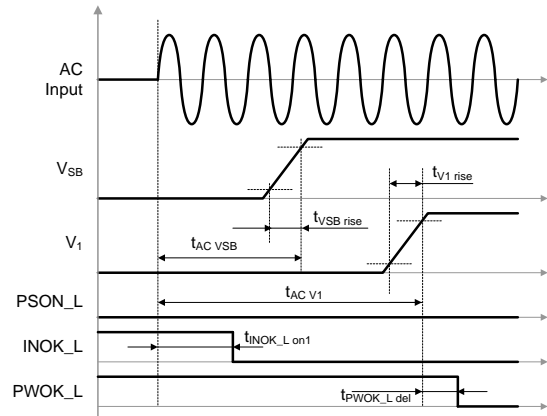


Figure 23. AC Turn-On Timing

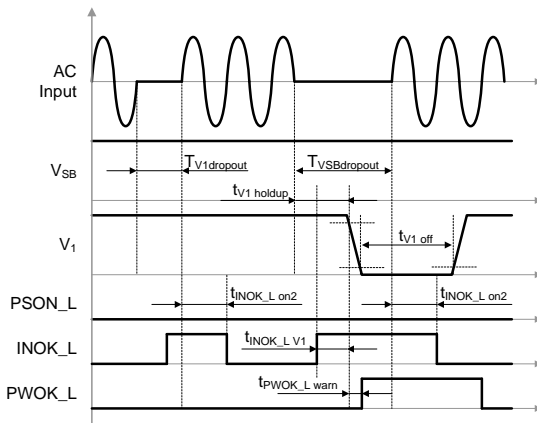


Figure 24. AC Short Dips

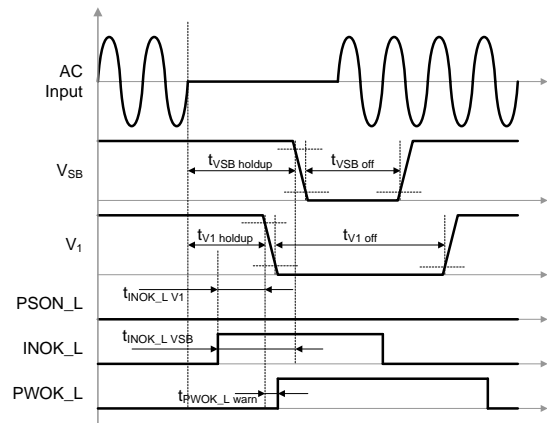


Figure 25. AC Long Dips

### 8.7 PSON\_L INPUT

The PSON\_L is an internally pulled-up (3.3V) input signal to enable / disable the main output  $V_1$  of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in *Figure 26* and the parameters in *Table 3*.

OPERATING CONDITION	MIN	MAX	UNIT
$t_{PSON\_L\ V1on}$ PSON_L to $V_1$ Delay (on)	150	250	ms
$t_{PSON\_L\ V1off}$ PSON_L to $V_1$ Delay (off)	0	100	ms

Table 3. PSON\_L Timing



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North America  
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### 8.8 PWOK\_L SIGNAL

The PWOK\_L is an open collector output that requires an external pull-up to a maximum of 12 V indicating whether both  $V_{SB}$  and  $V_1$  outputs are within regulation. This pin is active-low. The timing diagram is shown in *Figure 26* and referenced in *Table 4*.

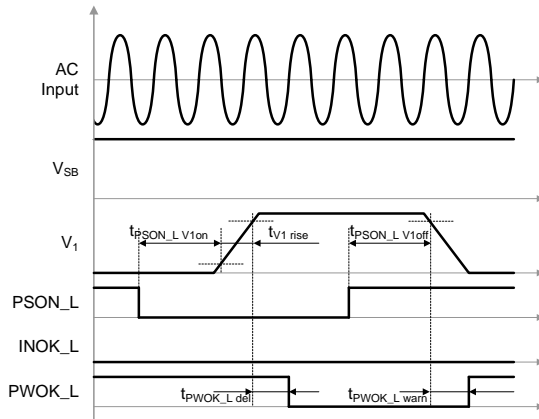


Figure 26. PSON\_L Turn-on/off Timing

OPERATING CONDITION	MIN	MAX	UNIT
$t_{PWOK\_L\ del}$ $V_1$ to PWOK_L Delay (on)	250	350	ms
$t_{PWOK\_L\ warn}$ $V_1$ to PWOK_L Delay (off)	0	5	ms

Table 4. PWOK\_H Timing

### 8.9 CURRENT SHARE

The PSU have an active current share scheme implemented for  $V_1$ . All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

No of paralleled PSUs	Maximum available power on main 12V without redundancy	Maximum available power on main 12V with n+1 redundancy	Maximum available power on standby output
1	3,200 W	-	36 W
2	6,240 W	3,200 W	36 W
3	9,280 W	6,240 W	36 W
4	12,320 W	9,280 W	36 W
5	15,360 W	12,320 W	36 W
6	18,400 W	15,360 W	36 W

Table 5. Power Available When PSU in Redundant Operation

### 8.10 SENSE INPUTS

Main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.11 I2C / POWER MANAGEMENT BUS COMMUNICATION

The interface driver in the power supply is referenced to the SGND. The power supply is a communication slave device only; it never initiates messages on the I<sup>2</sup>C buses by itself. The communication bus voltage and timing is defined in Table 6 and further characterized through:

- There are 10kΩ internal pull-up resistors
- The SDA/SCL IOs must be pull-up externally to 3.3 ± 0.3 V
- Pull-up resistor should be 2 – 5 kΩ to ensure SMBUS compliant signal rise times
- I2C clock speed up to 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

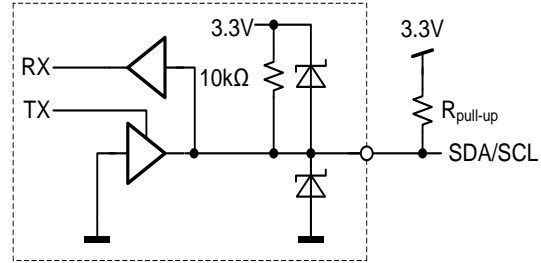


Figure 27. Physical Layer of Communication Interface

The SMB\_ALERT\_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. Communication to the DSP or the EEPROM will be possible as long as the input AC (DC) voltage is provided. If no AC (DC) is present, communication to the unit is possible as long as it is connected to a live V<sub>SB</sub> output (provided e.g. by the redundant unit). If only V<sub>I</sub> is provided, communication is not possible.

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V <sub>L</sub>	Input low voltage		-0.2	0.4	V
V <sub>H</sub>	Input high voltage		2.1	3.6	V
V <sub>hys</sub>	Input hysteresis		0.15		V
V <sub>oL</sub>	Output low voltage	4 mA sink current	0	0.4	V
t <sub>r</sub>	Rise time for SDA and SCL		20+0.1C <sub>b</sub> <sup>1</sup>	300	ns
t <sub>of</sub>	Output fall time V <sub>iHmin</sub> → V <sub>iLmax</sub>	10 pF < C <sub>b</sub> <sup>1</sup> < 400 pF	20+0.1C <sub>b</sub> <sup>1</sup>	250	ns
I	Input current SCL/SDA	0.1 VDD < V <sub>i</sub> < 0.9 VDD	-10	10	μA
C <sub>i</sub>	Capacitance for each SCL/SDA			47	pF
f <sub>SCL</sub>	SCL clock frequency		0	100	kHz
R <sub>pu</sub>	External pull-up resistor	f <sub>SCL</sub> ≤ 100 kHz		1000 ns / C <sub>b</sub> <sup>7)</sup>	Ω
t <sub>HDSTA</sub>	Hold time (repeated) START	f <sub>SCL</sub> ≤ 100 kHz	4.0		μs
t <sub>LOW</sub>	Low period of the SCL clock	f <sub>SCL</sub> ≤ 100 kHz	4.7		μs
t <sub>HIGH</sub>	High period of the SCL clock	f <sub>SCL</sub> ≤ 100 kHz	4.0		μs
t <sub>SUSTA</sub>	Setup time for a repeated START	f <sub>SCL</sub> ≤ 100 kHz	4.7		μs
t <sub>DDAT</sub>	Data hold time	f <sub>SCL</sub> ≤ 100 kHz	0	3.45	μs
t <sub>SUDAT</sub>	Data setup time	f <sub>SCL</sub> ≤ 100 kHz	250		ns
t <sub>SUSTO</sub>	Setup time for STOP condition	f <sub>SCL</sub> ≤ 100 kHz	4.0		μs
t <sub>BUF</sub>	Bus free time between STOP and START	f <sub>SCL</sub> ≤ 100 kHz	5		ms
<b>EEPROM_WP</b>					
V <sub>L</sub>	Input low voltage		-0.2	0.4	V
V <sub>H</sub>	Input high voltage		2.1	3.6	V
I	Input sink or source current		-1	1	mA
R <sub>pu</sub>	Internal pull-up resistor to 3.3V			10k	Ω

<sup>7)</sup> C<sub>b</sub> = Capacitance of bus line in pF, typically in the range of 10...400 pF

Table 6. I<sup>2</sup>C / SMBus Specification

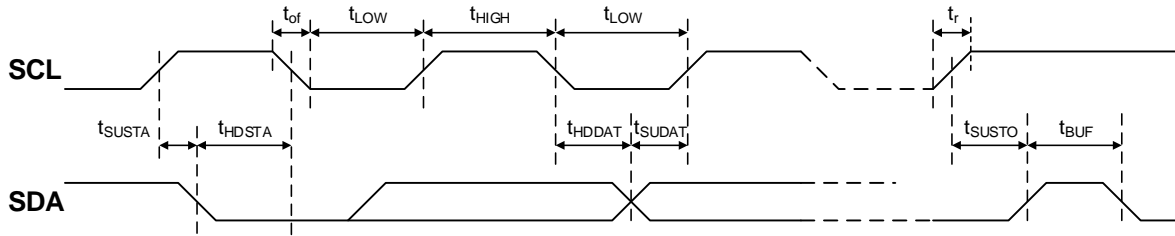


Figure 28.  $f_C$  / SMBus Timing

### 8.12 ADDRESS SELECTION

The supply supports Power Management Bus communication protocol, address for Power Management Bus communication is at fixed to 0x20. The EEPROM is at fixed address = 0xA0.

### 8.13 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I<sup>2</sup>C bus physical layer (see Figure 29). In order to write to the EEPROM, the write protection needs to be disabled by setting EEPROM\_WP input correctly. If EEPROM\_WP is High, write is not allowed to the EEPROM and if Low, write is allowed. The EEPROM provides 2K bits of user memory. None of the bytes are used for the operation of the power supply.

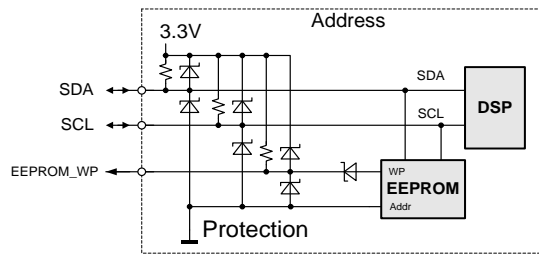


Figure 29.  $f_C$  Bus to DSP and EEPROM

### 8.14 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

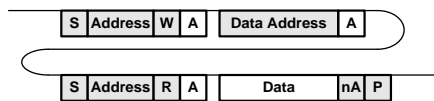
#### WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



#### READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.





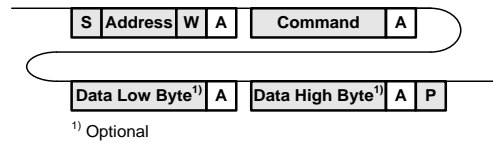
### 8.15 POWER MANAGEMENT BUS PROTOCOL

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: [www.powerSIG.org](http://www.powerSIG.org). Power Management Bus command codes are not register addresses. They describe a specific command to be executed. TET3200-12-069RA supply supports the following basic command structures:

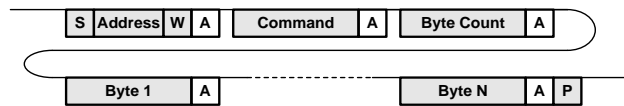
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

#### WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).

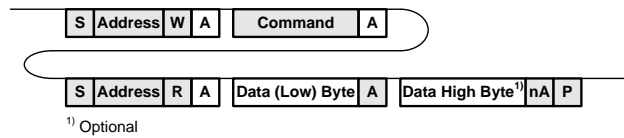


In addition, Block write commands are supported with a total maximum length of 255 bytes. See TET3200-12-069RA Programming Manual for further information.

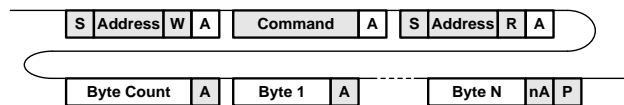


#### READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See TET3200-12-069RA Power Management Bus Communication Manual URP.00560 for further information.



### 8.16 GRAPHICAL USER INTERFACE

Bel Power Solutions provides I<sup>2</sup>C Utility™ a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the TET3200-12-069RA Front-End. The utility can be downloaded on [befuse.com/power-solutions](http://befuse.com/power-solutions) and supports both the PSM1 and Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring dialog, the power supply can be controlled and monitored.

If the GUI is used in conjunction with the TET3200-12-069RA Evaluation Kit it is also possible to control the PSON\_L pin(s) of the power supply.

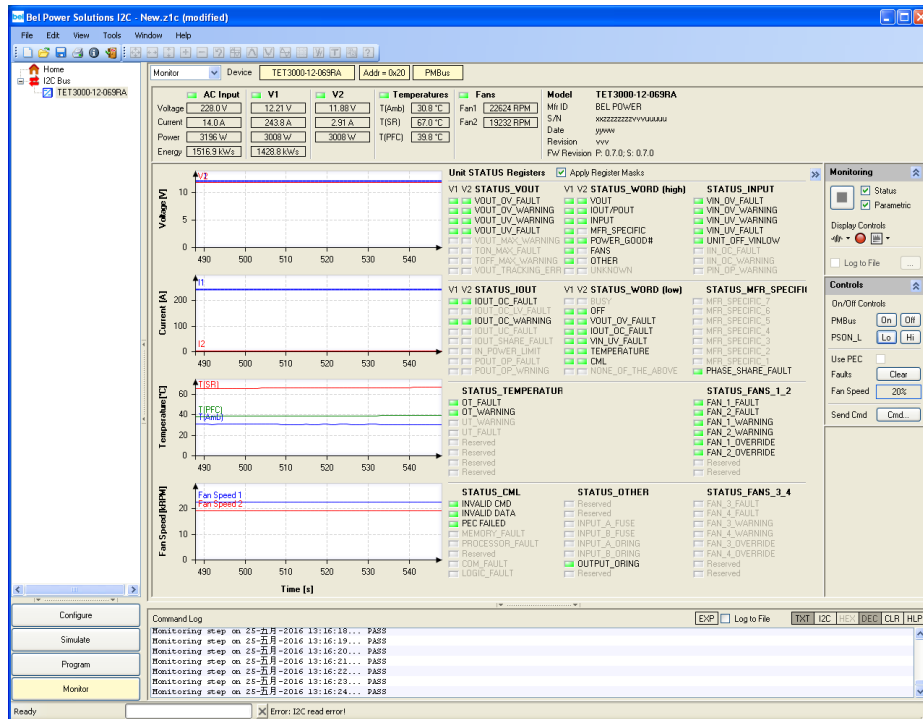


Figure 30. Monitoring dialog of the I<sup>2</sup>C Utility

### 9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The air enters through the front of the supply and leaves at the rear. The PSU has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

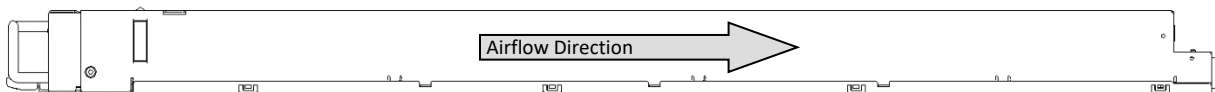


Figure 31. Airflow Direction of TET3200-12-069RA

Vin(Vac)	≤45C	≤50C	≤55C	≤60C
	Pout_Nom(W)	Pout_Nom(W)	Pout_Nom(W)	Pout_Nom(W)
90	1130	1060	990	920
100	1360	1280	1190	1110
110	1600	1500	1400	1300
120	1830	1720	1600	1490
130	2070	1940	1810	1680
140	2300	2160	2020	1870
150	2540	2380	2220	2060
160	2770	2600	2430	2250
170	3010	2820	2630	2450
180	3200	3000	2800	2600
190	3200	3000	2800	2600
200	3200	3000	2800	2600
210	3200	3000	2800	2600
220	3200	3000	2800	2600
230	3200	3000	2800	2600
240	3200	3000	2800	2600
250-300	3200	3000	2800	2600

Table 7. Main Output Nominal Output Power P1 nomII vs Inlet Temperature (degC) & Vin(Vac)

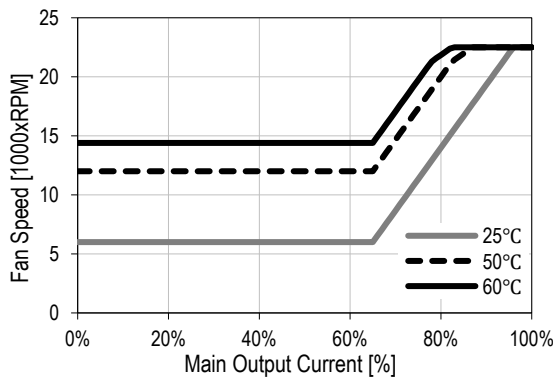


Figure 32. Fan Speed vs. Main Output Load

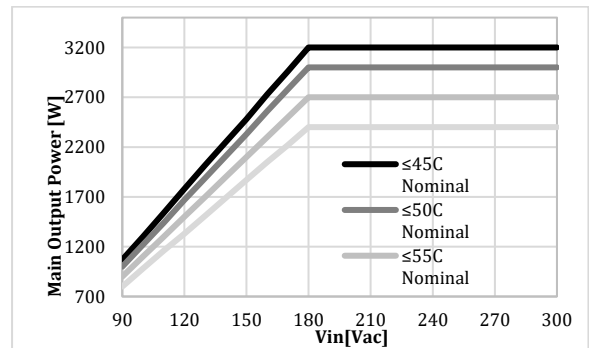


Figure 33. Thermal Derating

## 10. ELECTROMAGNETIC COMPATIBILITY

### 10.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filled	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz...2 GHz	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 ... 80 MHz	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1) Vi 230Volts, 80% Load, Dip 100%, Duration 12ms 2) Vi 230Volts, 100% Load, Dip 100%, Duration < 50 ms 3) Vi 230Volts, 100% Load, Dip 100%, Duration > 50 ms	A V1: B; VSB: A B



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## 10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55022 / CISPR 22: 0.15 ... 30 MHz, QP and AVG	Class A
Radiated Emission	EN55022 / CISPR 22: 30 MHz ... 1 GHz, QP	Class A
Harmonic Emissions	IEC61000-3-2, $V_{in} = 230$ VAC, 50 Hz, 100% Load	Class A
AC Flicker	IEC / EN 61000-3-3, $d_{max} < 3.3\%$	Pass
Acoustical Noise	Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load	60 dBA

## 11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950-1, IEC/EN 62368-1 & UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Agency Approvals	UL 62368-1, 3 <sup>rd</sup> Ed, CAN/CSA-C22.2 No. 62368-1:19 IEC 60950-1:2005, AMD1:2009, AND2:2013 IEC 62368-1:2018 EN 60950-1:2006, A11:2009, A1:2010, A12:2011, A2: 2013 EN 62368-1:2014, A11:2017		Approved		
Isolation Strength	Input (L/N) to case (PE) Input (L/N) to output Output to case (PE)		Basic Reinforced Functional		
Creepage / Clearance	Primary (L/N) to protective earth (PE) Primary to secondary	3.8/2.3 7.6/4.6			mm
Electrical Strength Test	Input to enclosure Input to output Output and Signals to case	2.5 5.0 0.1			kVDC

## 12. ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$T_A$ Ambient Temperature	$V_{min}$ to $V_{max}$ , $I_{nom}$ , $I_{SB nom}$ at 5000m $V_{min}$ to $V_{max}$ , $I_{nom}$ , $I_{SB nom}$ at 2000m	0 0		+40 +45	°C
$T_{Aext}$ Extended Temp. Range	Derated output (see <i>Figure 20</i> and <i>Figure 33</i> ) at 2000 m	+45		+60	°C
$T_S$ Storage Temperature	Non-operational	-40		+70	°C
Altitude	Operational, above Sea Level (see derating)	-		5000	m
$M_A$ Audible Noise	$V_{nom}$ , 60% $I_{nom}$ , $T_A = 25^\circ\text{C}$		53		dBA
Cooling	System Back Pressure			0.5	in-H <sub>2</sub> O

13. MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		69		mm
	Height		40.5		mm
	Depth		555		mm
M	Weight		2.4		kg

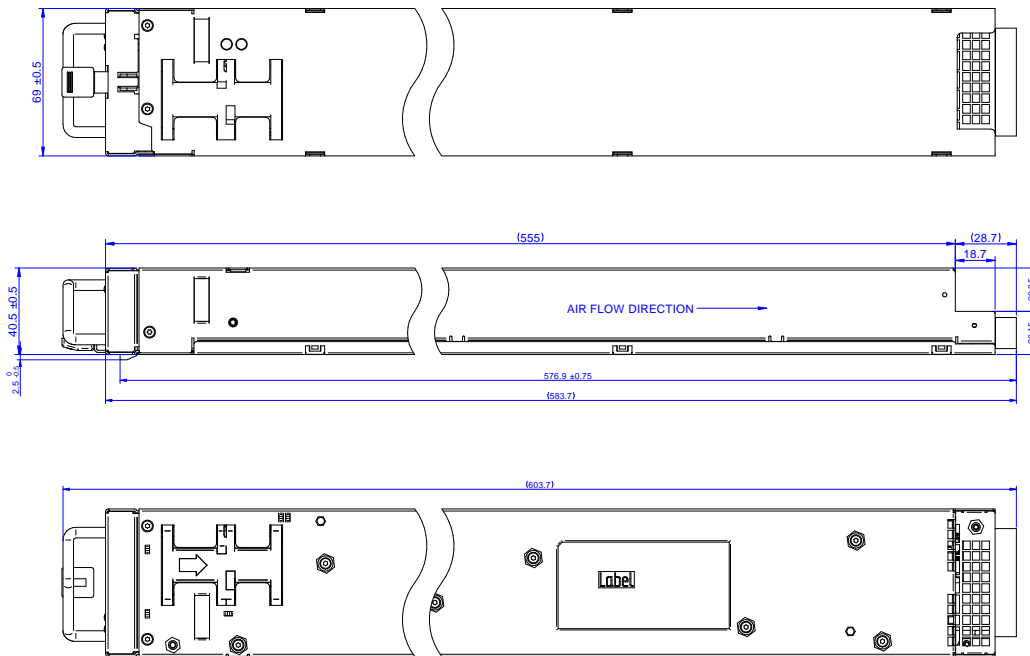


Figure 34. Bottom, top and side views

**NOTE:** A 3D step file of the power supply casing is available on request.

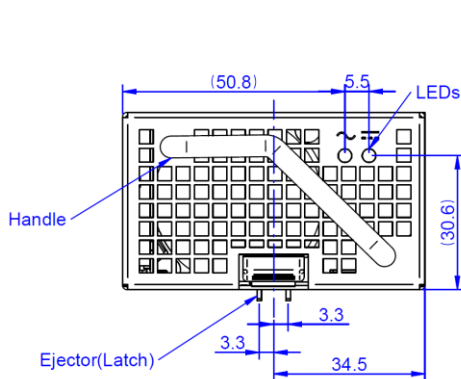


Figure 35. Front view

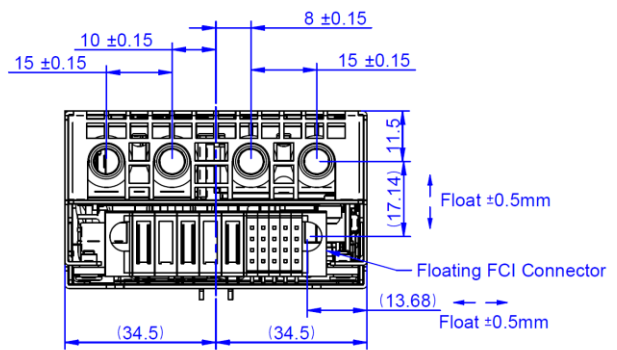
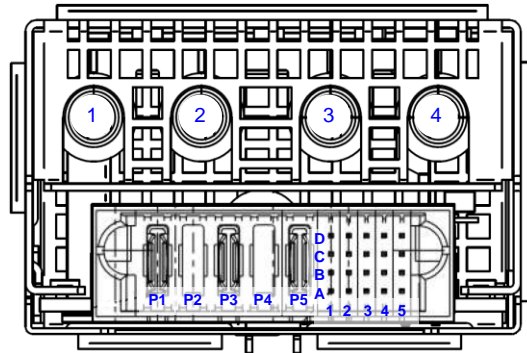


Figure 36. Rear view

## 14. CONNECTORS



Unit: FCI Connectors P/N 51939-768LF  
 Counterpart: FCI Connectors P/N 51915-401LF  
 For Main Output Pins, see section 15

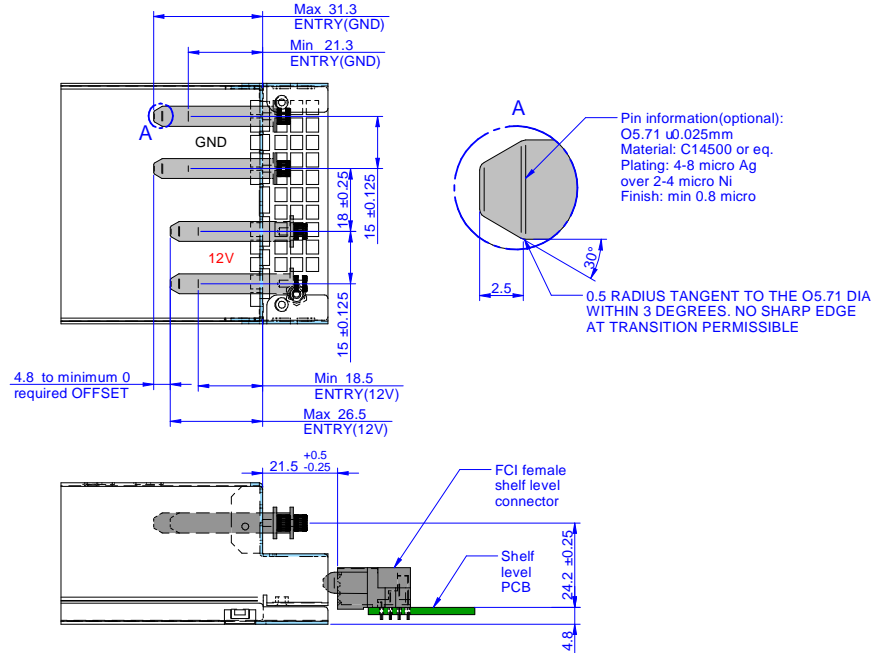
Note: A1 and A2 are Trailing Pin (short pins)

PIN	NAME	DESCRIPTION
<b>Output Pins</b>		
3,4	V1	+12 VDC main output
1,2	PGND	+12 VDC main output ground
<b>Input Pins</b>		
P1	LIVE	AC Live Pin
P2	N.C	No metal pin connection
P3	NEUTRAL	AC Neutral Pin
P4	N.C.	No metal pin connection
P5	P.E.	Protective Earth Pin
<b>Control Pins</b>		
A1	PSKILL	Power supply kill (trailing pin): active-high
B1	PWOK_L	Power OK signal output: active-low
C1	INOK_L	Input OK signal: active-low
D1	PSON_L	Power supply on input: active-low
A2	PRESENT_L	Power supply present (trailing pin): active-low
B2	SGND	Signal ground <sup>®)</sup> (return)
C2	SGND	Signal ground <sup>®)</sup> (return)
D2	SGND	Signal ground <sup>®)</sup> (return)
A3	SCL	I <sup>2</sup> C clock signal line
B3	SDA	I <sup>2</sup> C data signal line
C3	SMB_ALERT_L	SMB Alert signal output: active-low
D3	ISHARE	V <sub>1</sub> Current share bus
A4	EEPROM_WP	EEPROM write protect
B4	RESERVED	Reserved
C4	V1_SENSE_R	Main output negative sense
D4	V1_SENSE	Main output positive sense
A5	VSB	Standby positive output
B5	VSB	Standby positive output
C5	VSB_GND	Standby Ground <sup>®)</sup>
D5	VSB_GND	Standby Ground <sup>®)</sup>

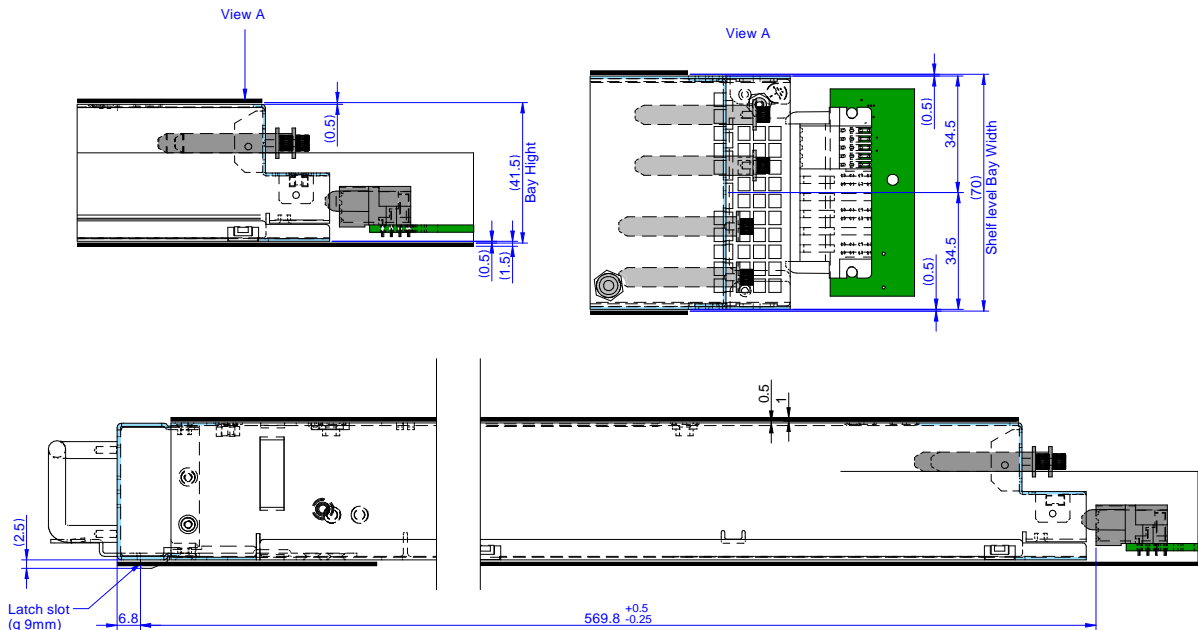
<sup>®)</sup> These pins should be connected to PGND on the system.  
 See section 8 for pull up resistor settings of signal pins  
 All signal pins are referred to SGND

**15. SHELF LEVEL CONFIGURATION (Provisional)**

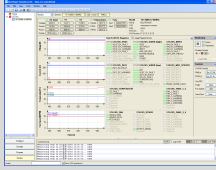


The recommended pin configuration below is based on company’s own Shelf design and provided here as reference. Customer pin lengths within the range indicated is acceptable.



The recommended system bay configuration below is based on company’s own Shelf design and provided here as a reference.



## 16. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	<b>I<sup>2</sup>C Utility</b> Windows XP/Vista/7 compatible GUI to program, control and monitor TET3200-12-069RA Front-Ends (and other I <sup>2</sup> C units)	N/A	<a href="http://befuse.com/power-solutions">befuse.com/power-solutions</a>
	<b>Single Connector Board</b> Connector board to operate TET3200-12-069RA unit. Includes an on-board USB to I <sup>2</sup> C converter (use <i>I<sup>2</sup>C Utility</i> as desktop software).	YTM.G1S01.0	<a href="http://befuse.com/power-solutions">befuse.com/power-solutions</a>
	<b>AC Can Filter</b> Recommended AC can filter used on system side.	C20F.0011  20GENG3E-R	Schurter Inc.  Delta Electronics

## 17. REVISION HISTORY

REVISION	DESCRIPTION OF CHANGES	DATE	ORIGINATOR
A	Initial release	2020-07-15	Jun.li

For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)

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