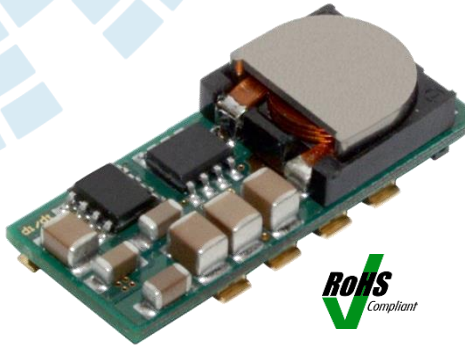


The YNS12S10 converter is not recommended for new designs and has been replaced by the YS12S10. Please refer to the YS12S10 data sheet for new product specifications.



Key Features & Benefits

- RoHS lead free and lead-solder-exempt products
- are available
- Delivers up to 10 A (55 W)
- Extended input range 9.6 to 14 VDC
- No derating up to 85 °C (70 °C for 5 VDC)
- Surface-mount package
- Industry-standard footprint and pinout
- Small size and low-profile: 1.30" x 0.53" x 0.314" (33.02 mm x 13.46 mm x 7.98 mm)
- Weight: 0.22 oz [6.12 g]
- Co-planarity < 0.003"
- Synchronous Buck Converter topology
- Start up into pre-biased output
- No minimum load required
- Programmable output voltage via external resistor
- Operating ambient temperature: -40 °C to 85 °C
- Remote output sense
- Remote ON/OFF (positive or negative)
- Fixed-frequency operation
- Auto-reset output overcurrent protection
- Auto-reset overtemperature protection
- High reliability, MTBF approx. 27.2 million hours calculated per Telcordia TR-332, Method I Case 1
- All materials meet UL94, V-0 flammability rating
- UL60950 recognition in U.S. & Canada, and DEMKO certification per IEC/EN60950

YNS12S10 DC-DC Converter

9.6 - 14 VDC Input; 0.7525 - 5.5 VDC
Programmable @ 10 A

Bel Power Solutions point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The Y-Series of non-isolated DC-DC converters deliver up to 10 A of output current in an industry-standard surface-mount package. Operating from a 9.6 to 14 VDC input, the YNS12S10 converters are ideal choices for Intermediate Bus Architectures where Point-of-Load power (POL) delivery is generally a requirement. They provide an extremely tight regulated, programmable output voltage of 0.7525 to 5.5 VDC.

The Y-Series of converters provide exceptional thermal performance, even in high temperature environments with minimal airflow. No derating is required up to 85 °C (up to 70 °C for 5 VDC output), even without airflow at natural convection. This performance is accomplished through the use of advanced circuitry, packaging, and processing techniques to achieve a design possessing ultra-high efficiency, excellent thermal management, and a very low-body profile.

The low-body profile and the preclusion of heat sinks minimize impedance to system airflow, thus enhancing cooling for both upstream and downstream devices. The use of 100% automation for assembly, coupled with advanced power electronics, and thermal design, results in a product with extremely high reliability.

Applications

- Intermediate Bus Architectures
- Telecommunications
- Data communications
- Distributed Power Architectures
- Servers, Workstations

Benefits

- High efficiency – no heat sink required
- Reduces Total Solution Board Area
- Tape and Reel Packing
- Compatible with Pick & Place Equipment
- Minimizes Part Numbers in Inventory

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YNS12S10 DC-DC Converter

Electrical Specifications

Conditions: $T_A = 25\text{ }^\circ\text{C}$, Airflow = 300 LFM (1.5 m/s), $V_{in} = 12\text{ VDC}$, $V_{out} = 0.7525 - 5.5\text{ VDC}$, unless otherwise specified.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Absolute Maximum Ratings					
Input Voltage	Continuous	-0.3		15	VDC
Operating Ambient Temperature		-40		85	$^\circ\text{C}$
Storage Temperature		-55		125	$^\circ\text{C}$
Feature Characteristics					
Switching Frequency			300		kHz
Output Voltage Trim Range ¹	By external resistor, See Trim Table 1	0.7525		5.5	VDC
Remote Sense Compensation ¹				0.5	VDC
Turn-On Delay Time	Full resistive load				
With V_{in} (Converter Enabled, then V_{in} applied)	From $V_{in} = V_{in}(\text{min})$ to $V_o = 0.1 * V_o(\text{nom})$		3		ms
With Enable ($V_{in} = V_{in}(\text{nom})$ applied, then enabled)	From enable to $V_o = 0.1 * V_o(\text{nom})$		3		ms
Rise time ² (Full resistive load)	From $0.1 * V_o(\text{nom})$ to $0.9 * V_o(\text{nom})$		4		ms
ON/OFF Control (Positive Logic) ³	Converter Off	-5		0.8	VDC
	Converter On	2.4		V_{in}	VDC
ON/OFF Control (Negative Logic) ³	Converter Off	2.4		V_{in}	VDC
	Converter On	-5		0.8	VDC
Input Characteristics					
Operating Input Voltage Range		9.6	12	14	VDC
Input Under Voltage Lockout					
Turn-on Threshold			9.0		VDC
Turn-off Threshold			8.5		VDC
Maximum Input Current	10 ADC Out @ 9.6 VDC In				
	$V_{OUT} = 5.0\text{ VDC}$			5.5	ADC
	$V_{OUT} = 3.3\text{ VDC}$			3.7	ADC
	$V_{OUT} = 2.5\text{ VDC}$			2.8	ADC
	$V_{OUT} = 2.0\text{ VDC}$			2.3	ADC
	$V_{OUT} = 1.8\text{ VDC}$			2.1	ADC
	$V_{OUT} = 1.5\text{ VDC}$			1.8	ADC
	$V_{OUT} = 1.2\text{ VDC}$			1.5	ADC
	$V_{OUT} = 1.0\text{ VDC}$			1.3	ADC
	$V_{OUT} = 0.7525\text{ VDC}$			1.1	ADC
Input Stand-by Current (Converter disabled)			5		mA
Input No Load Current (Converter enabled)	$V_{OUT} = 5.0\text{ VDC}$		76		mA
	$V_{OUT} = 3.3\text{ VDC}$		60		mA
	$V_{OUT} = 2.5\text{ VDC}$		45		mA
	$V_{OUT} = 2.0\text{ VDC}$		41		mA
	$V_{OUT} = 1.8\text{ VDC}$		38		mA
	$V_{OUT} = 1.5\text{ VDC}$		35		mA
	$V_{OUT} = 1.2\text{ VDC}$		33		mA
	$V_{OUT} = 1.0\text{ VDC}$		30		mA
	$V_{OUT} = 0.7525\text{ VDC}$		28		mA
Input Reflected-Ripple Current - i_s	See Fig. D for setup. (BW = 20 MHz)				
	$V_{OUT} = 5.0\text{ VDC}$		36		mA _{P-P}
	$V_{OUT} = 3.3\text{ VDC}$		34		mA _{P-P}
	$V_{OUT} = 2.5\text{ VDC}$		32		mA _{P-P}
	$V_{OUT} = 2.0\text{ VDC}$		31		mA _{P-P}
	$V_{OUT} = 1.8\text{ VDC}$		30		mA _{P-P}

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YNS12S10 DC-DC Converter

	$V_{OUT} = 1.5$ VDC	29	mA_{P-P}
	$V_{OUT} = 1.2$ VDC	26	mA_{P-P}
	$V_{OUT} = 1.0$ VDC	23	mA_{P-P}
	$V_{OUT} = 0.7525$ VDC	20	mA_{P-P}
Input Voltage Ripple Rejection	120 Hz	72	dB
Output Characteristics			
Output Voltage Set Point (no load)		-1.5	V_{out} +1.5 % V_{out}
Output Regulation ⁴			
Over Line	Full resistive load	1	2 mV
Over Load	From no load to full load	5	12 mV
Output Voltage Range (Overall operating input voltage, resistive load and temperature conditions until end of life)		-2.5	+2.5 % V_{out}
Output Ripple and Noise – 20 MHz bandwidth	Over line, load and temperature (Fig. D)		
Peak-to-Peak	$V_{OUT} = 1.0$ VDC	10	20 mV_{P-P}
Peak-to-Peak	$V_{OUT} = 5.0$ VDC	25	40 mV_{P-P}
External Load Capacitance	Plus full load (resistive)		
Min ESR > 1m Ω			1,000 μF
Min ESR > 10 m Ω			5,000 μF
Output Current Range		0	10 ADC
Output Current Limit Inception (I_{OUT})			15 ADC
Output Short-Circuit Current	Short = 10 m Ω , continuous		3 Arms
Dynamic Response			
I_{out} step from 5 A to 10 A with $di/dt = 5$ A/ μs	$C_o = 10$ μF ceramic. + 1 μF ceramic	150/(180 ⁵)	mV
Settling Time ($V_{OUT} < 10\%$ peak deviation)		30	μs
I_{out} step from 10 A to 5 A with $di/dt = -5$ A/ μs	$C_o = 10$ μF ceramic + 1 μF ceramic	150/(180 ⁵)	mV
Settling Time ($V_{OUT} < 10\%$ peak deviation)		30	μs
I_{out} step from 5 A to 10 with $di/dt = 5$ A/ μs	$C_o = 330$ μF polymer capacitors	100/(120 ⁵)	mV
Settling Time ($V_{OUT} < 10\%$ peak deviation)		55	μs
I_{out} step from 10 A to 5 A with $di/dt = -5$ A/ μs	$C_o = 330$ μF polymer capacitors	100/(120 ⁵)	mV
Settling Time ($V_{OUT} < 10\%$ peak deviation)		55	μs
Efficiency			
	Full load (10 A)		
	$V_{OUT} = 5.0$ VDC	95.0	%
	$V_{OUT} = 3.3$ VDC	94.0	%
	$V_{OUT} = 2.5$ VDC	93.0	%
	$V_{OUT} = 2.0$ VDC	91.5	%
	$V_{OUT} = 1.8$ VDC	90.5	%
	$V_{OUT} = 1.5$ VDC	89.5	%
	$V_{OUT} = 1.2$ VDC	87.5	%
	$V_{OUT} = 1.0$ VDC	86.0	%
	$V_{OUT} = 0.7525$ VDC	84.0	%

Notes:

- The output voltage should not exceed 5.5 VDC.
- Note that the startup time is the sum of turn-on delay time and rise time.
- The converter is ON if the ON/OFF pin is left open.
- Trim resistor connected across the GND and TRIM pins of the converter.
- For $V_{OUT} = 5.0$ VDC only. See the waveforms section for dynamic response and settling time for different output voltages.

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YNS12S10 DC-DC Converter

Operations

Input and Output Impedance

Y-Series converter should be connected via a low impedance to the DC power source. In many applications, the inductance associated with the distribution from the power source to the input of the converter can affect the stability of the converter. It is recommended to use decoupling capacitors (minimum 47 μF) placed as close as possible to the converter's input pins in order to ensure stability of the converter and reduce input ripple voltage. Internally, the converter has 20 μF (low ESR ceramics) of input capacitance.

In a typical application, low - ESR tantalum or POS capacitors will be sufficient to provide adequate ripple voltage filtering at the input of the converter. However, very low ESR ceramic capacitors 47 to 100 μF are recommended at the input of the converter in order to minimize the input ripple voltage. They should be placed as close as possible to the input pins of the converter.

The YNS12S10 has been designed for stable operation with or without external capacitance. Low ESR ceramic capacitors placed as close as possible to the load (minimum 47 μF) are recommended for better transient performance and lower output voltage ripple.

It is important to keep low resistance and low inductance PCB traces for connecting your load to the output pins of the converter. This is required to maintain good load regulation since the converter does not have a SENSE pin for compensating voltage drops associated with the power distribution system on your PCB.

ON/OFF (Pin 1)

The ON/OFF pin (Pin 1) is used to turn the power converter on or off remotely via a system signal. There are two remote control options available, positive logic (standard option) and negative logic, with both are referenced to GND (Pin 5). The typical connections are shown in Fig. A.

The positive logic version turns the converter on when the ON/OFF pin is at a logic high or left open, and turns the converter off when at a logic low or shorted to GND.

The negative logic version turns the converter on when the ON/OFF pin is at a logic low or left open, and turns the converter off when the ON/OFF pin is at a logic high or connected to V_{in} .

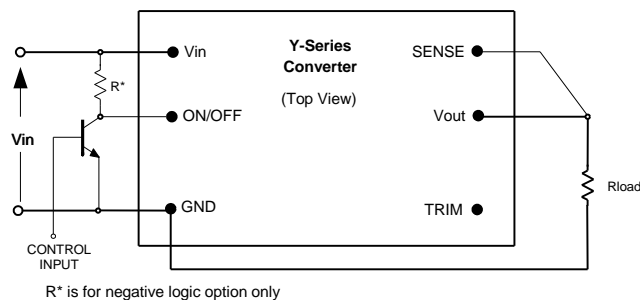


Fig. A: Circuit configuration for ON/OFF function.

The ON/OFF pin is internally pulled up to V_{in} for a positive logic version, and pulled down for a negative logic version. A TTL or CMOS logic gate, open-collector (open-drain) transistor can be used to drive the ON/OFF pin. When using open-collector (open-drain) transistor with a negative logic option, add a pull-up resistor (R^*) of 75 k Ω to V_{in} as shown in Fig. A. This device must be capable of:

- sinking up to 0.2 mA at a low level voltage of ≤ 0.8 V
- sourcing up to 0.25 mA at a high logic level of 2.3 to 5 V
- sourcing up to 0.75 mA when connected to V_{in}

Remote Sense (Pin 2)

The remote sense feature of the converter compensates for voltage drops occurring only between V_{out} pin (Pin 4) of the converter and the load. The SENSE (Pin 2) pin should be connected at the load or at the point where regulation is required (see Fig. B). There is no sense feature on the output GND return pin, where the solid ground plane should provide low voltage drop.

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YNS12S10 DC-DC Converter

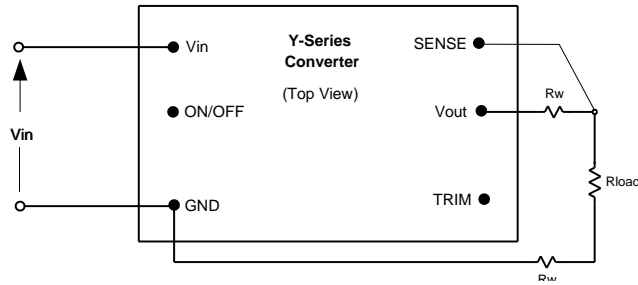


Fig. B: Circuit configuration for ON/OFF function.

If remote sensing is not required, the SENSE pin must be connected to the Vout pin (Pin 4) to ensure the converter will regulate at the specified output voltage. If these connections are not made, the converter will deliver an output voltage that is slightly higher than the specified value.

Because the sense lead carries minimal current, large traces on the end-user board are not required. However, sense trace should be located close to a ground plane to minimize system noise and ensure the optimum performance.

When utilizing the remote sense feature, care must be taken not to exceed the maximum allowable output power capability of the converter which is equal to the product of the nominal output voltage and the allowable output current for the given conditions.

When using remote sense, the output voltage at the converter can be increased up to 0.5 V above the nominal rating in order to maintain the required voltage across the load. Therefore, the designer must, if necessary, decrease the maximum current (originally obtained from the derating curves) by the same percentage to ensure the converter's actual output power remains at or below the maximum allowable output power.

Output Voltage Programming (Pin 3)

The output voltage can be programmed from 0.7525 to 5.5 V by connecting an external resistor between TRIM pin (Pin 3) and GND pin (Pin 5); see Fig. C. Note that when trim resistor is not connected, output voltage of the converter is 0.7525 V.

A trim resistor, R_{TRIM} , for a desired output voltage can be calculated using the following equation:

$$R_{TRIM} = \frac{10.5}{(V_{O-REQ} - 0.7525)} - 1 \quad [k\Omega]$$

where,

R_{TRIM} = Required value of trim resistor [k Ω]

V_{O-REQ} = Desired (trimmed) output voltage [V]

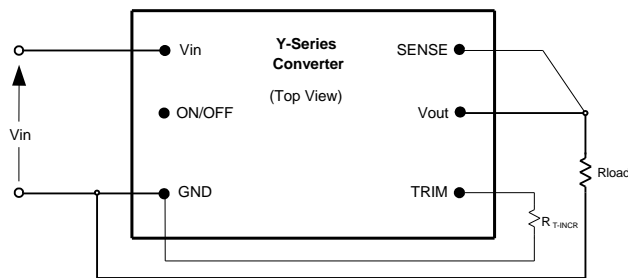


Fig. C: Configuration for programming output voltage.

Note that the tolerance of a trim resistor directly affects the output voltage tolerance. It is recommended to use standard 1% or 0.5% resistors; for tighter tolerance, two resistors in parallel are recommended rather than one standard value from Table 1.

The ground pin of the trim resistor should be connected directly to the converter GND pin (Pin 5) with no voltage drop in between. Table 1 provides the trim resistor values for popular output voltages.

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YNS12S10 DC-DC Converter

Table 1: Trim Resistor Value

V _{O-REG} [V]	R _{TRIM} [kΩ]	The Closest Standard Value [kΩ]
0.7525	open	
1.0	41.42	41.2
1.2	22.46	22.6
1.5	13.05	13.0
1.8	9.02	9.09
2.0	7.42	7.50
2.5	5.01	4.99
3.3	3.12	3.09
5.0	1.47	1.47
5.5	1.21	1.21

The output voltage can also be programmed by external voltage source. To make trimming less sensitive, a series external resistor R_{EXT} is recommended between TRIM pin and programming voltage source. Control Voltage can be calculated by the formula:

$$V_{CTRL} = 0.7 - \frac{(1 + R_{EXT})(V_{O-REQ} - 0.7525)}{15} \quad [V]$$

where

V_{CTRL} = Control voltage [V]

R_{EXT} = External resistor between TRIM pin and voltage source; the kΩ value can be chosen depending on the required output voltage range.

Control voltages with R_{EXT} = 0 and R_{EXT} = 15 kΩ are shown in Table 2.

Table 2: Control Voltage [VDC]

V _{O-REG} [V]	V _{CTRL} (R _{EXT} = 0)	V _{CTRL} (R _{EXT} = 15 kΩ)
0.7525	0.700	0.700
1.0	0.684	0.436
1.2	0.670	0.223
1.5	0.650	-0.097
1.8	0.630	-0.417
2.0	0.617	-0.631
2.5	0.584	-1.164
3.3	0.530	-2.017
5.0	0.417	-3.831
5.5	0.384	-4.364

Protection Features

Input Undervoltage Lockout

Input undervoltage lockout is standard with this converter. The converter will shut down when the input voltage drops below a pre-determined voltage; it will start automatically when V_{in} returns to a specified range.

The input voltage must be typically 9.0 V for the converter to turn on. Once the converter has been turned on, it will shut off when the input voltage drops below typically 8.5 V.

Output Overcurrent Protection (OCP)

The converter is protected against overcurrent and short circuit conditions. Upon sensing an overcurrent condition, the converter will enter hiccup mode. Once overload or short circuit condition is removed, V_{out} will return to nominal value.

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YNS12S10 DC-DC Converter

Overtemperature Protection (OTP)

The converter will shut down under an overtemperature condition to protect itself from overheating caused by operation outside the thermal derating curves, or operation in abnormal conditions such as system fan failure. After the converter has cooled to a safe operating temperature, it will automatically restart.

Safety Requirements

The converter meets North American and International safety regulatory requirements per UL60950 and EN60950. The maximum DC voltage between any two pins is V_{in} under all operating conditions. Therefore, the unit has ELV (extra low voltage) output; it meets SELV requirements under the condition that all input voltages are ELV. The converter is not internally fused. To comply with safety agencies' requirements, a recognized fuse with a maximum rating of 15 Amps must be used in series with the input line.

Characterization

General Information

The converter has been characterized for many operational aspects, to include thermal derating (maximum load current as a function of ambient temperature and airflow) for vertical and horizontal mountings, efficiency, startup and shutdown parameters, output ripple and noise, transient response to load step-change, overload, and short circuit. The figures are numbered as Fig. x.y, where x indicates the different output voltages, and y associates with specific plots ($y = 1$ for the vertical thermal derating, ...). For example, Fig. x.1 will refer to the vertical thermal derating for all the output voltages in general. The following pages contain specific plots or waveforms associated with the converter. Additional comments for specific data are provided below.

Test Conditions

All data presented were taken with the converter soldered to a test board, specifically a 0.060" thick printed wiring board (PWB) with four layers. The top and bottom layers were not metalized. The two inner layers, comprised of two-ounce copper, were used to provide traces for connectivity to the converter.

The lack of metalization on the outer layers as well as the limited thermal connection ensured that heat transfer from the converter to the PWB was minimized. This provides a worst-case but consistent scenario for thermal derating purposes.

All measurements requiring airflow were made in the vertical and horizontal wind tunnels using Infrared (IR) thermography and thermocouples for thermometry.

Ensuring components on the converter do not exceed their ratings is important to maintaining high reliability. If one anticipates operating the converter at or close to the maximum loads specified in the derating curves, it is prudent to check actual operating temperatures in the application. Thermographic imaging is preferable; if this capability is not available, then thermocouples may be used. The use of AWG #40 gauge thermocouples is recommended to ensure measurement accuracy. Careful routing of the thermocouple leads will further minimize measurement error. Refer to Fig. D for the optimum measuring thermocouple location.

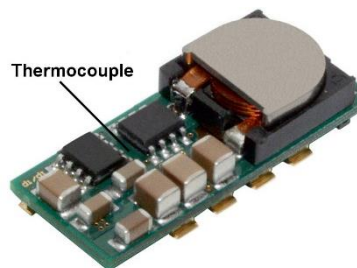


Fig. D: Location of the thermocouple for thermal testing.

YNS12S10 DC-DC Converter

Thermal Derating

Load current vs. ambient temperature and airflow rates are given in Figs. x.1 to x.2 for maximum temperature of 110°C. Ambient temperature was varied between 25 °C and 85 °C, with airflow rates from 30 to 500 LFM (0.15 m/s to 2.5 m/s), and vertical and horizontal converter mountings. The airflow during the testing is parallel to the long axis of the converter, going from pin 1 and pin 6 to pins 2–5.

For each set of conditions, the maximum load current is defined as the lowest of:

- (i) The output current at which any MOSFET temperature does not exceed a maximum specified temperature (110 °C) as indicated by the thermographic image, or
- (ii) The maximum current rating of the converter (10 A)

During normal operation, derating curves with maximum FET temperature less than or equal to 110 °C should not be exceeded. Temperature on the PCB at the thermocouple location shown in Fig. D should not exceed 110 °C in order to operate inside the derating curves.

Efficiency

Figure x.3 shows the efficiency vs. load current plot for ambient temperature of 25 °C, airflow rate of 200 LFM (1 m/s) and input voltages of 9.6 V, 12 V, and 14 V.

Power Dissipation

Fig. x.4 shows the power dissipation vs. load current plot for $T_a = 25$ °C, airflow rate of 200 LFM (1 m/s) with vertical mounting and input voltages of 9.6 V, 12 V, and 14 V.

Ripple and Noise

The output voltage ripple waveform is measured at full rated load current. Note that all output voltage waveforms are measured across a 1 μ F ceramic capacitor.

The output voltage ripple and input reflected ripple current waveforms are obtained using the test setup shown in Figure E.

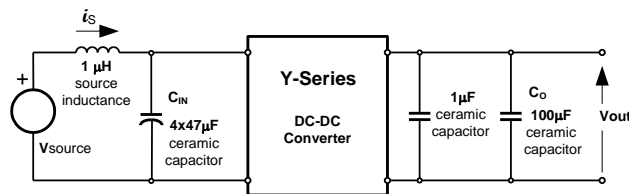


Fig. E: Test Setup for measuring input reflected-ripple currents, i_s and output voltage ripple.

YNS12S10 DC-DC Converter

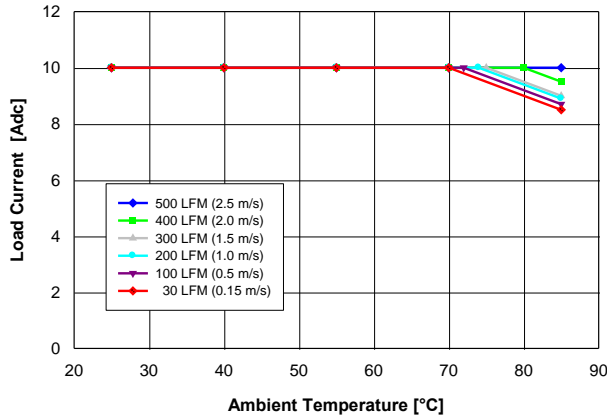


Fig. 5.0V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 5.0$ V converter mounted vertically with $V_{in} = 12$ V, and maximum MOSFET temperature ≤ 110 °C.

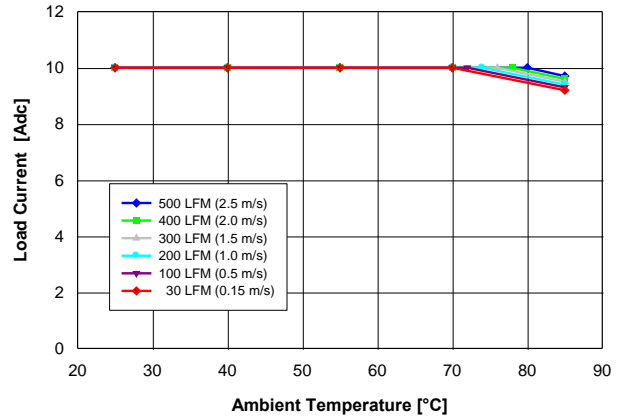


Fig. 5.0V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 5.0$ V converter mounted horizontally with $V_{in} = 12$ V, and maximum MOSFET temperature ≤ 110 °C.

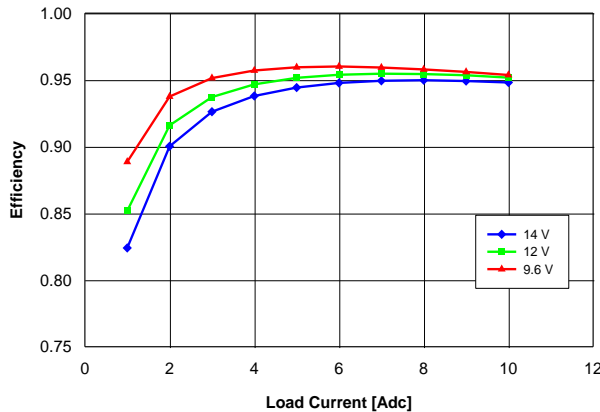


Fig. 5.0V.3: Efficiency vs. load current and input voltage for $V_{out} = 5.0$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

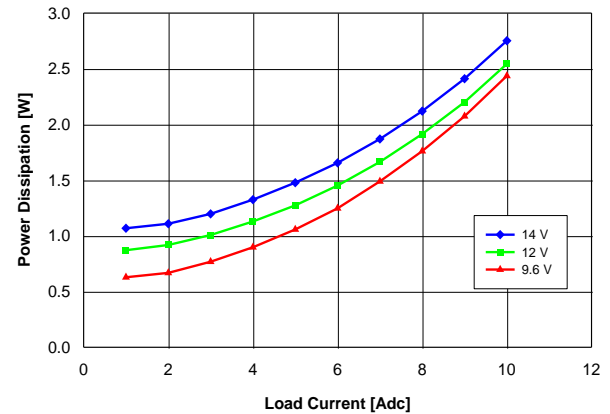


Fig. 5.0V.4: Power Loss vs. load current and input voltage for $V_{out} = 5.0$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

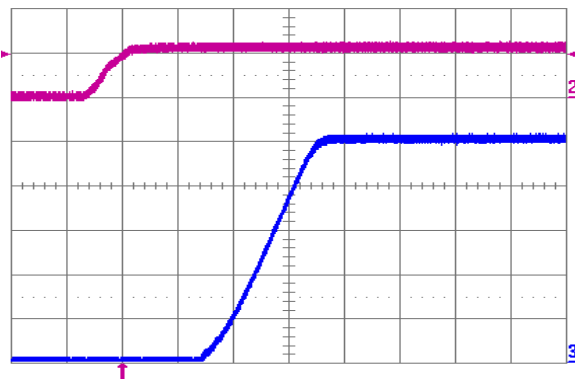


Fig. 5.0V.5: Turn-on transient for $V_{out} = 5.0$ V with application of V_{in} at full rated load current (resistive) and $100 \mu\text{F}$ external capacitance at $V_{in} = 12$ V. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

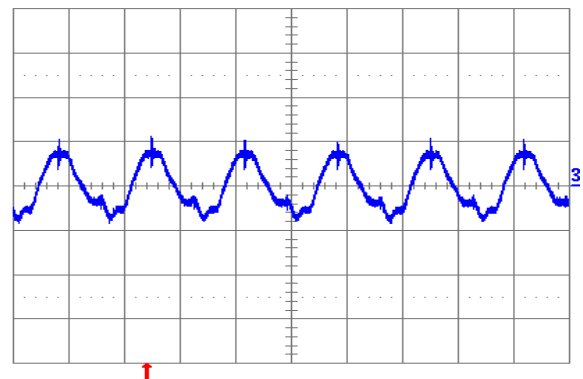


Fig. 5.0V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100 \mu\text{F}$ ceramic + $1 \mu\text{F}$ ceramic, and $V_{in} = 12$ V for $V_{out} = 5.0$ V. Time scale: 2 μs/div.

YNS12S10 DC-DC Converter

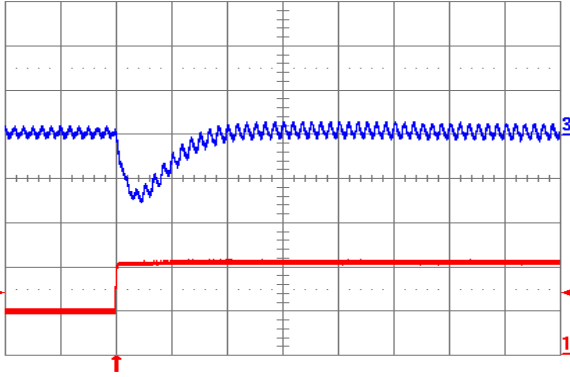


Fig. 5.0V.7: Output voltage response for $V_{out} = 5.0\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: $20\text{ }\mu\text{s}/\text{div}$.

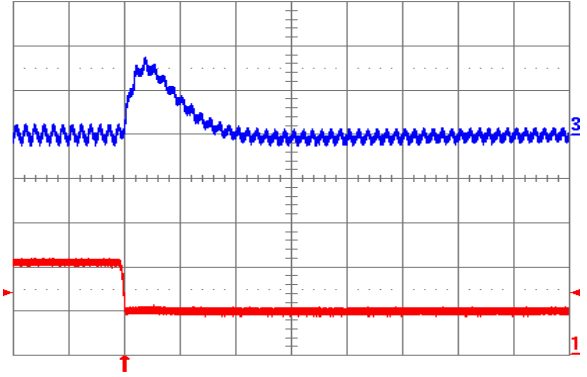


Fig. 5.0V.8: Output voltage response for $V_{out} = 5.0\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: $20\text{ }\mu\text{s}/\text{div}$.

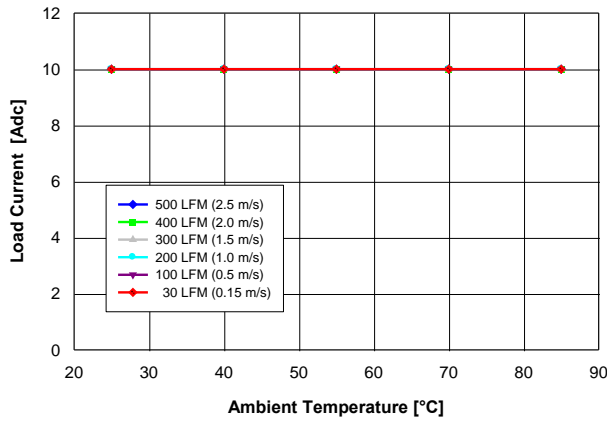


Fig. 3.3V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 3.3\text{ V}$ converter mounted vertically with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

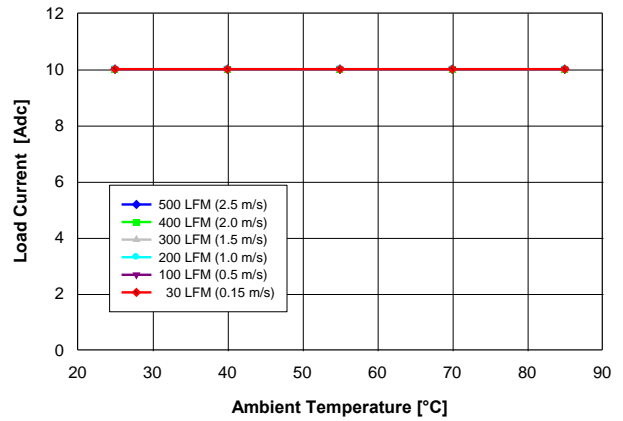


Fig. 3.3V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 3.3\text{ V}$ converter mounted horizontally with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

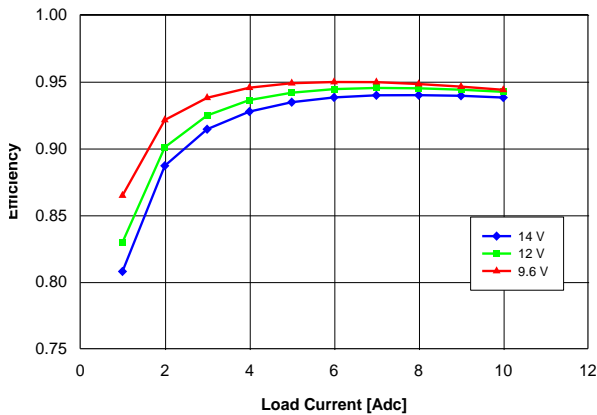


Fig. 3.3V.3: Efficiency vs. load current and input voltage for $V_{out} = 3.3\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

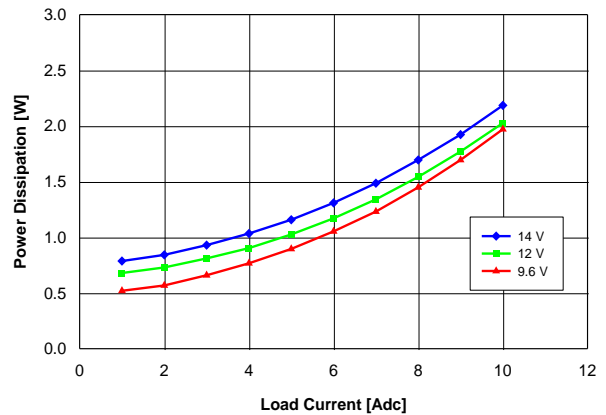


Fig. 3.3V.4: Power Loss vs. load current and input voltage for $V_{out} = 3.3\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

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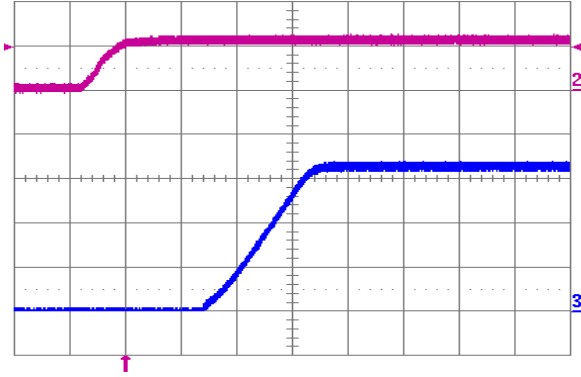


Fig. 3.3V.5: Turn-on transient for $V_{out} = 3.3\text{ V}$ with application of V_{in} at full rated load current (resistive) and $100\ \mu\text{F}$ external capacitance at $V_{in} = 12\text{ V}$. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

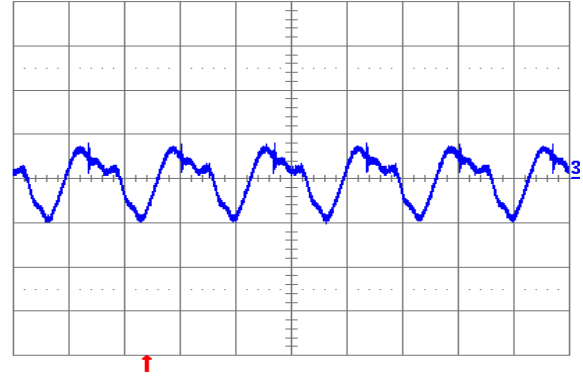


Fig. 3.3V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100\ \mu\text{F}$ ceramic + $1\ \mu\text{F}$ ceramic, and $V_{in} = 12\text{ V}$ for $V_{out} = 3.3\text{ V}$. Time scale: $2\ \mu\text{s/div.}$

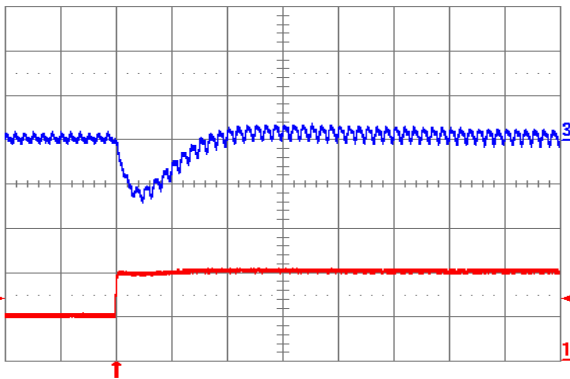


Fig. 3.3V.7: Output voltage response for $V_{out} = 3.3\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\ \mu\text{F}$ ceramic. Time scale: $20\ \mu\text{s/div.}$

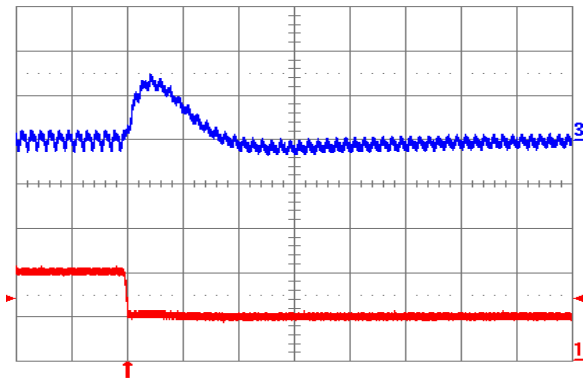


Fig. 3.3V.8: Output voltage response for $V_{out} = 3.3\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (2 A/div.). $C_o = 100\ \mu\text{F}$ ceramic. Time scale: $20\ \mu\text{s/div.}$

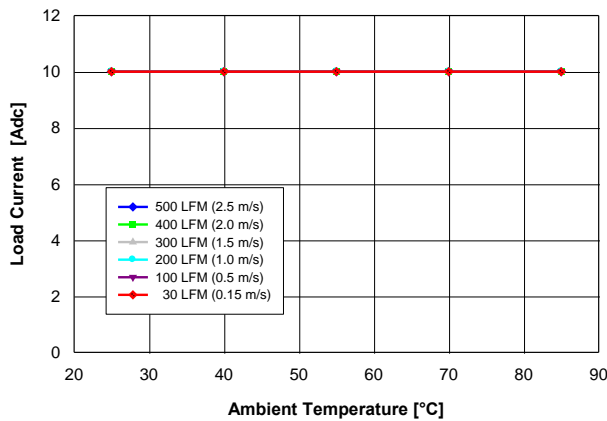


Fig. 2.5V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 2.5\text{ V}$ converter mounted vertically with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

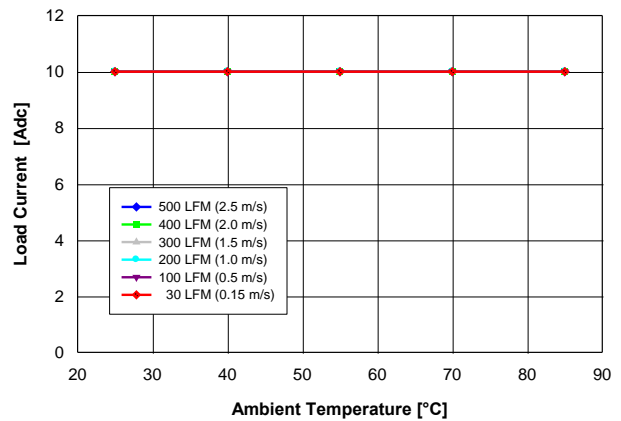


Fig. 2.5V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 2.5\text{ V}$ converter mounted horizontally with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

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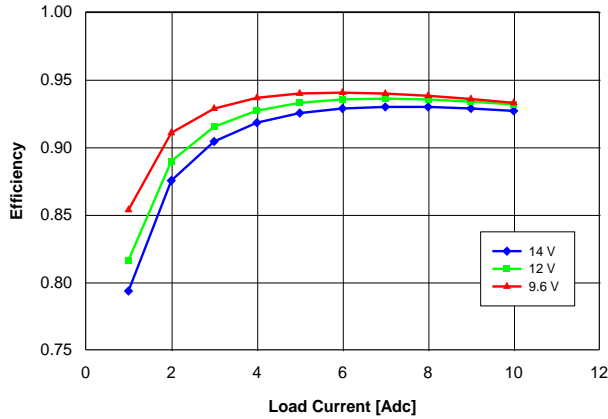


Fig. 2.5V.3: Efficiency vs. load current and input voltage for $V_{out} = 2.5\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

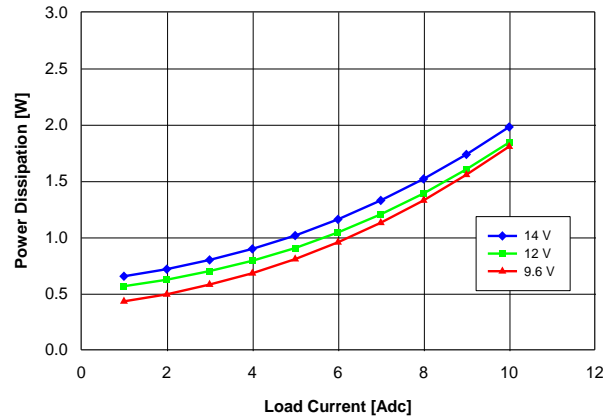


Fig. 2.5V.4: Power Loss vs. load current and input voltage for $V_{out} = 2.5\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

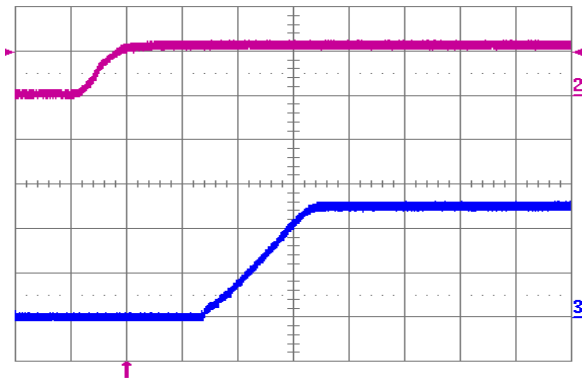


Fig. 2.5V.5: Turn-on transient for $V_{out} = 2.5\text{ V}$ with application of V_{in} at full rated load current (resistive) and $47\text{ }\mu\text{F}$ external capacitance at $V_{in} = 12\text{ V}$. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

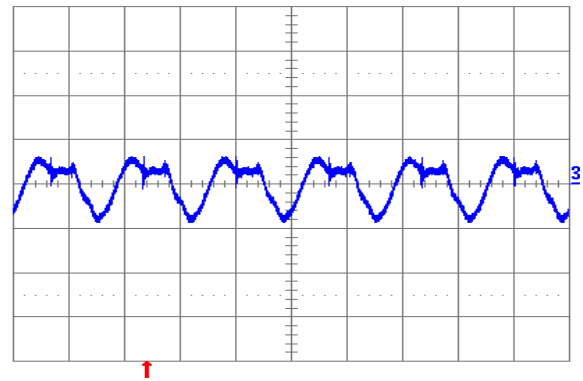


Fig. 2.5V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100\text{ }\mu\text{F}$ ceramic + $1\text{ }\mu\text{F}$ ceramic, and $V_{in} = 12\text{ V}$ for $V_{out} = 2.5\text{ V}$. Time scale: 2 μs /div.

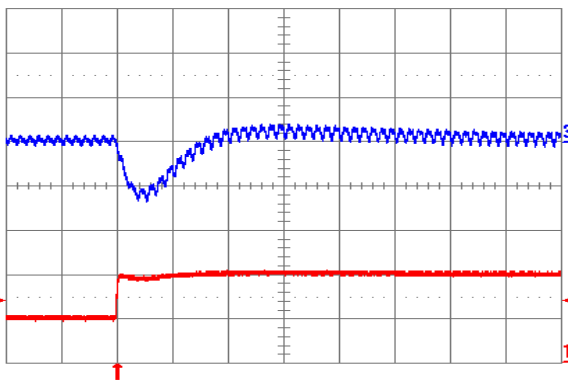


Fig. 2.5V.7: Output voltage response for $V_{out} = 2.5\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: 20 μs /div.

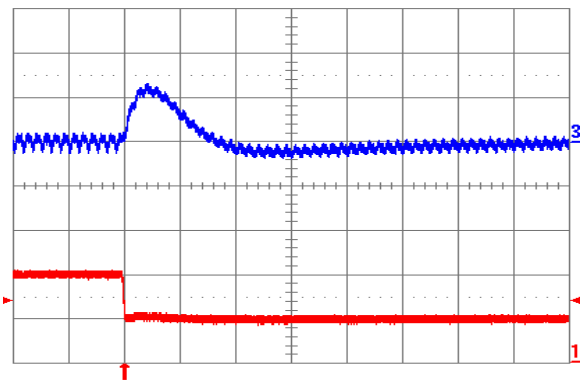


Fig. 2.5V.8: Output voltage response for $V_{out} = 2.5\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: 20 μs /div.

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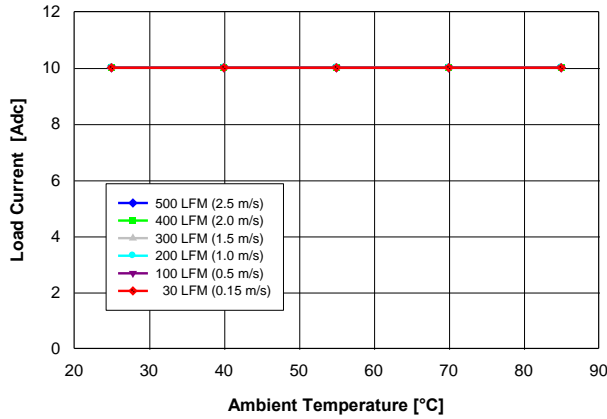


Fig. 2.0V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 2.0$ V converter mounted vertically with $V_{in} = 12$ V, and maximum MOSFET temperature ≤ 110 °C.

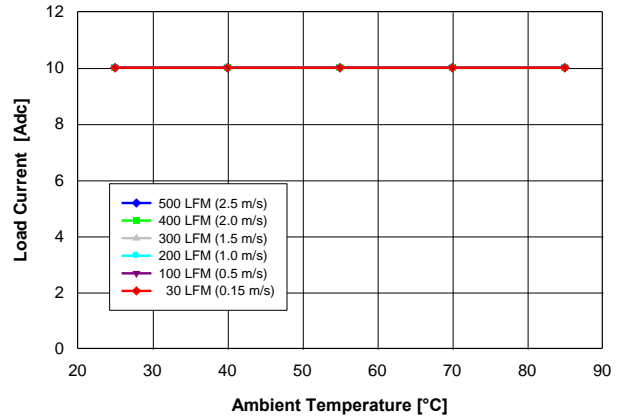


Fig. 2.0V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 2.0$ V converter mounted horizontally with $V_{in} = 12$ V, and maximum MOSFET temperature ≤ 110 °C.

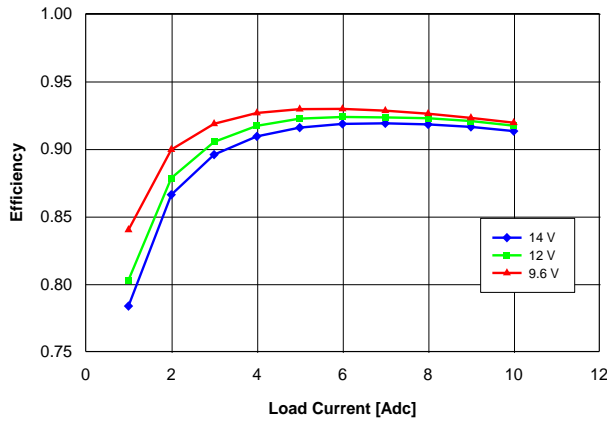


Fig. 2.0V.3: Efficiency vs. load current and input voltage for $V_{out} = 2.0$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

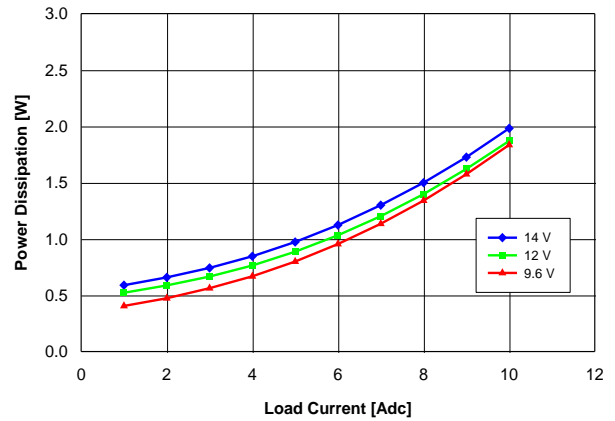


Fig. 2.0V.4: Power Loss vs. load current and input voltage for $V_{out} = 2.0$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

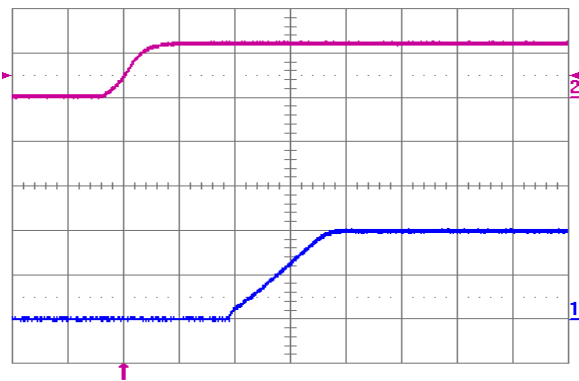


Fig. 2.0V.5: Turn-on transient for $V_{out} = 2.0$ V with application of V_{in} at full rated load current (resistive) and $100 \mu\text{F}$ external capacitance at $V_{in} = 12$ V. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

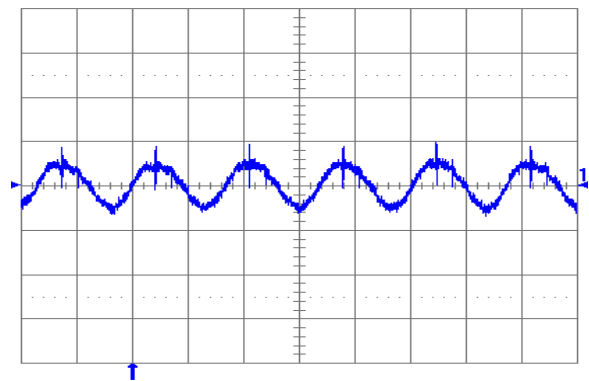


Fig. 2.0V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100 \mu\text{F}$ ceramic + $1 \mu\text{F}$ ceramic, and $V_{in} = 12$ V for $V_{out} = 2.0$ V. Time scale: 2 μs/div.

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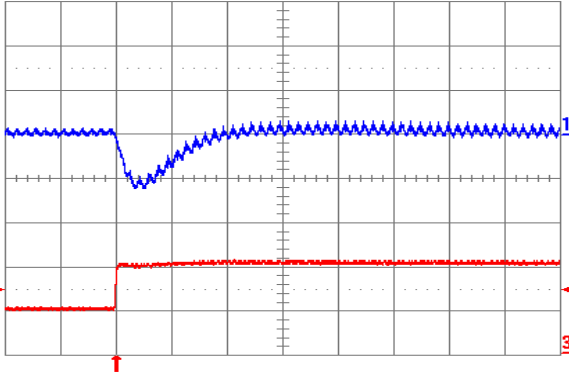


Fig. 2.0V.7: Output voltage response for $V_{out} = 2.0\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: $20\text{ }\mu\text{s}/\text{div}$.

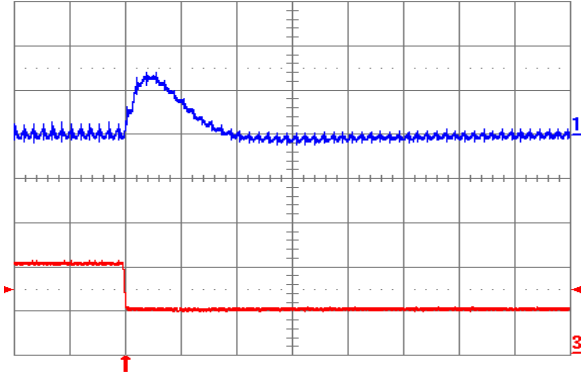


Fig. 2.0V.8: Output voltage response for $V_{out} = 2.0\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: $20\text{ }\mu\text{s}/\text{div}$.

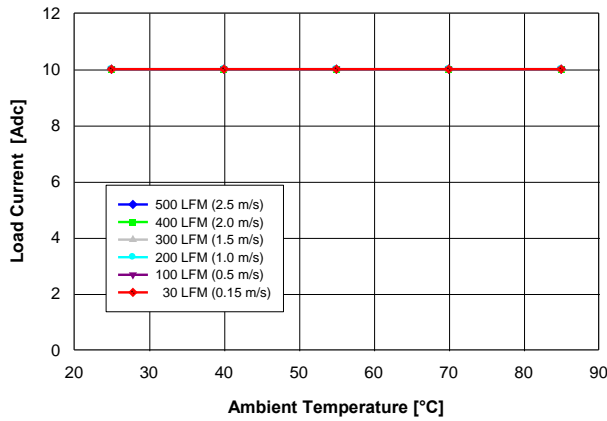


Fig. 1.8V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.8\text{ V}$ converter mounted vertically with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

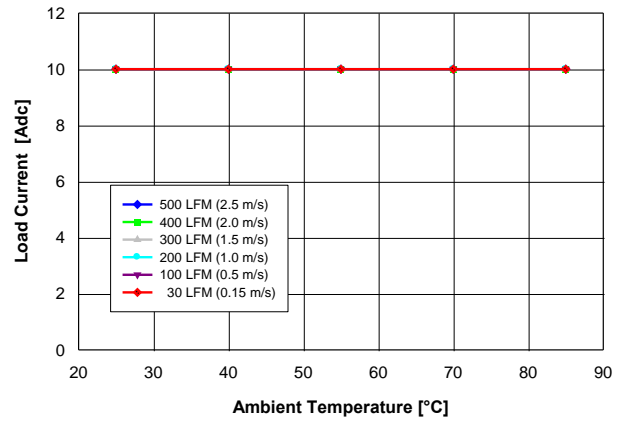


Fig. 1.8V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.8\text{ V}$ converter mounted horizontally with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

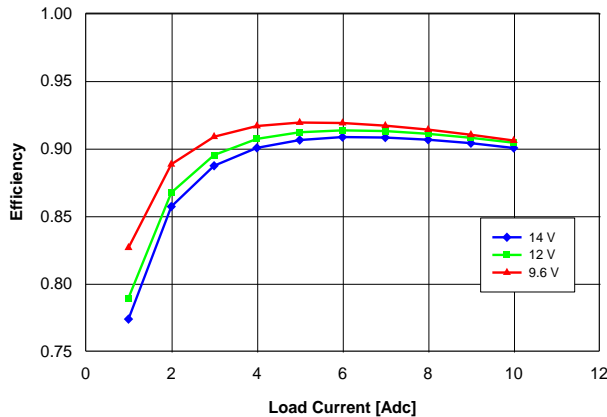


Fig. 1.8V.3: Efficiency vs. load current and input voltage for $V_{out} = 1.8\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

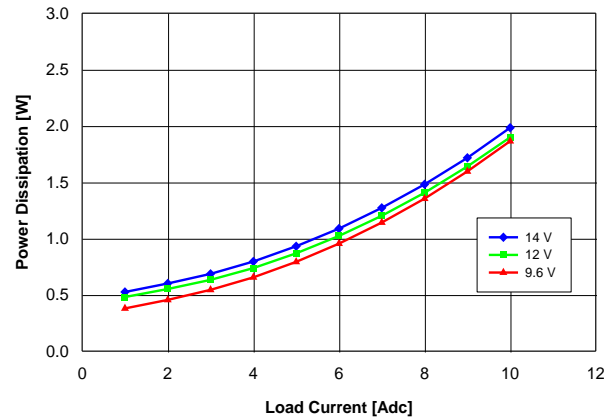


Fig. 1.8V.4: Power Loss vs. load current and input voltage for $V_{out} = 1.8\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

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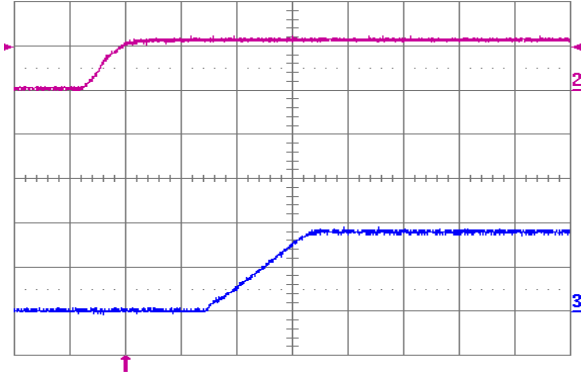


Fig. 1.8V.5: Turn-on transient for $V_{out} = 1.8\text{ V}$ with application of V_{in} at full rated load current (resistive) and $100\ \mu\text{F}$ external capacitance at $V_{in} = 12\text{ V}$. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

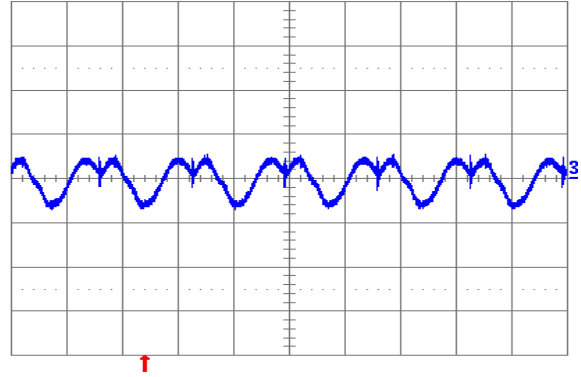


Fig. 1.8V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100\ \mu\text{F}$ ceramic + $1\ \mu\text{F}$ ceramic, and $V_{in} = 12\text{ V}$ for $V_{out} = 1.8\text{ V}$. Time scale: $2\ \mu\text{s/div.}$

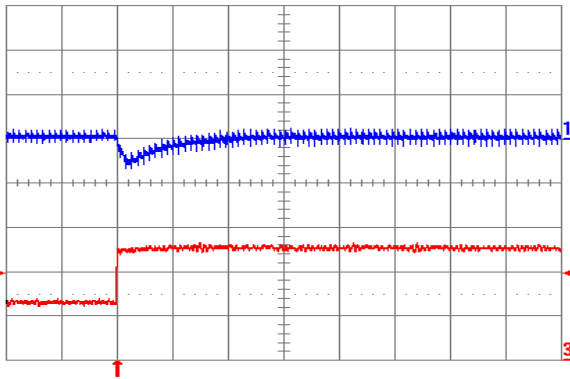


Fig. 1.8V.7: Output voltage response for $V_{out} = 1.8\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\ \mu\text{F}$ ceramic. Time scale: $20\ \mu\text{s/div.}$

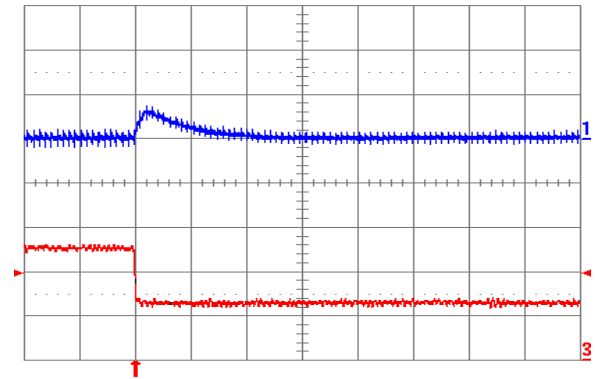


Fig. 1.8V.8: Output voltage response for $V_{out} = 1.8\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\ \mu\text{F}$ ceramic. Time scale: $20\ \mu\text{s/div.}$

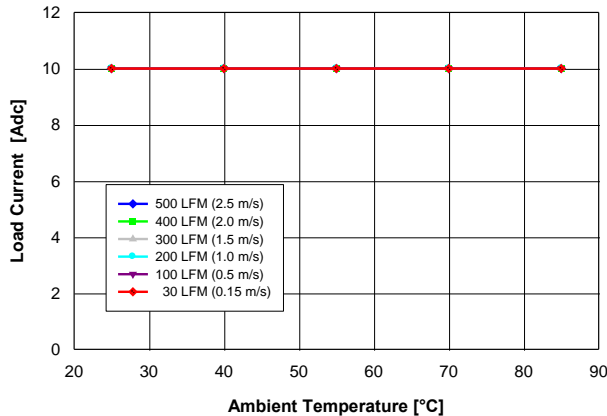


Fig. 1.5V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.5\text{ V}$ converter mounted vertically with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

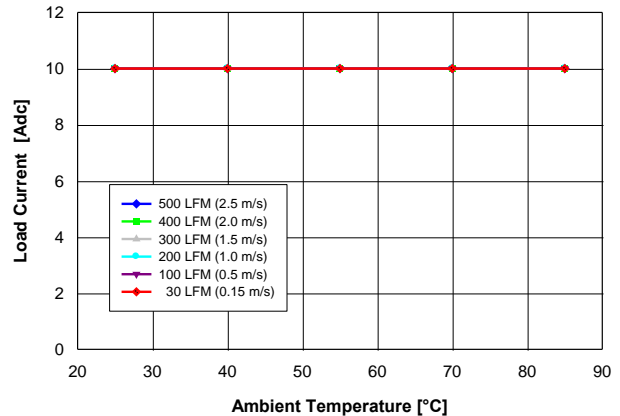


Fig. 1.5V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.5\text{ V}$ converter mounted horizontally with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

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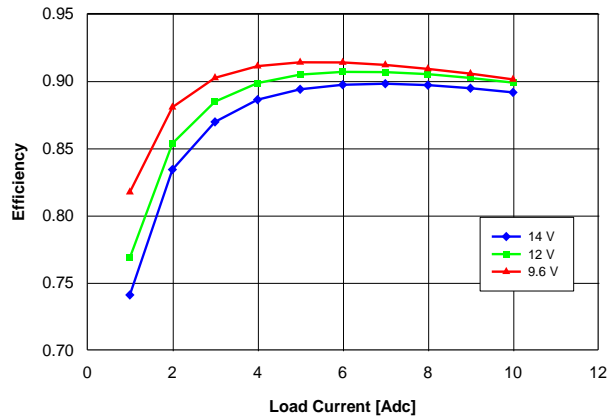


Fig. 1.5V.3: Efficiency vs. load current and input voltage for $V_{out} = 1.5\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

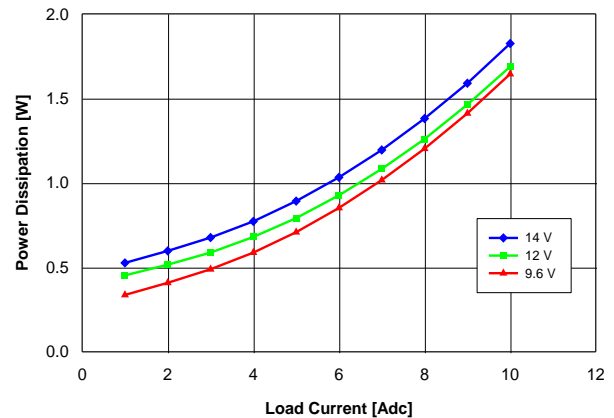


Fig. 1.5V.4: Power Loss vs. load current and input voltage for $V_{out} = 1.5\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

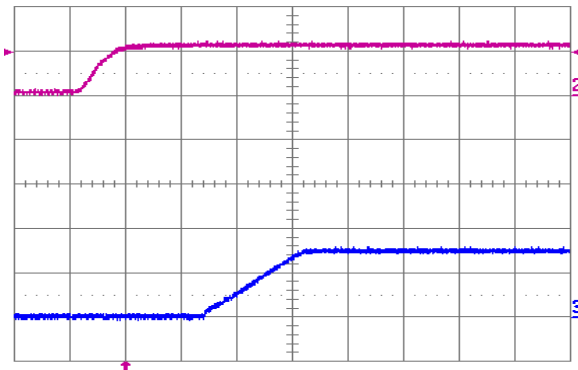


Fig. 1.5V.5: Turn-on transient for $V_{out} = 1.5\text{ V}$ with application of V_{in} at full rated load current (resistive) and $100\text{ }\mu\text{F}$ external capacitance at $V_{in} = 12\text{ V}$. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

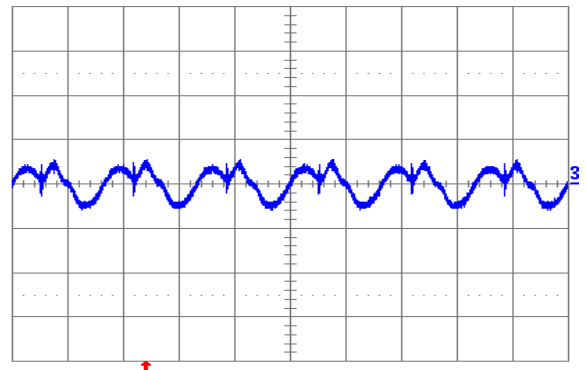


Fig. 1.5V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100\text{ }\mu\text{F}$ ceramic + $1\text{ }\mu\text{F}$ ceramic, and $V_{in} = 12\text{ V}$ for $V_{out} = 1.5\text{ V}$. Time scale: 2 μs /div.

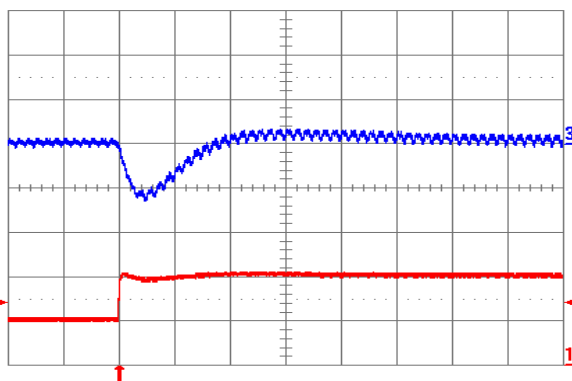


Fig. 1.5V.7: Output voltage response for $V_{out} = 1.5\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (2 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: 20 μs /div.

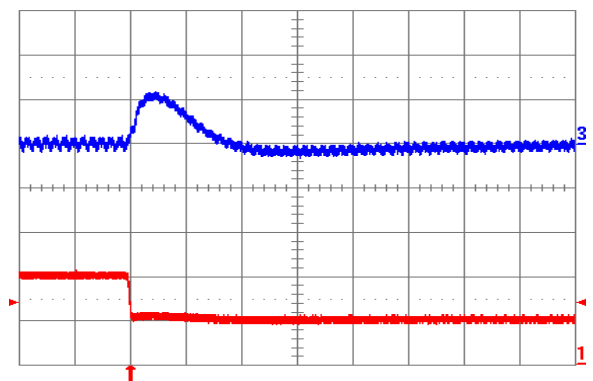


Fig. 1.5V.8: Output voltage response for $V_{out} = 1.5\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (2 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: 20 μs /div.

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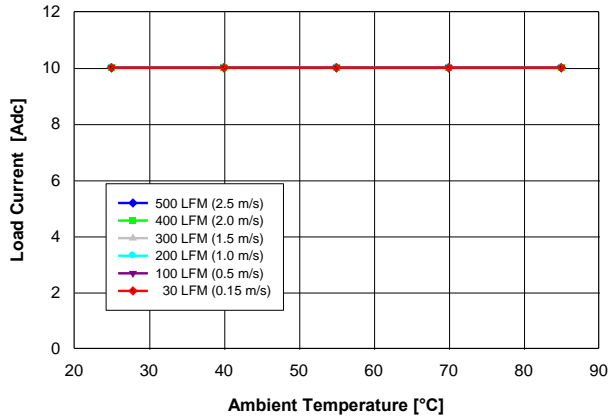


Fig. 1.2V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.2$ V converter mounted vertically with $V_{in} = 12$ V, and maximum MOSFET temperature ≤ 110 °C.

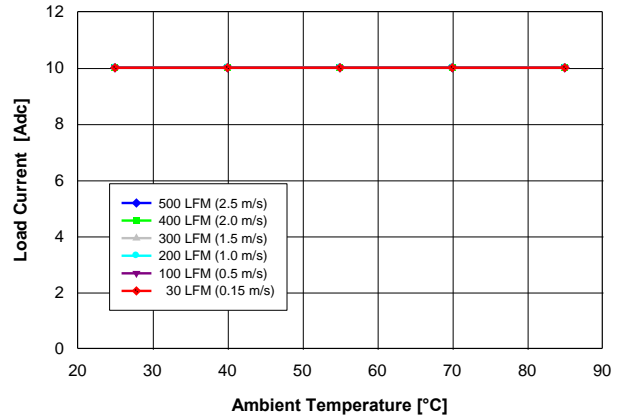


Fig. 1.2V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.2$ V converter mounted horizontally with $V_{in} = 12$ V, and maximum MOSFET temperature ≤ 110 °C.

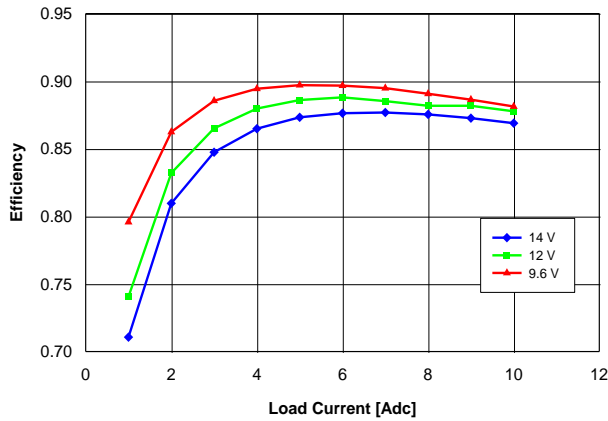


Fig. 1.2V.3: Efficiency vs. load current and input voltage for $V_{out} = 1.2$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

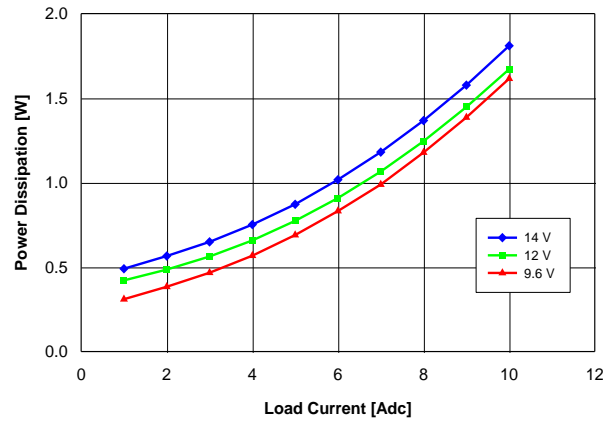


Fig. 1.2V.4: Power Loss vs. load current and input voltage for $V_{out} = 1.2$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

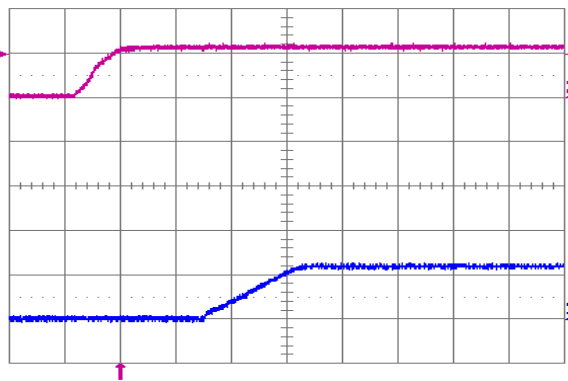


Fig. 1.2V.5: Turn-on transient for $V_{out} = 1.2$ V with application of V_{in} at full rated load current (resistive) and 100 μ F external capacitance at $V_{in} = 12$ V. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 5 ms/div.

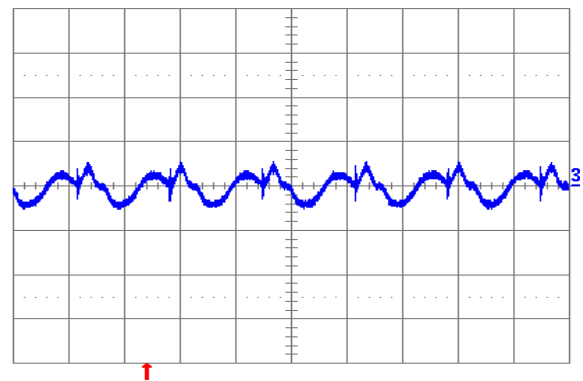


Fig. 1.2V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance 100 μ F ceramic + 1 μ F ceramic, and $V_{in} = 12$ V for $V_{out} = 1.2$ V. Time scale: 2 μ s/div.

YNS12S10 DC-DC Converter

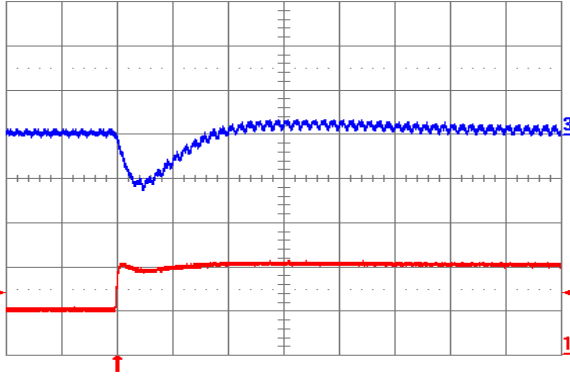


Fig. 1.2V.7: Output voltage response for $V_{out} = 1.2\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: $20\text{ }\mu\text{s}/\text{div}$.

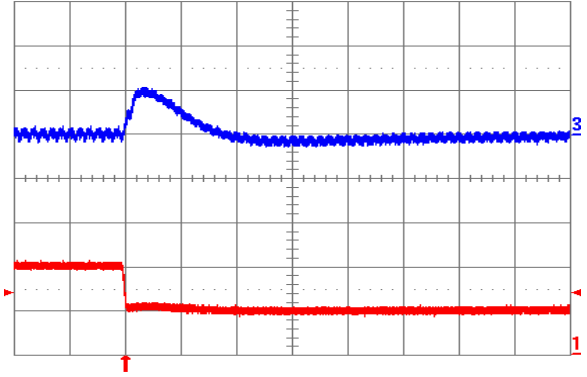


Fig. 1.2V.8: Output voltage response for $V_{out} = 1.2\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\text{ }\mu\text{F}$ ceramic. Time scale: $20\text{ }\mu\text{s}/\text{div}$.

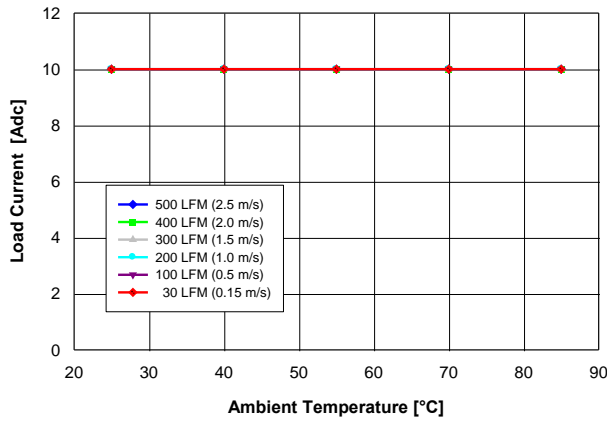


Fig. 1.0V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.0\text{ V}$ converter mounted vertically with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

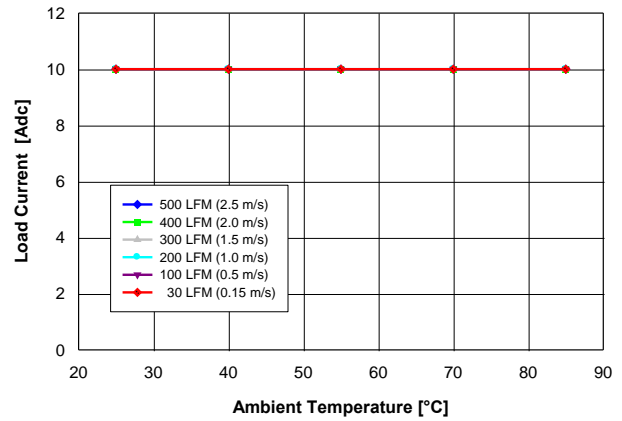


Fig. 1.0V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 1.0\text{ V}$ converter mounted horizontally with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

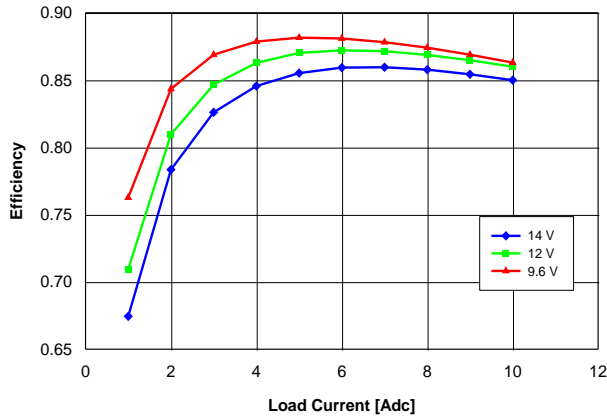


Fig. 1.0V.3: Efficiency vs. load current and input voltage for $V_{out} = 1.0\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

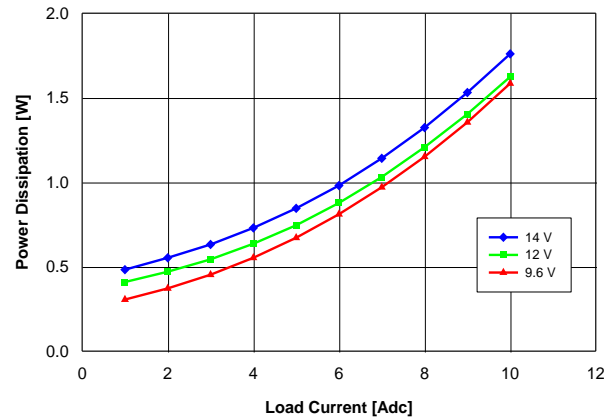


Fig. 1.0V.4: Power Loss vs. load current and input voltage for $V_{out} = 1.0\text{ V}$ converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25\text{ }^\circ\text{C}$.

YNS12S10 DC-DC Converter

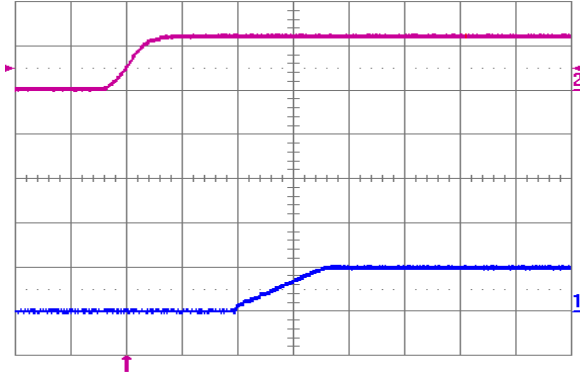


Fig. 1.0V.5: Turn-on transient for $V_{out} = 1.0\text{ V}$ with application of V_{in} at full rated load current (resistive) and $100\ \mu\text{F}$ external capacitance at $V_{in} = 12\text{ V}$. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (1 V/div.); Time scale: 2 ms/div.

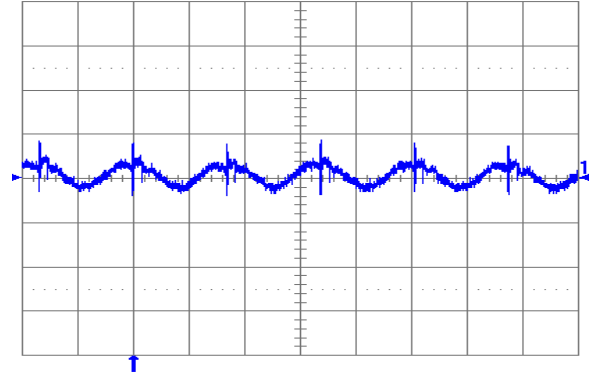


Fig. 1.0V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance $100\ \mu\text{F}$ ceramic + $1\ \mu\text{F}$ ceramic, and $V_{in} = 12\text{ V}$ for $V_{out} = 1.0\text{ V}$. Time scale: 2 μs /div.

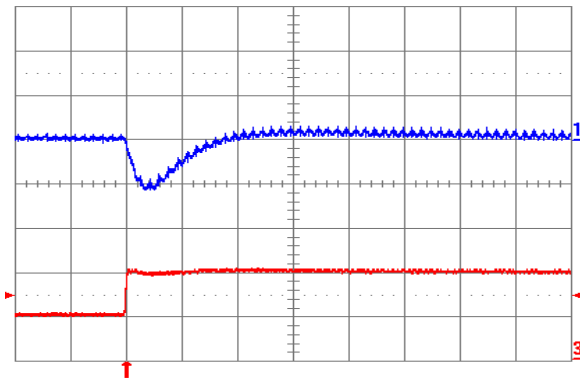


Fig. 1.0V.7: Output voltage response for $V_{out} = 1.0\text{ V}$ to positive load current step change from 5 A to 10 A with slew rate of $5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\ \mu\text{F}$ ceramic. Time scale: 20 μs /div.

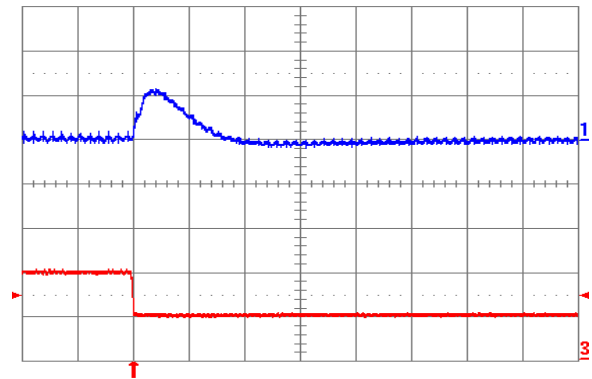


Fig. 1.0V.8: Output voltage response for $V_{out} = 1.0\text{ V}$ to negative load current step change from 10 A to 5 A with slew rate of $-5\text{ A}/\mu\text{s}$ at $V_{in} = 12\text{ V}$. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100\ \mu\text{F}$ ceramic. Time scale: 20 μs /div.

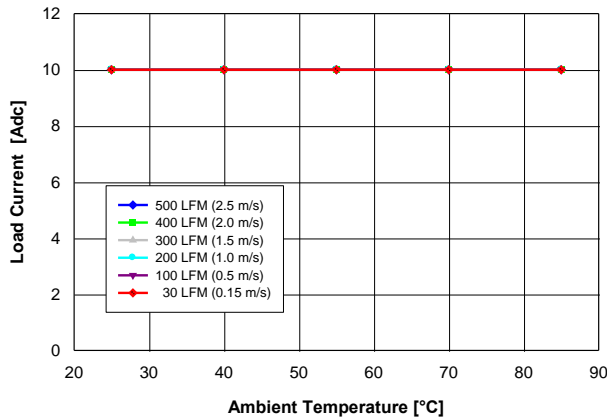


Fig. 0.7525V.1: Available load current vs. ambient temperature and airflow rates for $V_{out} = 0.7525\text{ V}$ converter mounted vertically with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

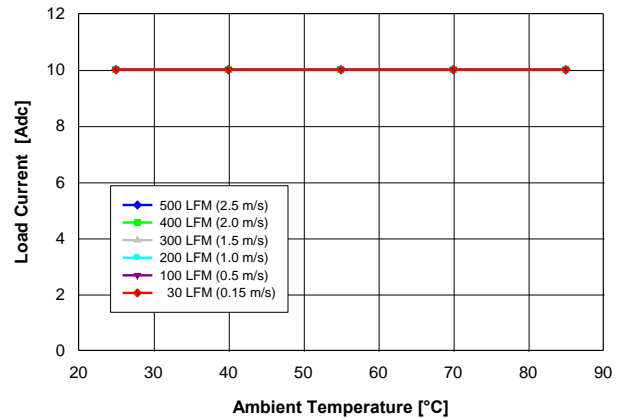


Fig. 0.7525V.2: Available load current vs. ambient temperature and airflow rates for $V_{out} = 0.7525\text{ V}$ converter mounted horizontally with $V_{in} = 12\text{ V}$, and maximum MOSFET temperature $\leq 110\text{ }^\circ\text{C}$.

YNS12S10 DC-DC Converter

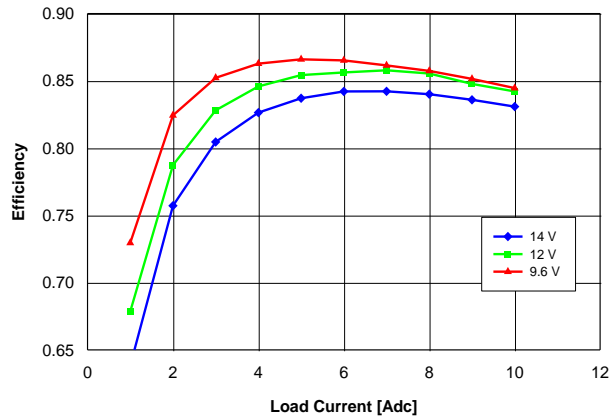


Fig. 0.7525V.3: Efficiency vs. load current and input voltage for $V_{out} = 0.7525$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

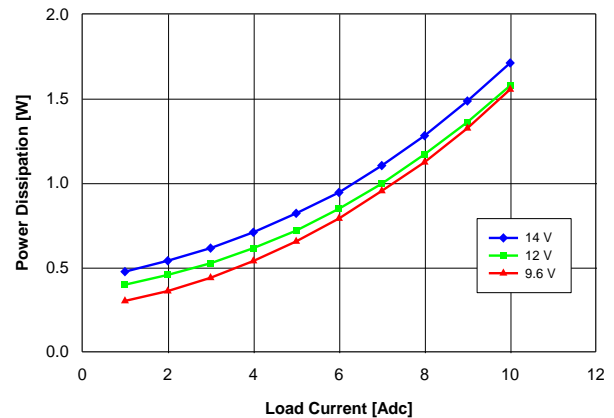


Fig. 0.7525V.4: Power Loss vs. load current and input voltage for $V_{out} = 0.7525$ V converter mounted vertically with air flowing at a rate of 200 LFM (1 m/s) and $T_a = 25$ °C.

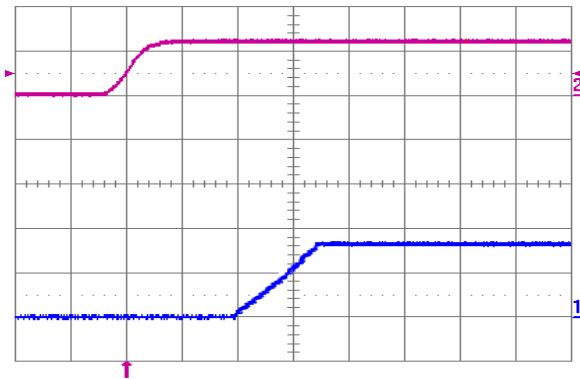


Fig. 0.7525V.5: Turn-on transient for $V_{out} = 0.7525$ V with application of V_{in} at full rated load current (resistive) and 100 μ F external capacitance at $V_{in} = 12$ V. Top trace: V_{in} (10 V/div.); Bottom trace: output voltage (0.5 V/div.); Time scale: 2 ms/div.

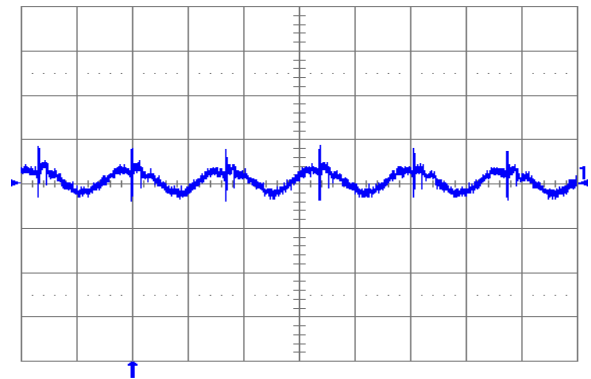


Fig. 0.7525V.6: Output voltage ripple (20 mV/div.) at full rated load current into a resistive load with external capacitance 100 μ F ceramic + 1 μ F ceramic, and $V_{in} = 12$ V for $V_{out} = 0.7525$ V. Time scale: 2 μ s/div.

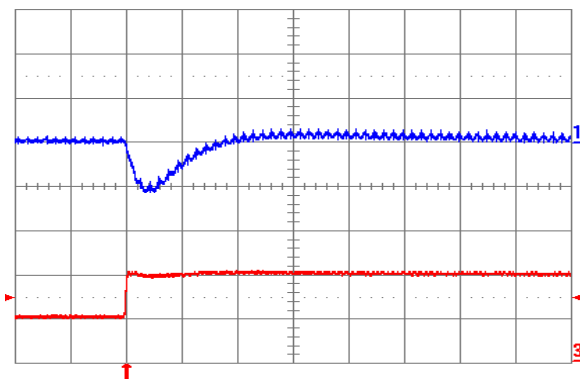


Fig. 0.7525V.7: Output voltage response for $V_{out} = 0.7525$ V to positive load current step change from 5 A to 10 A with slew rate of 5 A/ μ s at $V_{in} = 12$ V. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100$ μ F ceramic. Time scale: 20 μ s/div.

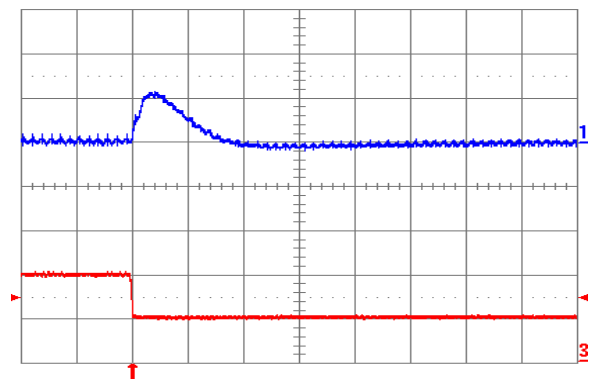
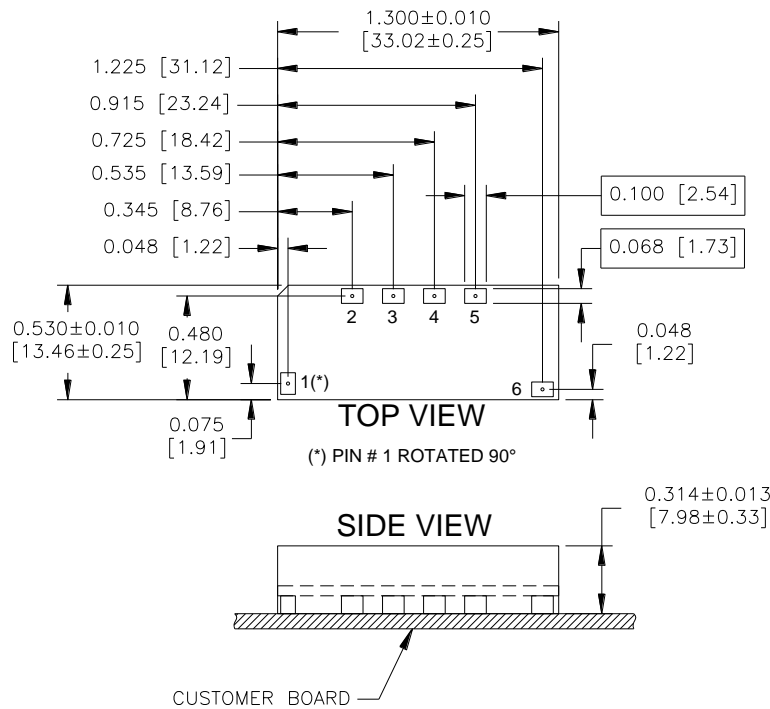


Fig. 0.7525V.8: Output voltage response for $V_{out} = 0.7525$ V to negative load current step change from 10 A to 5 A with slew rate of -5 A/ μ s at $V_{in} = 12$ V. Top trace: output voltage (100 mV/div.); Bottom trace: load current (5 A/div.). $C_o = 100$ μ F ceramic. Time scale: 20 μ s/div.

YNS12S10 DC-DC Converter

Physical Information



PAD/PIN CONNECTIONS	
Pad/Pin #	Function
1	ON/OFF
2	SENSE
3	TRIM
4	Vout
5	GND
6	Vin

YNS12S Platform Notes

- All dimensions are in inches [mm]
- Connector Material: Copper
- Connector Finish: Gold over Nickel
- Converter Weight: 0.22 oz [6.12 g]
- Converter Height: 0.327" Max., 0.301" Min.
- Recommended Surface-mount Pads: Min. 0.080" X 0.112" [2.03 x 2.84]

YNS05S Pinout (Surface Mount)

Ordering Information

Product Series	Input Voltage	Mounting Scheme	Rated Load Current	Enable Logic	Environmental
YNS	12	S	10	0	
Y-Series	9.6 to 14 VDC	S ⇒ Surface-Mount	10 A (0.7525 to 5.5 VDC)	0 ⇒ Standard (Positive Logic) D ⇒ Opposite of Standard (Negative Logic)	No Suffix ⇒ RoHS lead-solder-exempt compliant G ⇒ RoHS compliant for all six substances

The example above describes P/N YNS12S10-0: 9.6 to 14 VDC input, surface-mount, 10 A at 0.7525 to 5.5 VDC output, standard (positive logic), and Eutectic Tin/Lead solder. Please consult factory regarding availability of a specific version.

The YNS12S10 is not recommended for new designs and has been replaced by the YS12S10. Please refer to the YS12S10 data sheet for new product specifications.

For more information on these products consult: tech.support@psbel.com

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