

## 2.6 Watt Mono Filter-Free Class-D Audio Power Amplifier

### Features

- Efficiency With an 8-Ω Speaker:
  - 88% at 400 mW
  - 80% at 100 mW
- 3.8mA Quiescent Current
- 0.4μA Shutdown Current
- Optimized PWM Output Stage Eliminates LC Output Filter
- Internally Generated 250-kHz Switching Frequency Eliminates Capacitor and Resistor
- Improved PSRR (−75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- MSOP8, SOP8, DFN8 package

### General Description

The BL6306 is a 2.6W high efficiency filter-free class-D audio power amplifier that requires only three external components.

Features like 88% efficiency, −75dB PSRR, and improved RF-rectification immunity make the BL6306 ideal for cellular handsets. In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the BL6306.

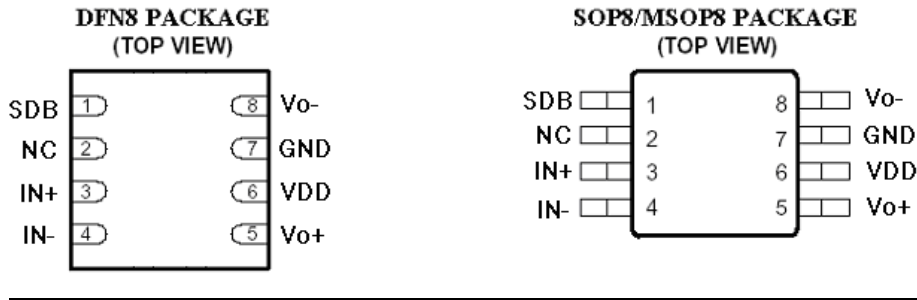
### Applications

- Mobile phone、PDA、MID
- MP3/4、PMP
- Portable electronic devices

### Order Information

Part Number	Package	Shipping
BL6306MM	MSOP8	3000 pcs / Tape & Reel
BL6306SO	SOP8	2500 pcs / Tape & Reel
BL6306DN	DFN8	3000 pcs / Tape & Reel

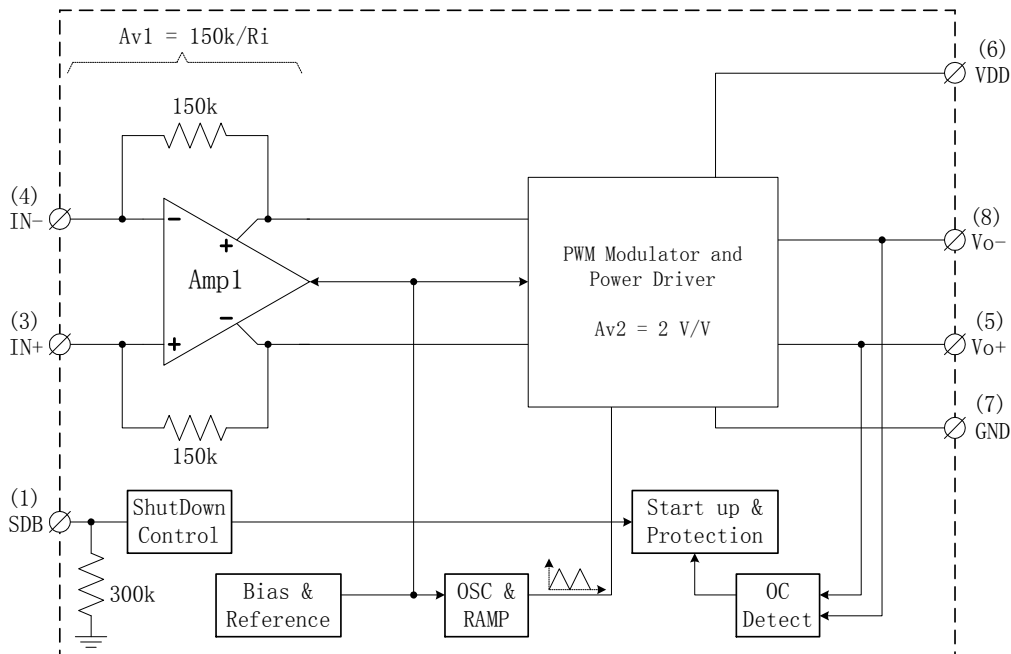
### Pin Diagrams



### Pin Description

Pin #	Name	Description
1	SDB	Shutdown terminal (low active)
2	NC	NC (No internal connection)
3	IN+	Positive differential input
4	IN-	Negative differential input
5	VO+	Positive BTL output
6	VDD	Power Supply
7	PGND	Power Ground
8	VO-	Negative BTL output

### Function Block Diagram



Notes: Total Voltage Gain =  $Av1 \times Av2 = 2 \times \frac{150k}{R_i}$

Figure 1. Function Block Diagram

**Application Circuit**

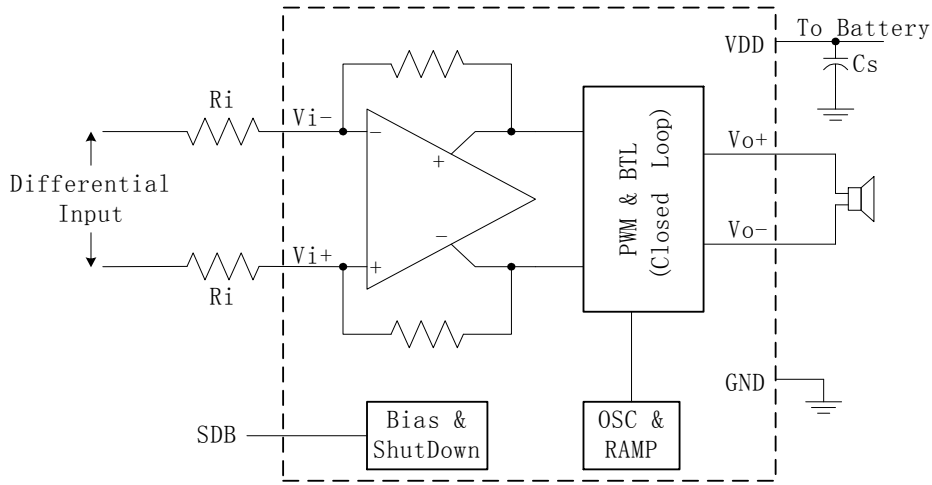


Figure 2. BL6306 Application Schematic With Differential Input

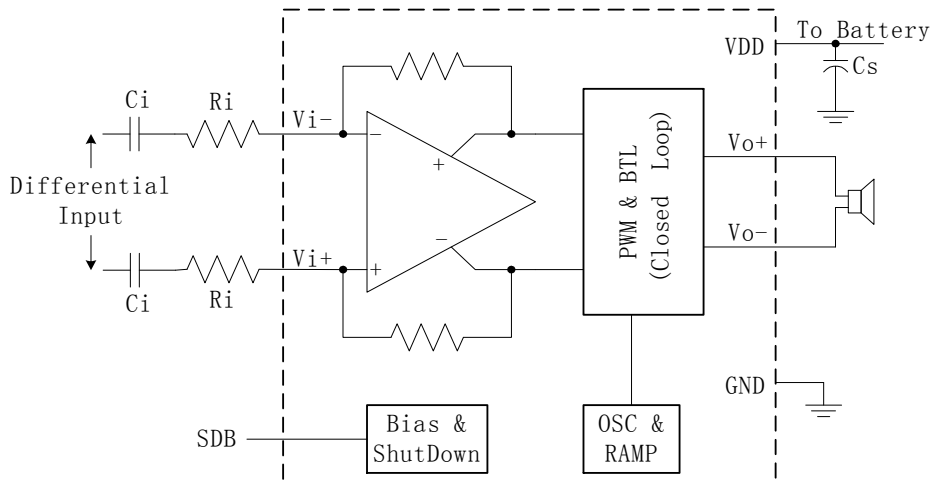


Figure 3. BL6306 Application Schematic With Differential Input and Input Capacitors

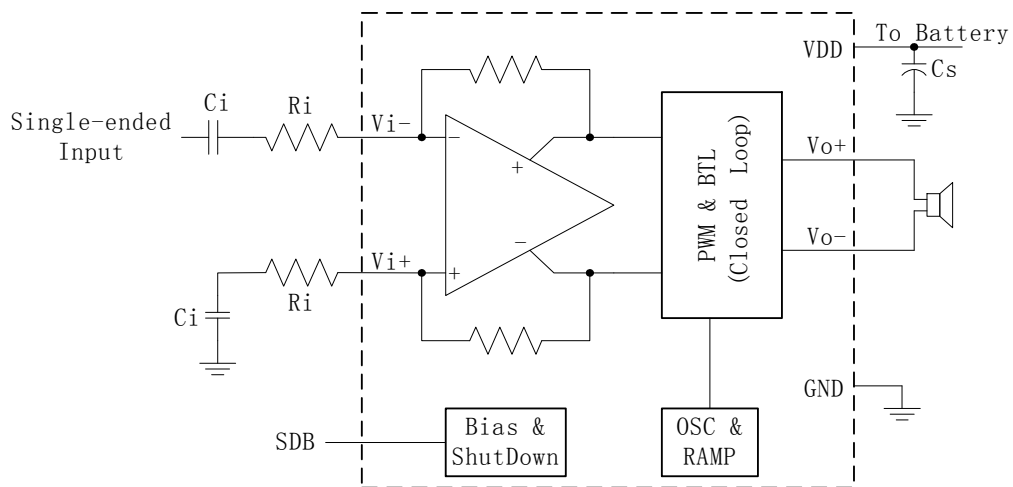


Figure 4. BL6306 Application Schematic With Single-Ended Input

**Absolute Maximum Ratings**

Supply Voltage	-0.3V to 6V
Input Voltage	-0.3V to VDD+0.3V
Storage Temperature	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

**NOTE:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is functional, but do not guarantee specific performance limits.

**Electrical Characteristics**

The following specifications apply for the circuit shown in Figure 5.

T<sub>A</sub> = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
I <sub>SD</sub>	Shutdown Current	V <sub>IN</sub> =0V, V <sub>SDB</sub> =0V, No Load		0.4	2	uA
I <sub>Q</sub>	Quiescent Current	V <sub>DD</sub> = 2.5V, V <sub>IN</sub> = 0V, No Load		2.2	3.2	mA
		V <sub>DD</sub> = 3.6V, V <sub>IN</sub> = 0V, No Load		2.6		
		V <sub>DD</sub> = 5.5V, V <sub>IN</sub> = 0V, No Load		3.8	8	
V <sub>OS</sub>	Output Offset Voltage	V <sub>IN</sub> = 0V, A <sub>V</sub> = 2V/V, V <sub>DD</sub> = 2.5V to 5.5V		2	25	mV
PSRR	Power Supply Rejection Ratio	V <sub>DD</sub> = 2.5V to 5.5V		-75		dB
CMRR	Common Mode Rejection Ratio	V <sub>DD</sub> = 2.5V to 5.5V, V <sub>IC</sub> = V <sub>DD</sub> /2 to 0.5V, V <sub>IC</sub> = V <sub>DD</sub> /2 to V <sub>DD</sub> - 0.8V		-68		dB
F <sub>SW</sub>	Modulation frequency	V <sub>DD</sub> = 2.5V to 5.5V	200	250	300	kHz
A <sub>V</sub>	Voltage gain	V <sub>DD</sub> = 2.5V to 5.5V	$\frac{270k}{R_1}$	$\frac{300k}{R_1}$	$\frac{330k}{R_1}$	V/V
R <sub>SDB</sub>	Resistance from SDB to GND			300		kΩ
Z <sub>I</sub>	Input impedance		135	150	165	kΩ
T <sub>WU</sub>	Wake-up time from shutdown	V <sub>DD</sub> = 3.6V		32		mS
r <sub>DS(on)</sub>	Drain-Source resistance (on-state)	V <sub>DD</sub> = 2.5V		700		mΩ
		V <sub>DD</sub> = 3.6V		500		
		V <sub>DD</sub> = 5.5V		400		
V <sub>SDIH</sub>	Shutdown Voltage Input High		1.3			V
V <sub>SDIL</sub>	Shutdown Voltage Input Low				0.4	V

**Operating Characteristics**

□  $V_{DD} = 5V$ ,  $R_I = 150k\Omega$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>L</sub> = 4Ω		2.60		W
		THD+N=1%, f=1KHz, R <sub>L</sub> = 4Ω		2.10		
		THD+N=10%, f=1KHz, R <sub>L</sub> = 8Ω		1.60		
		THD+N=1%, f=1KHz, R <sub>L</sub> = 8Ω		1.30		
THD+N	Total Harmonic Distortion + Noise	Po=1.0Wrms, f=1kHz, R <sub>L</sub> = 8Ω		0.21		%
SNR	Signal-to-Noise ratio	V <sub>DD</sub> =5V, Po=1.0Wrms, R <sub>L</sub> = 8Ω		91		dB

□  $V_{DD} = 3.6V$ ,  $R_I = 150k\Omega$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>L</sub> = 4Ω		1.35		W
		THD+N=1%, f=1KHz, R <sub>L</sub> = 4Ω		1.08		
		THD+N=10%, f=1KHz, R <sub>L</sub> = 8Ω		0.85		
		THD+N=1%, f=1KHz, R <sub>L</sub> = 8Ω		0.69		
THD+N	Total Harmonic Distortion + Noise	Po=0.5Wrms, f=1kHz, R <sub>L</sub> = 8Ω		0.21		%
K <sub>SVR</sub>	Supply ripple rejection ratio	V <sub>DD</sub> = 3.6V, input ac-grounded with C <sub>1</sub> = 2uF f=217Hz, V(Ripple)=200mV <sub>pp</sub>		-65		dB
V <sub>n</sub>	Output voltage noise	V <sub>DD</sub> = 3.6V, input ac-grounded with C <sub>1</sub> = 2uF, f=20~20kHz	No weighting	100		uV <sub>RMS</sub>
			A weighting	75		
CMRR	Common Mode Rejection Ratio	V <sub>DD</sub> = 3.6V, V <sub>IC</sub> = 1 V <sub>pp</sub> , f=217Hz		-70		dB

□  $V_{DD} = 2.5V$ ,  $R_I = 150k\Omega$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>L</sub> = 4Ω		0.60		W
		THD+N=1%, f=1KHz, R <sub>L</sub> = 4Ω		0.51		
		THD+N=10%, f=1KHz, R <sub>L</sub> = 8Ω		0.40		
		THD+N=1%, f=1KHz, R <sub>L</sub> = 8Ω		0.33		
THD+N	Total Harmonic Distortion + Noise	Po=0.2Wrms, f=1kHz, R <sub>L</sub> = 8Ω		0.21		%

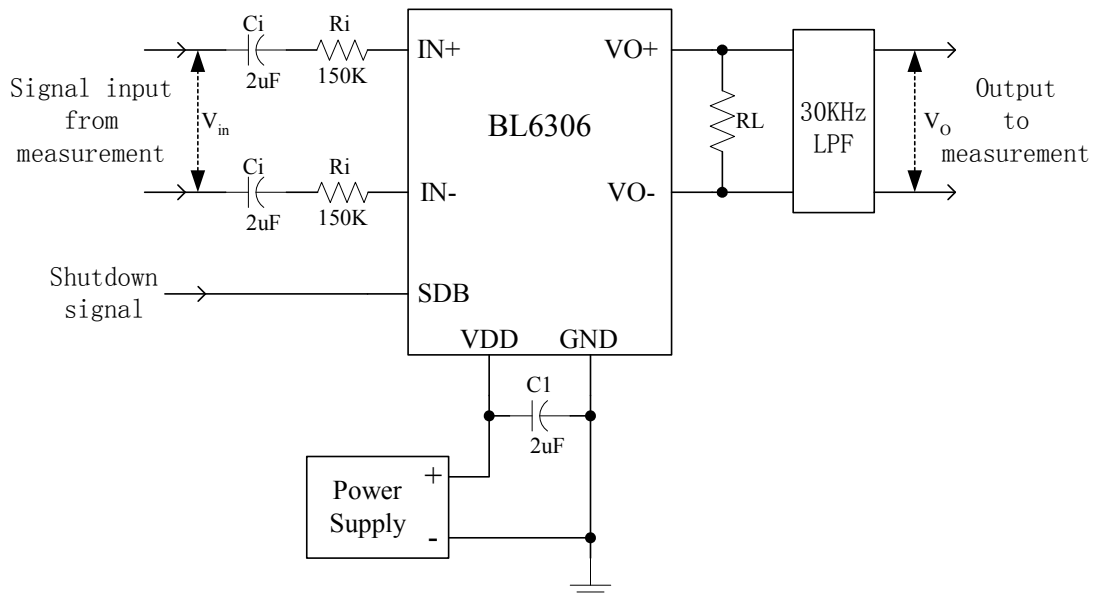
**Test Circuit**


Figure 5. BL6306 test set up circuit

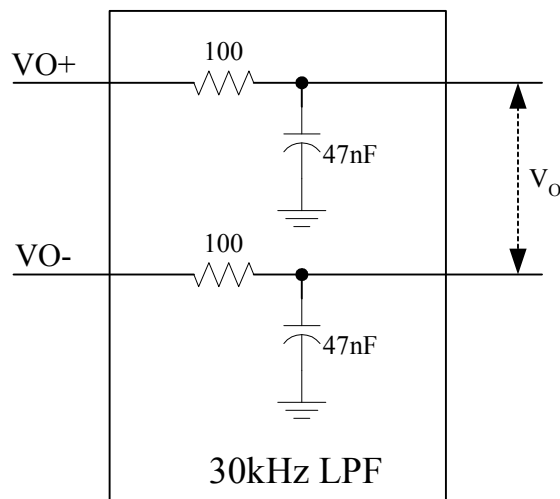


Figure 6. 30-kHz LPF for BL6306 test

- Notes:
- 1>.  $C_S$  should be placed as close as possible to VDD/GND pad of the device
  - 2>.  $C_i$  should be shorted for any Common-Mode input voltage measurement
  - 3>. A 33uH inductor should be used in series with  $R_L$  for efficiency measurement
  - 4>. The 30 kHz LPF (shown in figure 5) is required even if the analyzer has an internal LPF

**Component Recommended**

Due to the weak noise immunity of the single-ended input application, the differential input application should be used whenever possible. The typical component values are listed in the table:

$R_I$	$C_I$	$C_S$
150 k	3.3 nF	2 uF

- (1)  $C_1$  should have a tolerance of  $\pm 10\%$  or better to reduce impedance mismatch.
- (2) Use 1% tolerance resistors or better to keep the performance optimized, and place the  $R_1$  close to the device to limit noise injection on the high-impedance nodes.

### Input Resistors ( $R_1$ ) & Capacitors ( $C_1$ )

The input resistors ( $R_1$ ) set the total voltage gain of the amplifier according to Eq1

$$Gain = \frac{2 \times 150k\Omega}{R_1} \left( \frac{V}{V} \right) \quad Eq1$$

The input resistor matching directly affects the CMRR, PSRR, and the second harmonic distortion cancellation.

If a differential signal source is used, and the signal is biased from  $0.5V \sim V_{DD}-0.8V$  (shown in Figure2), the input capacitor ( $C_1$ ) is not required.

If the input signal is not biased within the recommended common-mode input range in differential input application (shown in Figure3), or in a single-ended input application (shown in Figure4), the input coupling capacitors are required.

If the input coupling capacitors are used, the  $R_1$  and  $C_1$  form a high-pass filter (HPF). The corner frequency ( $f_c$ ) of the HPF can be calculated by Eq2

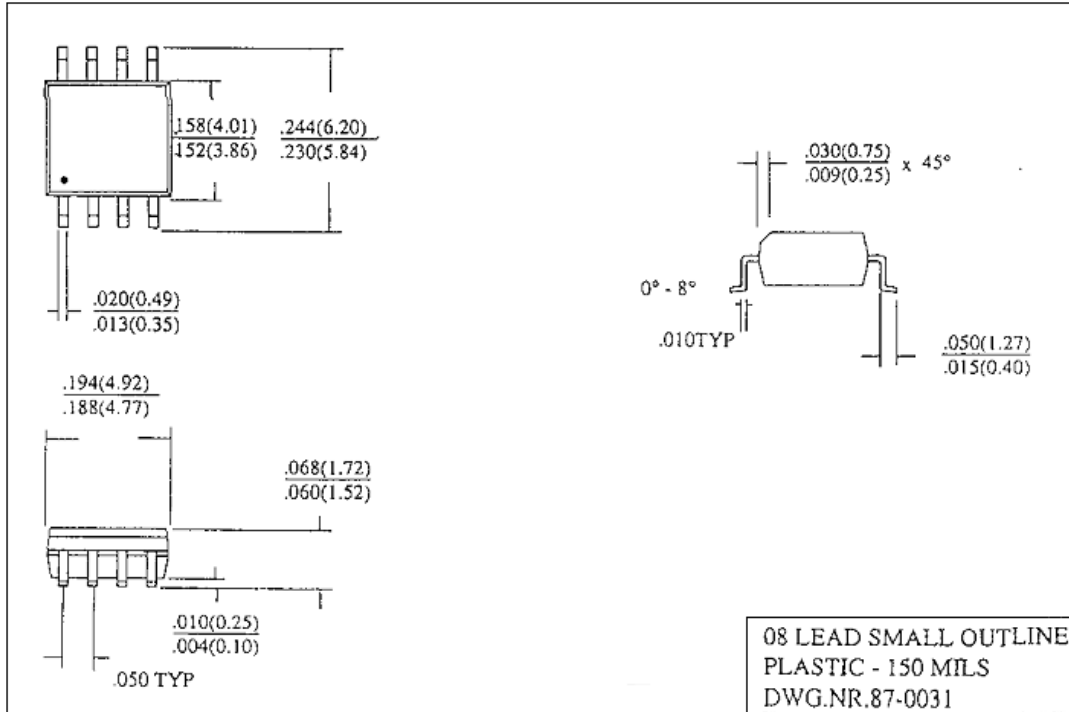
$$f_c = \frac{1}{2\pi \cdot R_1 \cdot C_1} \quad (Hz) \quad Eq2$$

### Decoupling Capacitor ( $C_S$ )

A good low equivalent-series-resistance (ESR) ceramic capacitor ( $C_S$ ), used as power supply decoupling capacitor ( $C_S$ ), is required for high power supply rejection (PSRR), high efficiency and low total harmonic distortion (THD).  $C_S$  is  $2\mu F$ , placed as close as possible to the device VDD pin.

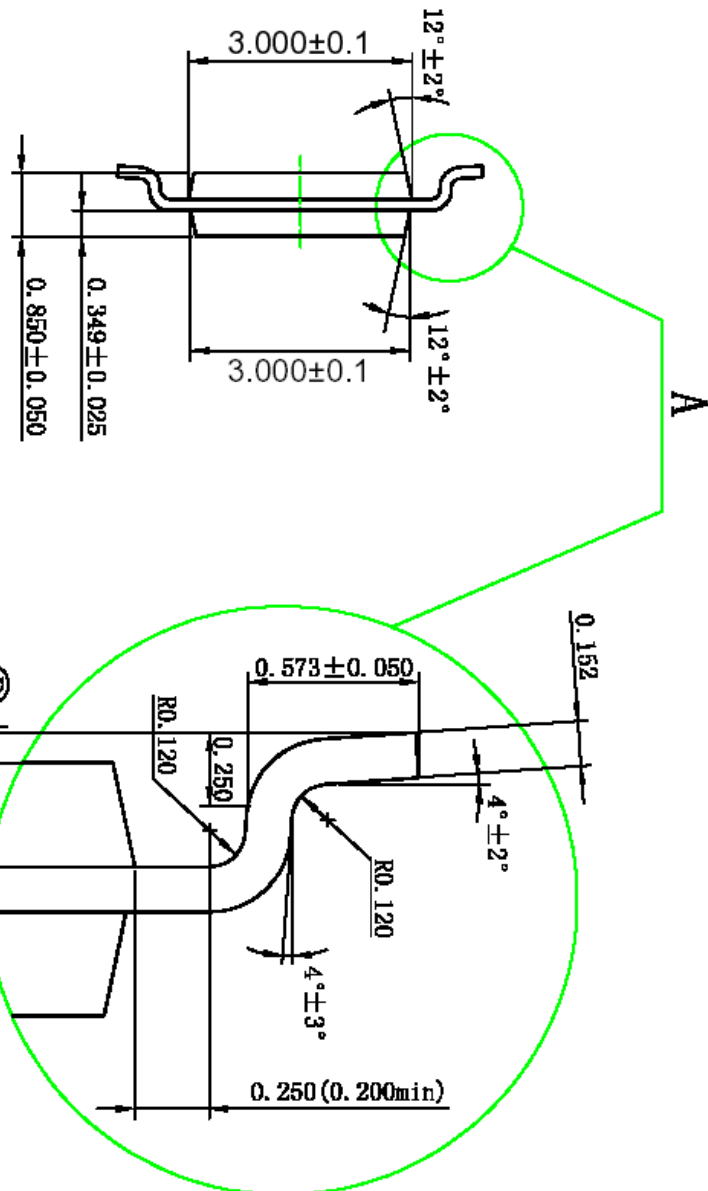
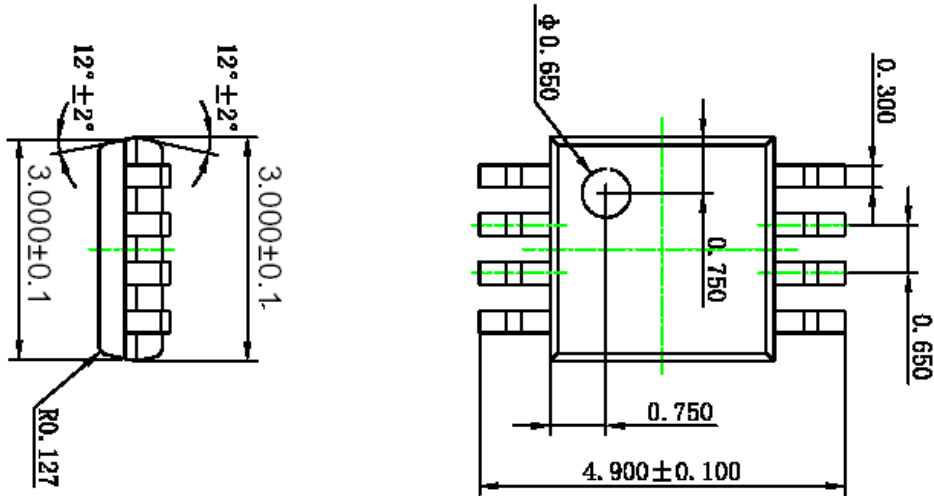
**Package Dimensions**

SOP8



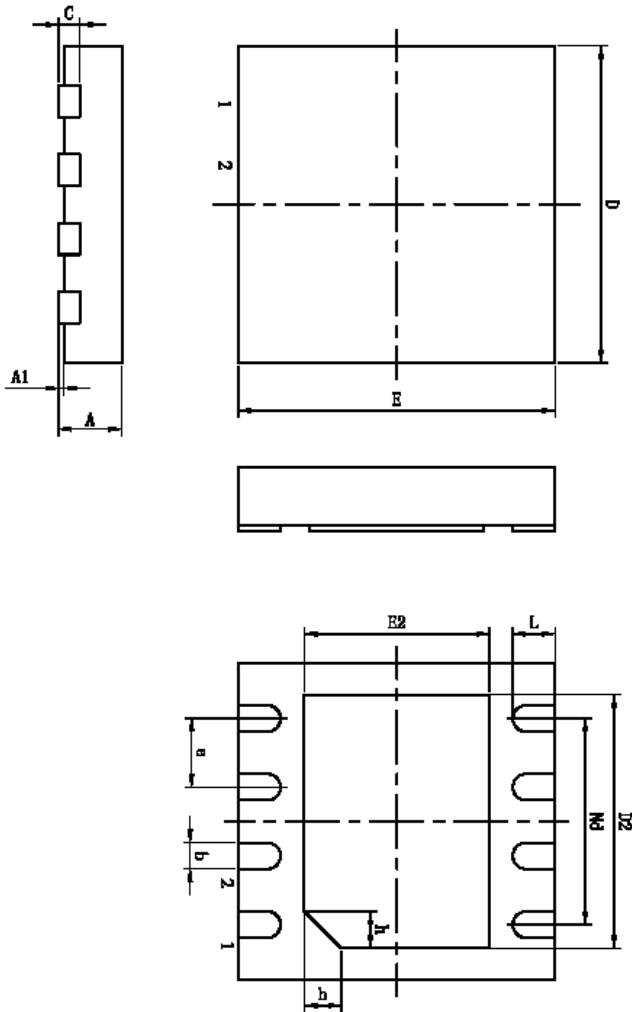


MSOP8



**技术要求**

1. 成型管脚各引线端相对于基准面B的距离偏差为±0.04 (共面性);
2. 所有尺寸为mm;
3. 视图方向:

**DFN8**


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.50REF		
e	0.65BSC		
Nd	1.95BSC		
E	2.90	3.00	3.10
E2	1.55REF		
L	0.30	0.40	0.50
h	0.20	0.25	0.30

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