1. Features

- 100 Mbps data rate
- Robust isolation barrier:
  - ±100 kV/μs Typical CMTI
  - Up to 3750 VRMS Isolation Rating
  - >50 years projected lifetime
  - Up to 8 kV surge capability
- Wide supply range: 2.5 V to 5.5 V
- 2.5-V to 5.5-V level translation
- Wide temperature range: –40°C to +125°C
- The default output high level (H) and low level (L) options
- Low propagation delay: 11ns (TYP value, 5V power supply)
- Low pulse width distortion: 3ns

2. Applications

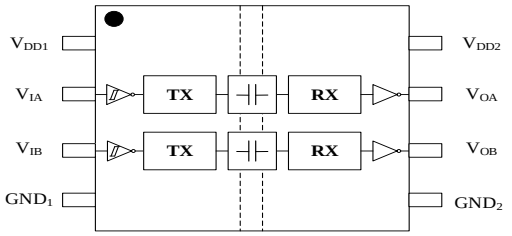
- Industrial automation
- Motor control
- Solar inverters
- Power supplies
- Medical equipment

3. Description

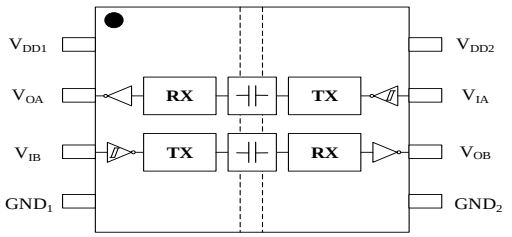
The BL712x devices are high-performance, dual- channel digital isolators, Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier，and data can be encoded and recovered independently. The BL7120 device has both channels in the same direction. The BL7121 device has one reverse channel and one forward channel while the BL7122 device has one forward channel and one reverse channel。In the event of input power or signal loss, the default output is high for devices without suffix H and low for devices with suffix L.

BL712x provide high electromagnetic immunity and low emissions at low power consumption, help prevent noise currents on data buses, from damaging sensitive circuitry. High CMTI capability can ensure the correct transmission. BL712x device packaged in 8 pin narrow SOIC（A）package, with 3.75KV$_{RMS}$ isolation and withstand voltage capability.

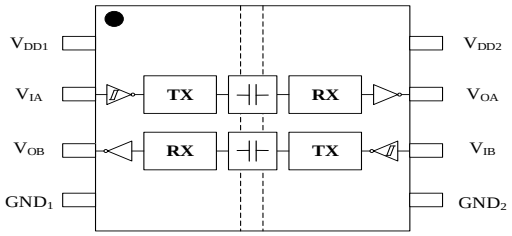
4. Block diagram



BL7120



BL7121



BL7122

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5. Specifications

5.1 Absolute Maximum Ratings

PARAMETER		Min	MAX	UNIT
V_{DD1}, V_{DD2}	Supply voltage[b]	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	V_{DD}+0.5[c]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature	-65	150	℃

[a] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[b] All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

[c] Maximum voltage must not exceed 6V.

5.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM) according to ANSI / ESDA / JEDEC JS-001-	±6000	V
	Module charging mode (CDM) according to ANSI / ESDA / JEDEC JESD22	±1500	
	Machine mode (mm) according to JESD22-a115c	±400	

5.3 Recommended Operating Conditions

PARAMETER		TYP		MAX	UNIT
V_{DD1}, V_{DD2} Supply voltage		2.35		5.5	V
$V_{DD(UVLO+)}$ UVLO threshold when supply voltage is rising			1.75	2.0	V
$V_{DD(UVLO-)}$ UVLO threshold when supply voltage is falling		1.55	1.65		V
$V_{HYS(UVLO)}$ Supply voltage UVLO hysteresis		10	70	230	mV
I_{OH} High level output current	V_{DDO}[a]=5V	-4			mA
	V_{DDO}=3.3V	-2			
	V_{DDO}=2.5V	-1			
I_{OL} Low level output current	V_{DDO}=5V			4	mA
	V_{DDO}=3.3V			2	
	V_{DDO}=2.5V			1	
V_{IH} High-level input voltage		0.7 x V_{DDI}[a]		V_{DDI}	V
V_{IL} Low-level input voltage		0		0.25 x V_{DDI}	V
DR[b] Data rate		0		100	Mbps
T_A Ambient temperature		-40	25	125	℃

Note：

[a] V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}.

[b] 100 Mbps is the maximum specified data rate, although higher data rates are possible.

5.4 Power Ratings

PARAMETER	TEST CONDITIONS	MAX	UNIT
BL7120			
Power consumption of P_D	V_{DD1} = V_{DD2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	130	mW
Power consumption of P_{D1}		26	mW
Power consumption of P_{D2}		104	mW
BL7121			
Power consumption of P_D	V_{DD1} = V_{DD2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	130	mW
Power consumption of P_{D1}		65	mW
Power consumption of P_{D2}		65	mW
BL7122			
Power consumption of P_D	V_{DD1} = V_{DD2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	130	mW
Power consumption of P_{D1}		65	mW
Power consumption of P_{D2}		65	mW

5.5 Insulation Specifications

PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR External clearance (1)	Shortest terminal-to-terminal distance through air	4	mm
CPG External creepage (1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI Distance through the insulation	Minimum internal gap (internal clearance)	18	μm
CTI Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	V
V_{IORM} VIORM Maximum repetitive peak isolation voltage	AC voltage (bipolar)	637	V_{PK}
V_{IOWM} Maximum working isolation voltage	AC voltage	450	V_{RMS}
	DC voltage	637	V_{DC}
V_{IOTM} Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM} Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.6 × V_{IOSM}	5000	V_{PK}
V_{ISO} Withstanding isolation voltage	(1) V_{TEST} = V_{ISO}, t = 60 s(qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	3.75	kV_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

5.6 Electrical Characteristics—5-V Supply

V_{DD1}=V_{DD2}= 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	I_{OH}=-4mA;Figure 7-1	V_{DDO}[a]-0.4	4.8		V
V_{OL} Low-level output voltage	I_{OL}=4mA;Figure 7-1		0.2	0.4	V
$V_{IT+(IN)}$ Rising input voltage threshold			0.6 x V_{DDI}	0.7 x V_{DDI}	V
$V_{IT-(IN)}$ Falling input voltage threshold		0.3 x V_{DDI}	0.4 x V_{DDI}		V
$V_{I(HYS)}$ Input threshold voltage hysteresis			1.23		V
I_{IH} High-level input current	V_{IH}=V_{DD1} at INx or ENx			5	μA
I_{IL} Low-level input current	V_{IL}=0V at INx or ENx	-5			μA
Z_O Output impedance	Z_O=V_{OL}/I_{OL}		42		Ω
CMTI Common-mode transient	Figure 7-2	80	100		kV/μs

Note：

[a] V_{DDO}= Output-side V_{DD}, V_{DDI}= Input-side V_{DD}。

[b] INx= Input, ENx=Output Enable

5.7 Electrical Characteristics—3.3-V Supply

V_{DD1}=V_{DD2}= 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH High-level output voltage	I_{OH}=-2mA;Figure 7-1	V_{DDO}[a] -0.3	3.2		V
VOL Low-level output voltage	I_{OL}=2mA;Figure 7-1		0.1	0.3	V
VIT+(IN) Rising input voltage threshold			0.6 x V_{DDI}	0.7 x V_{DDI}	V
VIT-(IN) Falling input voltage threshold		0.3 x V_{DDI}	0.4 x V_{DDI}		V
VI(HYS) Input threshold voltage			0.88		V
IIH High-level input current	V_{IH}=VDD1 at INx or ENx			5	μA
IIL Low-level input current	V_{IL}=0V at INx or ENx	-5			μA
ZO Output impedance	Z_O=V_{OL}/I_{OL}		30		Ω
CMTI Common-mode transient	Figure 7-2	80	100		kV/μs

Note：

[a] V_{DDO}= Output-side V_{DD}, V_{DDI}= Input-side V_{DD}。

[b] INx= Input, ENx=Output Enable

5.8 Electrical Characteristics—2.5-V Supply

V_{DD1}=V_{DD2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH High-level output voltage	I_{OH}=-1mA;Figure 7-1	V_{DDO}[a]-0.2	2.45		V
VOL Low-level output voltage	I_{OL}=1mA;Figure 7-1		0.05	0.2	V
VIT+(IN) Rising input voltage threshold			0.6 x V_{DDI}	0.7 x V_{DDI}	V
VIT-(IN) Falling input voltage threshold		0.3 x V_{DDI}	0.4 x V_{DDI}		V
VI(HYS) Input threshold voltage			0.82		V
IIH High-level input current	V_{DD1} at INX or ENX			5	μA
IIL Low-level input current	0V at INX or ENX	-5			μA
ZO Output impedance	Z_O=V_{OL}/I_{OL}		34		Ω
CMTI Common-mode transient	Figure 7-2	80	100		kV/μs

Note：

[a] V_{DDO}= Output-side V_{DD}, V_{DDI}= Input-side V_{DD}。

[b] INx= Input, ENx=Output Enable

5.9 Supply Current Characteristics—5-V Supply

V_{DD1}=V_{DD2}= 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNI
BL7120							
Supply current - DC signal	V_I=0V（BL7120AL） V_I=V_{DD1}（BL7120AH）		I_{DD1}		1.4	1.7	mA
			I_{DD2}		2.3	2.7	
	V_I=V_{DD1}（BL7120AL） V_I=0V（BL7120AH）		I_{DD1}		3.8	4.4	
			I_{DD2}		2.3	2.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.0	3.6	
			I_{DD2}		3.4	4.0	
		10Mbps (5MHz)	I_{DD1}		3.1	3.8	
			I_{DD2}		4.3	4.8	
		100Mbps (50MHz)	I_{DD1}		3.5	4.1	
			I_{DD2}		14.0	15.6	
BL7121							
Supply current - DC signal	V_I=0V（BL7121AL） V_I=V_{DDI} [a]（BL7121AH）		I_{DD1}		2.3	2.8	mA
			I_{DD2}		2.3	2.8	
	V_I=V_{DDI}（BL7121AL） V_I=0V（BL7121AH）		I_{DD1}		4.4	5.0	
			I_{DD2}		4.4	5.0	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.4	4.0	
			I_{DD2}		3.4	4.0	
		10Mbps (5MHz)	I_{DD1}		3.9	4.4	
			I_{DD2}		3.9	4.4	
		100Mbps (50MHz)	I_{DD1}		9.0	9.6	
			I_{DD2}		9.0	9.6	
BL7122							
Supply current - DC signal	V_I=0V（BL7122AL） V_I=V_{DDI}（BL7122AH）		I_{DD1}		2.3	2.8	mA
			I_{DD2}		2.3	2.8	
	V_I=V_{DDI}（BL7122AL） V_I=0V（BL7122AH）		I_{DD1}		4.4	5.0	
			I_{DD2}		4.4	5.0	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.4	4.0	
			I_{DD2}		3.4	4.0	
		10Mbps (5MHz)	I_{DD1}		3.9	4.4	
			I_{DD2}		3.9	4.4	
		100Mbps (50MHz)	I_{DD1}		9.0	9.6	
			I_{DD2}		9.0	9.6	

Note：

[a] V_{DDI}= Input-side V_{DD}.

5.10 Supply Current Characteristics—3.3-V Supply

V_{DD1}=V_{DD2}= 3.3V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNI
BL7120							
Supply current - DC signal	V_I=0V（BL7120AL） V_I=V_{DD1}（BL7120AH）		I_{DD1}		1.4	1.7	mA
			I_{DD2}		2.3	2.7	
	V_I=V_{DD1}（BL7120AL） V_I=0V（BL7120AH）		I_{DD1}		3.8	4.4	
			I_{DD2}		2.3	2.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		2.9	3.6	
			I_{DD2}		3.3	4.0	
		10Mbps (5MHz)	I_{DD1}		3.1	3.8	
			I_{DD2}		4.1	4.8	
		100Mbps (50MHz)	I_{DD1}		3.0	3.7	
			I_{DD2}		11.0	12.6	
BL7121							
Supply current - DC signal	V_I=0V（BL7121AL） V_I=V_{DDI} [a]（BL7121AH）		I_{DD1}		2.3	2.8	mA
			I_{DD2}		2.3	2.8	
	V_I=V_{DDI}（BL7121AL） V_I=0V（BL7121AH）		I_{DD1}		4.4	5.0	
			I_{DD2}		4.4	5.0	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.3	3.9	
			I_{DD2}		3.3	3.9	
		10Mbps (5MHz)	I_{DD1}		3.7	4.2	
			I_{DD2}		3.7	4.2	
		100Mbps (50MHz)	I_{DD1}		7.4	8.0	
			I_{DD2}		7.4	8.0	
BL7122							
Supply current - DC signal	V_I=0V（BL7122AL） V_I=V_{DDI}（BL7122AH）		I_{DD1}		2.3	2.8	mA
			I_{DD2}		2.3	2.8	
	V_I=V_{DDI}（BL7122AL） V_I=0V（BL7122AH）		I_{DD1}		4.4	5.0	
			I_{DD2}		4.4	5.0	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.3	3.9	
			I_{DD2}		3.3	3.9	
		10Mbps (5MHz)	I_{DD1}		3.7	4.2	
			I_{DD2}		3.7	4.2	
		100Mbps (50MHz)	I_{DD1}		7.4	8.0	
			I_{DD2}		7.4	8.0	

Note：

[a] V_{DDI}= Input-side V_{DD}.

5.11 Supply Current Characteristics—2.5-V Supply

V_{DD1}=V_{DD2}= 2.5V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNI
BL7120							
Supply current - DC signal	V_I=0V（BL7120AL） V_I=V_{DD1}（BL7120AH）		I_{DD1}		1.4	1.7	mA
			I_{DD2}		2.3	2.7	
	V_I=V_{DD1}（BL7120AL） V_I=0V（BL7120AH）		I_{DD1}		3.8	4.4	
			I_{DD2}		2.3	2.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		2.9	3.6	
			I_{DD2}		3.3	4.0	
		10Mbps (5MHz)	I_{DD1}		2.9	3.6	
			I_{DD2}		3.8	4.6	
		100Mbps (50MHz)	I_{DD1}		2.6	3.5	
			I_{DD2}		9.8	11.6	
BL7121							
Supply current - DC signal	V_I=0V（BL7121AL） V_I=V_{DDI} [a]（BL7121AH）		I_{DD1}		2.3	2.8	mA
			I_{DD2}		2.3	2.8	
	V_I=V_{DDI}（BL7121AL） V_I=0V（BL7121AH）		I_{DD1}		4.4	5.0	
			I_{DD2}		4.4	5.0	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.3	3.9	
			I_{DD2}		3.3	3.9	
		10Mbps (5MHz)	I_{DD1}		3.5	4.1	
			I_{DD2}		3.5	4.1	
		100Mbps (50MHz)	I_{DD1}		6.5	7.1	
			I_{DD2}		6.5	7.1	
BL7122							
Supply current - DC signal	V_I=0V（BL7122AL） V_I=V_{DDI}（BL7122AH）		I_{DD1}		2.3	2.8	mA
			I_{DD2}		2.3	2.8	
	V_I=V_{DDI}（BL7122AL） V_I=0V（BL7122AH）		I_{DD1}		4.4	5.0	
			I_{DD2}		4.4	5.0	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	2Mbps (1MHz)	I_{DD1}		3.3	3.9	
			I_{DD2}		3.3	3.9	
		10Mbps (5MHz)	I_{DD1}		3.5	4.1	
			I_{DD2}		3.5	4.1	
		100Mbps (50MHz)	I_{DD1}		6.5	7.1	
			I_{DD2}		6.5	7.1	

Note：

[a] V_{DDI}= Input-side V_{DD}.

5.12 Switching Characteristics—5-V Supply

V_{DD1}=V_{DD2}= 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	Figure 7-1	7	11	15	ns
PWD Pulse width distortion | t_{PLH} –t_{PHL} |			1.2	3	ns
$t_{sk(pp)}$ Part-to-part skew time [a]				4.5	ns
t_r Output signal rise time	Figure 7-1		1.7	2.4	ns
t_f Output signal fall time			1.7	2.4	ns

Note:

[a]$t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.13 Switching Characteristics—3.3-V Supply

V_{DD1}=V_{DD2}= 3.3V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	Figure 7-1	7	11	15	ns
PWD Pulse width distortion | t_{PLH} –t_{PHL} |			1.2	3	ns
$t_{sk(pp)}$ Part-to-part skew time [a]				4.5	ns
t_r Output signal rise time	Figure 7-1		1.6	2.3	ns
t_f Output signal fall time			1.6	2.3	ns

Note:

[a]$t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.14 Switching Characteristics—2.5-V Supply

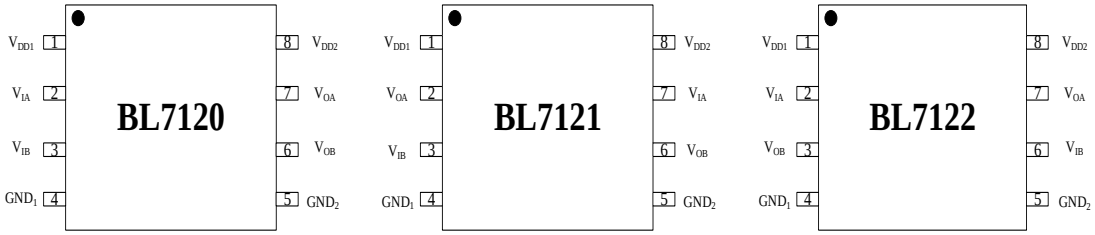
V_{DD1}=V_{DD2}= 2.5V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	Figure 7-1	9	13	17	ns
PWD Pulse width distortion | t_{PLH} –t_{PHL} |			1.2	3	ns
$t_{sk(pp)}$ Part-to-part skew time [a]				4.5	ns
t_r Output signal rise time	Figure 7-1		1.9	2.4	ns
t_f Output signal fall time			1.9	2.4	ns

Note:

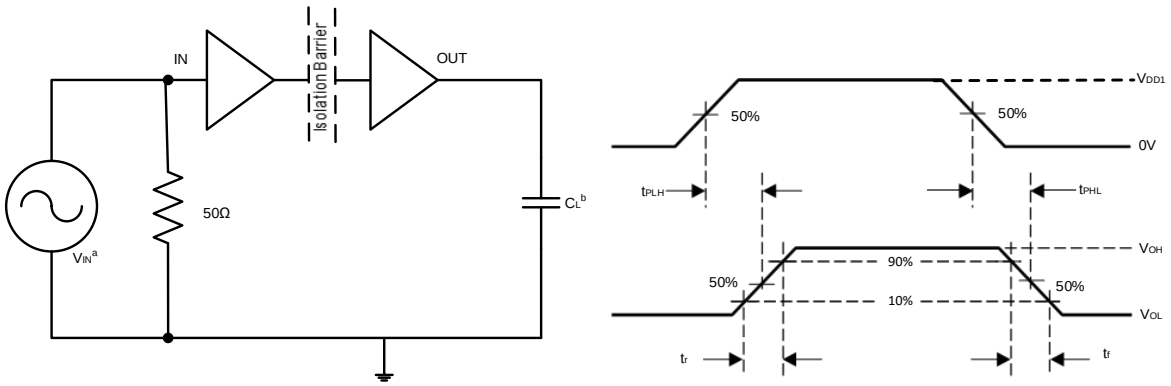
[a]$t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6. Pin function description



引脚编号	引脚名称	功能描述
1	V_{DD1}	Power supply, V_{DD1}
2	V_{IA}/V_{OA}	Input, channel A / Output, channel A
3	V_{IB} /V_{OB}	Input, channel B/ Output, channel B
4	GND_1	Ground connection for V_{DD1}
5	GND_2	Ground connection for V_{DD2}
6	V_{OB}/V_{IB}	Output, channel B / Input, channel B
7	V_{OA}/V_{IA}	Output, channel A / Input, channel A
8	V_{DD2}	Power supply, V_{DD2}

7. Parameter Measurement Information

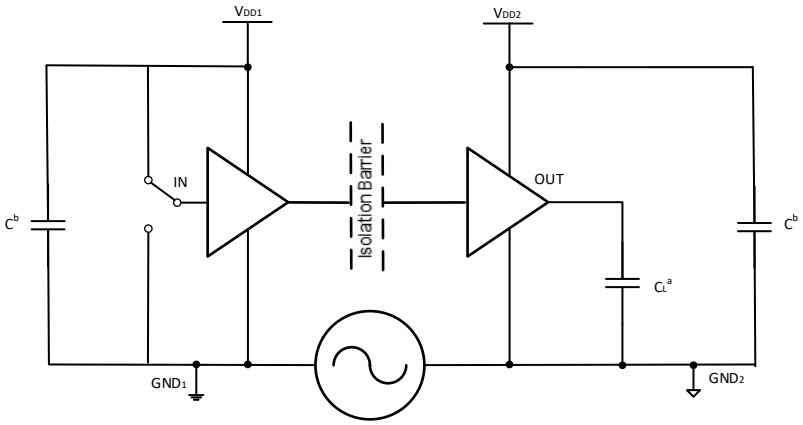


Note：

[a] The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

[b] C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7-1 Switching Characteristics Test Circuit and Voltage Waveforms



Note：

[a] C_L= 15pF, including load capacitance and instrument capacitance.

[b] C is 0.1μF Bypass capacitor

Figure 7-2 CMTI common mode transient immunity test circuit

8. Function Table

VDDI	VDDO	Input INX	Output OUTX	COMMENTS
PU	PU	H	H	Normal Operation: One channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode:（L suffix low，H suffix high） If the input remains disconnected, the output remains at its default value
PD	PU	X	Default	Default mode:（L suffix low，H suffix high） When V_{DDI}[a] is unpowered, he output remains at its default value
X	PD	X	Undetermined	When V_{DDO}[a] is unpowered, output is undetermined

Note：

[a] V_{DDO}=Output, V_{DD}，V_{DDI}=Input, V_{DD}.

[b] H= High level, L = Low leve, X = Irrelevant.

9. Reference circuit

Unlike optocouplers, external components are required to improve performance, provide bias, or limit current. BL712x Series Digital Isolators only need two external V_{DD} bypass capacitors to work

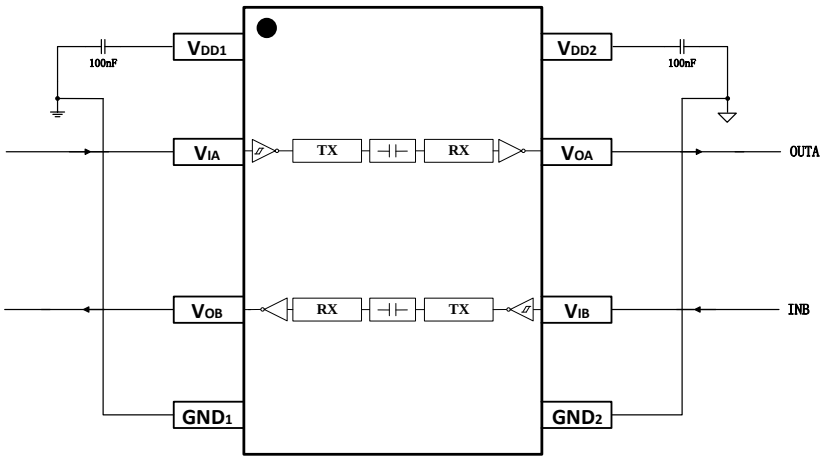
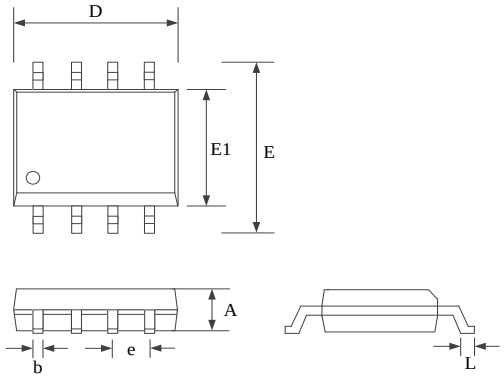


Figure 9-1 TYP application circuit of BL7122

10. PACKAGE INFORMATION

10.1 SOIC-8 Narrow (A)



Symbol	MIN	TYP	MAX
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
A	1.30	1.40	1.50
b	0.39	—	0.47
e		1.27BSC	
L	0.50	—	0.80

Figure 10-1 outline of SOIC-8 narrow body package

11. Ordering Info

Device	rate	Channel	Forward/Backward	Rated Voltage	Default	Package
BL7120AL	100Mbps	2	2/0	3750V_{RMS}	LOW	SOIC-8-Narrow
BL7120AH	100Mbps	2	2/0	3750V_{RMS}	HIGH	SOIC-8-Narrow
BL7121AL	100Mbps	2	1/1	3750V_{RMS}	LOW	SOIC-8-Narrow
BL7121AH	100Mbps	2	1/1	3750V_{RMS}	HIGH	SOIC-8-Narrow
BL7122AL	100Mbps	2	1/1	3750V_{RMS}	LOW	SOIC-8-Narrow
BL7122AH	100Mbps	2	1/1	3750V_{RMS}	HIGH	SOIC-8-Narrow

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