

### FEATURES

- Ultra-low Noise for RF Application
- Ultra-Fast Response in Line/Load Transient
- Quick Start-Up (Typically 50 $\mu$ S)
- <0.01 $\mu$ A Standby Current When Shutdown.
- Low Dropout:210mV@300mA
- Wide Operating Voltage Ranges:2V to 6V
- TTL-logic-Controlled Shutdown Input
- Low Temperature Coefficient
- Current Limiting Protection
- Thermal Shutdown Protection
- Only 1 $\mu$ F Output Capacitor Required for Stability
- High Power Supply Rejection Ratio
- Custom Voltage Available
- Fast output discharge
- Available in 5-Lead SOT-23 and SC-70 Package

### APPLICATIONS

- Cellular and Smart Phones
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers

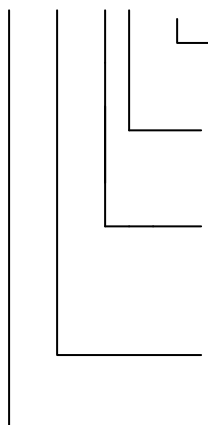
- Hand-Held Instruments
- PCMCIA Cards
- MP3/MP4/MP5 Players
- Portable Information Appliances

### DESCRIPTION

The BL9193 is designed for portable RF and wireless applications with demanding performance and space requirements. The BL9193 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The BL9193 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The BL9193 consumes less than 0.01 $\mu$ A in shutdown mode and has fast turn-on time less than 50 $\mu$ s. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the 5-lead of SC-70, SOT-23 packages.

### ORDERING INFORMATION

BL9193 XX X X X XXX



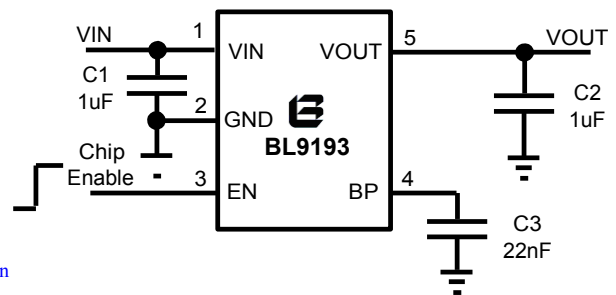
Package:  
 RN: SOT-23-5  
 URN: SC-70-5  
 Features  
 P: Standard (default, lead free)  
 C: Customized

Enable Option:  
 A: active high with internal 8 M $\Omega$  pull down  
 B: active high with external pull down  
 C: active low with internal 2 M $\Omega$  pull up  
 D: active low with external pull up

Output Voltage Accuracy  
 A:  $\pm$ 1%  
 B:  $\pm$ 2%

Output Voltage:  
 12:1.2V 15:1.5V 18:1.8V 25:2.5V  
 28:2.8V 30:3.0V 33:3.3V  
 CT: custom fixed output (50mV step)  
 AD: Adjustable

### TYPICAL APPLICATION



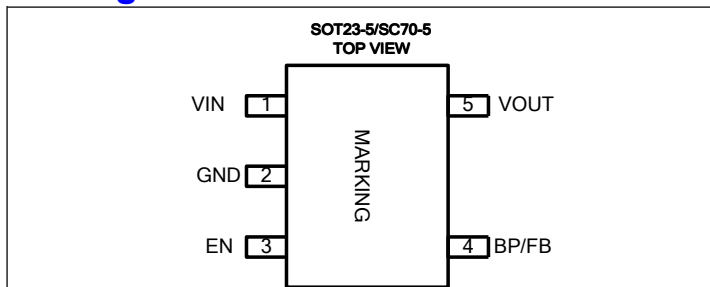
#### Application hints:

Output capacitor ( $C2 \geq 2.2\mu$ F) is recommended in BL9193-1.2V, BL9193-1.5V, BL9193-1.8V application to assure the stability of circuit.

### Absolute Maximum Rating (Note 1)

Input Supply Voltage ( $V_{CC}$ )	-0.3V to +6V	Maximum Junction Temperature	125°C
EN Input Voltage	-0.3V to $V_{in}$	Operating Temperature Range <small>(Note 2)</small>	-40°C to 85°C
Output Voltage	-0.3V to $V_{in}+0.3V$	Storage Temperature Range	-65°C to 125°C
BP Voltage	-0.3V to +6V	Lead Temperature (Soldering, 10s)	300°C
Output Current	300mA		

### Package Information



### Thermal Resistance (Note 4):

Package	$\theta_{JA}$	$\theta_{JC}$
SOT23-5	250°C/W	130°C/W
SC70-5	333°C/W	170°C/W

Part Number	Top Mark	Temp Range
BL9193-12BA	C A Y W <small>(Note 3)</small>	-40°C to +85°C
BL9193-15BA	C B Y W	-40°C to +85°C
BL9193-18BA	C C Y W	-40°C to +85°C
BL9193-25BA	C D Y W	-40°C to +85°C
BL9193-28BB	C E Y W	-40°C to +85°C
BL9193-30BA	C F Y W	-40°C to +85°C
BL9193-33BA	C G Y W	-40°C to +85°C
BL9193-12BB	C H Y W	-40°C to +85°C
BL9193-28BA	C I Y W	-40°C to +85°C
BL9193-ADBA	C J Y W	-40°C to +85°C

Y	4	5	6	...	0	1	...
Year	2014	2015	2016	...	2020	2021	...

W	A	...	Y	Z	a	...	y	z
Week	1	...	25	26	27	...	51	52

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The BL9193 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

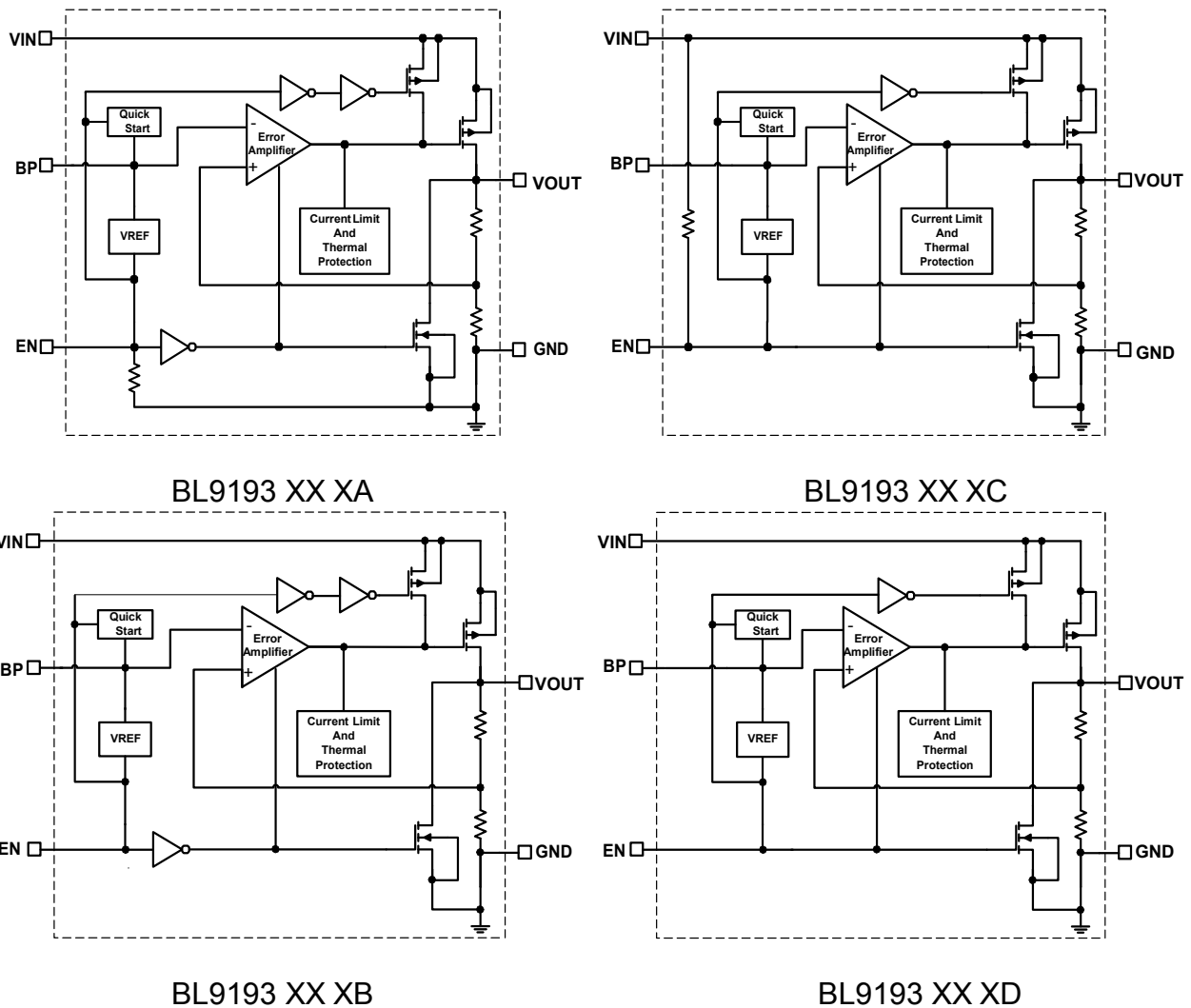
**Note 3:** Y: Year of manufacturing W: Week of manufacturing

**Note 4:** Thermal Resistance is specified with approximately 1 square of 1 ozcopper.

### Pin Description

PIN	NAME	FUNCTION
1	VIN	Power Input Voltage.
2	GND	Ground.
3	EN	Chip Enable Pin with four options. A: active high with internal 8 MΩ pull down B: active high with external pull down C: active low with internal 2 MΩ pull up D: active low with external pull up
4	BP/FB	Reference Noise Bypass. FB pin for adjustable version.
5	VOUT	Output Voltage.

### Block Diagram



### Electrical Characteristics (Note 5)

( $V_{IN}=3.6V$ ,  $EN=V_{IN}$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $C_{BP}=22nF$ ,  $T_A=25^\circ C$ , unless otherwise noted.)

Parameter		Symbol	Conditions	MIN	TYP	MAX	unit
Input Voltage		$V_{IN}$		2		6	V
Output Voltage Accuracy (Note 6)		$\Delta V_{OUT}$	$V_{IN}=3.6V$ , $I_{OUT}=1mA$	-1		+1	%
			$V_{IN}=3.4V$ , $I_{OUT}=300mA$	-2		+2	
Current Limit		$I_{LIM}$	$R_{LOAD}=1\Omega$	400	430		mA
Quiescent Current		$I_Q$	$V_{EN}>1.2V$ , $I_{OUT}=0mA$		90	130	$\mu A$
Dropout Voltage		$V_{DROP}$	$I_{OUT}=200mA$ , $V_{OUT}=2.8V$		130	180	mV
			$I_{OUT}=300mA$ , $V_{OUT}=2.8V$		210	300	
Line Regulation (Note 7)		$\Delta V_{LINE}$	$V_{IN}=3.6V$ to $5.5V$ $I_{OUT}=1mA$		0.05	0.17	%/V
Load Regulation (Note 8)		$\Delta V_{LOAD}$	$1mA < I_{OUT} < 300mA$			2	%/A
Output Voltage Temperature Coefficient (Note 9)		$TC_{V_{OUT}}$	$I_{OUT}=1mA$		$\pm 60$		ppm/ $^\circ C$
Standby Current		$I_{STBY}$	$V_{EN}=GND$ , Shutdown		0.01	1	$\mu A$
EN Input Bias Current		$I_{IBSD}$	$V_{EN}=GND$ or $V_{IN}$		0	100	nA
EN Input Threshold	Logic Low	$V_{IL}$	$V_{IN}=3V$ to $5.5V$ , Shutdown			0.4	V
	Logic High	$V_{IH}$	$V_{IN}=3V$ to $5.5V$ , Start up	1.2			V
Output Noise Voltage		$e_{NO}$	10Hz to 100KHz, $I_{OUT}=200mA$ $C_{OUT}=1\mu F$		100		$\mu V_{RMS}$
Power Supply Rejection Ratio	f=217Hz	PSRR	$C_{out}=1\mu F$ , $I_{out}=100mA$		-80		dB
	f=1KHz				-78		
	f=10KHz				-65		
Thermal Shutdown Temperature		$T_{SD}$	Shutdown, Temp increasing		165		$^\circ C$
Thermal Shutdown Hysteresis		$T_{SDHY}$			30		$^\circ C$

**Note 5:** 100% production test at  $+25^\circ C$ . Specifications over the temperature range are guaranteed by design and characterization.

**Note 6:** This IC includes two kinds of output voltage accuracy versions. A:  $\pm 1\%$ , B:  $\pm 2\%$ .

**Note 7:** Line regulation is calculated by 
$$\Delta V_{LINE} = \left| \frac{V_{OUT1} - V_{OUT2}}{\Delta V_{IN} \times V_{OUT(normal)}} \right| \times 100$$

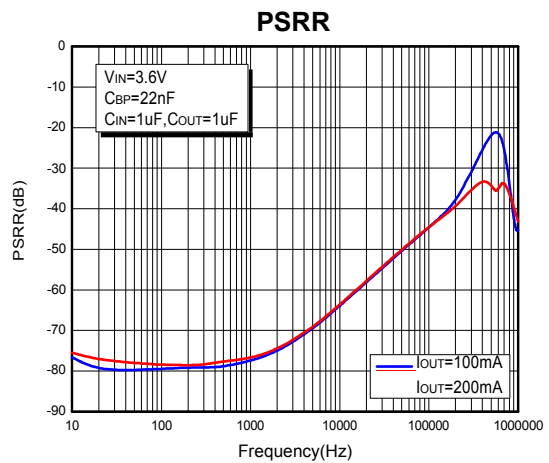
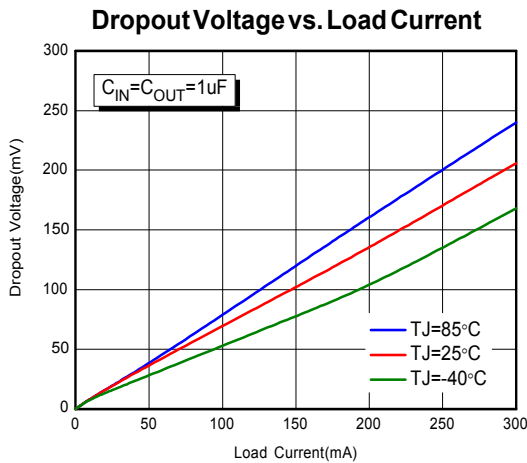
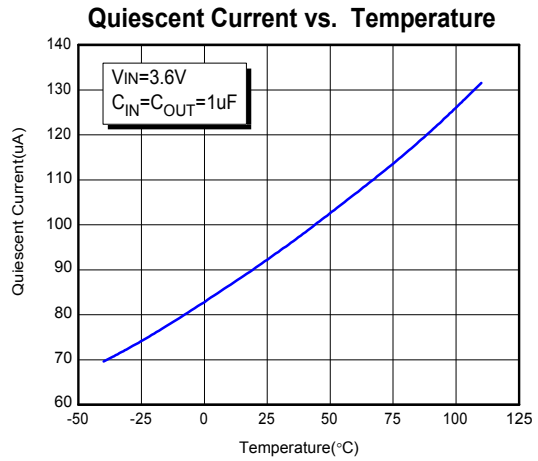
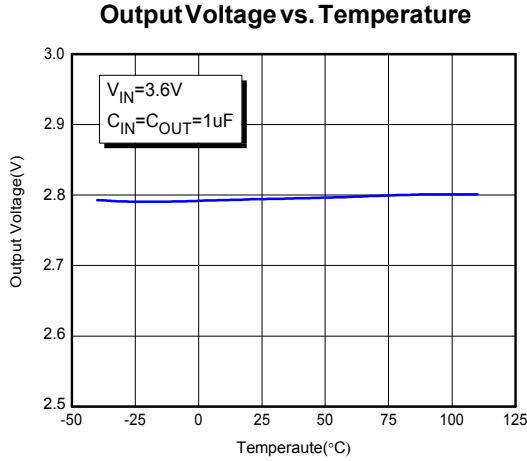
Where  $V_{OUT1}$  is the output voltage when  $V_{IN}=5.5V$ , and  $V_{OUT2}$  is the output voltage when  $V_{IN}=3.6V$ ,  $\Delta V_{IN}=1.9V$ .  $V_{OUT(normal)}=2.8V$ .

**Note 8:** Load regulation is calculated by 
$$\Delta V_{LOAD} = \left| \frac{V_{OUT1} - V_{OUT2}}{\Delta I_{OUT} \times V_{OUT(normal)}} \right| \times 100$$

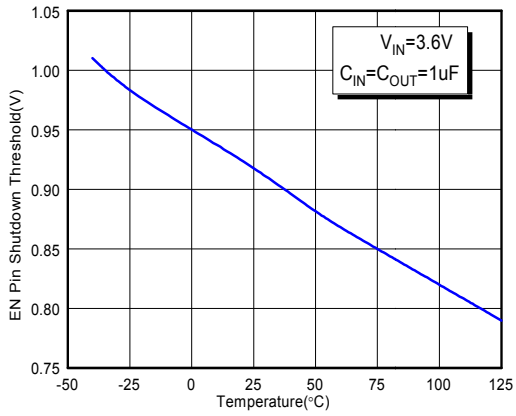
Where  $V_{OUT1}$  is the output voltage when  $I_{OUT}=1mA$ , and  $V_{OUT2}$  is the output voltage when  $I_{OUT}=300mA$ .  $\Delta I_{OUT}=0.299A$ ,  $V_{OUT(normal)}=2.8V$ .

**Note 9:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$

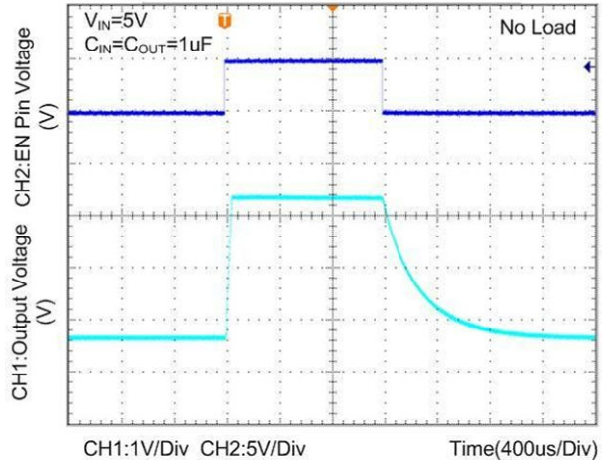
**Typical Performance Characteristics**



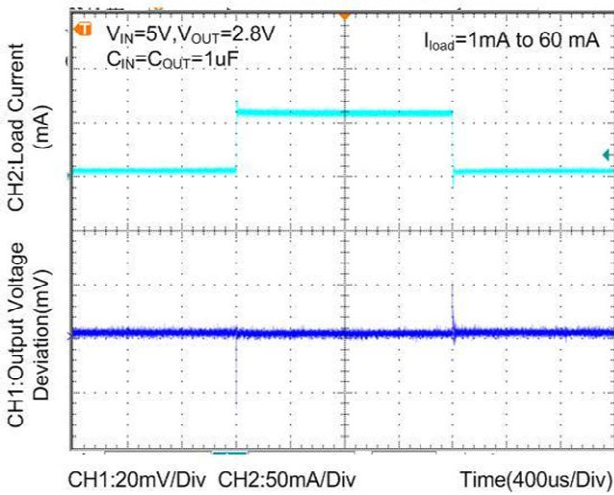
**EN Pin Shutdown Threshold vs. Temperature**



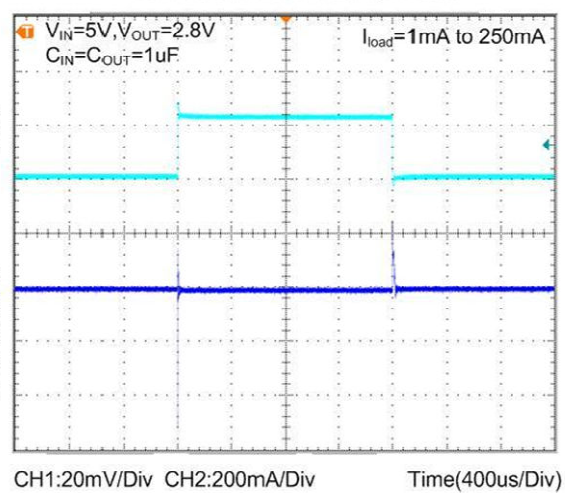
**EN Pin Shutdown Response**



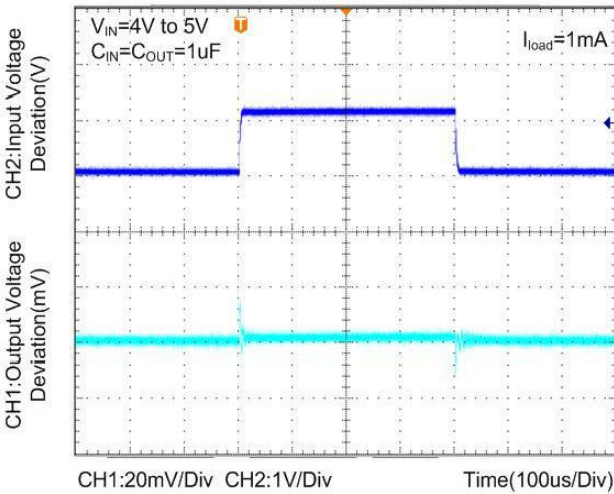
**Load Transient Response**



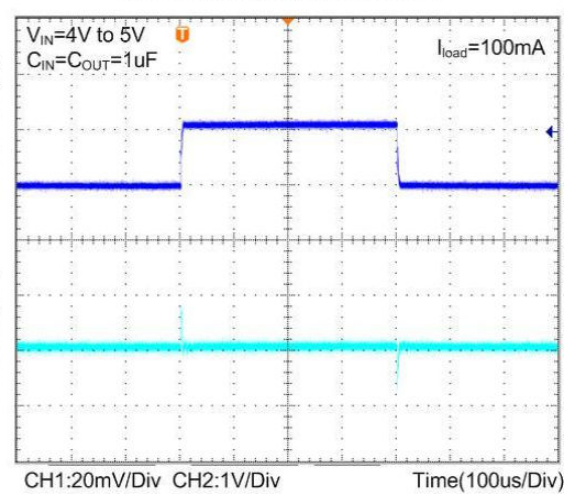
**Load Transient Response**



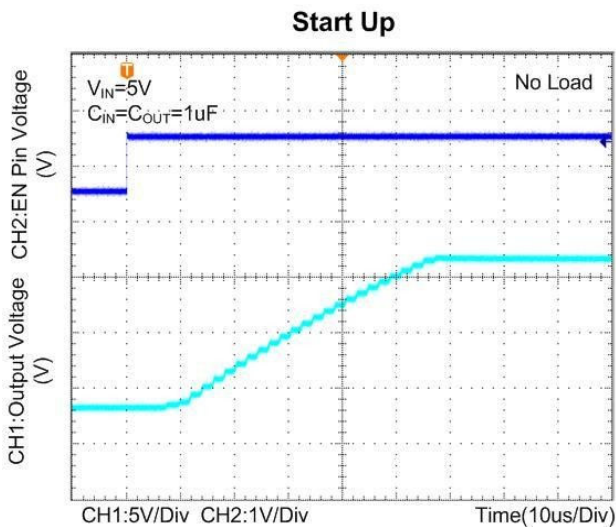
**Line Transient Response**



**Line Transient Response**







## Applications Information

Like any low-dropout regulator, the external capacitors used with the BL9193 must be carefully selected for regulator stability and performance. Using a capacitor whose value is  $> 1\mu F$  on the BL9193 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The BL9193 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least  $1\mu F$  with ESR is  $> 25m\Omega$  on the BL9193 output ensures stability. The BL9193 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of

larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the  $V_{OUT}$  pin of the BL9193 and returned to a clean analog ground.

### Bypass Capacitor and Low Noise

Connecting a  $22nF$  between the BP pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the BP pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the bypass capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

### Enable Function

The BL9193 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on; the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protect the

system, the BL9193 have a quick discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

### Programming the BL9193 Adjustable LDO regulator

The output voltage of the BL9193 adjustable regulator is programmed using an external resistor divider as show in Figure as below. The output voltage is calculated using equation as below:

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right)$$

Where:

$V_{REF}=1.23V$  typ (the internal reference voltage)  
 Resistors R1 and R2 should be chosen for approximately 50uA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decrease/increases  $V_{OUT}$ . The recommended design procedure is to choose  $R2=30.1k\Omega$  to set the divider current at 50uA,  $C1=22pF$  for stability, and then calculate using Equation as below:

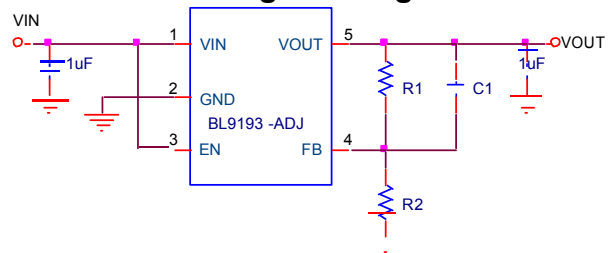
$$R1 = \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. The suggested value of this capacitor for several resistor ratios is shown in the table below.

### OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.8V	13.9 kΩ	30.1 kΩ	22pF
2.5V	31.6 kΩ	30.1 kΩ	22pF
3.3V	51 kΩ	30.1 kΩ	22pF
3.6V	59 kΩ	30.1 kΩ	22pF

### BL9193 Adjustable LDO regulator Programming



### Thermal Considerations

Thermal protection limits power dissipation in BL9193. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 30°C.

For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$$

Where  $T_J(MAX)$  is the maximum operation junction temperature 125°C,  $T_A$  is the



ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of BL9193, where  $T_J(\text{MAX})$  is the maximum junction temperature of the die ( $125^\circ\text{C}$ ) and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance ( $\theta_{JA}$  is layout dependent) for SOT-23-5 package is  $250^\circ\text{C/W}$ , SC-70-5 package is  $333^\circ\text{C/W}$ , on standard JEDEC 51-3 thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

$$P_D(\text{MAX}) = (125^\circ\text{C} - 25^\circ\text{C}) / 333 = 300\text{mW} \quad (\text{SC-70-5})$$

$$P_D(\text{MAX}) = (125^\circ\text{C} - 25^\circ\text{C}) / 250 = 400\text{mW} \quad (\text{SOT-23-5})$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_J(\text{MAX})$  and thermal resistance  $\theta_{JA}$ . It is also useful to calculate the junction of temperature of the BL9193 under a set of

specific conditions. In this example let the

input voltage  $V_{IN} = 3.3\text{V}$ , the output current  $I_O = 300\text{mA}$  and the case temperature

$T_A = 40^\circ\text{C}$  measured by a thermal couple during operation. The power dissipation for the  $V_O = 2.8\text{V}$  version of the BL9193 can be calculated as:

$$P_D = (3.3\text{V} - 2.8\text{V}) \times 300\text{mA} + 3.6\text{V} \times 100\mu\text{A} = 150\text{mW}$$

And the junction temperature,  $T_J$ , can be calculated as follows:

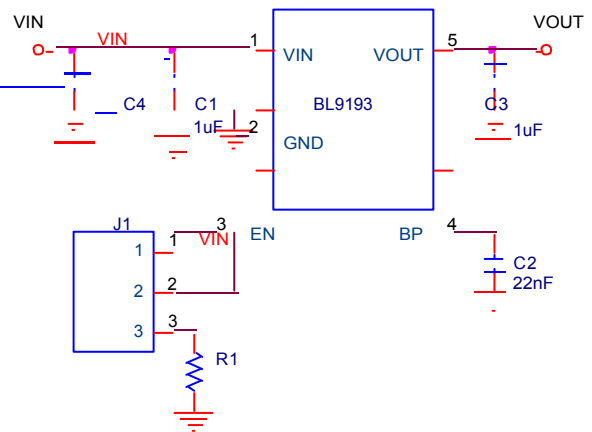
$$T_J = T_A + P_D \times \theta_{JA} = 40^\circ\text{C} + 0.15\text{W} \times 250^\circ\text{C/W} = 40^\circ\text{C} + 37.5^\circ\text{C} = 77.5^\circ\text{C} < T_J(\text{MAX}) = 125^\circ\text{C}$$

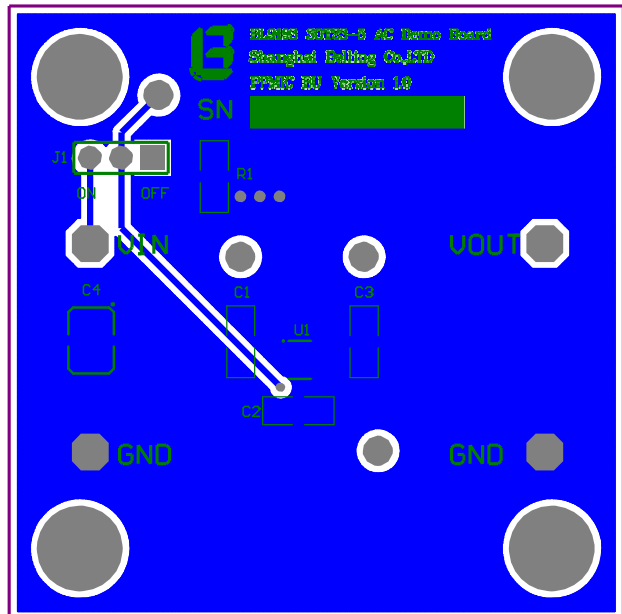
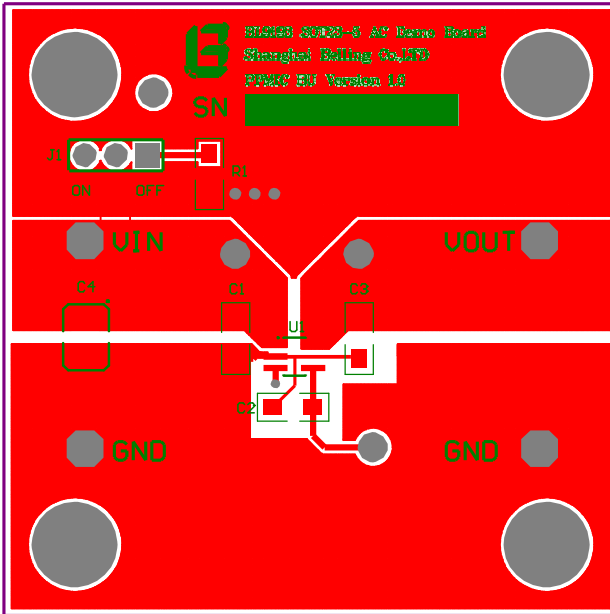
For this operating condition,  $T_J$  is lower than the absolute maximum operating junction temperature,  $125^\circ\text{C}$ , so it is safe to use the BL9193 in this configuration.

### Layout considerations

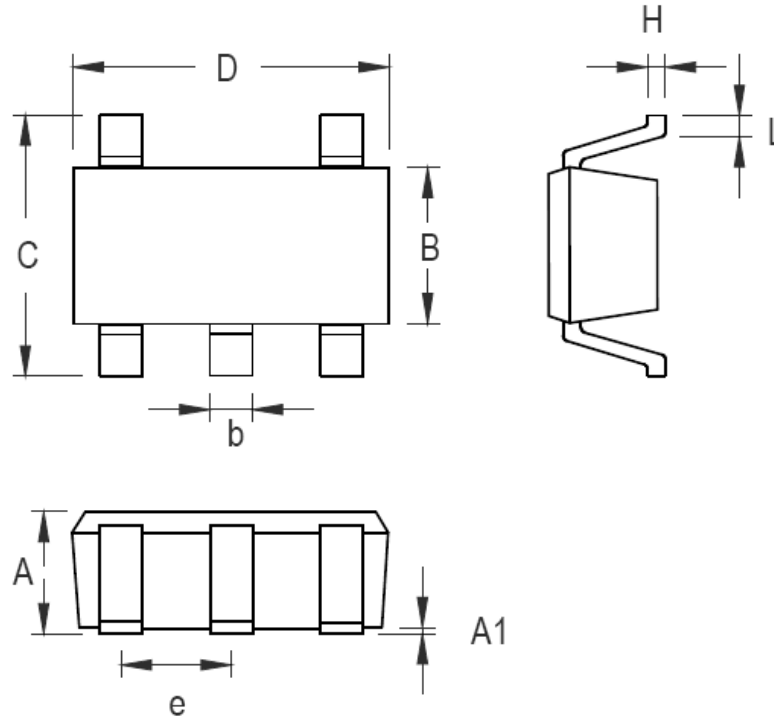
To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

### BL9193-2.8V Layout Circuit





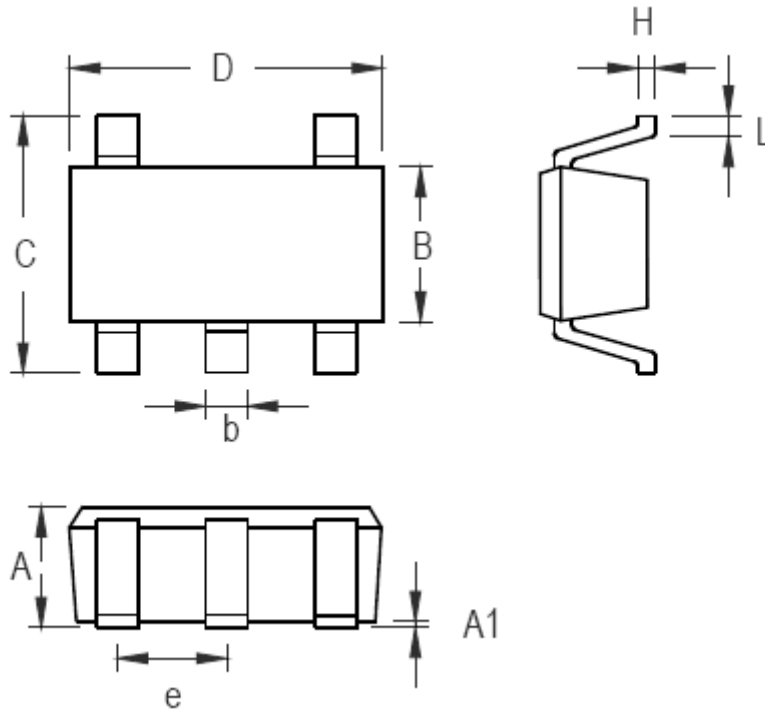
## Package Description



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.044
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.054
b	0.150	0.400	0.006	0.016
C	1.800	2.450	0.071	0.096
D	1.800	2.250	0.071	0.089
e	0.650		0.026	
H	0.080	0.260	0.003	0.010
L	0.210	0.460	0.008	0.018

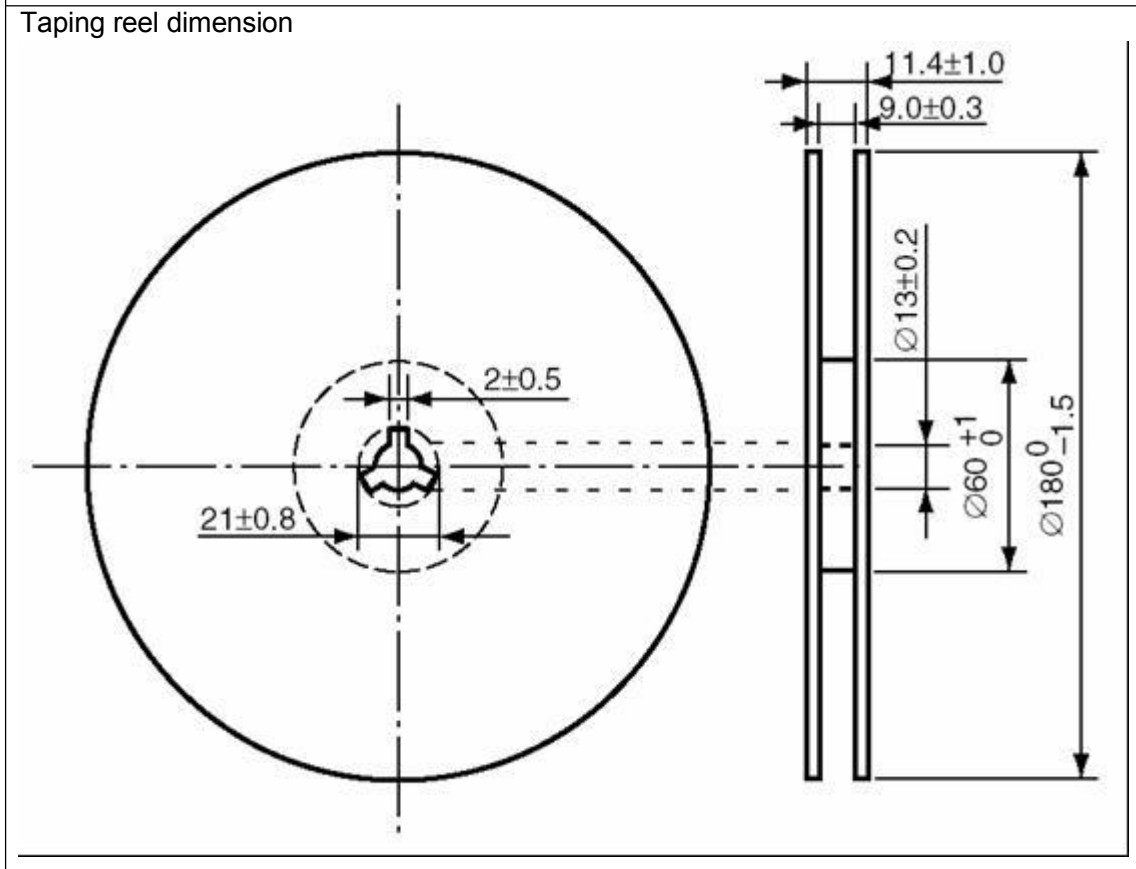
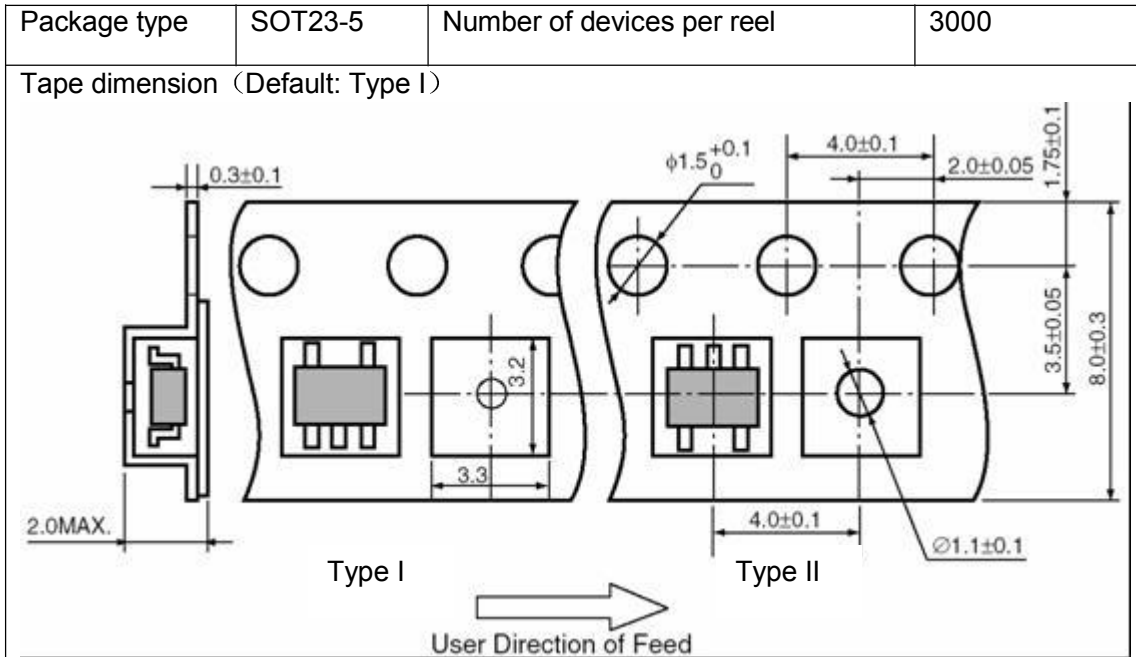
SC-70-5 Surface Mount Package





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package





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