# PCI-PIO

**PCI Digital Input/
Output Card**



# User Manual

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# INTRODUCTION

The PCI-PIO is a PCI-compatible half-card which provides digital input/outputs and counter/timers.

There are 48 TTL-compatible programmable digital input/outputs available from the board.  If the controlling devices are used in handshake mode, the handshake lines are available as interrupt sources.

There are also three programmable counter/timers, the enable and clock inputs being available externally, if required , and the outputs being accessible externally or as interrupt sources.  A 4MHz crystal oscillator is available on board to allow the counter/timers to act as accurate timebases.

All input/output lines are available at an industry standard 50 way D-type plug connector.

One PCI interrupt line may be selectively driven by the seven interrupt sources on the board, the interrupting source being readily identified by the board.

The PCI-PIO is intended to be installed with the minimum of user interaction. The board is configured by the system BIOS and by the application drivers and no on-board links are required to select functionality.

## ABOUT THE MANUAL

This manual is organised into four chapters.  Each chapter covers a different aspect of using the PCI-PIO.  In order to get the best results from the product, the user is urged to read all chapters, paying particular note to Chapter 1 which deals with the initial installation of the card.

**Chapter 1**    Explains how to install the card in your computer.

**Chapter 2**    Details the connections to and from the card.

**Chapter 3**    Gives details of the card's address mapping and internal register details allowing the user to write custom software to control the card.

**Chapter 4**    Presents the card's technical specification.  Use this section to determine the card's suitability for a particular application

This manual describes the complete hardware functionality of the PCI-PIO board.  All the functions may not necessarily be supported by the current release of the NT driver and DLL set.

# CHAPTER 1

## INSTALLING THE PCI-PIO

The card is installed by removing the cover of the host computer and inserting the card into a free PCI slot. The rear panel of the card should then be secured to the rear panel of the host computer with the screw supplied with the computer.

When the computer is switched on, the BIOS will detect the presence of the card and will allocate it with a  base address and an interrupt.  These parameters may then be used to configure application software to access the card.

If the card is to be directly accessed by a user's application, it will be necessary for the application to determine where the BIOS has located the card.

To this end a software function has been provided.   Refer to the "Readme.txt" file on the supplied disk for details.

# CHAPTER 2

# CONNECTION DETAILS

The following table refers to the 50 way D-type plug at the rear of the card.

| PIN | USAGE | PIN | USAGE | PIN | USAGE |
|-----|-------|-----|-------|-----|-------|
| 1 | PIO1 port A, b0 (PAA0) | 18 | PIO1 port C, b1 (PAC1) | 34 | PIO2 port B, b1 (PBB1) or Counter I/O |
| 2 | PIO1 port A, b1 (PAA1) | 19 | PIO1 port C, b2 (PAC2) | 35 | PIO2 port B, b2 (PBB2) or Counter I/O |
| 3 | PIO1 port A, b2 (PAA2) | 20 | PIO1 port C, b3 (PAC3) and/or interrupt source or Counter I/O | 36 | PIO2 port B, b3 (PBB3) |
| 4 | PIO1 port A, b3 (PAA3) | 21 | PIO1 port C, b4 (PAC4) | 37 | PIO2 port B, b4 (PBB4) |
| 5 | PIO1 port A, b4 (PAA4) | 22 | PIO1 port C, b5 (PAC5) | 38 | PIO2 port B, b5 (PBB5) |
| 6 | PIO1 port A, b5 (PAA5) | 23 | PIO1 port C, b6 (PAC6) | 39 | PIO2 port B, b6 (PBB6) |
| 7 | PIO1 port A, b6 (PAA6) | 24 | PIO1 port C, b7 (PAC7) | 40 | PIO2 port B, b7 (PBB7) |
| 8 | PIO1 port A, b7 (PAA7) | 25 | PIO2 port A, b0 (PBA0) | 41 | PIO2 port C, b0 (PBC0) and/or interrupt source or Counter I/O |
| 9 | PIO1 port B, b0 (PAB0) | 26 | PIO2 port A, b1 (PBA1) | 42 | PIO2 port C, b1 (PBC1) |
| 10 | PIO1 port B, b1 (PAB1) | 27 | PIO2 port A, b2 (PBA2) | 43 | PIO2 port C, b2 (PBC2) |
| 11 | PIO1 port B, b2 (PAB2) | 28 | PIO2 port A, b3 (PBA3) | 44 | PIO2 port C, b3 (PBC3) and/or interrupt source or Counter I/O |
| 12 | PIO1 port B, b3 (PAB3) | 29 | PIO2 port A, b4 (PBA4) | 45 | PIO2 port C, b4 (PBC4) |
| 13 | PIO1 port B, b4 (PAB4) | 30 | PIO2 port A, b5 (PBA5) | 46 | PIO2 port C, b5 (PBC5) |
| 14 | PIO1 port B, b5 (PAB5) | 31 | PIO2 port A, b6 (PBA6) | 47 | PIO2 port C, b6 (PBC6) |
| 15 | PIO1 port B, b6 (PAB6) | 32 | PIO2 port A, b7 (PBA7) | 48 | PIO2 port C, b7 (PBC7) |
| 16 | PIO1 port B, b7 (PAB7) | 33 | PIO2 port B, b0 (PBB0) or Counter I/O | 49 | Digital Ground |
| 17 | PIO1 port C, b0 (PAC0) and/or Interrupt source or Counter I/O | | | 50 | Digital Ground |

## Suitable Interface Signal Types

The input and output signals for the PCI-PIO parallel ports and counter/timers are strictly digital TTL levels with voltage limits of zero volts for a logic low and +5 volts for a logic high. Voltages outside these limits may cause damage to the card. The output current drive capability makes the card suitable for connection to TTL logic type circuits. The PCI-PIO is compatible with most types of TTL logic. Because the lines are TTL it is recommended that input signal lines do not exceed 2 metres in length. Operation at longer lengths may cause drive level problems.

Driving conventional relay coils is not recommended without external protection even if the coil current required is less than the PCI-PIO can provide. Relay coils are inductive and as such can generate large flyback voltages when de-energised which will destroy the device outputs.

## CHAPTER 3

## PROGRAMMING DETAILS

This chapter provides details of the cards internal registers.

The board's input/output facilities are provided by two Intel i8255, or NEC μPD71055 PIO devices (compatible with the Intel part) and an Intel i8254, or NEC μPD71054 Counter/timer (compatible with the Intel part).

Each PIO provides 24 programmable digital I/O channels. It is suitable for sensing the presence of, or driving TTL connections only. These connections should be kept as short as possible, less than 2 metres is recommended.

Each PIO appears to the PC as four I/O addressable registers. The first three registers control the I/O ports which can be set as input or output by writing suitable codes to the fourth Control Port.

Three modes of operation are available within the device:-

Mode 0 is for general purpose I/O and allows all three ports to be configured as either inputs or outputs.

Mode 1 is for full duplex parallel communication and allows one port to be configured for inputs, another for outputs and the third as transfer handshake lines and interrupt sources.

Mode 2 is for half duplex parallel data communication, and allows one port to be configured for data transfer I/O, a second as transfer handshake lines and an interrupt source, and the third as a general purpose I/O port (similar to mode 0).

For mode 0, a summary of the codes required to change the operation of the ports are given later. A typical sequence of events to use this feature would be :

- Decide on the mix of input/outputs required and write the appropriate code to the Control Register.

- Read from the selected input port or write to the selected output port.

The 8254 contains three 16-bit Counter/timers each of which has separate clock and enable inputs and an output, all of which are TTL compatible. Connections to these signals should be kept as short as possible, less than 2 metres is recommended.

The 8254 appears to the PC as four ports.  The first three are count registers for the three counter/timers, and the fourth is a Control Register which configures the mode of operation of the three counters.  These are accessed at the addresses shown in the map below.

A summary of the codes required to change the port operations are given later.


## Address Map

The address map for the PCI-PIO occupies a 16-byte block of addresses.

All the following addresses are relative to PCI base address register 2, located at address 18 (hex) in the PCI configuration space.

| ADDRESS | FUNCTION | READ/ WRITE |
|---|---|---|
| Base + 0 | PIO 1, Port A Input/Output Register  (Channel 0 to 7) | R/W |
| Base + 1 | PIO 1, Port B Input/Output Register  (Channel 8 to 15) | R/W |
| Base +2 | PIO 1, Port C Input/Output Register  (Channel 16 to 23) | R/W |
| Base + 3 | PIO 1, Control Register | W |
| Base + 4 | PIO 2, Port A Input/Output Register  (Channel 24 to 31) | R/W |
| Base + 5 | PIO 2, Port B Input/Output Register  (Channel 32 to 39) | R/W |
| Base + 6 | PIO 2, Port C Input/Output Register  (Channel 40 to 47) | R/W |
| Base + 7 | PIO 2, Control Register | W |
| Base + 8 | Counter/timer 0 Count Register | R/W |
| Base + 9 | Counter/timer 1 Count Register | R/W |
| Base + 10 | Counter/timer 2 Count Register | R/W |
| Base + 11 | Counter/timer Control Register | W |
| Base + 12 | Interrupt enable register | R/W |
| Base + 13 | Interrupt status register | R |
| Base + 14 | Counter control register A | R/W |
| Base + 15 | Counter control register B | R/W |

The i8255 / μPD71055 PIO and i8254 / μPD71054 Counter/timer ICs are complex devices. For full details on how to program these devices, refer to the manufacturer's data sheets. Presented here is a brief summary of the main features of each.

## i8255 / μPD71055 PIO

The PIO chip can operate in one of three modes.

The first (Mode 0) provides for simple inputs and outputs for three, 8-bit ports. Data is written to or read from a specified port (A, B, or C) without the use of handshaking. The following table gives a summary of the most commonly used control words which must be written to the control port to configure the i8255 / μPD71055 I/O ports in Mode 0.

| CONTROL WORD (hex) | CONTROL WORD (decimal) | SET ALL of PORT A as | SET ALL of PORT B as | SET HIGH 4 BITS of C as | SET LOW 4 BITS of C as |
|---|---|---|---|---|---|
| 80 | 128 | Output | Output | Output | Output |
| 81 | 129 | Output | Output | Output | Input |
| 82 | 130 | Output | Input | Output | Output |
| 83 | 131 | Output | Input | Output | Input |
| 88 | 136 | Output | Output | Input | Output |
| 89 | 137 | Output | Output | Input | Input |
| 8A | 138 | Output | Input | Input | Output |
| 8B | 139 | Output | Input | Input | Input |
| 90 | 144 | Input | Output | Output | Output |
| 91 | 145 | Input | Output | Output | Input |
| 92 | 146 | Input | Input | Output | Output |
| 93 | 147 | Input | Input | Output | Input |
| 98 | 152 | Input | Output | Input | Output |
| 99 | 153 | Input | Output | Input | Input |
| 9A | 154 | Input | Input | Input | Output |
| 9B | 155 | Input | Input | Input | Input |

Mode 1 enables the transfer of data to or from a specified 8 bit port (A or B) in conjunction with strobes or handshaking signals on port C. These handshaking signals may be used to drive interrupt channels if required.

In Mode 2, data is transferred via one bi-directional 8 bit port (A) with handshaking (port C). These handshaking signals may be used to drive interrupt channels if required.

Refer to the i8255 or µPD71055 data sheet for full details of the settings and use of Modes 1 and 2.

## i8254 / µPD71054 Counter / Timer

The counter/timer circuit contains three independent 16-bit counters which may be operated in a variety of modes. There are five basic modes of operation with each mode providing a different output signal. Presented here is a brief summary of some of the modes possible by programming the counter / timer's internal registers.

All three counter/timers may be operated independently, with separate clocks and enable controls.

Counter 0, Counter 1 and Counter 2 may be connected in series. Counter 0 output to Counter 1 clock input and/or Counter 1 output to Counter 2 clock input, to allow the facility of generating very long delay periods.

The outputs from any counter/timer may be configured to generate an interrupt when going high or low, and may also be made accessible on the back panel connector.

The clock and enable inputs of the counter/timers may also be made accessible on the back panel connector.

## Counter / Timer Modes

The following modes of operation exist by programming the control register within the i8254 / µPD71054. N.B. The interrupts may be generated when the Counter/timer outputs go low or high, selected by bits in the counter control registers.

## Mode 0

When programmed, the output pin will go LOW. When the counter decrements from the value loaded into the count registers to zero, the output pin will go HIGH. It will remain high until the count is re-programmed into the count registers.

## Mode 1

When the count registers are programmed the output pin will be HIGH. When a LOW going signal is applied to the gate input, the count starts and the output will fall LOW, returning HIGH at the end of the count.

## Mode 2

This mode operates as a frequency divider. When programmed the output pin is HIGH. When the count decrements to a value of 1 the output pin will go LOW for ONE clock cycle only and then return HIGH. This cycle repeats continuously without the need to re-program the count value.

## Mode 3

When programmed the output pin will toggle each time the count register decrements to its base level from the value programmed into it. If the count value loaded is an odd number then the counter will reach zero before the output pin toggles. This mode therefore acts as a frequency divider with an approximate 1:1 mark-space ratio.

## Mode 4

This mode is similar to mode 2 but the output pin pulses when the count reaches zero instead of 1.

## Mode 5

This mode is similar to mode 4 except that the count sequence is triggered by the gate line.

## Counter Control

The control and output lines of the counter/timer may be accessed on the rear panel connector by sacrificing some of the digital I/O lines.

The clock inputs of the i8254 counter/timer are selected using the Counter Input Select Register A at Base + E (Hex), as shown below:-

| Counter Input Select Register A (Base + E) | | |
|---|---|---|
| **Bit no.** | **Function** | |
| b7 | Enable counter outputs such that | PBB0 = Counter 2 output<br>PBB1 = Counter 0 output<br>PBB2 = Counter 1 output |
| b6 | Counter 0 interrupt level:- | 0 = Interrupt on counter out low<br>1 = Interrupt on counter out high |
| b5..b4 | Counter 2 clock source:- | 00 = 4 MHz oscillator<br>01 = PBB2 port line<br>10 = Counter 1 output<br>11 = PBC0 port line |
| b3..b2 | Counter 1 clock source:- | 00 = 4 MHz oscillator<br>01 = PBB1 port line<br>10 = Counter 0 output<br>11 = PAC3 port line |
| b1..b0 | Counter 0 clock source:- | 00 = 4 MHz oscillator<br>01 = PBB0 port line<br>10 = Counter 2 output<br>11 = PAC0 port line |

If Bit b7 in the counter control register is set, then the counter outputs are enabled onto port lines PBB0, PBB1 & PBB2, which connect to the 50 way D-type connector.  Consequently this port must be set as an input in the relevant 71055 device to avoid contention.   This same condition applies to any port line which is used for a counter/timer function.

The enable inputs of the i8254 counter are selected using the Counter Input Select Register B at Base + F (Hex), as shown below:-

| Counter Input Select Register B (Base + F) | |
|---|---|
| **Bit no.** | **Function** |
| b7 | Counter 2 interrupt level:-      0 = Interrupt on counter out low<br>1 = Interrupt on counter out high |
| b6 | Counter 1 interrupt level:-      0 = Interrupt on counter out low<br>1 = Interrupt on counter out high |
| b5..b4 | Counter 2 enable source:-      00 = Permanently enabled<br>01 = PBB1 port line<br>10 = PBC0 port line<br>11 = PBC3 port line |
| b3..b2 | Counter 1 enable source:-      00 = Permanently enabled<br>01 = PBB0 port line<br>10 = PAC3 port line<br>11 = PBC0 port line |
| b1..b0 | Counter 0 enable source:-      00 = Permanently enabled<br>01 = PBB2 port line<br>10 = PAC0 port line<br>11 = PAC3 port line |

Notice that it is possible by judicious setting of Counter Input Registers A and B, to set each timer/counter to operate with an external count input, enable and counter output if required.  For example it is possible to set Counter 0 to use PBB0 as a count input, PBB2 as an  enable input, and PBB1 as a count output. Other combinations are possible, but because of the flexibility which is permitted, care must be exercised to avoid conflicting uses of the same port lines.

## Interrupt Selection

A total of seven sources of interrupt are available from the two PIO devices and the counter/timers.  These interrupts are summarised below:-

- INT1 (AC0) is available when PIO1 is operating in mode 1.  It provides a Read Request interrupt for input operations or a Write Request interrupt for output operations on PIO1 port A (PAA[0:7]).

- INT2 (AC3) is available when PIO1 is operating in mode 1.  It provides a Read Request interrupt for input operations or a Write Request interrupt for output operations on PIO1 port B (PAB[0:7]).

- INT3 (BC0) is available when PIO2 is operating in mode 1.  It provides a Read Request interrupt for input operations or a Write Request interrupt for output operations on PIO2 port A (PBA[0:7]).

- INT4 (BC3) is available when PIO2 is operating in mode 1.  It provides a Read Request interrupt for input operations or a Write Request interrupt for output operations on PIO2 port B (PBB[0:7]).

- INT5 is the output from Counter/timer 0, and may be used to generate interrupts on timed events.

- INT6 is the output from Counter/timer 1, and may be used to generate interrupts on timed events.

- INT7 is the output from Counter/timer 2, and may be used to generate interrupts on timed events.

The use of interrupts is not essential but greatly enhances the functionality of the card.

To enable the generation of an interrupt or a combination of interrupts, an
enable word must be written to the Interrupt Enable Register at Base + C (Hex),
as shown below:-

| Interrupt Enable Register (Base + C) | | |
|---|---|---|
| **Bit no.** | **Function** | |
| b7 | Not used | |
| b6 | Counter/timer 2 interrupt control | (1 = Enable, 0 = Disable) |
| b5 | Counter/timer 1 interrupt control | (1 = Enable, 0 = Disable) |
| b4 | Counter/timer 0 interrupt control | (1 = Enable, 0 = Disable) |
| b3 | Port BC3 interrupt control | (1 = Enable, 0 = Disable) |
| b2 | Port BC0 interrupt control | (1 = Enable, 0 = Disable) |
| b1 | Port AC3 interrupt control | (1 = Enable, 0 = Disable) |
| b0 | Port AC0 interrupt control | (1 = Enable, 0 = Disable) |

When an interrupt is recognised by the processor, the source or sources of
interrupt may be read from the Interrupt Status Register at Base + D (Hex), as
shown below:-

| Interrupt Status Register (Base + D) | |
|---|---|
| **Bit no.** | **Function** |
| b7 | Not used |
| b6 | Counter/timer 2 interrupt occurred |
| b5 | Counter/timer 1 interrupt occurred |
| b4 | Counter/timer 0 interrupt occurred |
| b3 | Port BC3 interrupt control occurred |
| b2 | Port BC0 interrupt control occurred |
| b1 | Port AC3 interrupt control occurred |
| b0 | Port AC0 interrupt control occurred |

Having serviced an interrupt, the source may be cleared by momentarily
clearing the relevant bit in the Interrupt Enable Register.

# CHAPTER 4

## TECHNICAL SPECIFICATIONS

Number Of I/O Channels:    48 arranged as 2 x 3 x 8 I/O bits

Signal Levels:    5 Volt TTL Logic Levels

Outputs:
    Logic Low Level:    0 Volts (min.) - 0.4 Volts (max.) @ $I_{OL}$ = 2.5mA
    Logic High Level:    3.5 Volts (min.) - 5 Volts (max.) @ $I_{OH}$ = -400μA

    Drive Current:    2.5 mA. (Logic Low)  Vout = 0.4 Volts
                             -400 μA (Logic High)  Vout = 3.5 Volts

Input Loading:    -10 μA (Logic Low)
                         +10 μA (Logic High)

Counter/timers:    3 x 16 Bit.
                         Counter/timers 0,1 and 2 may be cascaded to
                         provide a single 48 bit Counter/timer.
                         All Counter/timers may be clocked externally at a
                         maximum rate of 4 MHz.

On board Oscillator:    Frequency 4MHz.
                         Stability ñ 100ppm 0 - 70øC

Interrupt Sources:    Register selectable to 3 Counter/timer outputs, and
                         4 PIO handshake control lines.

Interrupt Levels Supported:  All PCI interrupts

Address Overhead:    16 contiguous addresses in 16 byte block

Board Power Requirement:  +5 Volts, 1.2 W maximum

| | |
|---|---|
| Signal Connections: | 1 x 50 way male 'D-type' plug |
| Dimensions: | 125 (L) x 91 (H) board only<br>135 (L) x 122 (H) x 22 (W) including bracket |

## Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in our standard industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements of EN55022:1995 for a Class A product subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for an industrial environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.

- Most EMC problems are caused by the external cabling to boards. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple "pig-tail". Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC.

- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

- Cables which connect externally to boards at TTL levels should not exceed two metres in length.

Failure to observe these recommendations may invalidate the EMC compliance.

| |
|---|
| Warning<br>This is a Class A product.  In a domestic environment this product may cause radio-interference in which case the user may be required to take adequate measures. |

### EMC Specification

A suitably compliant industrial PC fitted with this card meets the following specification:

| | | |
|---|---|---|
| Emissions | EN 55022:1995 | |
| | Radiated | Class A |
| | Conducted | Class A & B |
| | | |
| Immunity | EN 50082-2:1995 incorporating: | |
| | Electrostatic Discharge | EN 61000-4-2 |
| | | Performance Criteria B |
| | Radio Frequency Susceptibility | ENV50140 |
| | | ENV50204 |
| | | Performance Criteria A |
| | Fast Burst Transients | EN 61000-4-4 |
| | | Performance Criteria B |

# PCB LAYOUT DIAGRAM
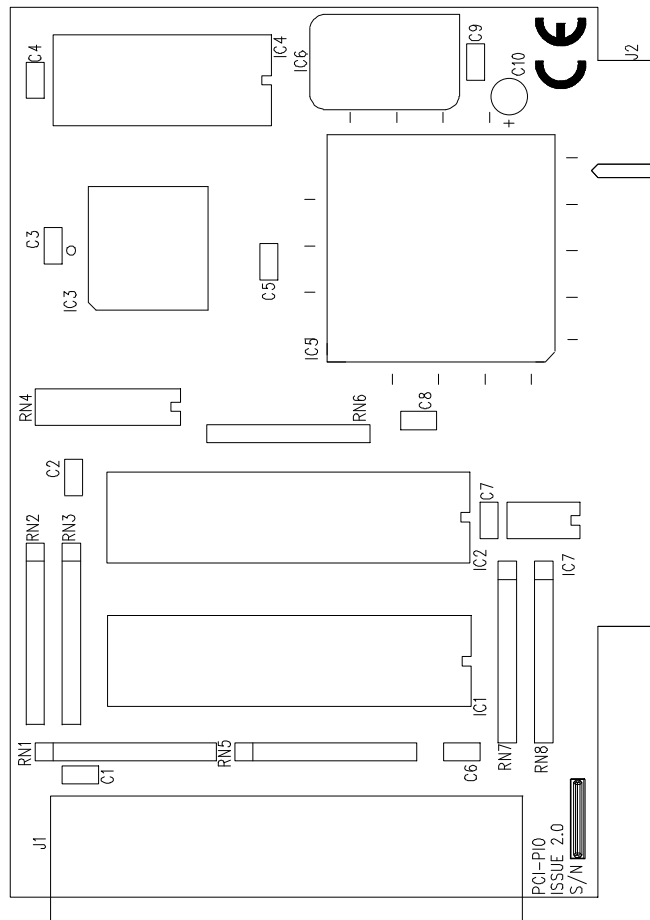
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