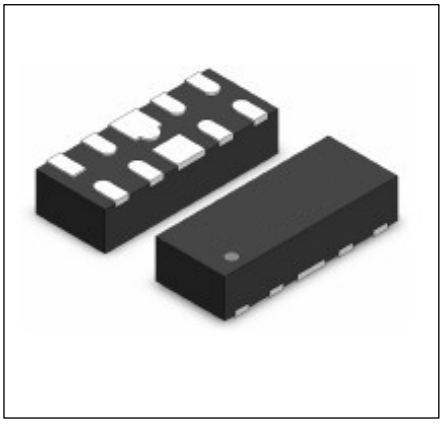
Features

- Solid-state silicon-avalanche technology
- Low operating and clamping voltage
- Up to four I/O Lines of Protection
- Ultra low capacitance: 0.35pF typical(I/O to I/O)
- Low Leakage
- Low operating voltage:5V
- Flow-Through design



IEC COMPATIBILITY (EN61000-4)

- **IEC 61000-4-2 (ESD) ±15kV (air), ± 8kV (contact)**
- **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- **IEC 61000-4-5 (Lightning) 3A (8/20μs)**

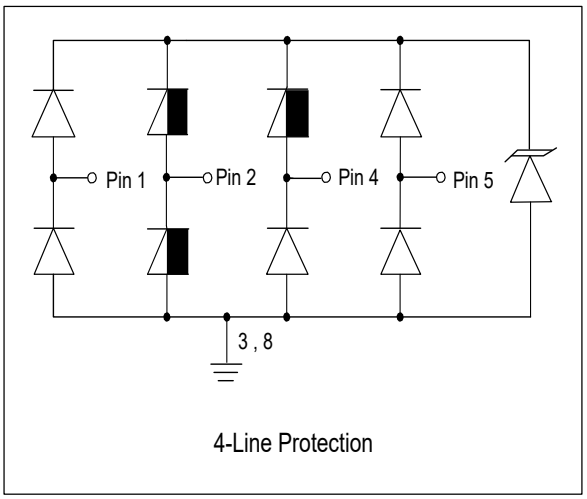
Mechanical Characteristics

- DFN-10L package (2.5×1.0×0.58mm)
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS/WEEE Compliant

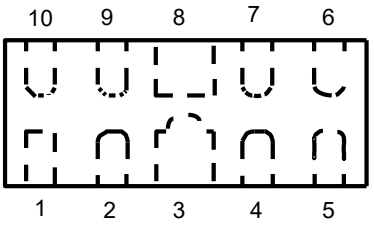
Application

- Digital Visual Interface(DVI)
- MDDI Ports
- DisplayPortTM Interface
- PCI Express
- High Definition Multi-Media Interface(HDMI)
- eSATA Interfaces

Circuit Diagram



Schematic & PIN Configuration



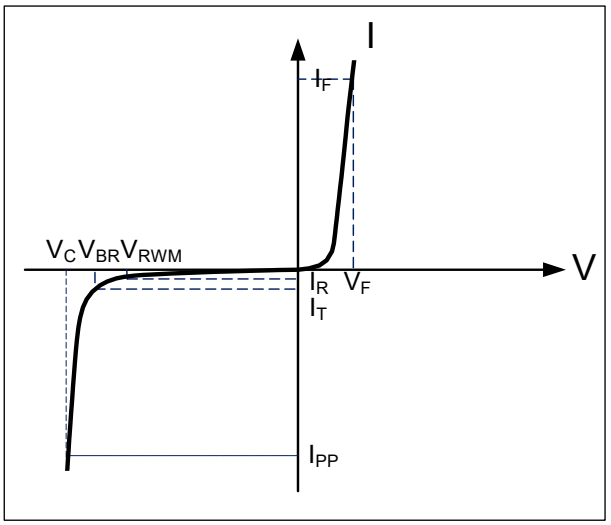
Pin	Identificaion
1,2,4,5	Input Lines
6,7,9,10	Output Lines (No Internal Connection)
3,8	Ground

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p =8/20μs)	P_{PP}	100	Watts
Peak Pulse Current (t_p =8/20μs)	I_{pp}	5	A
ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2(contact)	V_{ESD}	+/-15 +/-8	kV
Operating Temperature	T_J	-55 to + 125	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Electrical Parameters (T=25℃)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F

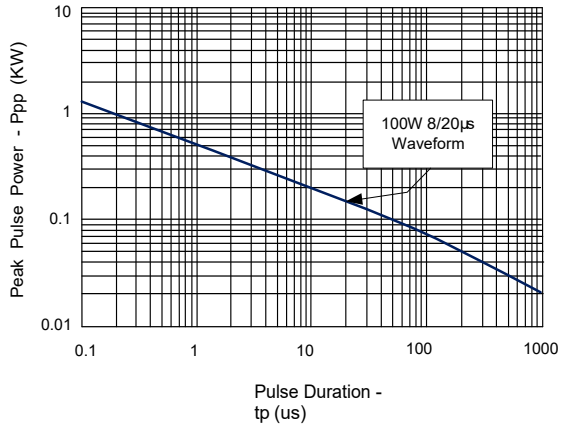


Electrical Characteristics

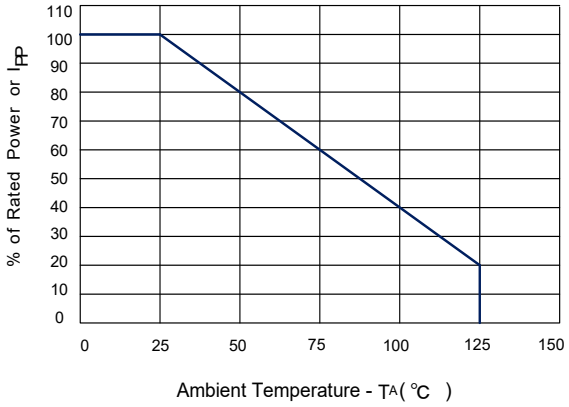
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to ground			5.0	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Any I/O pin to ground	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25℃ Any I/O pin to ground			1	μA
Clamping Voltage	Vc	I_{pp}=3A, t_p=8/20μs Any I/O pin to ground			20	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz I/O pin to GND			0.7	pF
		V_R = 0V, f = 1MHz Between I/O pins		0.35	0.5	pF

Typical Characteristics

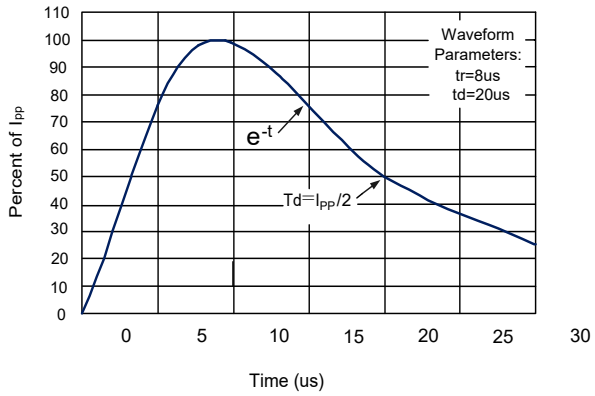
Non-Repetitive Peak Pulse Power vs. Pulse Time



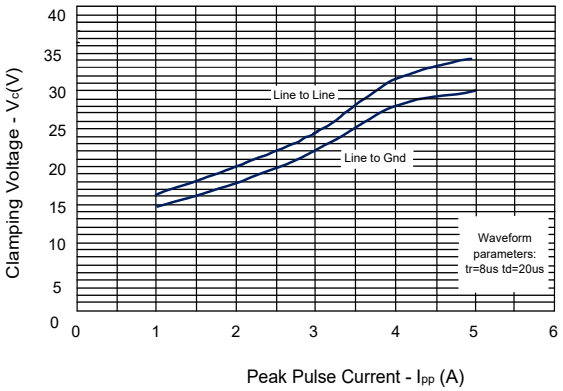
Power Derating curve



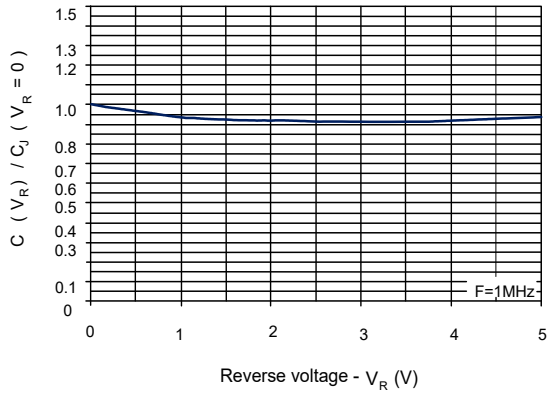
Pulse Waveform



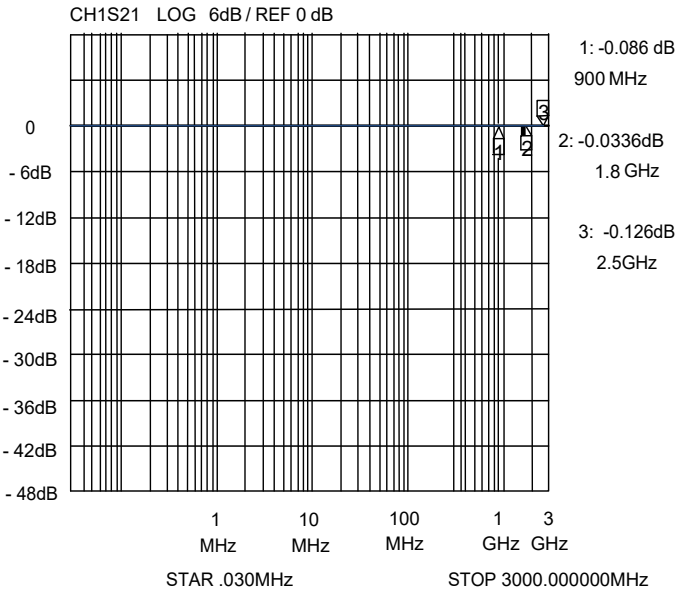
Clamping Voltage vs.Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage



Insertion Loss S21 - I/O to GND



Design Recommendations for HDMI protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance. Furthermore, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The B0524P are specifically designed for protection of high-speed interfaces such as HDMI.

They present <0.5pF capacitance between the pairs while being rated to handle ±8kV ESD contact discharges (±15kV air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the B0524P . The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads. The same layout rules apply for the B0524P

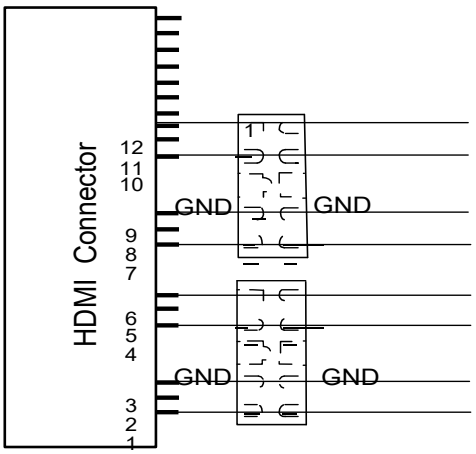


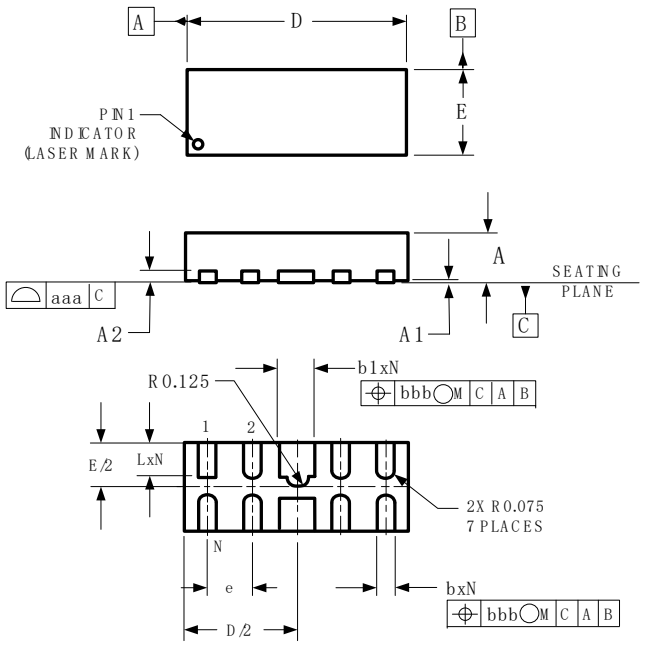
Figure 1.Flow though layout Using B0524P

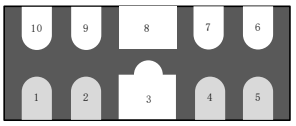
Design Recommendations for HDMI Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible.This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible.
  Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.

Outline Drawing – DFN-2L



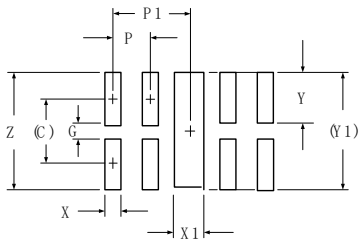


DFN2.5x1-10L

DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	.023	.026	0.50	0.58	0.65
A1	0.00	.001	.002	0.00	0.03	0.05
A2		(0.005)			(0.13)	
b	.006	.008	.010	0.15	0.20	0.25
b1	.014	.016	.018	0.35	0.40	0.45
D	.094	.098	.102	2.40	2.50	2.60
E	.035	.039	.043	0.90	1.00	1.10
e		.020 BSC			0.50 BSC	
L	.012	.015	.017	0.30	0.38	0.425
N		8			8	
aaa		0.003			0.08	
bbb		0.004			0.10	

NOTES:

1.CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.875)
G	.008	0.20
P	.020	0.50
P1	.039	1.00
X	.008	0.20
X1	.016	0.40
Y	.027	0.675
Y1	(.061)	(1.55)
Z	.061	1.55

NOTES:

1.CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING TO ENSURE YOUR COMPANYS MANNUFACTURING GUIDELINES ARE MET.

Marking Codes

Part Number	Marking Code
B0524P	0524P

Package Information

Qty：3k/Reel

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