ULN2803A

Darlington Transistor Arrays

1 Features

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic

2 Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers
- Stepper Motors
- IP Camera
- HVAC Valve and LED Dot Matrix

3 Description

The ULN2803A device is a 50 V, 500 mA Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

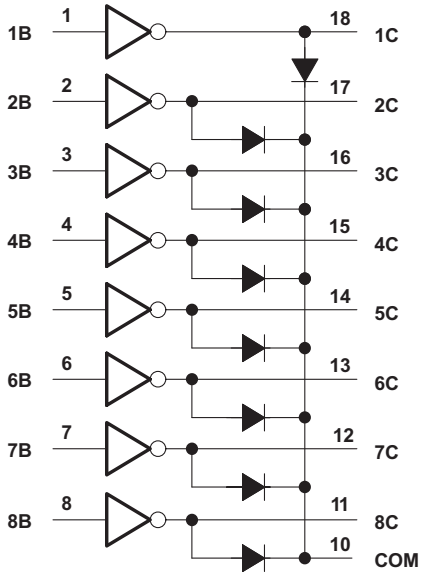
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A device has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULN2803A	SOP (18)	11.55 mm × 7.50 mm
ULN2803AQ	QFN4x4 (20)	4.0 mm × 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2015) to Revision H **Page**

- Deleted obsolete orderable ULN2803AN and removed all references to N package ... 1
- Added Storage temperature, T_{stg} in *Absolute Maximum Ratings* ... 4
- Deleted V_I from *Recommended Operating Conditions* ... 4
- Added Ambient temperature, T_A in *Recommended Operating Conditions* ... 4
- Changed coil supply voltage specifications in *Design Parameters* ... 11
- Added *Receiving Notification of Documentation Updates* section and *Community Resources* section ... 13

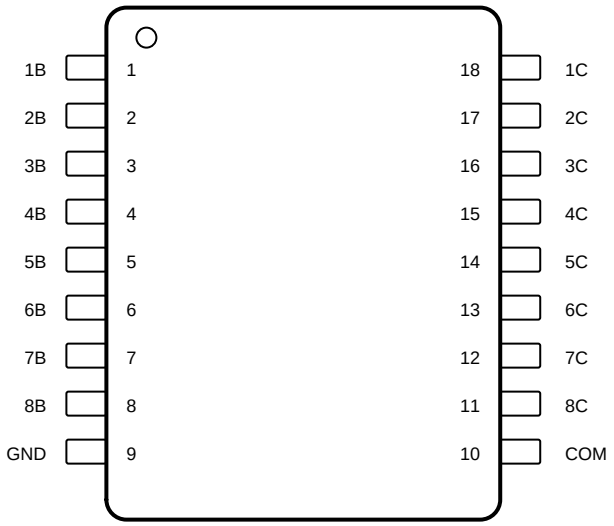
Changes from Revision F (January 2014) to Revision G **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision E (July 2006) to Revision F **Page**

5 Pin Configuration and Functions

DW Package
18-Pin SOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 8 Darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
8B	8		
1C	18	O	Channel 1 through 8 Darlington collector output
2C	17		
3C	16		
4C	15		
5C	14		
6C	13		
7C	12		
8C	11		
GND	9	—	Common emitter shared by all channels (typically tied to ground)
COM	10	I/O	Common cathode node for flyback diodes (required for inductive loads)

6 Specifications

6.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage		50	V
V_I	Input voltage(2)		30	V
	Peak collector current		500	mA
I(clamp)	Output clamp current		500	mA
	Total substrate-terminal current		–2.5	A
T_J	Junction temperature	–65	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage	0	50	V
T_A	Ambient temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		ULN2803A DW (SOP) 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		ULN2803A			UNIT
				MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, see Figure 3	I_I = 0			50	µA
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA, see Figure 4	50	65		µA
$I_{I(on)}$	Input current	V_I = 3.85 V,	See Figure 5		0.93	1.35	mA
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see Figure 6	I_C = 200 mA			2.4	V
			I_C = 250 mA			2.7	
			I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, see Figure 7	I_C = 100 mA		0.9	1.1	V
		I_I = 350 µA, see Figure 7	I_C = 200 mA		1	1.3	
		I_I = 500 µA, see Figure 7	I_C = 350 mA		1.3	1.6	
I_R	Clamp diode reverse current	V_R = 50 V,	see Figure 8			50	µA
V_F	Clamp diode forward voltage	I_F = 350 mA	see Figure 9		1.7	2	V
C_i	Input capacitance	V_I = 0,	f = 1 MHz		15	25	pF

6.6 Switching Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω, See Figure 10		130		ns
t_{PHL}	Propagation delay time, high- to low-level output			20		
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, see Figure 11	V_S – 20			mV

6.7 Typical Characteristics

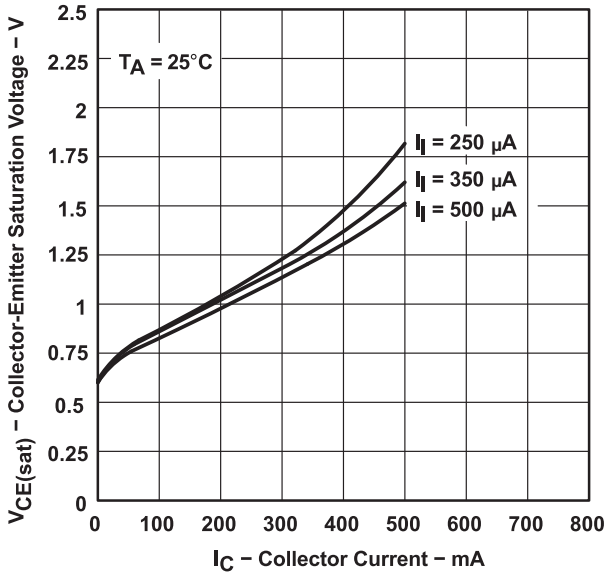


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

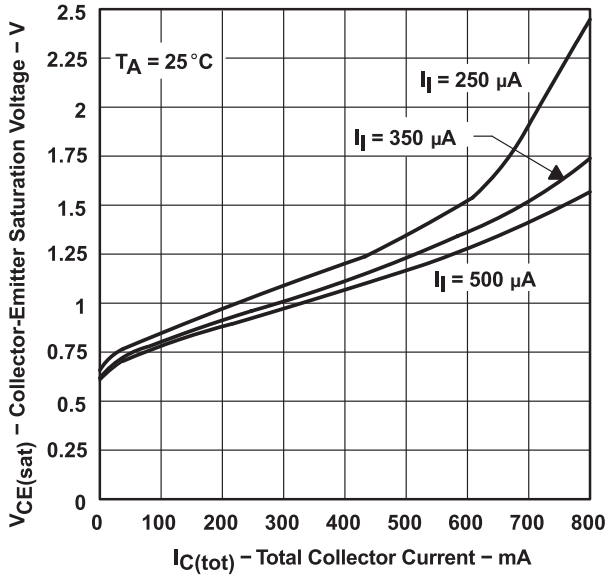


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

7 Parameter Measurement Information

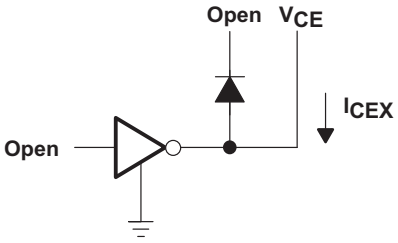


Figure 3. I_{CEX} Test Circuit

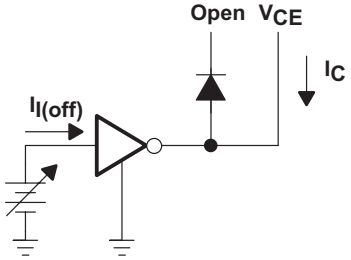


Figure 4. $I_{I(off)}$ Test Circuit

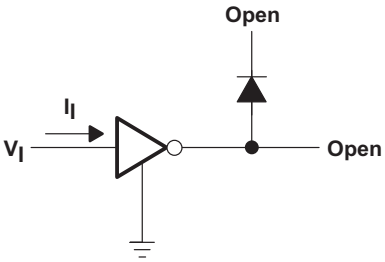


Figure 5. $I_{I(on)}$ Test Circuit

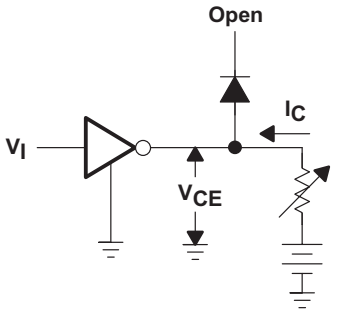


Figure 6. $V_{I(on)}$ Test Circuit

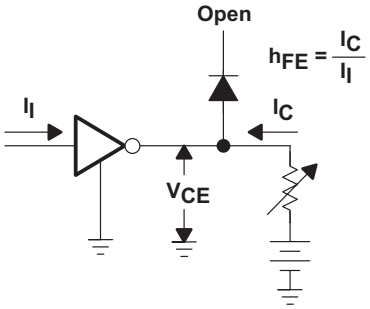


Figure 7. h_{FE}, $V_{CE(sat)}$ Test Circuit

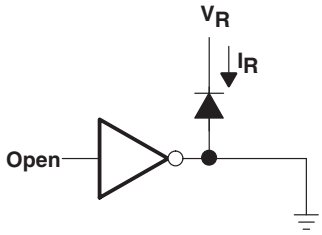


Figure 8. I_R Test Circuit

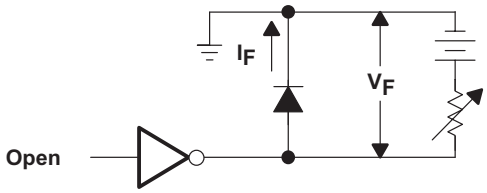
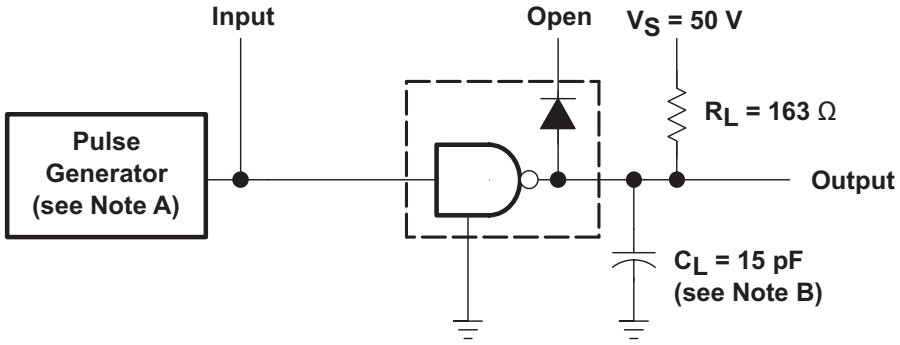
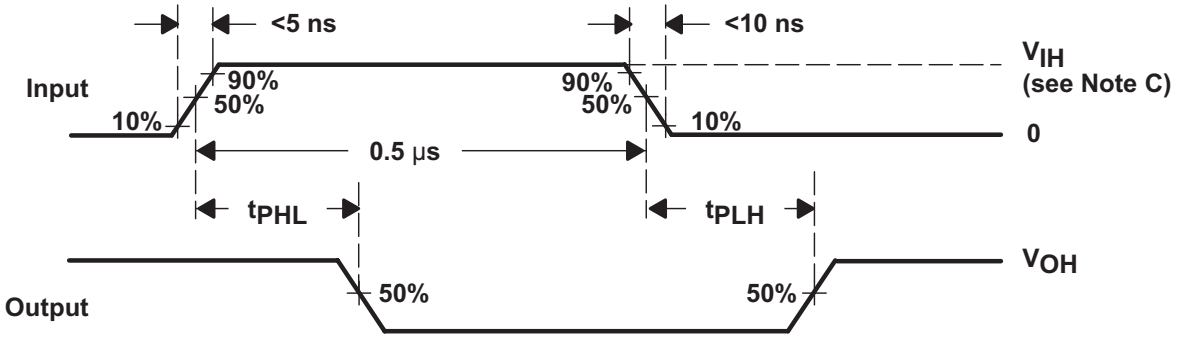


Figure 9. V_F Test Circuit

Parameter Measurement Information (continued)



Test Circuit



Voltage Waveforms

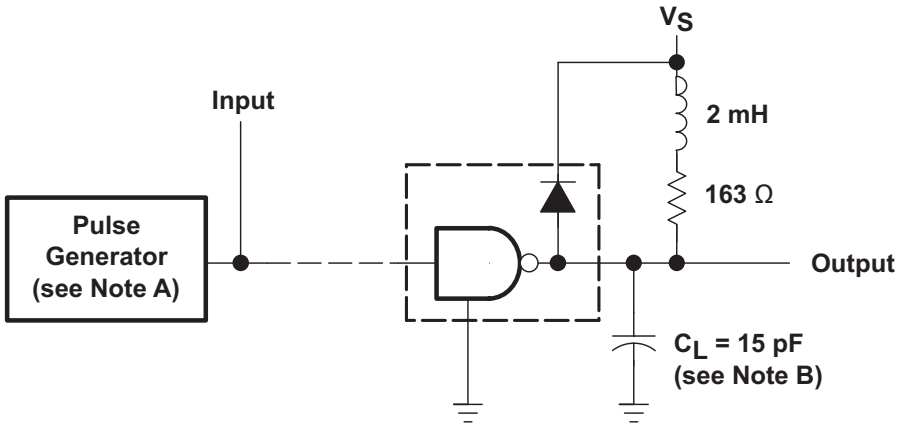
A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

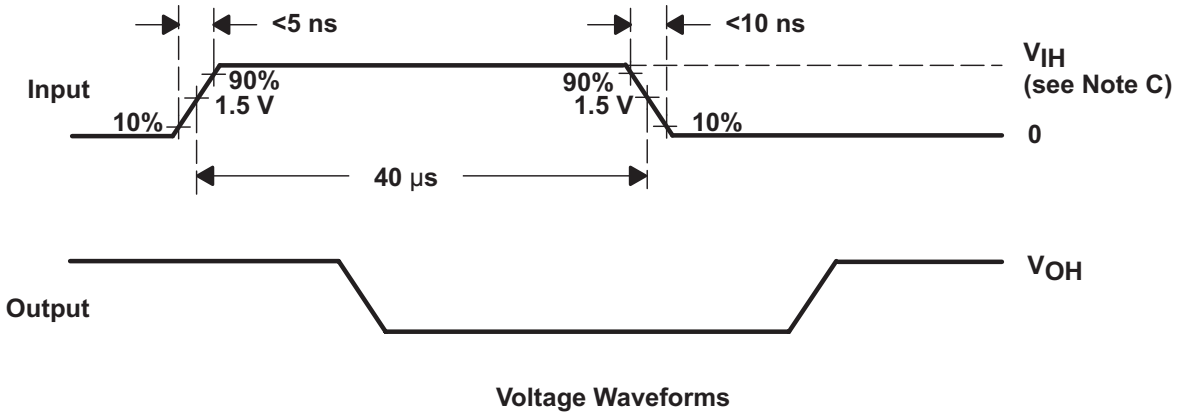
C. V_{IH} = 3 V

Figure 10. Propagation Delay Times

Parameter Measurement Information (continued)



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. V_{IH} = 3 V

Figure 11. Latch-Up Test

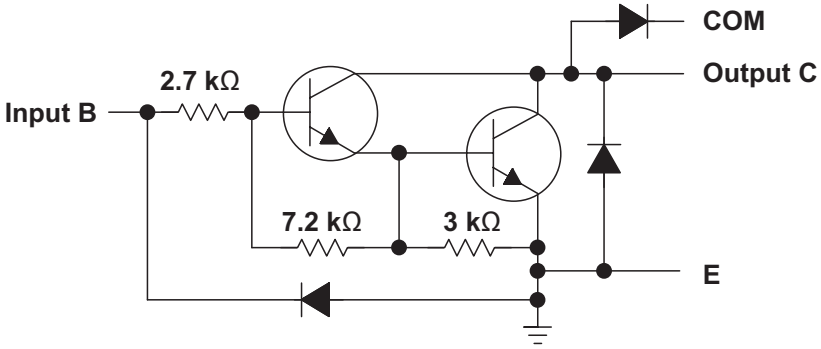
8 Detailed Description

8.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 8 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803A is comprised of eight high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803A has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2803A offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

8.2 Functional Block Diagram



8.3 Feature Description

Each channel of ULN2803A consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very-high current gain. The very high β allows for high output current drive with a very-low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN.

The diodes connected between the output and COM pin are used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation, the diodes on base and collector pins to emitter will be reverse biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2803A is able to drive inductive loads and suppress the kick-back voltage through the internal free wheeling diodes.

8.4.2 Resistive Load Drive

When driving resistive loads, COM can be left unconnected or connected to the load voltage supply. If multiple supplies are used, connect to the highest voltage supply.

9 Application and Implementation

9.1 Application Information

ULN2803A will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803A, driving inductive loads. This includes motors, solenoids, and relays. Each load type can be modeled by what is seen in Figure 12.

9.2 Typical Application

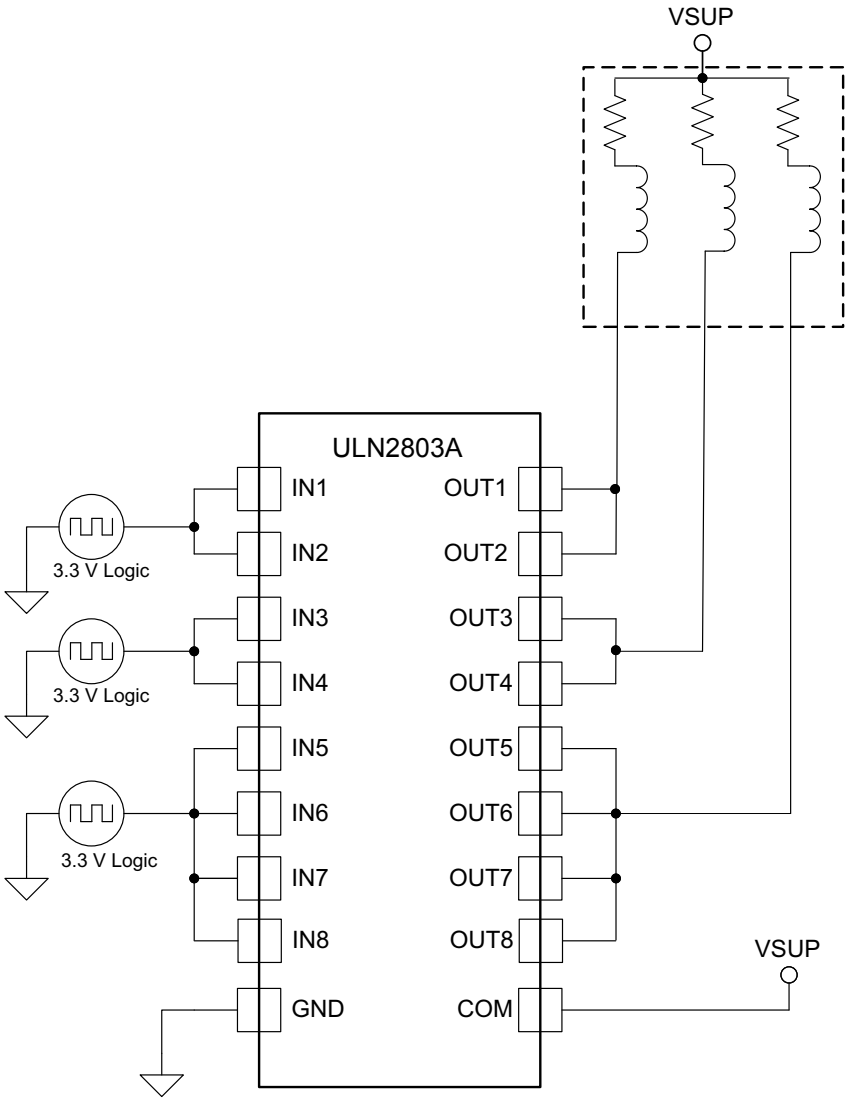


Figure 12. ULN2803A as Inductive Load Driver

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 or 5 V
Coil supply voltage	12 to 50 V
Number of channels	8
Output current (R_{COIL})	20 to 300 mA per channel
Duty cycle	100%

9.2.2 Detailed Design Procedure

When using ULN2803A in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

9.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance, and output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

9.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by Figure 1, Figure 2, or *Electrical Characteristics*.

9.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use Equation 2 to calculate ULN2803A on-chip power dissipation P_D.

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (2)

To ensure the reliability of ULN2803A and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (P_D) dictated by Equation 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA}$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance. (3)

TI recommends to limit ULN2803A IC's die junction temperature to <125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

9.2.3 Application Curves

The following curves were generated with ULN2803A driving an OMRON G5NB relay – V_{in} = 5.0 V; V_{sup}= 12 V and R_{COIL}= 2.8 kΩ

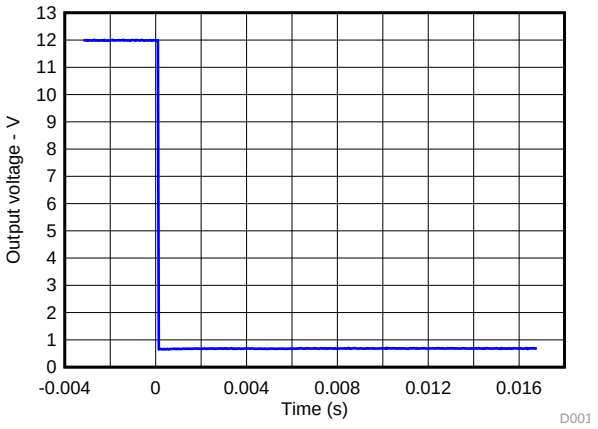


Figure 13. Output Response With Activation of Coil (Turn On)

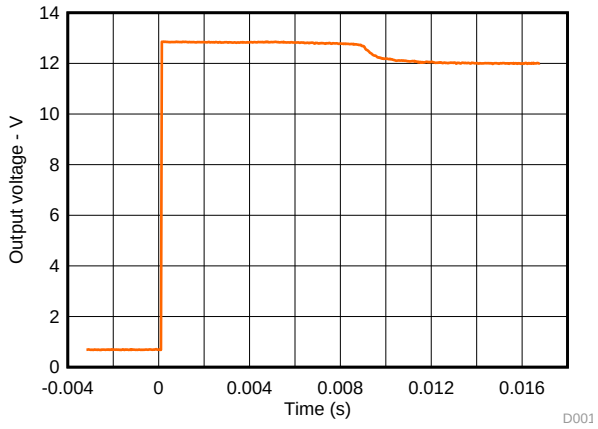


Figure 14. Output Response With De-Activation of Coil (Turn Off)

10 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the flyback diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or overheating the part.

11 Layout

11.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803A. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output, in order to drive high currents as desired. Wire thickness can be determined by the trace material's current density and desired drive current.

Because all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

11.2 Layout Example

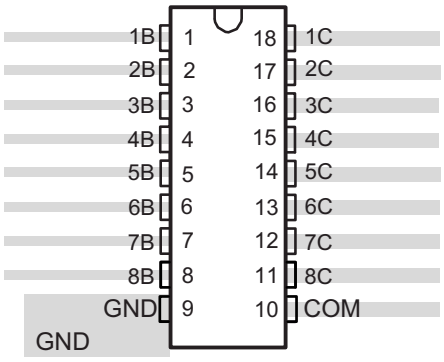


Figure 15. Package Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Glossary

SLYZ022 — *Glossary* .

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

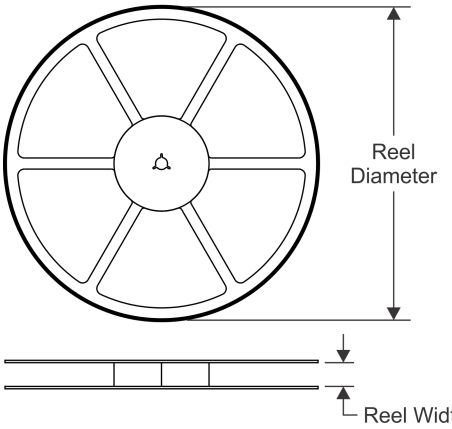
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)
ULN2803A	ACTIVE	SOP	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BN2803A
ULN2803ADWG4	ACTIVE	SOP	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BN2803A
ULN2803ADWR	ACTIVE	SOP	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BN2803A
ULN2803ADWRG4	ACTIVE	SOP	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BN2803A

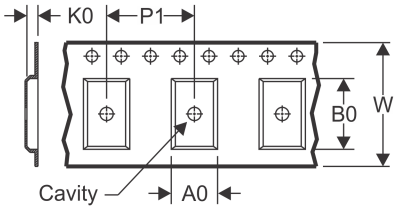
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

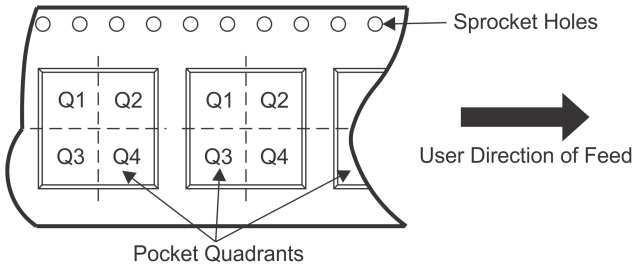


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



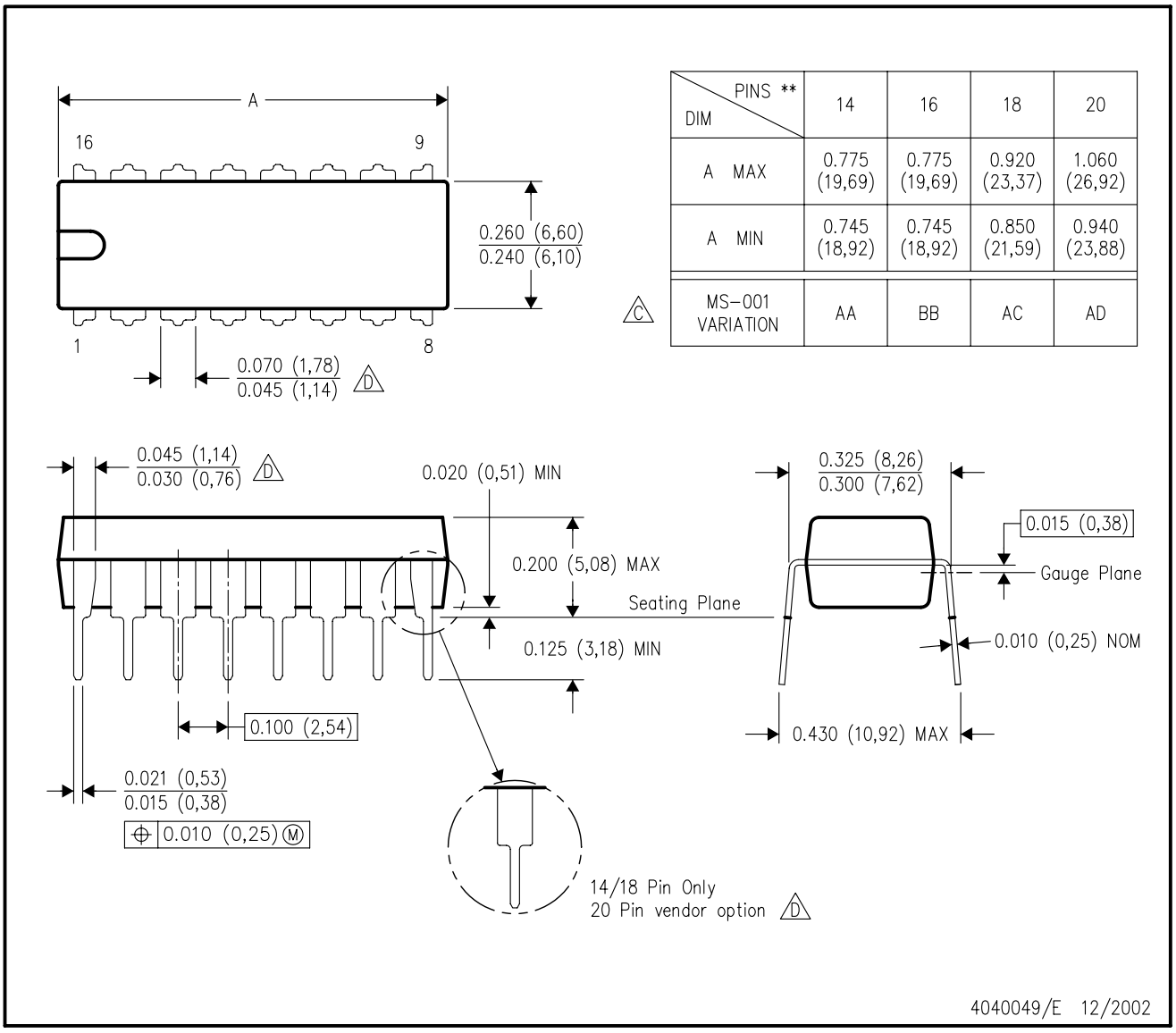
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2803A	SOP	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

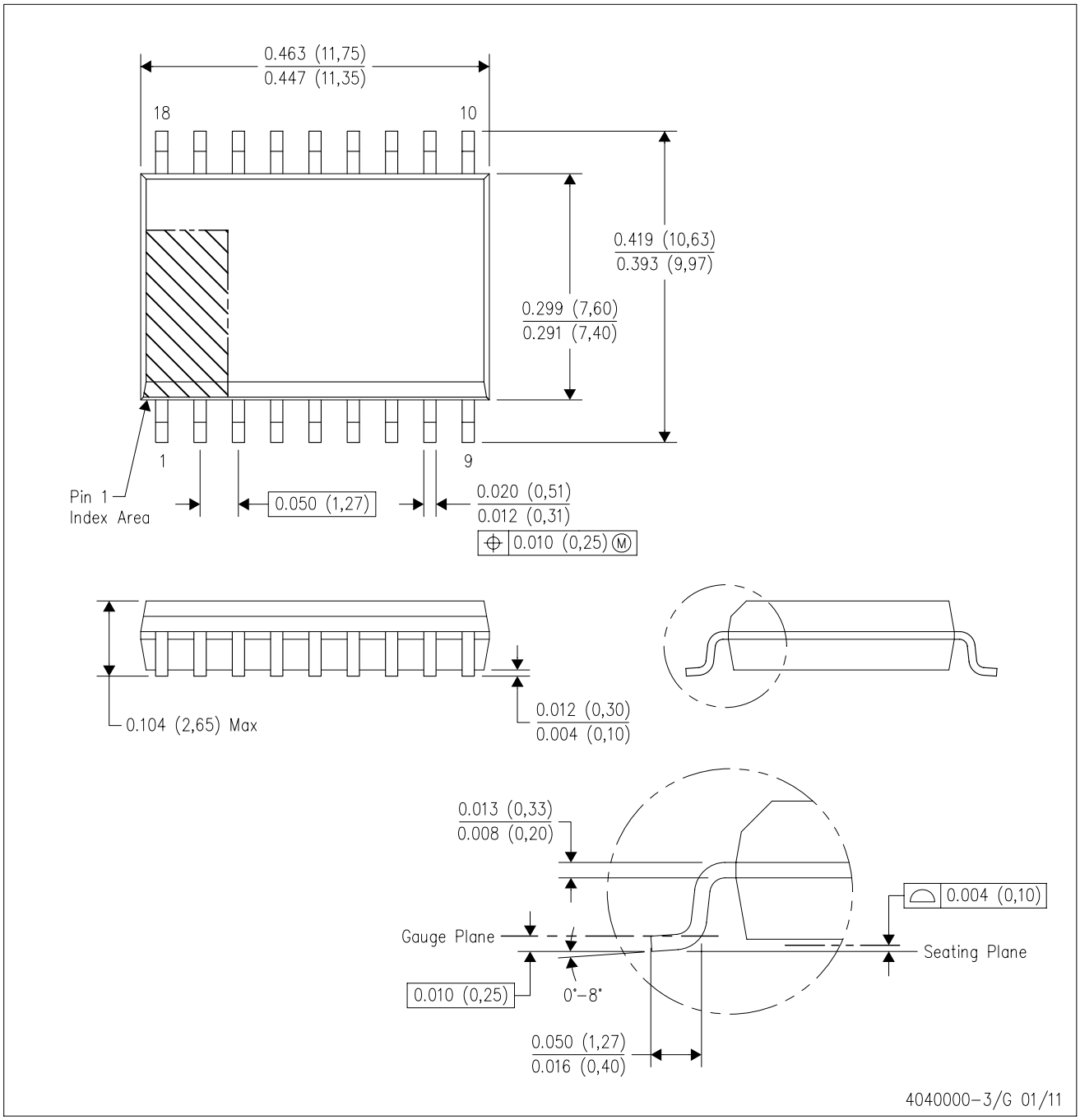


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

C

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D The 20 pin end lead shoulder width is a vendor option, either half or full width.

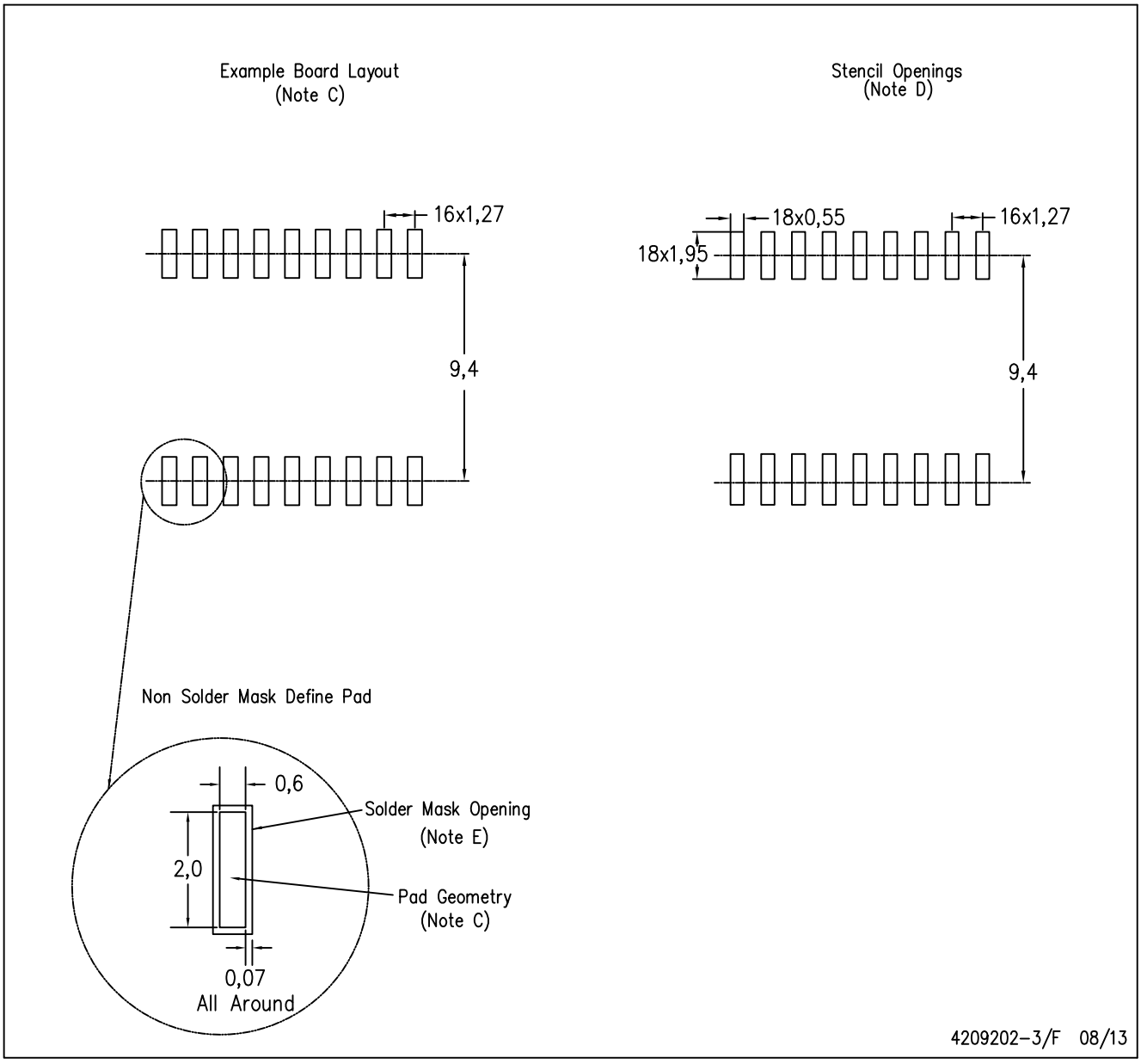
DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

LAND PATTERN DATA

DW (R-PDSO-G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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