

#### **Features**

- Superior circuit protection
- Overcurrent & overvoltage protection
- Blocks surges up to rated limits
- High-speed performance
- Small SMT package
- RoHS compliant\*
- Agency recognition: **SN®**

#### **Applications**

- SLIC protection
- Cable & DSL
- MDU/MTU modems
- ONT
- Voice/DSL line cards

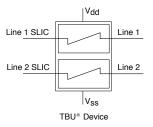
# TBU-PL Series - TBU® High-Speed Protectors

#### **General Information**

The TBU-PL Series of Bourns® TBU® products are low capacitance dual bidirectional high-speed protection components, constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges.

In addition to overcurrent protection, an added feature is the voltage monitoring on the two lines. If the voltage on the line drops below V<sub>SS</sub> then the voltage will trigger the device to switch to the blocking state.

The TBU® high-speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large voltages or currents during surge events. The TBU® device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.



#### **Agency Approval**

#### Industry Standards (in Conjunction with OVP Device)

Description		Solutions available for GR-1089-CORE, ITU-T and a combination of both.
LII	File Number: E315805	

#### Absolute Maximum Ratings (@ TA = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Part Number	Value	Unit
		TBU-PL050-xxx-WH	500	
V.	Peak impulse voltage withstand with duration less than 10 ms	TBU-PL060-xxx-WH	600	V
V <sub>imp</sub>	reak impulse voltage with stand with duration less than 10 ms	TBU-PL075-xxx-WH	750	V
		TBU-PL085-xxx-WH	850	
		TBU-PL050-xxx-WH	300	
V	Continuous A.C. RMS voltage	TBU-PL060-xxx-WH	350	V
V <sub>rms</sub>	Continuous A.C. hivis voitage	TBU-PL075-xxx-WH	400	V
		TBU-PL085-xxx-WH	425	
T <sub>op</sub>	Operating temperature range		-55 to +125	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C	
T <sub>imax</sub>	Maximum Junction Temperature	+125	°C	
ÉSD	HBM ESD Protection per IEC 61000-4-2 on line pads		±2	kV

#### Electrical Characteristics (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Part Nur	nber	Min.	Тур.	Max.	Unit
1.	Current required for the device to go from	TB	TBU-PLxxx-100-WH		150	200	mA
<sup>I</sup> trigger	operating state to protected state	TB	U-PLxxx-200-WH	200	300	400	IIIA
R <sub>device</sub>	Series resistance of the TBU® device			40	50	55	Ω
R <sub>match</sub>	Package resistance matching of the TBU® devi	ce #1 - TBU® device #2			±0.5	±1.0	Ω
t <sub>block</sub>	Time taken for the device to go into current limi	ting				1	μs
lQ	Current through the triggered TBU® device with	50 Vdc circuit voltage		0.25	0.70	1.50	mA
I <sub>SS</sub>	Operating current with V <sub>SS</sub> = -50 V		100		μΑ		
		TBU-PLxxx-100-WH	Forward Mode	12	15	22	V
\ ,,	Voltage below which the triggered TBU®	IDU-PLXXX-100-WII	Reverse Mode	10	13	20	
V <sub>reset</sub>	device will transition to normal operating state	TBU-PLxxx-200-WH	Forward Mode	15	20	25	
			Reverse Mode	12	17	22	
V <sub>to</sub>	Voltage threshold offset with 60 Hz applied volt	age, with V <sub>ss</sub> -50 V (V <sub>s</sub>	ss - V <sub>lineSLIC</sub> )	-1.0		0.2	V
V <sub>ss</sub>	Operating voltage range relative to V <sub>dd</sub>		-180		-20	V	
R <sub>th(j-l)</sub>	One side junction to package pads - FR4 using	ed pad layout		110		°C/W	
R <sub>th(j-l)</sub>	Both sides junction to package pads - FR4 usir		65		°C/W		
R <sub>th(j-l)</sub>	One side junction to package pads - FR4 using	heat sink on board (6	cm <sup>2</sup> ) (0.5 in. <sup>2</sup> )		70		°C/W
R <sub>th(j-l)</sub>	Both sides junction to package pads - FR4 usir	ng heat sink on board (6	6 cm <sup>2</sup> ) (0.5 in. <sup>2</sup> )		40		°C/W

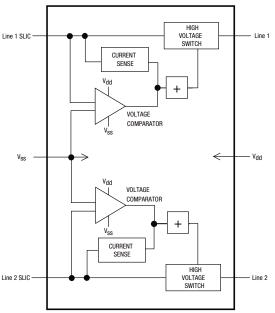


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#### **Environmental Characteristics**

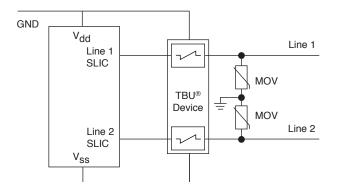
Parameter	Value
Moisture Sensitivity Level	1
ESD Classification (HBM)	1B

# Functional Block Diagram



#### **Reference Application**

The TBU-PL Series are high-speed protectors used in voice/ VoIP SLIC applications. The maximum voltage rating of the TBU® device should never be exceeded. Where necessary, an OVP device should be employed to limit the maximum voltage. A cost-effective protection solution combines Bourns® TBU® protection devices with a pair of Bourns® MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV. If EN55024 EMC compliance is required, the TBU® device may require capacitors to be fitted between the Tip and Ring connections and ground.



#### **Basic TBU Operation**

The TBU® device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The TBU® device operates in approximately 1  $\mu$ s - once line current exceeds the TBU® device's trigger current l<sub>trigger</sub>. When operated, the TBU® device will limit the current to less than the l<sub>trigger</sub> value within the t<sub>block</sub> duration. If voltage above V<sub>reset</sub> is continuously sustained, the TBU® device will subsequently reduce the current to a quiescent current level within a period of time that is dependent upon the applied voltage.

When the voltage on the SLIC output is driven below  $(V_{bat} - V_{to})$  the TBU-PL series device switches to the blocking state, regardless of output current in the device.

After the surge, the TBU® device resets when the voltage across the TBU® device falls to the  $V_{reset}$  level. The TBU® device will automatically reset on lines which have no DC bias or have DC bias below  $V_{reset}$  (such as unpowered signal lines).

If the line has a normal DC bias above V<sub>reset</sub>, the voltage across the TBU® device may not fall below V<sub>reset</sub> after the surge. In such cases, special care needs to be taken to ensure that the TBU® device will reset, with software monitoring as one method used to accomplish this. Bourns application engineers can provide further assistance.

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#### Bourns® TBU® Device Solutions

Industry Standard	Surge & AC Withstand	TBU® Device P/N	Qty.	OVP Device P/N	Qty.
Telcordia GR-1089-CORE Intra-building Port Type 4	1500 V, 100 A 2/10 µs 120 V <sub>rms</sub> , 25 A, 900 s	TBU-PL050-200-WH	1	MOV-07D201K	2
Telcordia GR-1089-CORE Intra-building Port Type 4a	1000 V, 100 A 10/1000 μs 120 V <sub>rms</sub> , 25 A, 900 s	TBU-PL060-200-WH	1	MOV-10D201K	2
Non-GR-1089-CORE Intra-building	5000 V, 500 A 2/10 μs 230 V <sub>rms</sub> , 25 A, 900 s	TBU-PL085-200-WH	1	MOV-10D361K	2
Specifications	1500 V, 100 A 2/10 μs 275 V <sub>rms</sub> , 25 A, 900 s	TBU-PL085-200-WH	1	MOV-10D431K	2
ITILIT Pasia K 00 K 04 K 45	$4000$ V, $40$ Ω $10/700$ $\mu$ s $230$ V <sub>rms</sub> $10$ Ω - $1000$ Ω, $900$ s $600$ V <sub>rms</sub> $600$ Ω, $0.2$ s	TBU-PL075-200-WH	1	MOV-10D361K	2
ITU-T Basic K.20, K.21, K.45	$4000$ V, $40$ Ω $10/700$ $\mu$ s $230$ V rms $10$ Ω $-1000$ Ω, $900$ s $600$ V rms $600$ Ω, $0.1$ s	TBU-PL060-200-WH	1	TISP4400M3BJ	2
ITU-T Enhanced K.20, K.21, K.45	$6000$ V, $40$ Ω $10/700$ $\mu$ s $240$ V <sub>rms</sub> $10$ Ω - $1000$ Ω, $900$ s $600$ V <sub>rms</sub> $600$ Ω, $0.2$ s $600$ V <sub>rms</sub> $600$ Ω, $1$ s* $1500$ V <sub>rms</sub> , $200$ Ω, $2$ s*	TBU-PL085-200-WH	1	MOV-10D391K	2
	$6000 \text{ V}$ , $40 \Omega 10/700 \mu \text{s}$ 240 V <sub>rms</sub> $10 \Omega$ - $1000 \Omega$ , $900 \text{ s}$ $600 \text{ V}_{rms}$ $600 \Omega$ , $1 \text{ s}$ $1500 \text{ V}_{rms}$ , $200 \Omega$ , $2 \text{ s}$	TBU-PL060-200-WH	1	TISP4500H3BJ	2

<sup>\*</sup> GDT Special Test Protector with DC breakdown (DCBD) of less than 330 V.

#### Notes:

- 1) The MOV maximum continuous rms voltage rating should not be exceeded. The exception is where the data sheet highlights withstand capability such as the 600 V<sub>rms</sub>, 1 A for 0.2 s, for example.
- 2) If EN55024 EMC compliance is required, the TBU® device may require capacitors to be fitted between the Tip and Ring connections and ground (i.e. in parallel with the MOV device). The capacitance value can be chosen to meet levels as follows:
  - 10 nF for EN55024 Level 1
  - · 20 nF for EN55024 Level 2
  - 47 nF for EN55024 Level 3

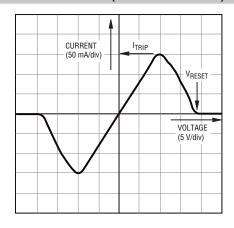
Selection of capacitor voltage rating depends upon TBU® part number selection. Recommendations include:

- TBU-PL050 & TBU-PL060 Series: 120 VAC, 500 V Peak Surge Rated
- TBU-PL075 & TBU-PL085 Series: 240 VAC, 750 V Peak Surge Rated

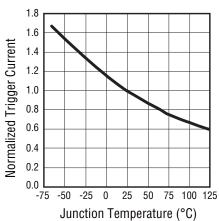
Depending upon the SLIC type, it is usually possible to remove any EMI capacitors present between the output of the SLIC and ground when using capacitors C1 and C2 in parallel with the MOVs.

#### **Performance Graphs**

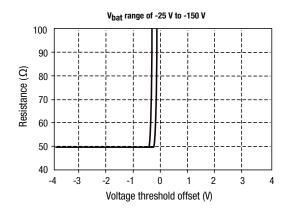
#### Typical V-I Characteristics (TBU-PL085-200-WH)



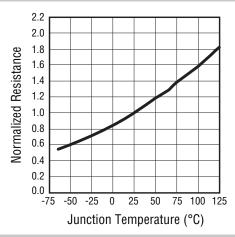
#### **Typical Trigger Current vs. Temperature**



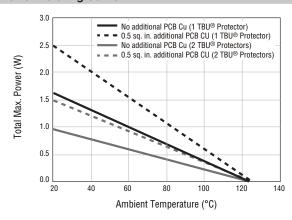
#### **Tracking Voltage Characteristics**



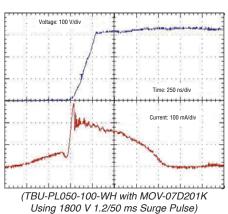
#### Typical Resistance vs. Temperature



#### **Power Derating Curve**

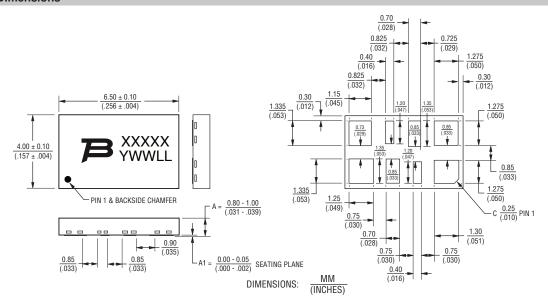


#### **Typical Surge Response**



Specifications are subject to change without notice. Users should verify actual device performance in their specific applications.

#### **Product Dimensions**

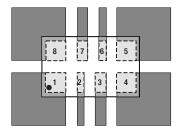


#### **Recommended Pad Layout**

TBU® High-Speed Protectors have a 100 % matte-tin termination finish. For improved thermal dissipation, the recommended layout uses PCB copper areas which extend beyond the exposed solder pad. The exposed solder pads should be defined by a solder mask which matches the pad layout of the TBU® device in size and spacing. It is recommended that they should be the same dimension as the TBU® pads but if smaller solder pads are used, they should be centered on the TBU® package terminal pads and not more than 0.10-0.12 mm (0.004-0.005 in.) smaller in overall width or length. Solder pad areas should not be larger than the TBU® pad sizes to ensure adequate clearance is maintained. The recommended

opening size 0.025 mm (0.0010 in.) less than the solder pad size. Extended copper areas beyond the solder pad significantly improve the junction to ambient thermal resistance, resulting in operation at lower junction temperatures with a corresponding benefit of reliability. All pads should soldered to the PCB, including pads marked as NC or NU but no electrical connection should be made to these pads. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad.

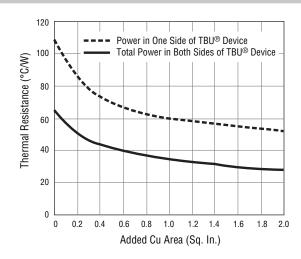
stencil thickness is 0.10-0.12 mm (0.004-0.005 in.) with a stencil



Dark grey areas show added PCB copper area for better thermal resistance.

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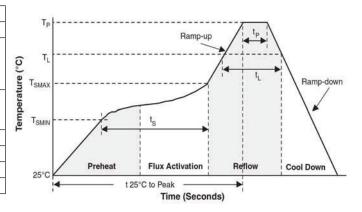
#### Thermal Resistance vs Additional PCB Cu Area



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#### **Reflow Profile**

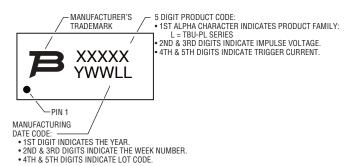
Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



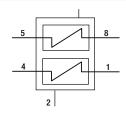
#### **How to Order** TBU - PL 085 - 100 - WH TBU® Product PL = Dual Bidirectional Series Impulse Voltage Rating 050 = 500 V 060 = 600 V075 = 750 V 085 = 850 V Trigger Current 100 = 100 mA 200 = 200 mAHold to Trip Ratio Suffix W = Hold to Trip Ratio Package Suffix -H = DFN Package

#### **Typical Part Marking**

**Pad Designation** 



#### **Device Pin Out**

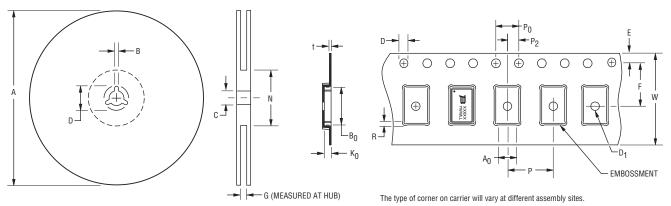


Pad # Pin Out					
1	Line 1				
2	V <sub>dd</sub> (SLIC Ground or 0 V)				
3	Not Used				
4	Line 1 SLIC				

# Pad # Pin Out 5 Line 2 SLIC 6 V<sub>SS</sub> (SLIC Negative Supply or -V<sub>bat</sub>) 7 Not Used 8 Line 2

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#### **Packaging Specifications**



USER DIRECTION OF FEED

QUANTITY: 3000 PIECES PER REEL

	A B C		В		D		G	N	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
326	330	1.5	2.5	12.8	13.5	20.2	_	16.5	_102_
(12.835)	(13.002)	(.059)	(.098)	(.504)	(.531)	(.795)		(.650)	(4.016)

Δ	0	В	0	I	)	D	1	E		ı	F
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
4.30	4.50	6.70	6.90	1.5	1.6	1.5		1.65	1.85	7.4	7.6
(.169)	(.177)	(.264)	(.272)	(.059)	(.063)	(.059)	_	(.065)	(.073)	(.291)	(.299)

K <sub>0</sub>		Р		Р	0	P	2	F	7	1	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1.0 (.039)	1.2 (.047)	7.9 (.311)	8.1 (.319)	3.9 (.159)	<u>4.1</u> (.161)	1.9 (.075)	<u>2.1</u> (.083)		<u>0.5</u> (.020)	0.25 (.010)	<u>0.35</u> (.014)

W						
Min.	Max.					
15.7	16.3					
(.618)	(.642)					

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