

800V 7A N-Channel Enhancement Mode Power MOSFET

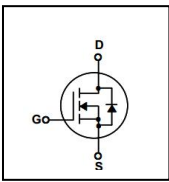
General Description

BXP7N80 is Bridgelux high voltage MOSFET family based on advanced planar stripe DMOS technology. This advanced MOSFET family has optimized on-state resistance, and also provides superior switching performance and higher avalanche energy strength. This device family is suitable for high efficiency switch mode power supplies.

FEATURES

- $R_{DS(ON)} \leq 2 \Omega$ @ $V_{GS}=10V, I_D=3.5A$
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Fast switching capability
- Lead free product is acquired

SYMBOL


TO-220

TO-220F

ASSEMBLY MESSAGE

Product Name	Marking	Package	Packaging
BXP7N80P	BXP7N80P	TO-220	Tube
BXP7N80F	BXP7N80F	TO-220F	Tube

ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Rating		Unit
		BXP7N80P	BXP7N80F	
Drain-Source Voltage	V_{DSS}	800		V
Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	7		A
		4.2		A
Drain Current	Pulsed (Note1)	28		A
Gate-Source Voltage	V_{GSS}	± 30		V
Avalanche Energy	Single Pulse (Note2)	450		mJ
	Repetitive (Note1)	22		mJ
Avalanche Current (Note1)	I_{AR}	7		A
Peak Diode Recovery dv/dt (Note3)	dv/dt	4.6		V/ns
Power Dissipation (Note 2)	$T_C = 25^\circ\text{C}$	198	43.9	W
	Derate above 25°C	1.58	0.35	W/ $^\circ\text{C}$
Maximum Junction Temperature	T_J	150		$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150		$^\circ\text{C}$

- Note:**
1. Repetitive Rating: Pulse width limited by maximum junction temperature
 2. $L=18.4\text{mH}, I_{AS}=7.0\text{A}, V_{DD}=50\text{V}, R_G=25 \Omega$, Starting $T_J = 25^\circ\text{C}$
 3. $I_{SD} \leq 7.0\text{A}, di/dt \leq 300\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Max.		Unit
		BXP7N80P	BXP7N80F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.63	2.85	$^{\circ}C / W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	41	62.5	$^{\circ}C / W$

ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}C$, unless otherwise Noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	800			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=800V, V_{GS}=0V$			1	μA
		$V_{DS}=640V, T_C = 125^{\circ}C$			100	μA
Gate-Body Leakage Current, Forward	I_{GSS}	$V_{GS}=30V$			100	nA
Gate-Body Leakage Current, Reverse		$V_{GS}=-30V$			-100	nA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	$I_D = 250 \mu A$		0.62		$V/^{\circ}C$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	4	5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=3.5A$		1.75	2	Ω
Forward Transconductance (Note4)	g_{FS}	$V_{DS} = 50V, I_D = 3.5A$		5.3		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$		1300		pF
Output Capacitance	C_{OSS}			128		pF
Reverse Transfer Capacitance	C_{RSS}			10		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=400V, I_D=7A, V_{GS} = 10V, R_G=10\Omega$ (Note4,5)		41		ns
Turn-ON Rise Time	t_R			106		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			53		ns
Turn-OFF Fall-Time	t_F			64		ns
Total Gate Charge(Note5)	Q_G	$V_{DS} = 640V, V_{GS} = 10V, I_D = 7A$ (Note4,5)		40		nC
Gate Source Charge	Q_{GS}			8		nC
Gate Drain Charge	Q_{GD}			20		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=7A, V_{GS}=0V$			1.4	V
Diode Continuous Forward Current	I_S				7	A
Pulsed Drain-Source Current	I_{SM}				28	A
Reverse Recovery Time	t_{RR}	$V_{GS} = 0V, I_{SD} = 7A$		645		ns
Reverse Recovery Charge	Q_{RR}	$di/dt=100A/\mu s$ (Note4,5)		6		μC

Note: 4. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

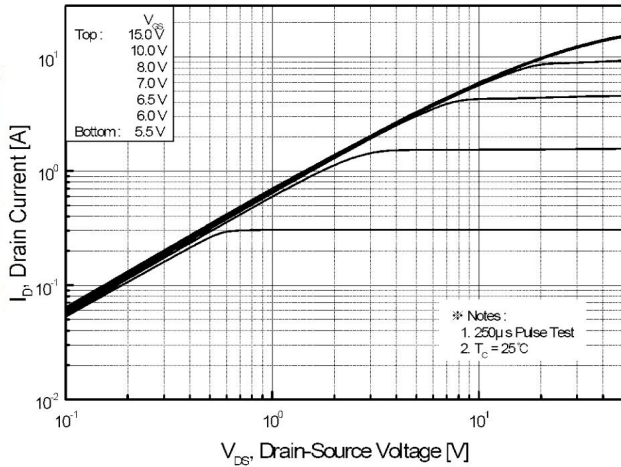


Figure 1. Typical Output Characteristics

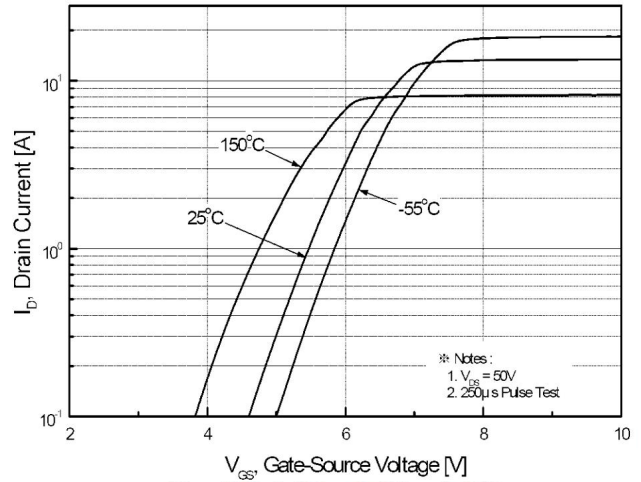


Figure 2. Typical Transfer Characteristics

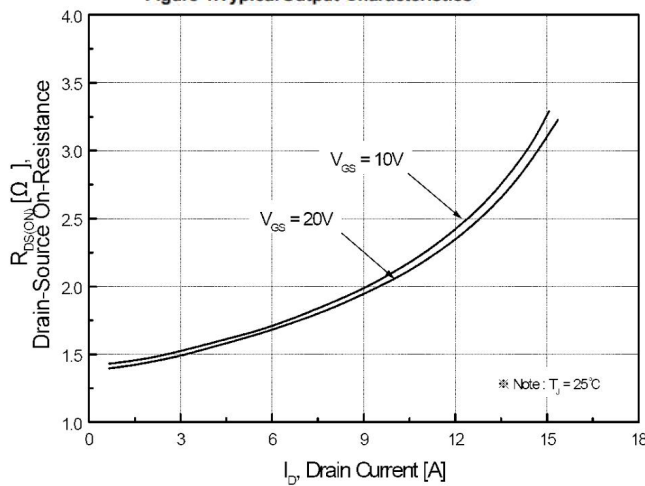


Figure 3. On-Resistance versus Drain Current

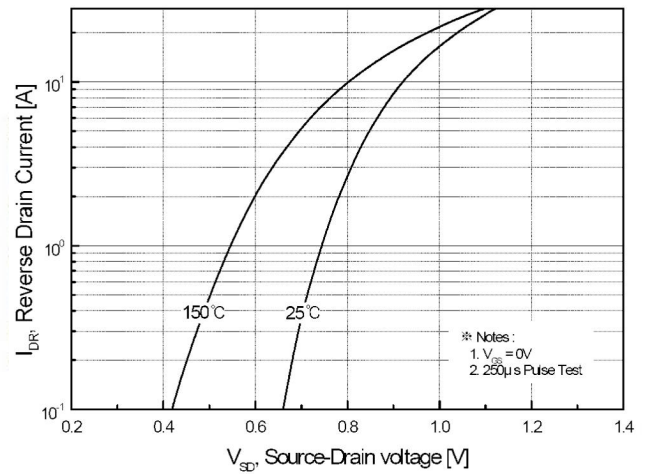


Figure 4. Diode Forward Voltage versus Current

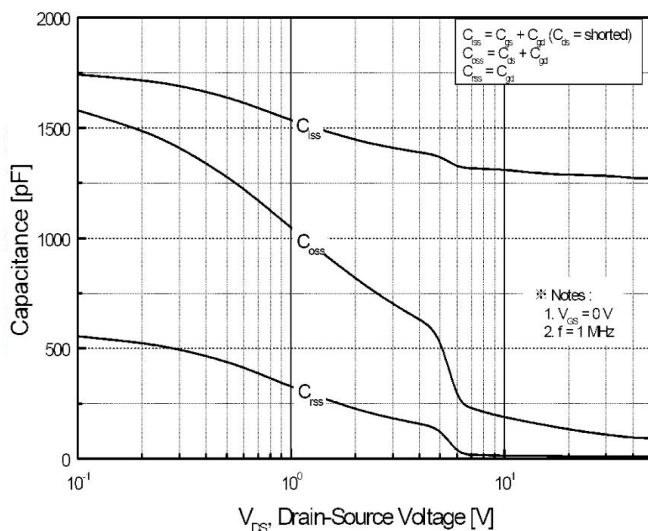


Figure 5. Typical Capacitance vs. Drain-to-Source Voltage

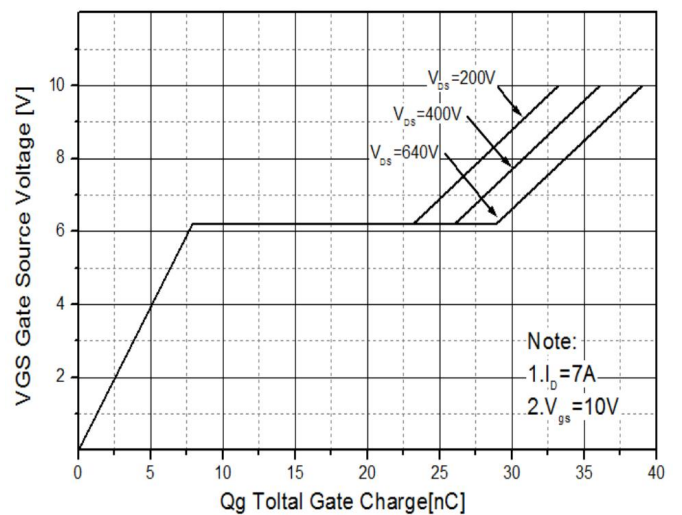


Figure 6. Typical Gate Charge vs. Vgs

TYPICAL CHARACTERISTICS(Cont.)

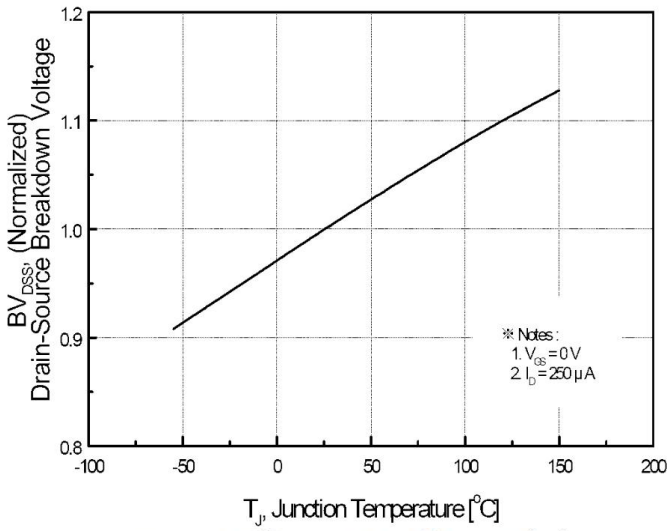


Figure 7. Bvdss Variation with Temperature

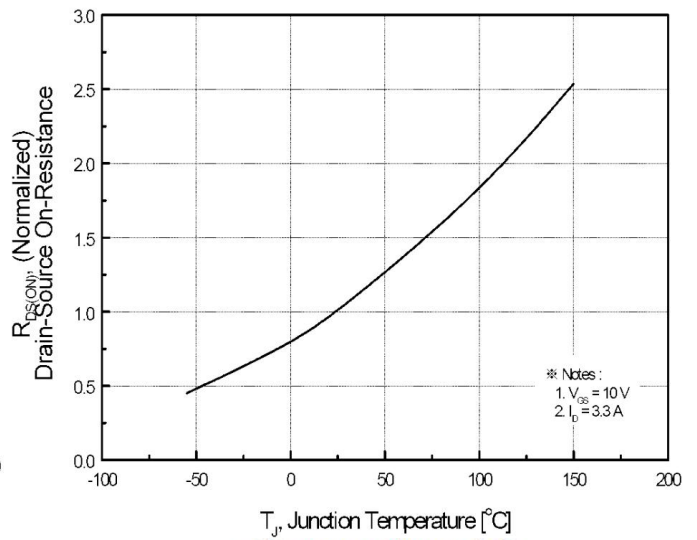


Figure 8. On-Resistance Variation with Temperature

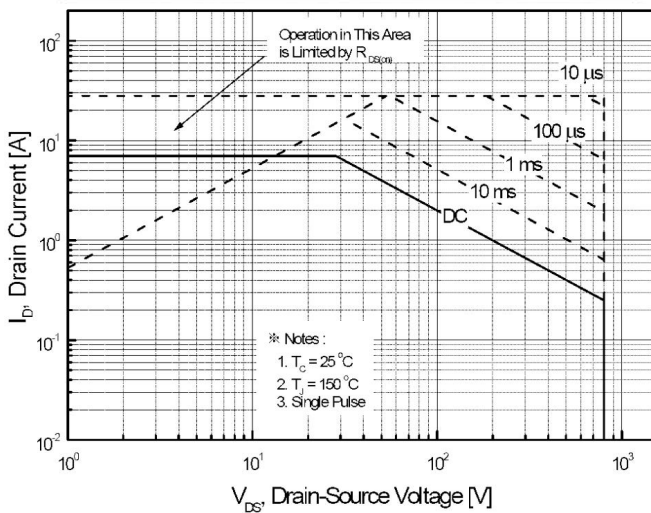


Figure 9. Maximum Safe Operating Area For BXP7N65U/D/P

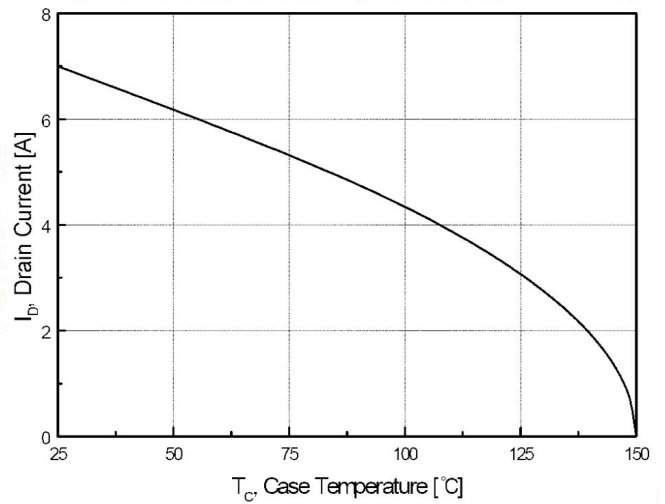
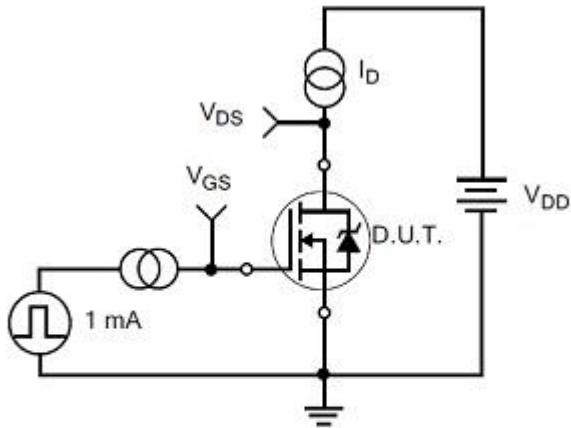
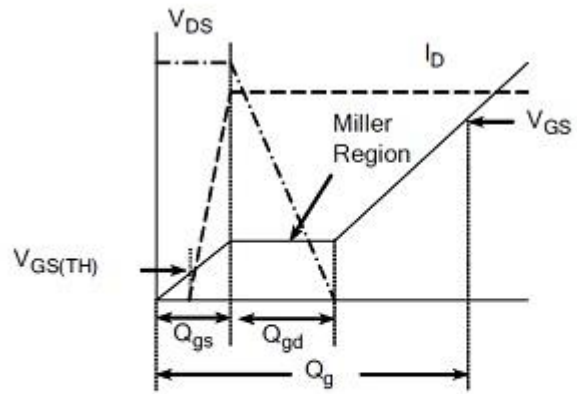


Figure 10. Maximum Continuous Drain Current vs Case Temperature

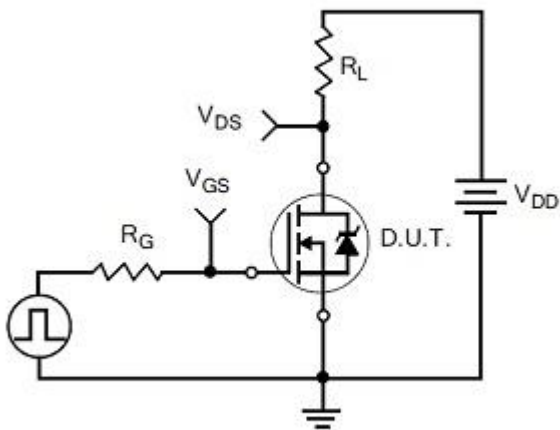
TEST CIRCUITS AND WAVEFORMS



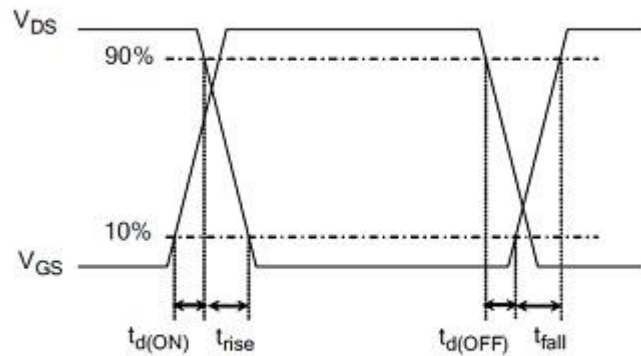
Gate Charge Test Circuit



Gate Charge Waveform

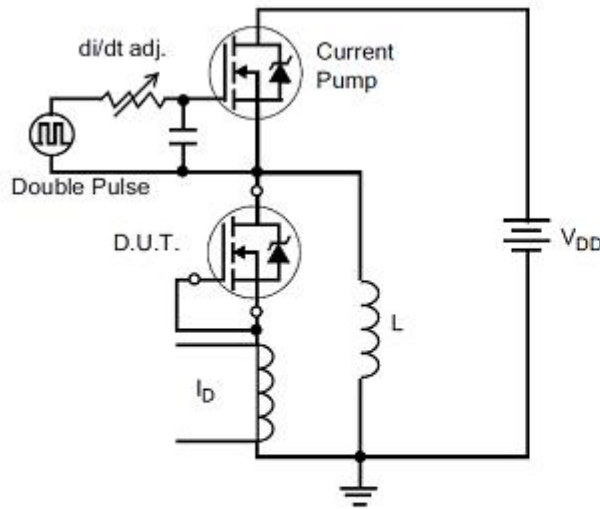


Resistive Switching Test Circuit

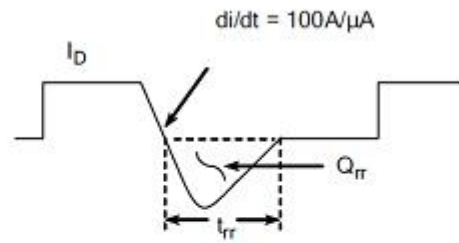


Resistive Switching Waveforms

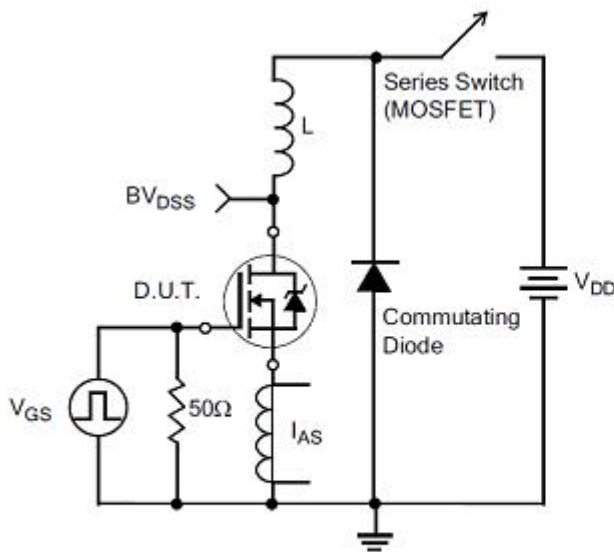
TEST CIRCUITS AND WAVEFORMS(Cont.)



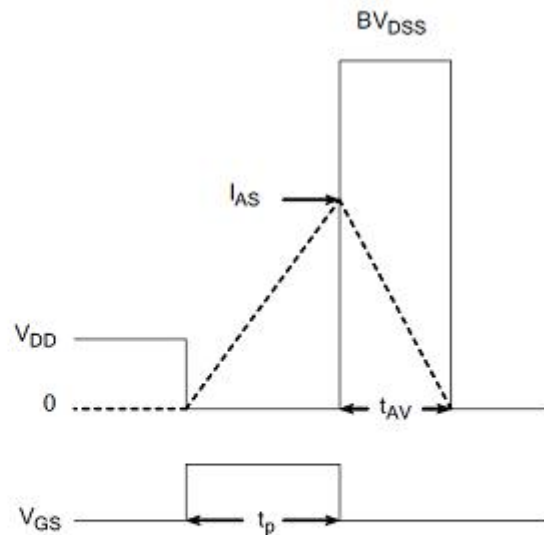
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms

Revision history

Document revision history

Date	Revision	Changes
15-Nov-2020	1.0	First release
6-Jan-2022	1.1	Update parameter

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