



## BCT4221 USB2.0 Hi-Speed Switches

### GENERAL DESCRIPTION

The BCT4221 is a high bandwidth, fast double-pole double-throw (DPDT) analog switch. Its wide bandwidth and low bit-to-bit skew allow it to pass high-speed differential signals with good signal integrity. Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Industry-leading advantages include a propagation delay of less than 250ps, resulting from its low channel resistance and low I/O capacitance. Its high channel-to-channel crosstalk rejection results in minimal noise interference.

The BCT4221 is available in Green QFN2.0X1.5-10L packages. It operates over an ambient temperature range of -40°C to +85°C.

### FEATURES

- V<sub>CC</sub> Operating Range: 2.7V-5.5V
- Analog Signal Range: 0 to V<sub>CC</sub>
- -3dB Bandwidth: 720MHz
- Off Isolation:-38dB @250MHz
- Crosstalk Rejection:- 38dB @250MHz
- ON-Resistance:6Ω Typical
- Extended Temperature Range: -40°C to 85°C
- Green QFN2.0X1.5-10L packages
- ESD:HBM 8000V

### APPLICATIONS

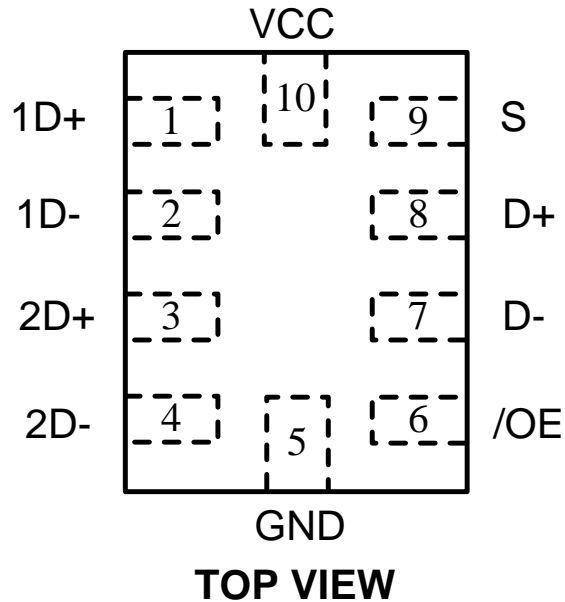
Cell Phones  
Hi-Fi Audio Switching  
USB 2.0 High Speed Data Switching  
USB 3.x Type C Switching

### ORDERING INFORMATION

Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT4221EGB-TR	QFN2.0X1.5-10L	-40°C to +85°C	4221 YWTG	3000

NOTE 1: Y: year, W: weeks

### PIN CONFIGURATION



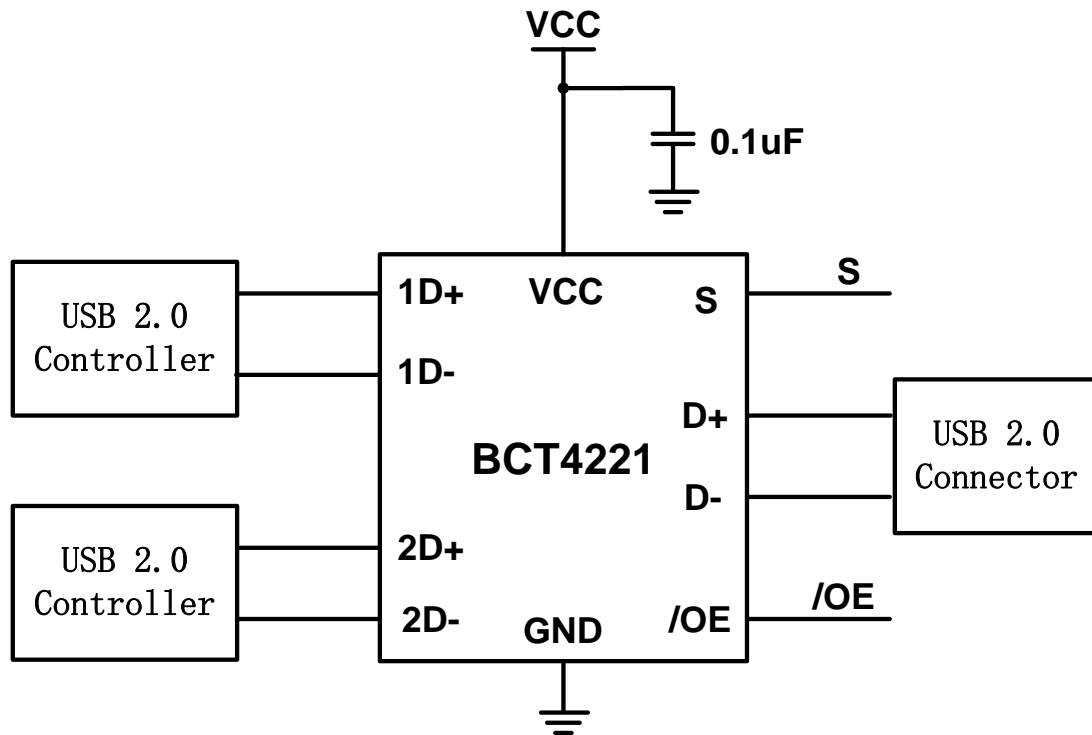
### PIN DESCRIPTION

PIN	NAME	FUNCTION
1	1D+	USB port 1 DATA+
2	1D-	USB Port 1 DATA-
3	2D+	USB port 2 DATA+
4	2D-	USB Port 2 DATA-
5	GND	Power Ground
6	/OE	Outputs enable input, active low.
7	D-	USB data bus DATA-
8	D+	USB data bus DATA+
9	S	Logic Control, 0 select port 1
10	VCC	Power Supply

## Truth Table

S1	/OE	PORT 1	PORT 2
0	0	ON	OFF
1	0	OFF	ON
X	1	OFF	OFF

## TYPICAL APPLICATION CIRCUIT





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## ABSOLUTE MAXIMUM RATINGS

VCC to GND.....	-0.5V to +6.0V
All Other Pins to GND.....	-0.5V to ( $V_{CC} + 0.3V$ )
Continuous Current (D+/-, 1 D+/-, 2D+/-).....	$\pm 120mA$
Continuous Power Dissipation.....	0.4W
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature.....	+150°C
Lead Temperature (soldering, 10s).....	+260°C

## ESD Protection

Human Body Model.....	8000V
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Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.



# BCT4221

## USB2.0 Hi-Speed Switches

### ELECTRICAL CHARACTERISTICS

(VCC = 2.7V to 5.5V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VCC = 3.3V, TA = +25°C.) (Note 2)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Voltage Range	V <sub>CC</sub>		2.7		5.5	V
Supply Current	I <sub>CC</sub>	V <sub>CC</sub> =3.6V, S =0 or V <sub>CC</sub> , D+/-,nD+/- = floating		0.02	1	uA
Analog Signal Range			0		V <sub>CC</sub>	V
On-Resistance	R <sub>ON</sub>	I <sub>SW</sub> = 30mA, V <sub>D+</sub> , V <sub>D-</sub> = 0V (Note 3)		6	12	Ω
On-Resistance Match	ΔR <sub>ON</sub>	I <sub>SW</sub> = 30mA, V <sub>D+</sub> , V <sub>D-</sub> =0V (Note 3,4)		0.2		Ω
On-Resistance Flatness	R <sub>FLAT</sub>	I <sub>SW</sub> = 30mA, V <sub>D+</sub> , V <sub>D-</sub> = 0 to V <sub>CC</sub> (Note 5)		1		Ω
D+,D-,1D+,1D-,2D+,2D- Power off Leakage Current	I <sub>OFF</sub>	V <sub>CC</sub> =0V , V <sub>SW</sub> = 0 to 3.6V			1	uA
D+,D-,1D+,1D-,2D+,2D- Off Leakage Current	I <sub>OZ</sub>	Switch off, V <sub>SW</sub> = 0 to V <sub>CC</sub>			1	uA
Input-Logic High	V <sub>IH</sub>	V <sub>CC</sub> =2.7 – 5.5V	1.5		V <sub>CC</sub>	V
Input-Logic Low	V <sub>IL</sub>	V <sub>CC</sub> =2.7 – 5.5V	0		0.4	V
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1		1	uA



### ELECTRICAL CHARACTERISTICS

(VCC = 2.7V to 5.5V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VCC = 3.3V, TA = +25°C.) (Note 2)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-On Time	T <sub>ON</sub>	V <sub>nD+</sub> or V <sub>nD-</sub> = 1.5V, RL = 50Ω, CL = 35pF, (Figure 1)		20	50	nS
Turn-Off Time	T <sub>OFF</sub>	V <sub>nD+</sub> or V <sub>nD-</sub> = 1.5V, RL = 50Ω, CL = 35pF, (Figure 1)		15	50	nS
Break-Before-Make Time	T <sub>BBM</sub>	V <sub>nD+</sub> and V <sub>nD-</sub> = 1.5V RL = 50Ω, CL = 35pF, (Figure 2)	2	15		nS
On-Channel Bandwidth -3dB	BW	RL = 50Ω, (Figure 3)		720		MHz
Off-Isolation	Q <sub>IRR</sub>	RL = 50Ω, f = 250MHz (Note 6)		-38		dB
Crosstalk	X <sub>TALK</sub>	RL = 50Ω, f = 250MHz (Figure 4)		-38		dB
D+,D- Off-Capacitance	C <sub>OFF</sub>	f = 1MHz, (Figure 5)		5		pF
D+,D- On-Capacitance	C <sub>ON</sub>	f = 1MHz, (Figure 5)		7		pF

#### NOTES:

Note 2: Devices are 100% tested at TA = +25°C. Limits across the full temperature range are guaranteed by design and correlation.

Note 3: RON and RON matching specifications are guaranteed by design,

Note 4: ΔRON = RON(MAX) - RON(MIN).

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over the specified analog signal ranges.

Note 6: Between any two switches.

## Test Diagram

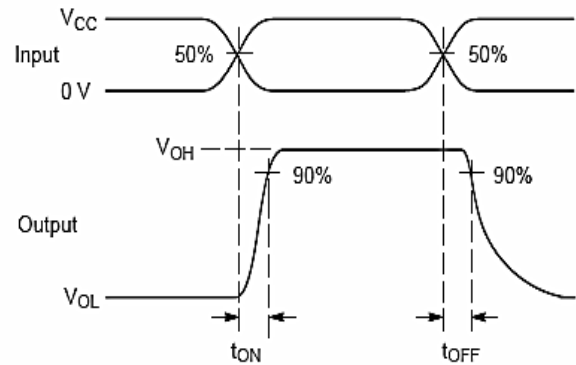
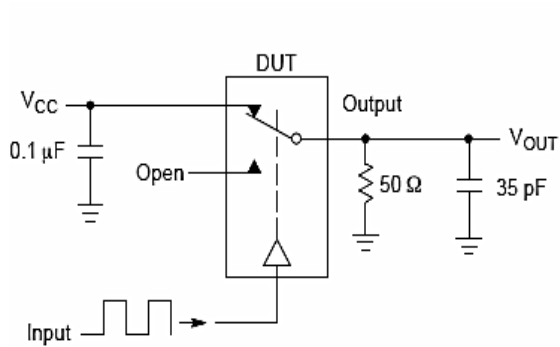


Figure 1.  $t_{ON/OFF}$

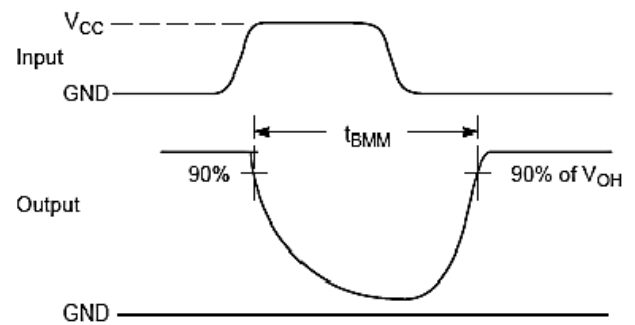
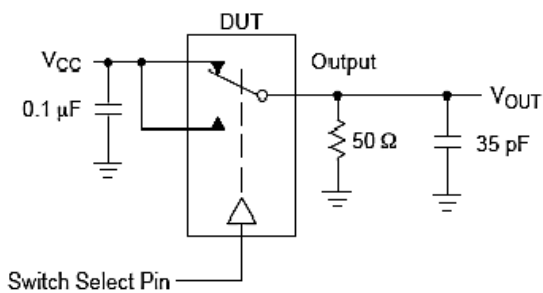


Figure 2.  $t_{BMM}$  (Time Break-Before-Make)

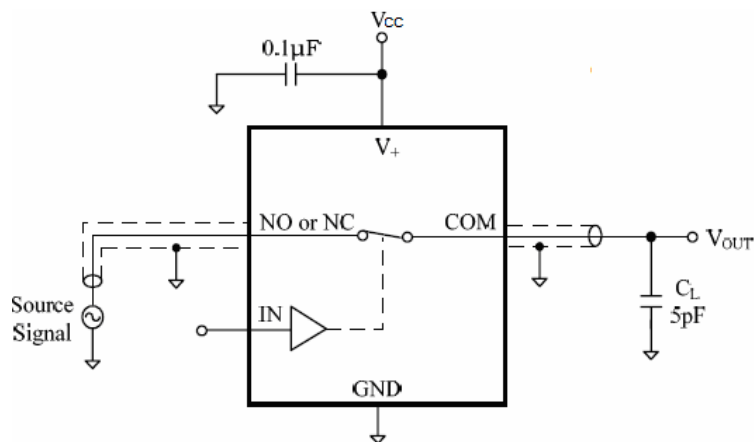
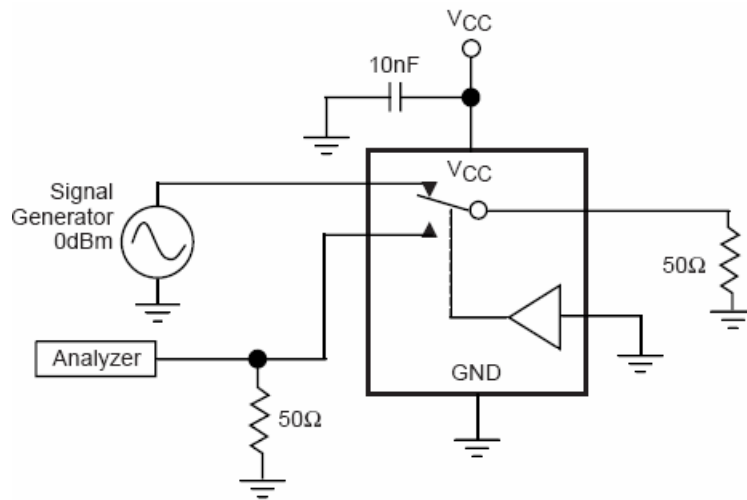
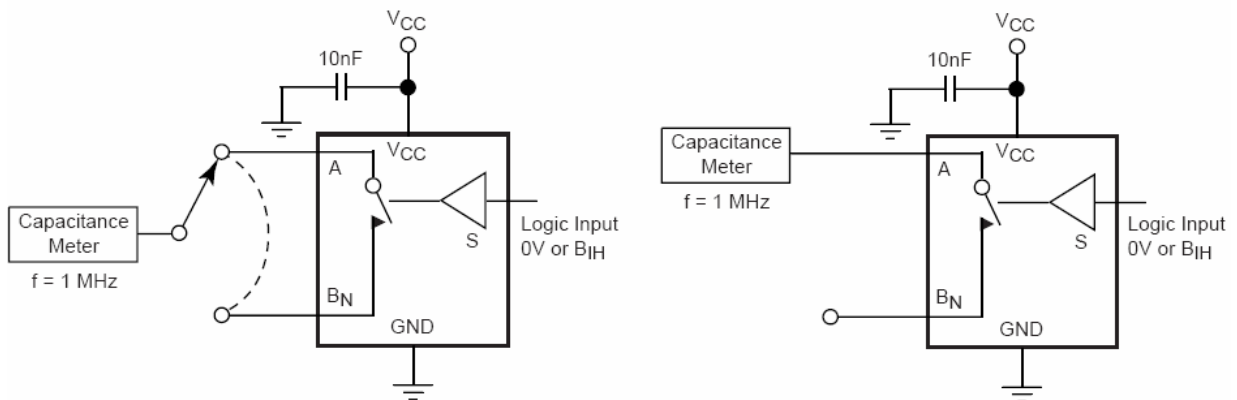


Figure 3. Bandwidth -3dB



**Figure 4. Crosstalk**

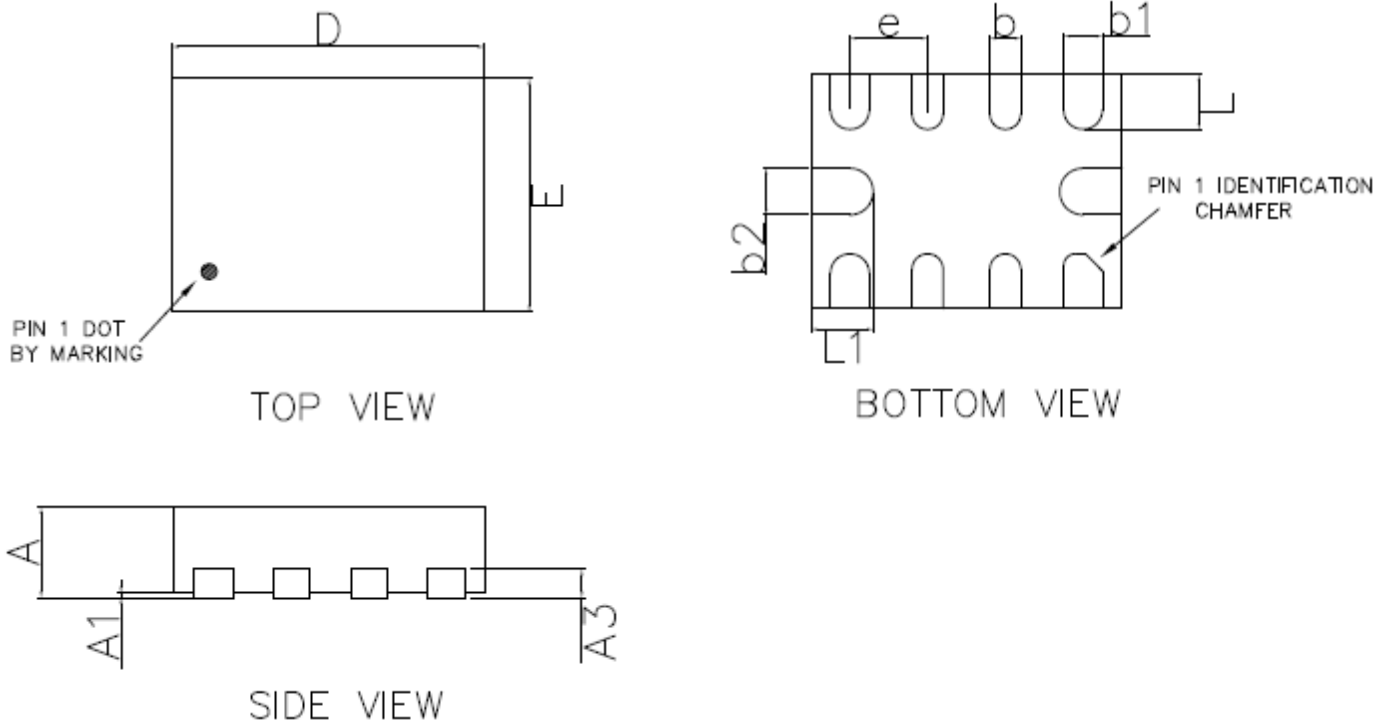


**Figure 5. Channel ON/OFF Capacitance**



### PACKAGE OUTLINE DIMENSIONS

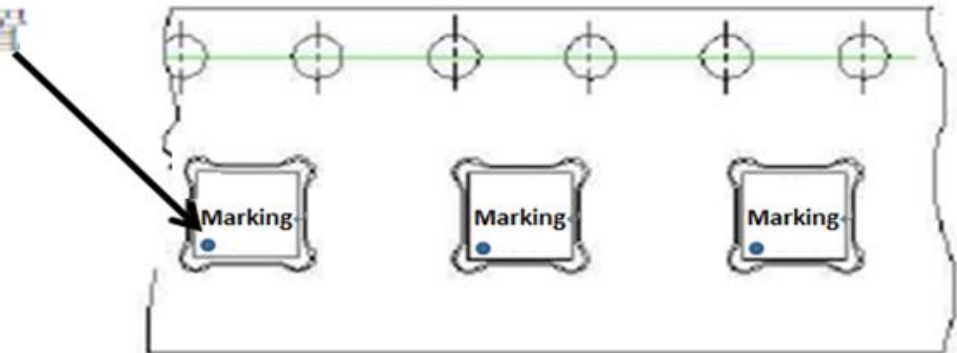
#### QFN2.0x1.5-10L



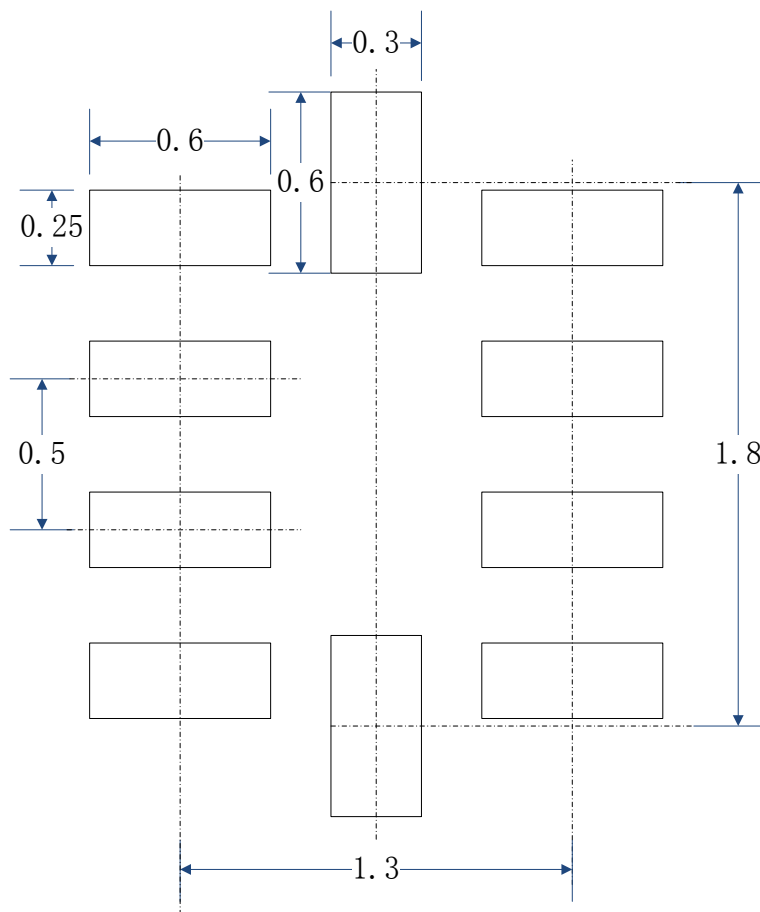
COMMON DIMENSIONS(mm)			
PKG	UT:ULTRA THIN		
REF	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	--	0.05
A3	0.15 REF		
D	1.95	2.00	2.05
E	1.45	1.50	1.55
b	0.15	0.20	0.25
b1	0.20	0.25	0.30
b2	0.25	0.30	0.35
L	0.30	0.35	0.40
L1	0.35	0.40	0.45
e	0.50 BSC		

**TAPING DESCRIPTION**

PIN1 脚位置



**PCB Layout Pattern: QFN2.0x1.5-10L**



**RECOMMENDED PCB LAYOUT PATTERN (Unit: mm)**

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