BCT4302B

Dual SIM Card Controller

General Description

The BCT4302B is a dual SIM card control chip optimized for GSM/EDGE/GPRS/3G handsets, It provides the power conversion and signal level translation needed for advanced cell phones to interface with 1.8V and 3V SIMs. The device meets all requirements for 1.8V and 3V SIMs and contains LDO regulators to power 1.8V or 3V SIM card from a 2.7V to 5.5V input. A serial port interface(SPI) is used to control dual SIM channel individually. The BCT4302B I/O voltage can support 1.65V to 5.5V.

The BCT4302B is available in 20-pin 3mm x 3mm QFN package. The operating temperature range is from -25°C to +85°C.

Applications

Support dual SIM card interface
GSM, EDGE, GPRS and 3G Cell Phones

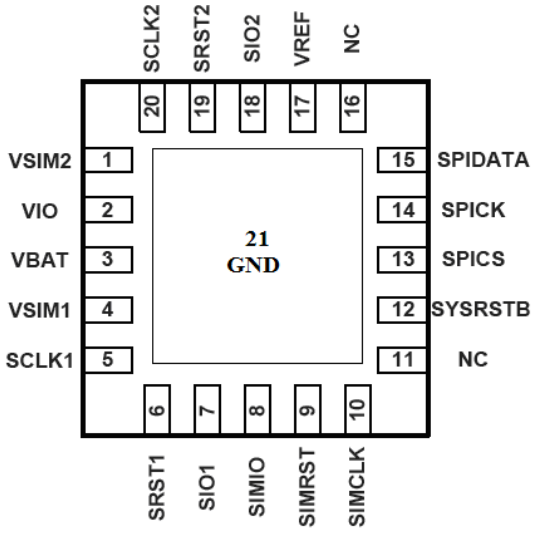
Features

- CMOS Technology for dual SIM card controlling
- Control and communication through a SPI interface with baseband processor.
- Power management and control for two SIM cards
- Independent 1.8/3V VCC control for each SIM card
- Fast channel switching
- Independent clock stop mode (at high or low level) for each SIM card
- Temperature Range: –25°C to 85°C
- 8KV ESD on SIM Card Pins
- 20-pin 3mm x 3mm QFN package (Pb-free & Green available):

ORDERING INFORMATION

Ordering Code	Package Description	Temp Range	Top Marking
BCT4302BEGP-TR	QFN-20	–25°C to +85°C	4302B

Connection Diagram (Top View)



BCT4302B Dual SIM Card Controller

Pin Description

Pin	Name	Description
1	VSIM2	SIM2 Supply
2	VIO	Digital IO Supply
3	VBAT	Battery Input Voltage
4	VSIM1	SIM1 Supply
5	SCLK1	Level-Shifted SIM1 Clock Output
6	SRST1	Level-Shifted SIM1 Reset Output
7	SIO1	Level-Shifted SIM1 Bidirectional Data Input/Output
8	SIMIO	Non-Level-Shifted Bidirectional Data I/O
9	SIMRST	Non-Level-Shifted SIM Reset Input, Internal Pull High to VIO
10	SIMCLK	Non-Level-Shifted SIM Clock Input
11	NC	
12	/SYSRSTB	System Reset, Low Active
13	SPICS	Serial bus selection
14	SPICK	Serial bus clock
15	SPIDATA	Serial bus data
16	NC	
17	VREF	Reference Voltage Output
18	SIO2	Level-Shifted SIM2 Bidirectional Data Input/Output
19	SRST2	Level-Shifted SIM2 Reset Output
20	SCLK2	Level-Shifted SIM2 Clock Output
21	GND	Ground

Detailed Description Overview

The BCT4302B is a dual SIM card control chip optimized for use with GSM baseband chipsets in handset applications. Figure 1 shows the block diagram of the BCT4302B.

The BCT4302B contains several blocks:

- Serial Port Interface (SPI)
- Signal Processing Blocks
- Analog Blocks
- SIM Card Interface

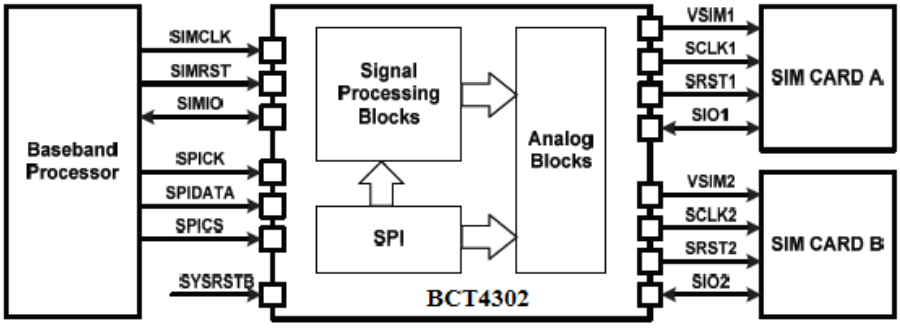
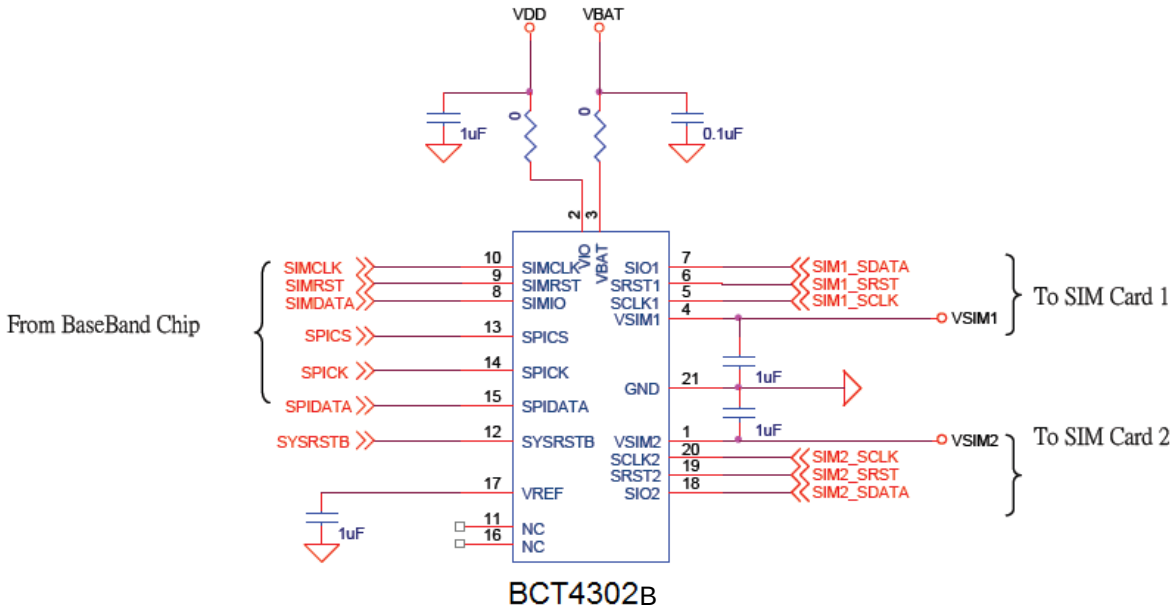


Figure 1. BCT4302B Block Diagram

BCT4302B Dual SIM Card Controller

Application Circuit Example



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage V_{CC}.....–0.5V to +7V
DC Switch Voltage (V_S)…….. .....–0.5V to V_{CC} +0.5V
DC Input Voltage (V_{IN})…….…..…. .....–0.5V to +7.0V
Storage Temperature Range (T_{STG}) ..... –65°C to +150°C
Junction Temperature under Bias (T_J) .....…..... 150°C

Junction Lead Temperature (T_L)
(Soldering, 10 seconds) ..... 260°C
Power Dissipation (P_D) @ +85°C 180mW

Note 1:Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical CHARACTERISTICS

(VBAT=2.7V-5.5V, CVREF=CVSIM1=CVSIM2=2.2uF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at TA=+25 ºC, VIO=3.0V, VBAT=4.0V)

Parameter	Condition	Min	Typical	Max	Unit
Input power supply					
VBAT Operating Voltage		2.7		5.5	V
VBAT Shutdown Current	VIO=0V	---	0.1	1	uA
VBAT Operating Ground Current	VSIM1=3.0V, VSIM2=0V, no load VSIM1=1.8V, VSIM2=0V, no load	---	30 30	70 70	uA
VIO Operating Voltage		1.65		5.5	V
VIO Shutdown Current		---	0.1	1	uA
VIO Operating Ground Current		---	3	5	uA
Input Control					
Low Input Threshold	SPIDATA, SPICK, SPICS, SYSRSTB			0.15*VIO	V
High Input Threshold	SPIDATA, SPICK, SPICS, SYSRSTB	0.85*VIO			V

BCT4302B Dual SIM Card Controller

Parameter	Condition	Min	Typical	Max	Unit
SIM Card Supplies (VSIM1, VSIM2)					
1.8V Output Voltage		1.65	1.8	1.95	V
3.0V Output Voltage		2.82	3.0	3.18	V
Output Short Current Limit		---	38	---	mA
Load Regulation(1.8V) Load Regulation(3.0V)	0.05mA<I_load<20mA at Vbat=3.6V	---	1 1.7	10 10	mV
Turn-On Time	No load, Enable to VSIM1,2 at 90% selected voltage		0.8	1.5	ms
GSM Interface					
Vih(SIMCLK, SIMRST)		Vio-0.6	---	---	V
Vil (SIMCLK, SIMRST)		---	---	0.6	V
Vil (SIMIO)	Vol<=0.4V, Iol=1mA Vol<=o.4V, Iol=0mA	--- ---	--- ---	0.23 0.335	V
Vih(SIMIO), Voh(SIMIO)	Iih,Ioh=±20uA	Vio-0.6	---	---	V
Iil(SIMIO)	Vil=0V	---	---	0.9	mA
Vo(SIMIO)	Vil=0.4V	---	---	0.42	V
Interface to 3V SIM Card					
Vol(SRST)	Sink Current=-20uA (VSIMRST=0.6V)	---	---	0.4	V
Voh(SRST)	Source Current=200uA(VSIMRST=Vio-0.6V)	0.9*VSIM	__	__	V
Vol(SCLK)	Sink Current= -20uA (VSIMCLK=0.6V	---	---	0.4	V
Voh(SCLK)	Source Current=200uA(VSIMCLK=Vio-0.6V)	0.9*VSIM	__	__	V
Vil(SIO)		---	---	0.15*VSIM	V
Vih(SIO), Voh(SIO)	Source Current=20uA	VSIM-0.4	---	---	V
Iil(SIO)	VSIO=0V	---	---	-1	mA
Vol(SIO)	Sink Current=-1mA(VSIMIO=0V)	---	---	0.15*VSIM	V
Interface to 1.8V SIM Card					
Vol(SRST)	Sink Current=-20uA(VSIMRST=0.6V)			0.2*VSIM	V
Voh(SRST)	Source Current=200uA(VSIMRST=Vio-0.6V)	0.9*VSIM			V
Vol(SCLK)	Sink Current= -20uA (VSIMCLK=0.6V			0.2*VSIM	V
Voh(SCLK)	Source Current=200uA(VSIMCLK=Vio-0.6V)	0.9*VSIM			V
Vil(SIO)				0.15*VSIM	V
Vih(SIO), Voh(SIO)	Source Current=20uA	VSIM-0.4			V
Iil(SIO)	VSIO=0V			-1	mA
Vol(SIO)	Sink Current=-1mA(VSIMIO=0V)			0.15*VSIM	V
SIM Card Interface Timing					
SRST, SIO rise/fall times	VSIM=3, 1.8V, loaded with 30uF (10%~90%)			500	ns
SCLK rise/fall times	VSIM=3, 1.8V, loaded with 30uF(10%~90%)			15	ns
	VSIM=1.8V, loaded with 30uF (10%~90%)			40	ns
SCLK frequency		5			MHz
SCLK duty cycle	SIMCLK Duty=50%, fSIMCLK=5MHz	47		53	%
SCLK propagation delay	From SIMCLK to SCLK,load with30pF		8	10	ns

Details of the individual subsystems and blocks are described in following Chapters.

Serial Port Interface (SPI)

This module is used to receive the commands transmitted by baseband processor. It will decode the received data and send corresponding commands to signal processing and analog blocks. The 8-bit serial interface uses three pins –SPICS#, SPIDATA an SPICK- to enter data. Data read is not available with the serial interface and data entered must be 8 bits. The description of three pins is:

Signal Name	Attribute	Direction	Description
SPICK	Edge Triggered	BB->BCT4302B	Serial bus clock
SPIDATA	Level	BB->BCT4302B	Serial data
SPICS	Active Low	BB->BCT4302B	SPI bus selection

Figure 2 shows the timing diagram of this serial interface. When the block is idle, SPICK is forced LOW and SPICS# is forced HIGH. Once the data register contains data and the interface is enabled, SPICS# is pulled LOW and remains LOW for the duration of the transmission. The first three bits are address bits and the others are data bits.

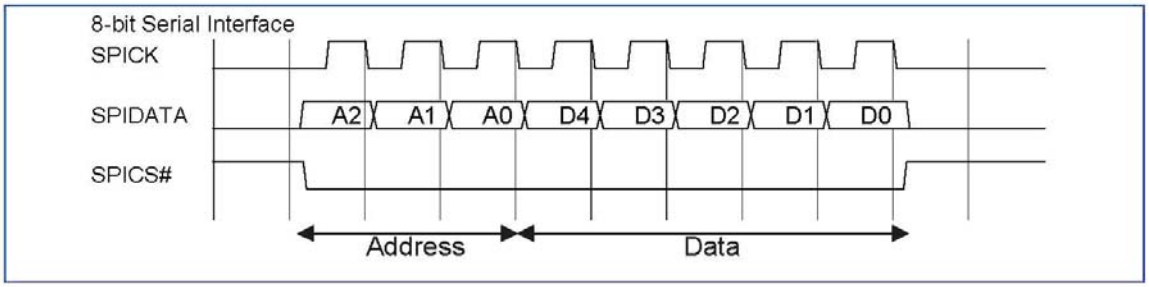


Figure 2. SPI Interface Transfer Diagram

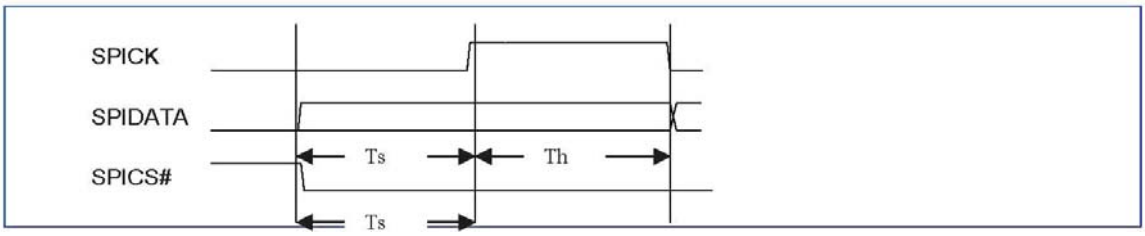


Figure 3. SPI Interface Timing Diagram

Serial Port Interface Timing

Symbol	Parameter	Min	Tye	Max	Unit
Ts	SPIDATA to SPICK setup time	4			ns
Th	SPIDATA to SPICK hold time	4			ns

Register Definitions

0000H Reset control Register

Bit	4	3	2	1	0
Name		RSTVAL		RSTSEL	
Type		WO	WO	WO	WO
Reset		0	0	0	0

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd

RSTSEL SIM card RST pin control, only valid when VCCEN is 1.

0 The RST pin of SIM card is the same as BCT4302 input pin SIMRST.

1 The RST pin of SIM card is controlled by RSTVAL as show below.

RSTVAL Control the value of SIM card RST pin, only valid when VCCEN is 1 an RSTSEL is 1.

0 Force the SIM card RST pin to 0.

1 Force the SIM card RST pin to 1.

0001H Clock Control Register

Bit	4	3	2	1	0
Name		CPOH		CPOL	
Type		WO	WO	WO	WO
Reset		0	0	1	1

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd one. The value of SIM card pin is controlled by the combination of the two signals when VCCEN is 1.

CPOH, CPOL

01 The CLK pin of SIM card is the same as BCT4302B input pin SIMCLK.

11 Force the SIM card CLK pin to stop at high.

00 Force the SIM card CLK pin to stop at low.

10 Not allowed.

0002H Data Control Register

Bit	4	3	2	1	0
Name		DATA_L		DATAEN	
Type		WO	WO	WO	WO
Reset		0	0	0	0

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd one.

DATAEN SIM card DATA pin control, only valid when VCCEN is 1.

0 The channel between SIM card DATA pin and BCT4302B I/O pin SIMDATA will be gapped. If there were no drivers of these two pins, the they will be pulled high.

1 The channel between SIM card DATA pin and BCT4302B I/O pin SIMDATA will be opened. If there Were no drivers of these two pins, then they will be pulled high.

DATA_L Control the value of SIM card DATA pin, only valid when both VCCEN and DATAEN are “1”

0 normal function.

1 Force the SIM card DATA pin to 0.

0003H VCC Control Register

Bit	4	3	2	1	0
Name		VCCEN		VSEL	
Type		WO	WO	WO	WO
Reset		0	0	0	0

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd one.

VCCEN SIM card power control.

0 Turn off SIM card VCC pin, all signals to SIM card will be 0.

1 Turn on SIM card VCC pin.

VSEL Choose the supply voltage level of SIM card.

0 Supply voltage is 1.8V.

1 Supply voltage is 3V.

0004H

Bit	4	3	2	1	0
Name	REFSEL				
Type	WO				
Reset	0				

REFSEL **LDO reference selection**

0 **VIO**

1 **Bandgap**

0005H Bandgap Control Register

Bit	4	3	2	1	0
Name	BG_EN	RBGSEL			
Type	WO	WO	WO		
Reset	0	0	0		

BG_EN Embedded bandgap enable

0 Disable

1 Enable

RGBSEL Bandgap T.C. fine turning

00 initial setting

01 minus 1 step

10 plus 1 step

11 plus 2 step

Signal Processing Blocks

The main function of this block is to handle the command ordered by baseband processor about SCLK and SRST. When it receivers commands sent by SPI, it will do the corresponding signal processing, and then sent the results to analog blocks. The commands is transmitted through serial port interface (SPI) and stored in the register set. Signal processing blocks will process signals with corresponding commands. The truth table of SCLK and SRST is shown in the following tables.

VSIM	CPOH	CPOL	SIMCLK	SCLK
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	Not allowed
1	1	0	1	Not allowed
1	1	1	0	1
1	1	1	1	1

Table 1. Truth table of SCLK

VSIM	RSTSEL	RSETVAL	SIMRST	SRST
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Table 2. Truth table of SRST

It will be noticed that the effect of those controlled signal may not be valid immediately due to the delay of some processing time.

Analog Blocks

This module contains SIM LDO, level shifter and bandgap function. It will accept the command set by SPI and also transfer the signals to suitable voltage level to SIM cards. The SIM LDO is a regulator that could source 40mA(max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules(SIM) card.

SIM Card Interface

The SIM card interface circuitry of BCT4302B meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output.

Card Activation and Deactivation

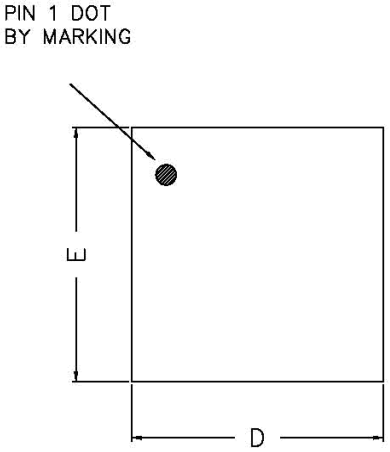
The role of BCT4302B at card activation and deactivation is just a signal bypasser. It will bypass SIMCLK and SIMRST transmitted by baseband processor and turn on the channel between SIMIO and SIO.
When card activation, user just needs to follow the steps listed below.

- Set VSEL to desired level.
- Turn on VCCEN and DATAEN in sequence, and the other registers just keep their default settings.
- Turn on SIM interface of baseband processor to start activation sequence.

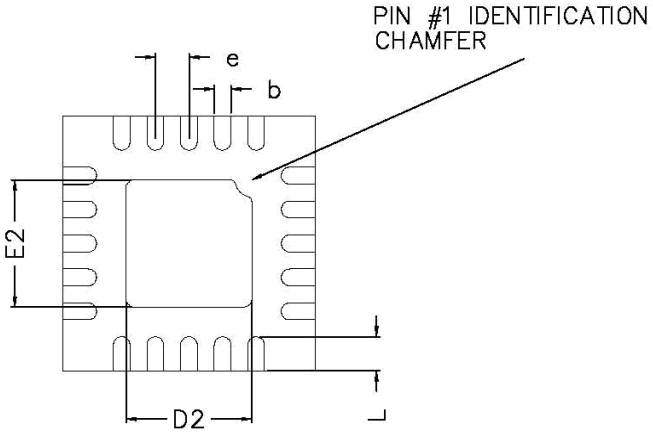
Similarly, when card deactivation, user just follows the steps listed below.

- Turn off SIM interface of baseband processor to start deactivation sequence.
- Set DATA_L and then turn off VCCEN, and the other registers just keep their default settings.

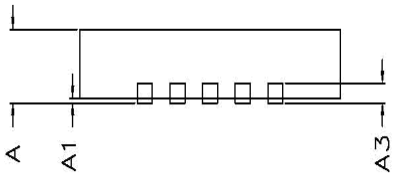
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.2 REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.15	0.20	0.25
L	0.30	0.40	0.50
D2	1.35	1.50	1.60
E2	1.35	1.50	1.60
e	0.40 BSC		

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