4N55, 5962-87679, HCPL-553x, HCPL-653x, HCPL-257K, HCPL-655x, 5962-90854, HCPL-550x[1]

Hermetically Sealed, Transistor Output Optocouplers for Analog and Digital Applications

Data Sheet

Description

These units are single-, dual-, and quad-channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either Commercial product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DLA Standard Microcircuit Drawing (SMD). All devices are manufactured and tested on a MIL-PRF-38534 certified line and Class H and K devices are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Features

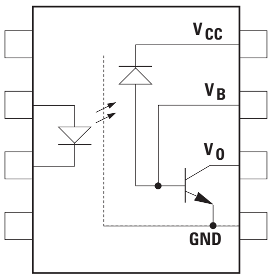
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Five hermetically sealed package configurations
- Performance guaranteed over full military temperature range: –55°C to +125°C
- High speed: 400 kb/s typical
- 9-MHz bandwidth
- Open collector output
- V_{CC} ranges from 2V to 18V
- 1500 VDC withstand test voltage
- High radiation immunity
- 6N135, 6N136, HCPL-2530/2531 function compatibility
- Reliability data

Applications

- Military and aerospace
- High reliability systems
- Vehicle command, control, life critical systems
- Line receiver
- Switching power supply
- Voltage level shifting
- Analog signal ground isolation (see Figures 7, 8, and 13)
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Isolation for test equipment systems

1. See the Selection Guide – Package Styles and Lead Configuration Options table for available extensions.

Functional Diagram



Multiple channel devices available.

Truth Table

(Positive Logic)

Input	Output
On (H)	L
Off (L)	H

NOTE The connection of a 0.1 µF bypass capacitor between V_{CC} and GND is recommended.

Each channel contains a GaAsP light emitting diode that is optically coupled to an integrated photon detector. Separate connections for the photodiodes and output transistor collectors improve the speed up to one-hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

These devices are suitable for wide-bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16 mA. The 18V V_{CC} capability enables the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

Package styles for these parts are 8- and 16-pin DIP through-hole (case outlines P and E, respectively), 16-pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options, see the selection guide table for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

Because the same functional die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

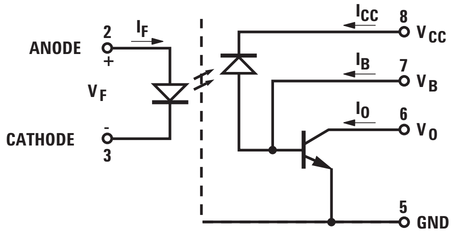
Selection Guide – Package Styles and Lead Configuration Options

Package	16-Pin DIP	8-Pin DIP	8-Pin DIP	16-Pin Flat Pack	20-Pad LCCC
Lead Style	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	2	1	2	4	2
Common Channel Wiring	None	None	V_{CC}, GND	V_{CC}, GND	None
Part Number and Options					
Commercial	4N55	HCPL-5500	HCPL-5530	HCPL-6550	HCPL-6530
MIL-PRF-38534, Class H	4N55/883B	HCPL-5501	HCPL-5531	HCPL-6551	HCPL-6531
MIL-PRF-38534, Class K	HCPL-257K	HCPL-550K	HCPL-553K	HCPL-655K	HCPL-653K
Standard Lead Finish	Gold Plate[a]	Gold Plate[a]	Gold Plate[a]	Gold Plate[a]	Solder Pads[b]
Solder Dipped[b]	Option #200	Option #200	Option #200		
Butt Joint/Gold Plate[a]	Option #100	Option #100	Option #100		
Gull Wing/Soldered[b]	Option #300	Option #300	Option #300		
Class H SMD Part Number					
Prescript for all below	*5962-*	*5962-*	*5962-*	*5962-*	*5962-*
Gold Plate[a]	8767901EC	9085401HPC	8767902PC	8767904FC	
Solder Dipped[b]	8767901EA	9085401HPA	8767902PA		87679032A
Butt Joint/Gold Plate[a]	8767901UC	9085401HYC	8767902YC		
Butt Joint/Soldered[b]	8767901UA	9085401HYA	8767902YA		
Gull Wing/Soldered[b]	8767901TA	9085401HXA	8767902XA		
Class K SMD Part Number					
Prescript for all below	*5962-*	*5962-*	*5962-*	*5962-*	*5962-*
Gold Plate[a]	8767905KEC	9085401KPC	8767906KPC	8767908KFC	
Solder Dipped[b]	8767905KEA	9085401KPA	8767906KPA		8767907K2A
Butt Joint/Gold Plate[a]	8767905KUC	9085401KYC	8767906KYC		
Butt Joint/Soldered[b]	8767905KUA	9085401KYA	8767906KYA		
Gull Wing/Soldered[b]	8767905KTA	9085401KXA	8767906KXA		

a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.

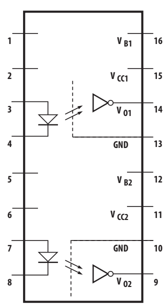
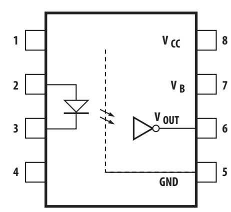
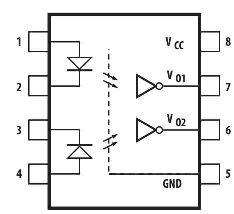
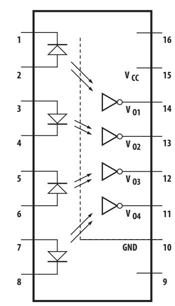
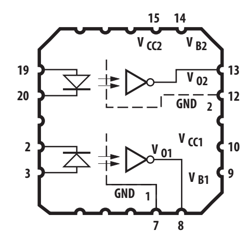
b. Solder lead finish: Sn63/Pb37.

8-Pin Ceramic DIP Single Channel Schematic



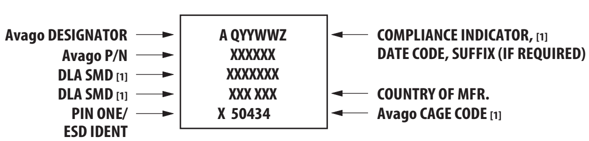
NOTE Base is pin 7.

Functional Diagrams

16-Pin DIP	8-Pin DIP	8-Pin DIP	16-Pin Flat Pack	20-Pad LCCC
Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
2 Channels	1 Channel	2 Channels	4 Channels	2 Channels
				

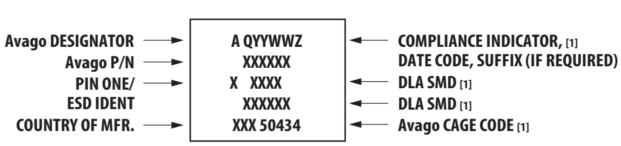
NOTE 8-pin DIP and flat pack devices have common V_{CC} and ground. 16-pin DIP and LCCC (leadless ceramic chip carrier) packages have isolated channels with separate V_{CC} and ground connections. All diagrams are top view.

Leaded Device Marking



[1] QML PARTS ONLY

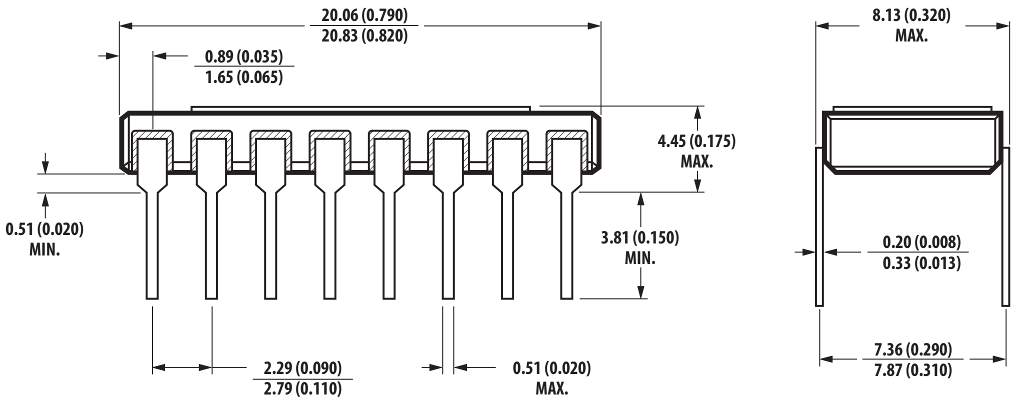
Leadless Device Marking



[1] QML PARTS ONLY

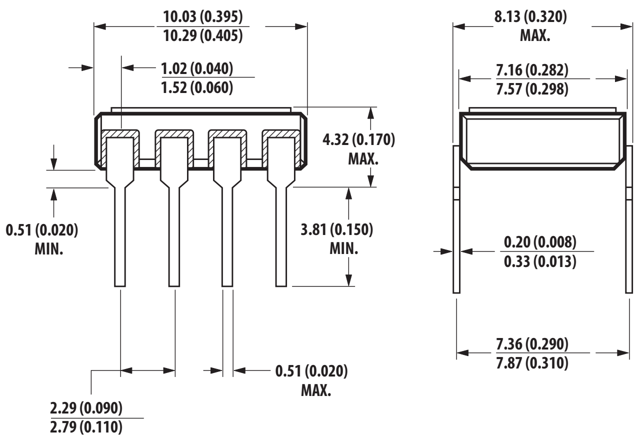
Outline Drawings

16-Pin DIP, Through Hole, 2 Channels



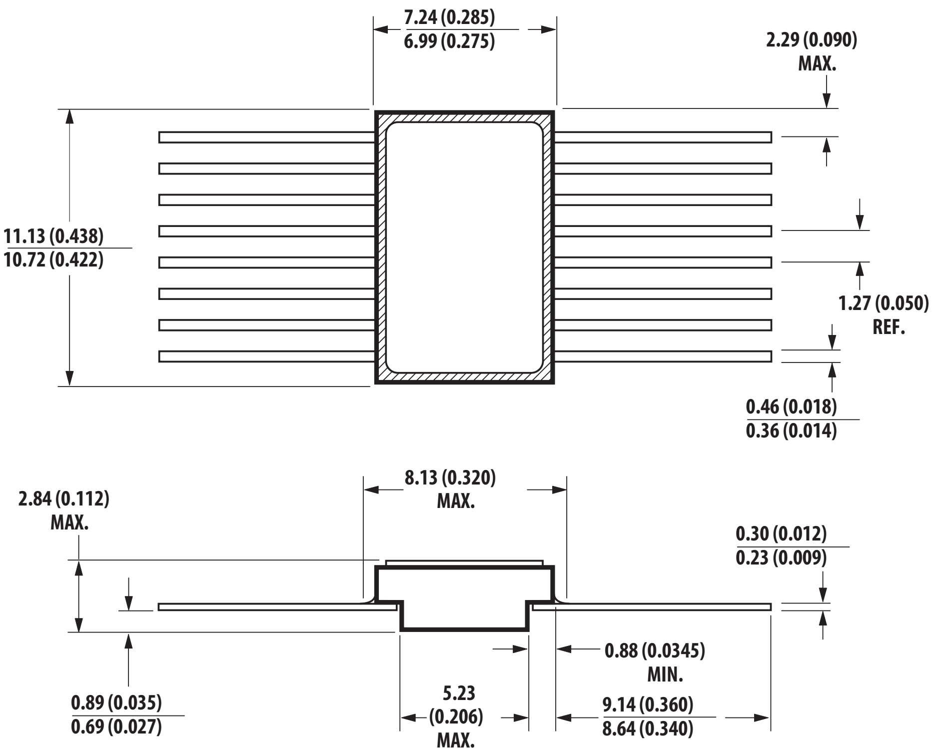
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin DIP, Through Hole, 1 and 2 Channels



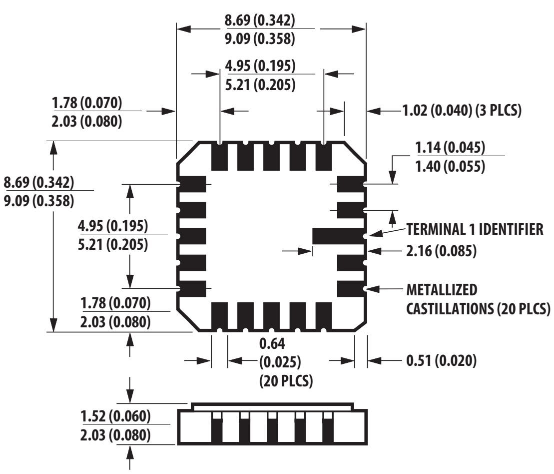
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

16-Pin Flat Pack, 4 Channels



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

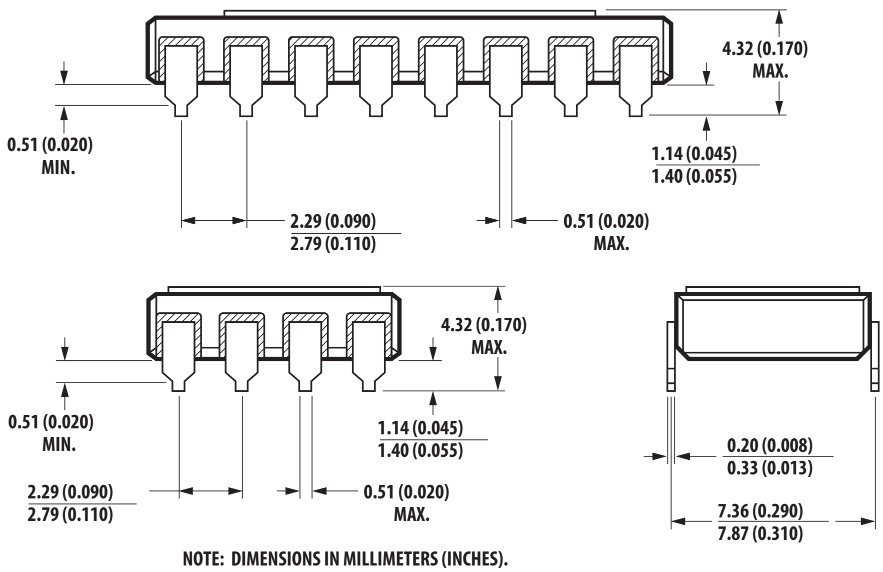
20-Terminal LCCC, Surface Mount, 2 Channels



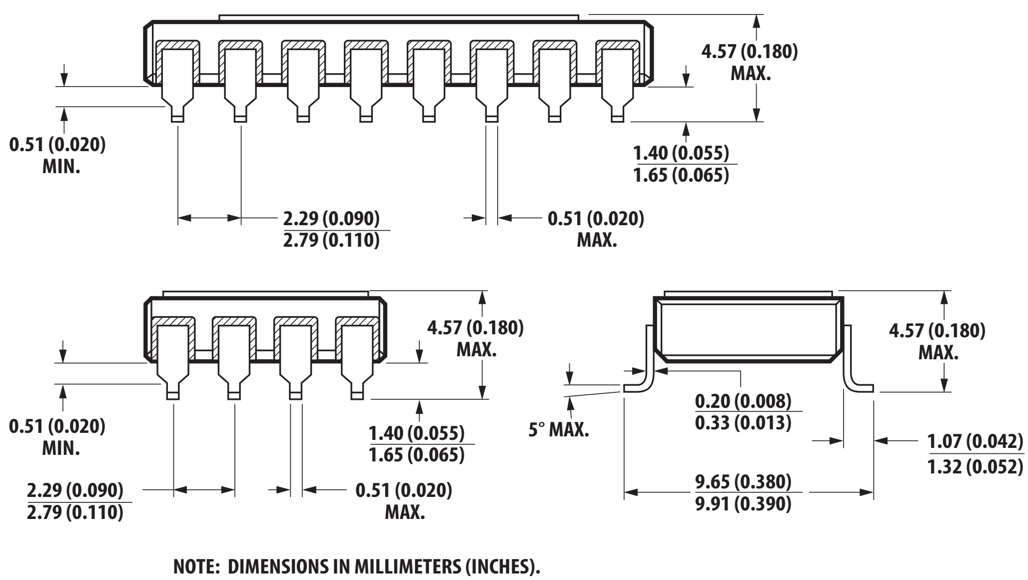
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Hermetic Optocoupler Options

<table>
<tr><th>Option</th><th>Description</th></tr>
<tr><td>100</td><td>
Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H, and Class K products in 8- and 16-pin DIP (see the following drawings for details).



</td></tr>
<tr><td>200</td><td>Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H, and Class K products in 8- and 16-pin DIP. DLA Drawing (SMD) part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder-dipped terminals as a standard feature.</td></tr>
<tr><td>300</td><td>
Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H, and Class K products in 8- and 16-pin DIP (see the following drawings for details). This option has solder-dipped leads.



</td></tr>
</table>

Absolute Maximum Ratings

No derating required up to +125°C.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	T_S	–65	+150	°C
Operating Temperature	T_A	–55	+125	°C
Junction Temperature	T_J	—	175	°C
Case Temperature	T_C	—	170	°C
Lead Solder Temperature		—	260 for 10 sec	°C
Average Input Forward Current	$I_{F\ AVG}$	—	20	mA
Peak Forward Input Current (each channel, 1 ms duration)	I_{FPK}	—	40	mA
Reverse Input Voltage	BV_R	See Electrical Characteristics.		
Average Output Current (each channel)	I_O	—	8	mA
Peak Output Current (each channel)	I_O	—	16	mA
Supply Voltage	V_{CC}	–0.5	+20	V
Output Voltage	V_O	–0.5	+20	V
Input Power Dissipation (each channel)	—	—	36	mW
Output Power Dissipation (each channel)	—	—	50	mW
Package Power Dissipation (each channel)	P_D	—	200	mW

Single-Channel 8-Pin, Dual-Channel 16-Pin, and LCCC Only

Parameter	Symbol	Min.	Max.	Unit
Emitter Base Reverse Voltage	V_{EBO}	—	3	V
Base Current (each channel)	I_B	—	5	mA

ESD Classification

(MIL-STD-883, Method 3015)

4N55, 4N55/883B, HCPL-257K, HCPL-5500/01/0K, and HCPL-6530/31/3K	▲, Class 1
HCPL-5530/31/3K, HCPL-6550/51/5K	●, Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Input Current, Low Level	I_{FL}	—	250	µA
Input Current, High Level	I_{FH}	12	20	mA
Supply Voltage, Output	V_{CC}	2	18	V

Electrical Characteristics

T_A = –55°C to +125°C, unless otherwise specified.

Parameter		Symbol	Group A[a] Subgroup	Test Conditions	Limits			Unit	Fig.	Note
					Min.	Typ.[b]	Max.			
Current Transfer Ratio		CTR	1, 2, 3	V_O = 0.4V, I_F = 16 mA, V_{CC} = 4.5V	9	20		%	2, 3	c, d
Logic High Output Current		I_{OH}	1, 2, 3	I_F = 0, I_F (other channels) = 20 mA $V_O = V_{CC}$ = 18V	—	5	100	µA	4	c
Output Leakage Current		I_{OLeak}	1, 2, 3	I_F = 250 µA, I_F (other channels) = 20 mA $V_O = V_{CC}$ = 18V	—	30	250	µA	4	c
Input-Output Insulation Leakage Current		I_{I-O}	1	V_{I-O} = 1500 Vdc RH ≤ 65%, T_A = 25°C, t = 5 s	—	—	1.0	µA	—	e, f
Input Forward Voltage		V_F	1, 2, 3	I_F = 20 mA	—	1.55	1.8	V	1	c, g
							1.9			c, h
Reverse Breakdown Voltage		BV_R	1, 2, 3	I_R = 10 µA	5	—		V	—	c, g
					3				—	c, h
Logic High Supply Current	Single Channel	I_{CCH}	1, 2, 3	V_{CC} = 18V, I_F = 0 mA	—	0.1	10	µA	—	c
	Dual Channel			V_{CC} = 18V, I_F = 0 mA (all channels)		0.2	20	µA	—	c, i
	Quad Channel			V_{CC} = 18V, I_F = 0 mA (all channels)		0.4	40	µA	—	c
Logic Low Supply Current	Single Channel	I_{CCL}	1, 2, 3	V_{CC} = 18V, I_F = 20 mA	—	35	200	µA	—	c
	Dual Channel			V_{CC} = 18V, $I_{F1} = I_{F2}$ = 20 mA		70	400	µA	—	c, i
	Quad Channel			V_{CC} = 18V, $I_{F1} = I_{F2} = I_{F3} = I_{F4}$ = 20 mA		140	800	µA	—	c
Propagation Delay Time to Logic High at Output		t_{PLH}	9, 10, 11	R_L = 8.2 kΩ, C_L = 50 pF, I_F = 16 mA V_{CC} = 5V,	—	1.0	6.0	µs	6, 9	c, j
Propagation Delay Time to Logic Low at Output		t_{PHL}			—	0.4	2.0			

a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at +25°C, +125°C, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

b. All typical values are at V_{CC} = 5 V, T_A = 25°C.

c. Each channel of a multi-channel device.

d. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, IF, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle, and system on time. In short, it is recommended that designers allow at least 20 to 25% guardband for CTR degradation.

e. All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.

f. This is a momentary withstand test, not an operating condition.

g. Required for 4N55, 4N55/883B, HCPL-257K, 5962-8767901, and 5962-8767905 types only.

h. Not required for 4N55, 4N55/883B, HCPL-257K, 5962-8767901, and 5962-8767905 types.

i. The 4N55, 4N55/883B, HCPL-257K, HCPL-6530, HCPL-6531, and HCPL-653K dual channel parts function as two independent single channel units. Use the single channel parameter limits. I_F = 0 mA for channel under test and I_F = 20 mA for other channels.

j. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

Typical Characteristics

$T_A = 25°C, V_{CC} = 5V.$

Parameter	Sym.	Test Conditions	Typ.	Unit	Fig.	Note
Input Capacitance	C_{IN}	$V_F = 0$ V, f = 1 MHz	60	pF	—	a
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	$I_F = 20$ mA	–1.5	mV/°C	—	a
Resistance (Input-Output)	R_{I-O}	$V_{I-O} = 500$ V	10^{12}	Ω	—	b
Capacitance (Input-Output)	C_{I-O}	f = 1 MHz	1.0	pF	—	a, c
Transistor DC Current Gain	h_{FE}	$V_O = 5V, I_O = 3$ mA	250	—	—	a
Small Signal Current Transfer Ratio	$\Delta I_O/\Delta I_F$	$V_{CC} = 5V, V_O = 2V$	21	%	7	a
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	$I_F = 0$ mA, $R_L = 8.2$ kΩ, V_O (min.) = 2.0V, $V_{CM} = 10V_{P-P}$	1000	V/µs	10	a, d
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	$I_F = 16$ mA, $R_L = 8.2$ kΩ, V_O (max.) = 0.8V, $V_{CM} = 10V_{P-P}$	–1000	V/µs	10	a, d
Bandwidth	BW		9	MHz	8	e

a. Each channel of a multi-channel device.

b. All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.

c. Measured between each input pair shorted together and all output connections for that channel shorted together.

d. CML is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$). CMH is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).

e. Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote. For the HCPL-553x the typical bandwidth is 2 MHz.

Multi-Channel Product Only

Parameter	Symbol	Test Conditions	Typ.	Unit	Note
Input-Input Insulation Leakage Current	I_{I-I}	Relative Humidity ≤ 65% $V_{I-I} = 500V, t = 5s$	1	pA	a, b
Resistance (Input-Input)	R_{I-I}	$V_{I-I} = 500V$	10^{12}	Ω	a
Capacitance (Input-Input)	C_{I-I}	f = 1 MHz	0.8	pF	a

a. Measured between adjacent input pairs shorted together for each multichannel device.

b. This is a momentary withstand test, not an operating condition.

Figure 1 Input Diode Forward Current vs. Forward Voltage

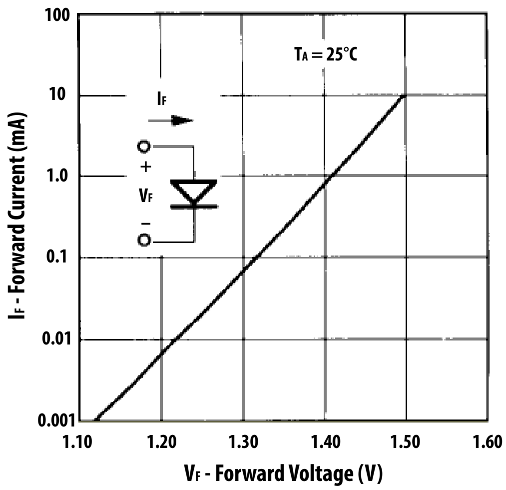


Figure 2 DC and Pulsed Transfer Characteristic

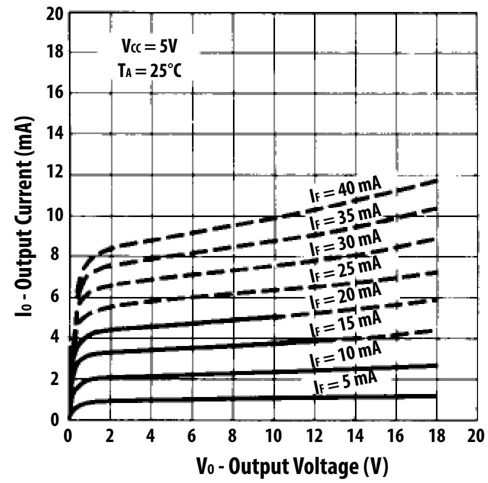


Figure 3 Normalized Current Transfer Ratio vs. Input Diode Forward Current

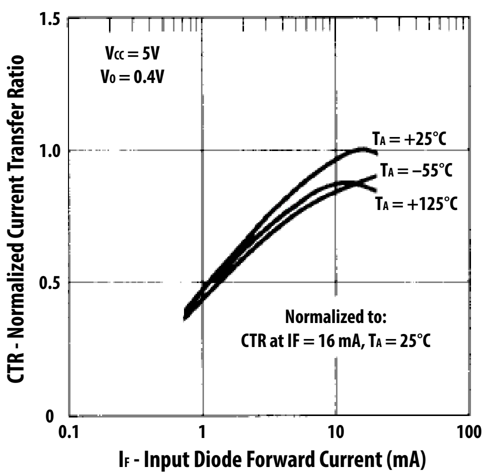


Figure 4 Logic High Output Current vs. Temperature

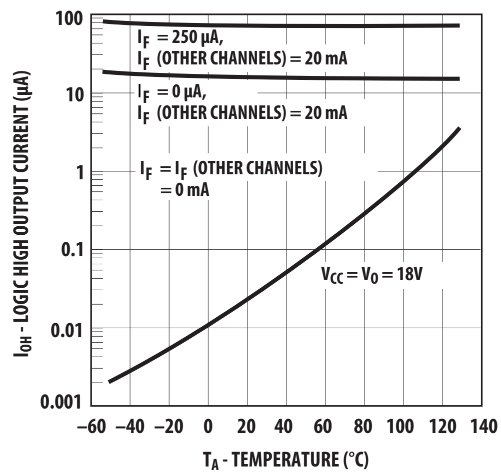


Figure 5 Logic Low Supply Current vs. Input Diode Forward Current

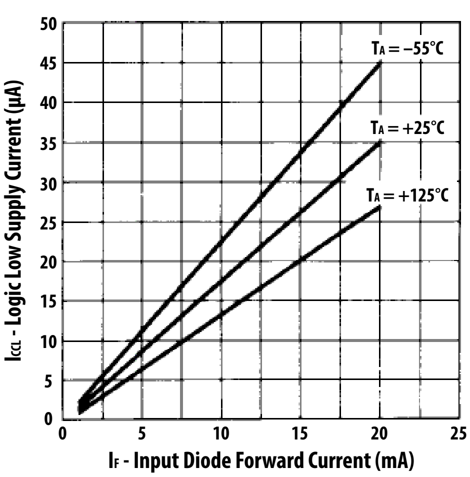


Figure 6 Propagation Delay vs. Temperature

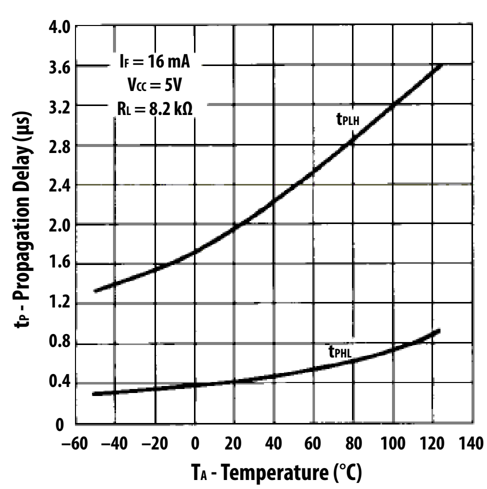


Figure 7 Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current

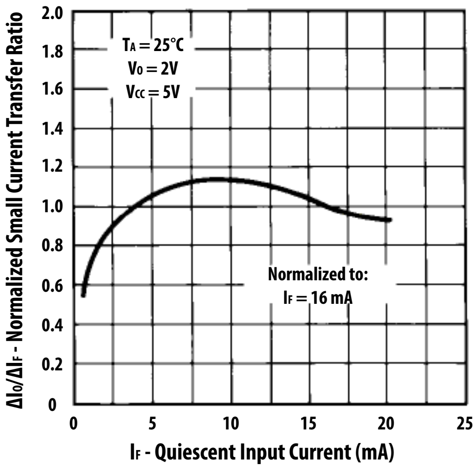
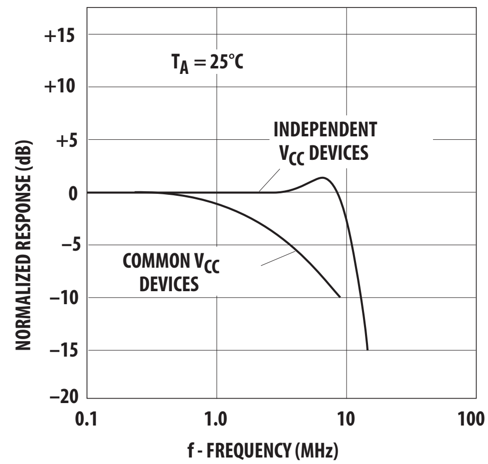
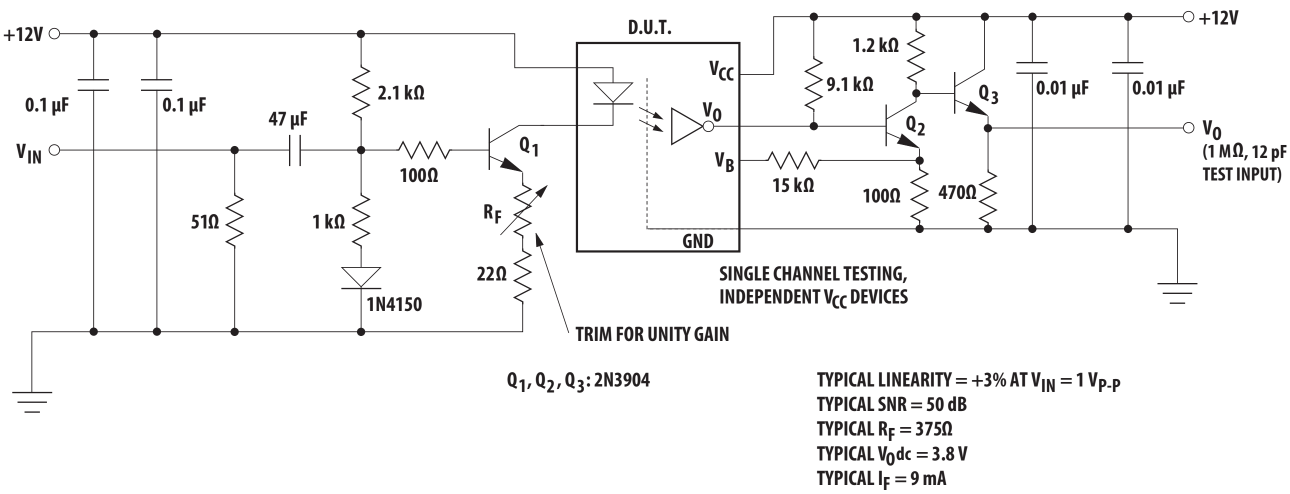


Figure 8 Frequency Response





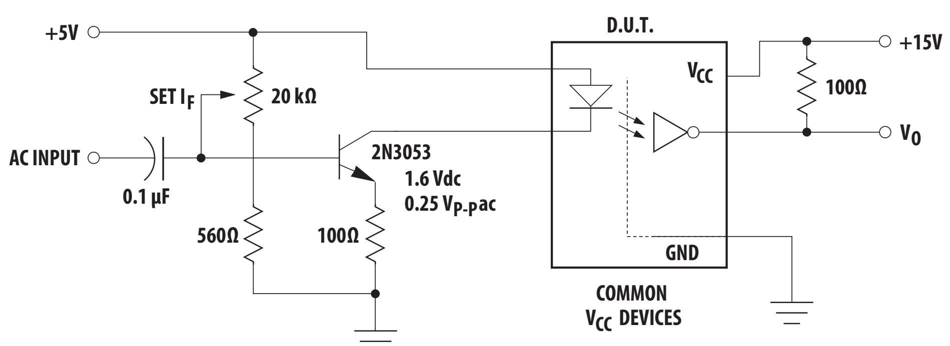


Figure 9 Switching Test Circuit

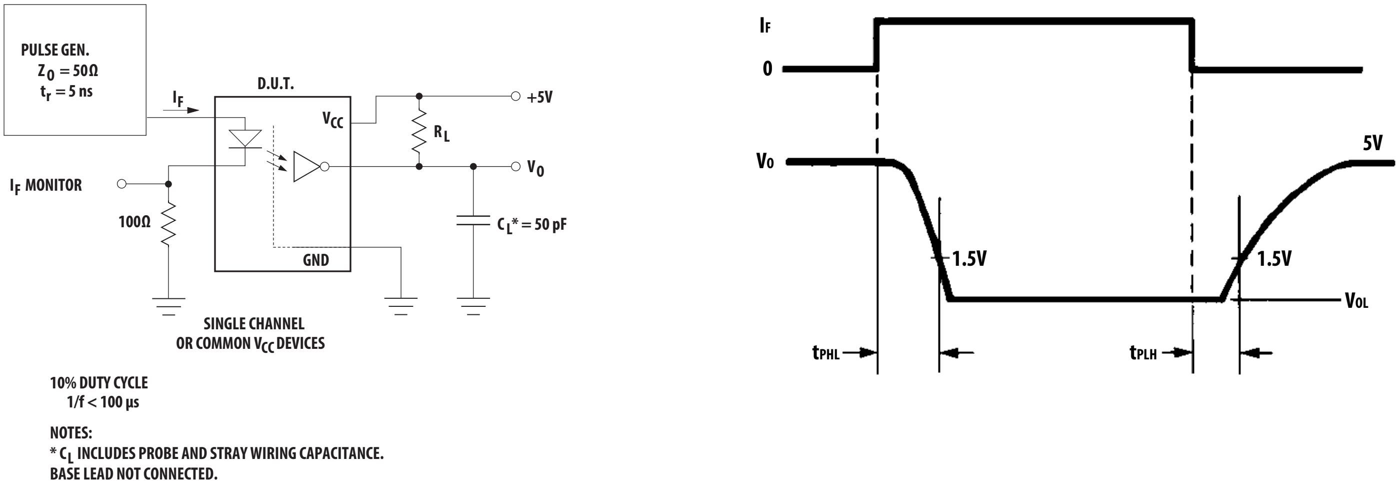


Figure 10 Test Circuit for Transient Immunity and Typical Waveforms

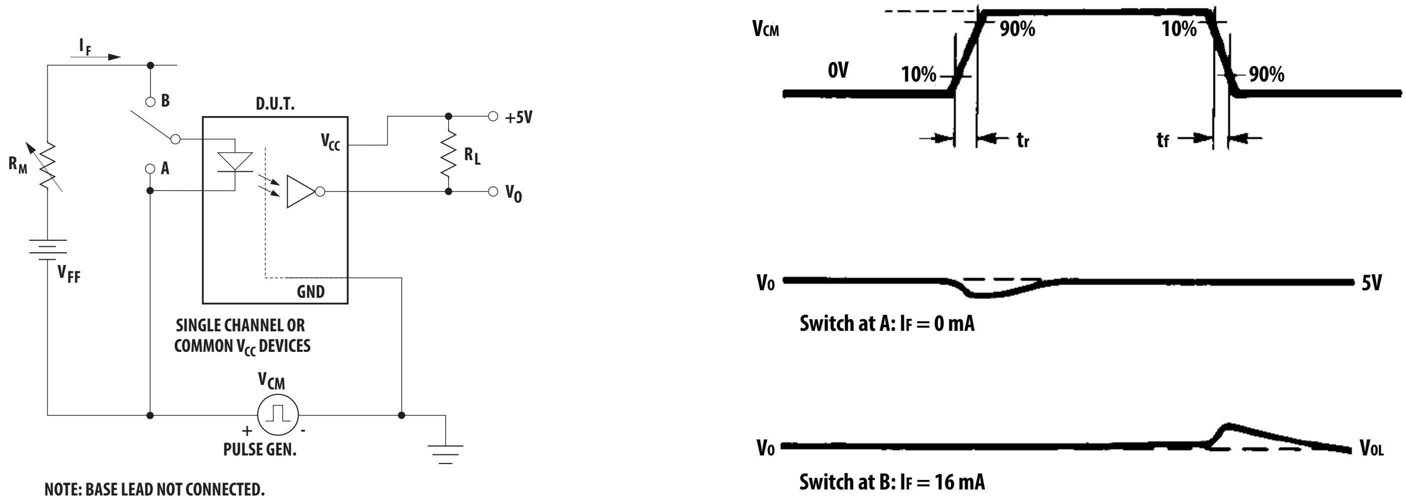
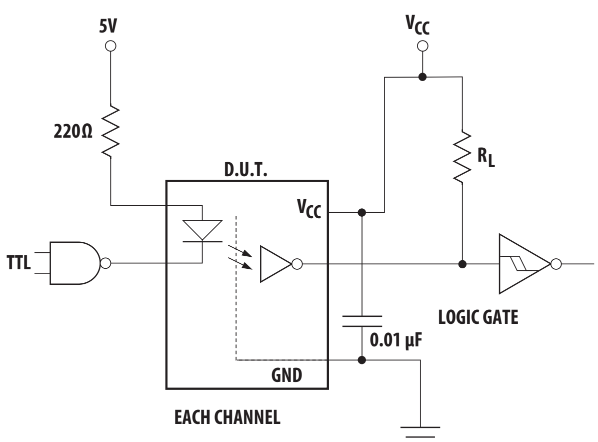


Figure 11 Recommended Logic Interface.



Logic Family	LSTTL	CMOS	
Device #	54LS14	CD40106BM	
V_{CC}	5V	5V	15V
R_L 5% Tolerance	18 kΩ[a]	8.2 kΩ	22 kΩ

a. The equivalent output load resistance is affected by the LSTTL input current and is approximately 8.2 kΩ. This is a worst case design that takes into account 25% degradation of CTR.

Figure 12 Operating Circuit for Burn-In and Steady State Life Tests (All Channels Tested Simultaneously)

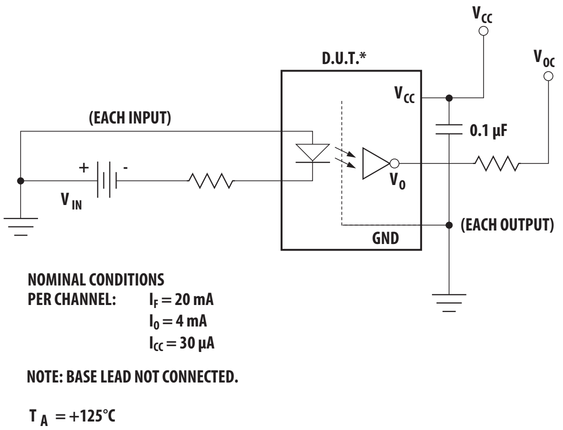
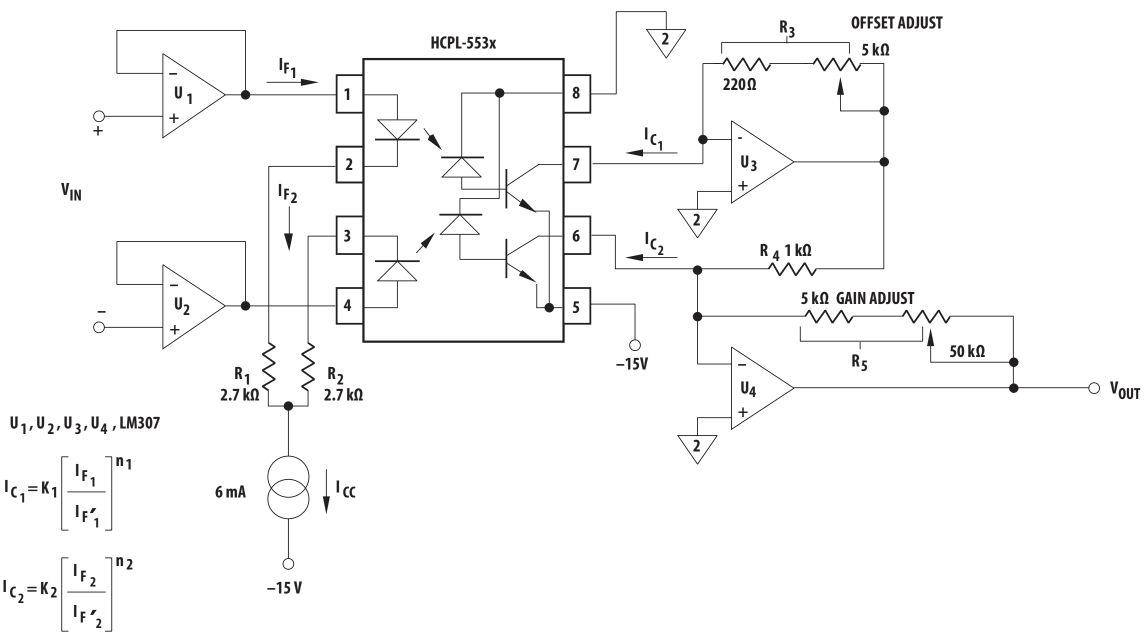


Figure 13 Isolation Amplifier Application Circuit



Description

The schematic uses a dual-channel, high-speed optocoupler (HCPL-553x) to function as a servo type DC isolation amplifier. This circuit operates on the principle that two optocouplers will track each other if their gain changes by the same amount over a specific operating region.

Performance of Circuit

- 1% linearity for 10V peak-to-peak dynamic range
- Gain drift: –0.03 %/°C
- Offset Drift: ±1 mV/°C
- 25 kHz bandwidth (limited by Op-Amps U1, U2)

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