# ACCL-9410

## High Speed Quad-Channel 3/1 Digital Isolator

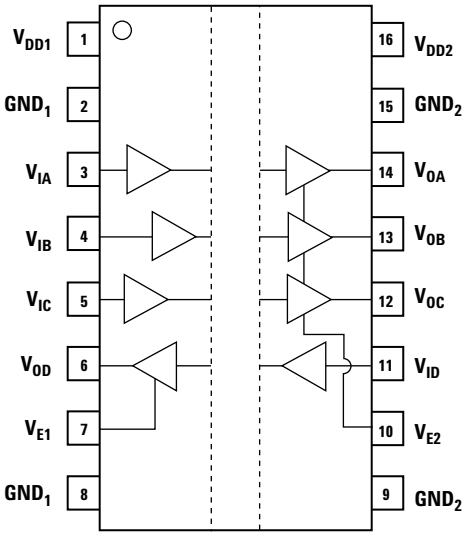
## Data Sheet

## Description

ACCL-9410 is a quad-channel bi-directional digital isolator. Using capacitive coupling through an insulation barrier, the isolator enables high speed digital transmissions. The device is capable of running at 25 MBd data rate, with propagation delay of 40ns.

ACCL-9410 is available in 150mils narrow body 16-pin SOIC package. The isolator operates at 3.3V/5V supply. The electrical DC and timing AC specifications are specified over the temperature range of -40°C to +125°C.

## Functional Diagram




## Features

- Supply voltage: 3.3 V / 5 V
- Wide operating temperature: -40 °C to 125 °C
- High data rate: 25 MBd
- Low power consumption: 2 mA per channel
- Low propagation delay: 40 ns max
- Pulse width distortion: 8 ns max
- Propagation delay part skew: 15 ns max
- Propagation delay channel skew: 8 ns max
- Output enable function
- Safety and Regulatory Approvals (Pending)
  - UL 1577

## Applications

- Industrial control isolated data interfaces, eg SPI
- High speed digital systems
- Isolated DC-DC converters
- Logic level shifting

**CAUTION** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments

# Ordering Information

| Part number | Channel Configuration | Option RoHS Compliant | Package | Surface Mount | Tape & Reel | Quantity |
|---|---|---|---|---|---|---|
| ACCL-9410 | Quad, Bi-directional, 3/1 | -000E | Narrow Body SOIC-16 | X | | 50 per tube |
| | | -500E | | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

Pending approval by the following organizations:

UL Pending UL1577, component recognition program

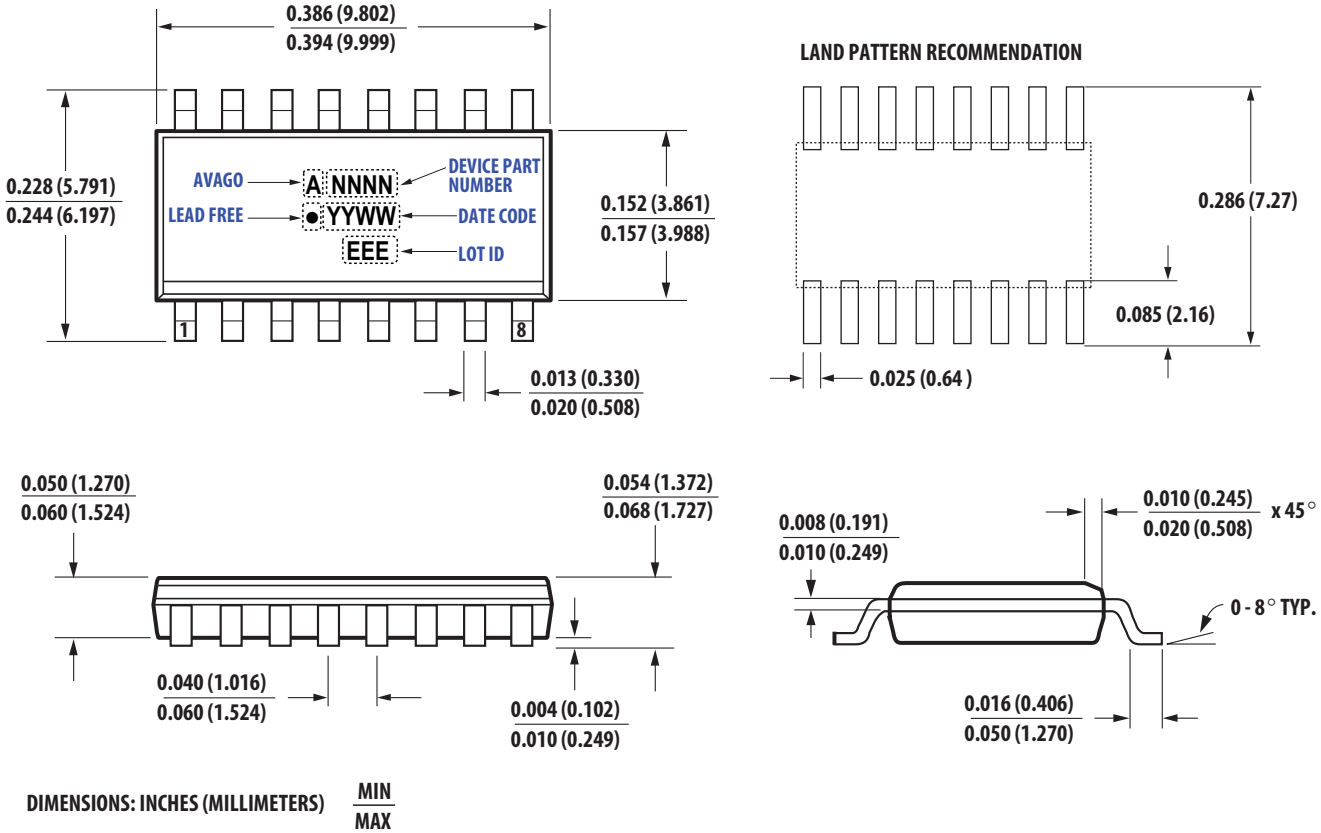
## Truth Table

| Input Supply VDD | Input | Output Supply VDD | Output Enable | Output | Remark |
|---|---|---|---|---|---|
| H | H | H | H or Open | H | Input logic High during normal operation. |
| H | L | H | H or Open | L | Input logic Low during normal operation. |
| H | X | H | L | Z | Output is at high impedance state when output Enable is set Low |
| L | X | H | H or Open | H | When input $V_{DD}$ is not powered, the output default is logic High. |
| X | X | L | X | Indeterminate | When output $V_{DD}$ is not powered, the output goes into indeterminate state. |

H - high level. L - Low level, X - insignificant

# Package Outline Drawings

## ACCL-9410 Narrow Body SOIC-16 Package




DIMENSIONS: INCHES (MILLIMETERS) MIN / MAX

# Insulation and Safety Related Specifications

| Parameter | Symbol | ACCL-9410 | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (Clearance) | L(101) | 4.0 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 4.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 400 | Volts | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

# Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | -55 | 125 | °C |
| Operating Temperature | $T_A$ | -40 | 125 | °C |
| Supply Voltage | $V_{DD1}$, $V_{DD2}$ | 0 | 6 | V |
| Input Voltage | $V_I$ | -0.5 | $V_{DD}$ + 0.5 | V |
| Output Voltage | $V_O$ | -0.5 | $V_{DD}$ + 0.5 | V |
| Average Output Current | $I_O$ | | 15 | mA |

# Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | 125 | °C |
| Supply Voltage (3.3V) | $V_{DD1}$, $V_{DD2}$ | 3.15 | 3.6 | V |
| Supply Voltage (5V) | $V_{DD1}$, $V_{DD2}$ | 4.5 | 5.5 | V |
| Logic High Input Voltage | $V_{IH}$ | 2 | $V_{DD}$ | V |
| Logic Low Input Voltage | $V_{IL}$ | 0 | 0.8 | V |

# Electrical Specifications (DC)

Over recommended temperature ($T_A$ = -40°C to 125°C) and supply voltage (4.5V≤$V_{DD1}$≤5.5V, 4.5V≤$V_{DD2}$≤5.5V), (3.15V≤$V_{DD1}$≤3.6V, 3.15V≤$V_{DD2}$≤3.6V), (4.5V≤$V_{DD1}$≤5.5V, 3.15V≤$V_{DD2}$≤3.6V) and (3.15V≤$V_{DD1}$≤3.6V, 4.5V≤$V_{DD2}$≤5.5V). All typical specifications are at $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Supply Current, No data [1] | $I_{DD1(0)}$ | | 2.8 | 5 | mA | $V_{DD1}$ = 3.6 V, DC |
| | | | 2.9 | 5 | mA | $V_{DD1}$ = 5.5 V, DC |
| Input Supply Current, 10MBd data (All channels) [2] | $I_{DD1(10)}$ | | 3.7 | 6 | mA | $V_{DD1}$ = 3.6 V, 5 MHz logic signal |
| | | | 4.1 | 7 | mA | $V_{DD1}$ = 5.5 V, 5 MHz logic signal |
| Input Supply Current, 25MBd data (All channels) [2] | $I_{DD1(25)}$ | | 5.0 | 8 | mA | $V_{DD1}$ = 3.6 V, 12.5 MHz logic signal |
| | | | 5.9 | 9 | mA | $V_{DD1}$ = 5.5 V, 12.5 MHz logic signal |
| Output Supply Current, No data [3] | $I_{DD2(0)}$ | | 6.5 | 10 | mA | $V_{DD2}$ = 3.6 V, DC |
| | | | 6.6 | 10 | mA | $V_{DD2}$ = 5.5 V, DC |
| Output Supply Current, 10MBd data (All channels) [4] | $I_{DD2(10)}$ | | 7.6 | 11 | mA | $V_{DD2}$ = 3.6 V, 5 MHz logic signal |
| | | | 8.1 | 12 | mA | $V_{DD2}$ = 5.5 V, 5 MHz logic signal |
| Output Supply Current, 25MBd data (All channels) [4] | $I_{DD2(25)}$ | | 9.2 | 13 | mA | $V_{DD2}$ = 3.6 V, 12.5 MHz logic signal |
| | | | 10.3 | 15 | mA | $V_{DD2}$ = 5.5 V, 12.5 MHz logic signal |
| Input Current | $I_I$ | -10 | | 10 | µA | |
| Logic High Output Voltage | $V_{OH}$ | $V_{DD}$-0.1 | $V_{DD}$ | | V | $I_O$ = -20 µA, $V_I$ = $V_{IH}$ |
| | | $V_{DD}$-1.0 | $V_{DD}$ | | V | $I_O$ = -4 mA, $V_I$ = $V_{IH}$ |
| Logic Low Output Voltage | $V_{OL}$ | | 0.02 | 0.1 | V | $I_O$ = 20 µA, $V_I$ = $V_{IL}$ |
| | | | 0.14 | 0.4 | V | $I_O$ = 4 mA, $V_I$ = $V_{IL}$ |
| High Level Enable Voltage | $V_{EH}$ | 0.7x$V_{DD}$ | | | V | |
| Low Level Enable Voltage | $V_{EL}$ | | | 0.3x$V_{DD}$ | V | |

# Switching Specifications (AC)

Over recommended temperature ($T_A$ = -40°C to 125°C) and supply voltage (4.5V≤$V_{DD1}$≤5.5V, 4.5V≤$V_{DD2}$≤5.5V), (3.15V≤$V_{DD1}$≤3.6V, 3.15V≤$V_{DD2}$≤3.6V), (4.5V≤$V_{DD1}$≤5.5V, 3.15V≤$V_{DD2}$≤3.6V) and (3.15V≤$V_{DD1}$≤3.6V, 4.5V≤$V_{DD2}$≤5.5V). All typical specifications are at $T_A$ = 25 °C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low Output | $t_{PHL}$ | | 29 | 40 | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 27 | 40 | | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Propagation Delay Time to Logic High Output | $t_{PLH}$ | | 29 | 40 | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 27 | 40 | | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Pulse Width | $t_{PW}$ | 40 | | | ns | CL= 15pF, CMOS Signal Levels |
| Maximum Data Rate | | | | 25 | MBd | CL= 15pF, CMOS Signal Levels |
| Pulse Width Distortion \| $t_{PHL}$ - $t_{PLH}$ \| | PWD | | 0.3 | 8 | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 0.5 | 8 | ns | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Propagation Delay Channel Skew | $t_{CSK}$ | | 2 | 8 | ns | CL= 15pF, CMOS Signal Levels |
| Propagation Delay Part Skew | $t_{PSK}$ | | | 15 | ns | CL= 15pF, CMOS Signal Levels |
| Propagation Delay Time of Enable from $V_{EH}$ to $V_{EL}$ | $t_{ELH}$ | | 8 | | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 6 | | | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Propagation Delay Time of Enable from $V_{EL}$ to $V_{EH}$ | $t_{EHL}$ | | 26 | | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 23 | | | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Output Rise Time (10% - 90%) | $t_R$ | | 3.5 | | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 2 | | | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Output Fall Time (90% - 10%) | $t_F$ | | 2.5 | | ns | $V_{DD1}$ = $V_{DD2}$ = 3.3 V, $C_L$= 15pF, CMOS Signal Levels |
| | | | 2 | | | $V_{DD1}$ = $V_{DD2}$ = 5 V, $C_L$= 15pF, CMOS Signal Levels |
| Common Mode Transient Immunity at Logic High Output | \| $CM_H$ \| | | 10 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 C, $V_{DD}$ = 5V, $V_O$ > 2V |
| Common Mode Transient Immunity at Logic Low Output | \| $CM_L$ \| | | 10 | | kV/µs | $V_{CM}$ = 1000 V, $T_A$ = 25 C, $V_{DD}$ = 0 V, $V_O$ < 0.8 V |

# Package Characteristics

All typical at $T_A$ = 25 °C

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input-Output Insulation [5] | $V_{ISO}$ | 1500 | | | Vrms | RH < 50% for 1 min. $T_A$ = 25 °C |
| Input-Output Resistance | $R_{I-O}$ | | $10^{15}$ | | | $V_{I-O}$ = 500 V |
| Input-Output Capacitance | $C_{I-O}$ | | 1.6 | | pF | f=1 MHz, $T_A$ = 25 °C |
| Package Power Dissipation | $P_{PD}$ | | | 155 | mW | |

Notes:
1. $I_{DD1(0)}$ is the supply current consumption at $V_{DD1}$ when there is no signal to all inputs.
2. $I_{DD1(F)}$ is the supply current consumption at $V_{DD1}$ when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.
3. $I_{DD2(0)}$ is the supply current consumption at $V_{DD2}$ when there is no signal to all inputs.
4. $I_{DD2(F)}$ is the supply current consumption at $V_{DD2}$ when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.
5. In accordance with UL 1577, each isolator is proof tested by applying an insulation test voltage ≥ 1800 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).

# Performance

**Figure 1 Typical $I_{DD1(0)}$ vs Temperature**

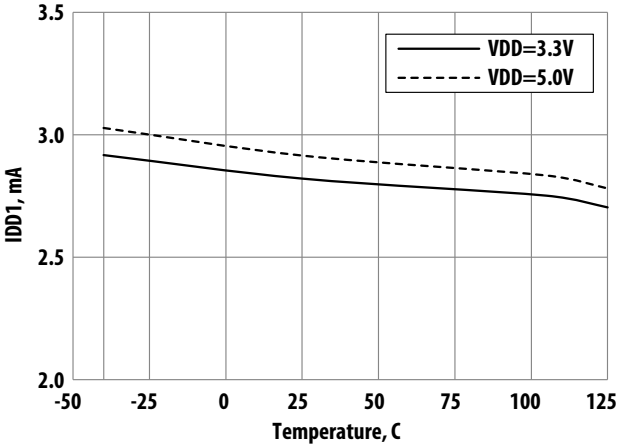



**Figure 2 Typical $I_{DD1(25)}$ vs Temperature**

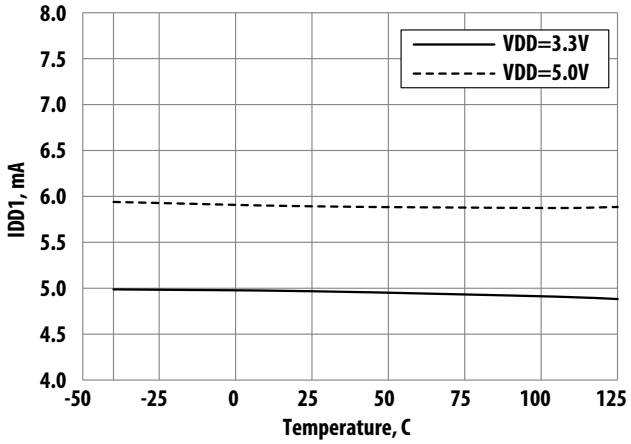


**Figure 3 Typical $I_{DD2(0)}$ vs Temperature**

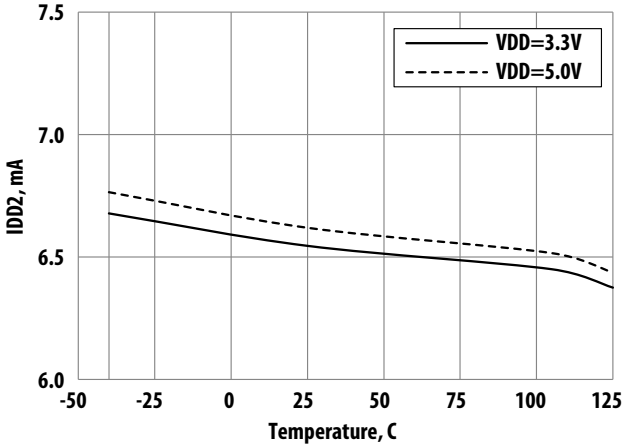



**Figure 4 Typical $I_{DD2(25)}$ vs Temperature**

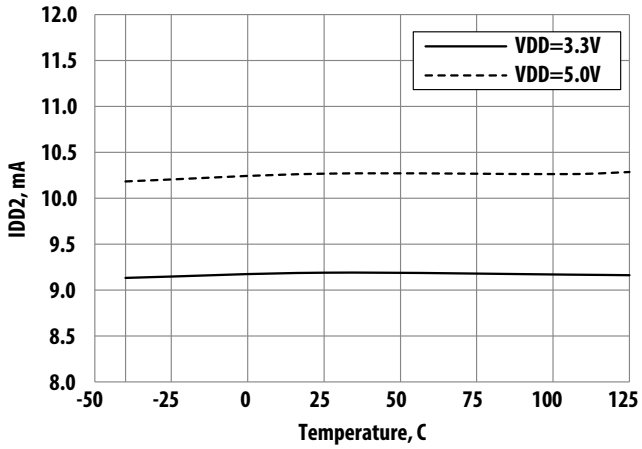



**Figure 5 Typical Propagation Delay $t_{PLH}$ vs Temperature**

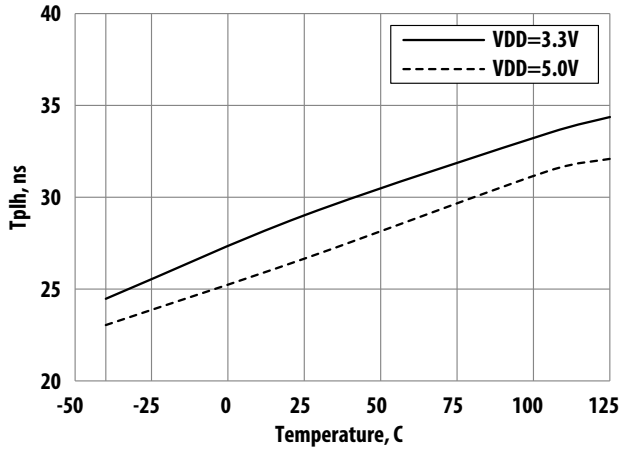



**Figure 6 Typical Propagation Delay $t_{PHL}$ vs Temperature**

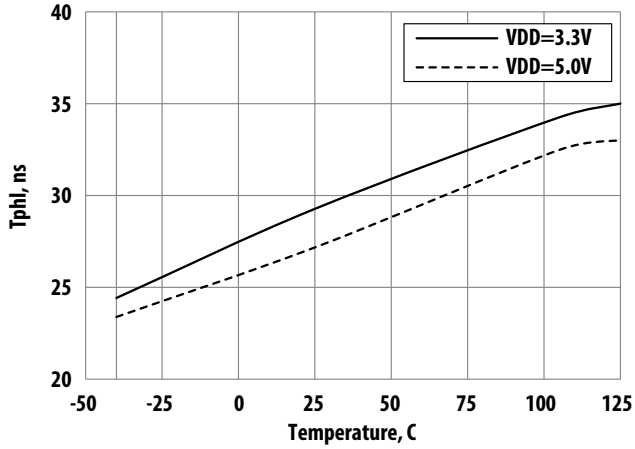



**Figure 7 Typical Pulse Width Distortion PWD vs Temperature**

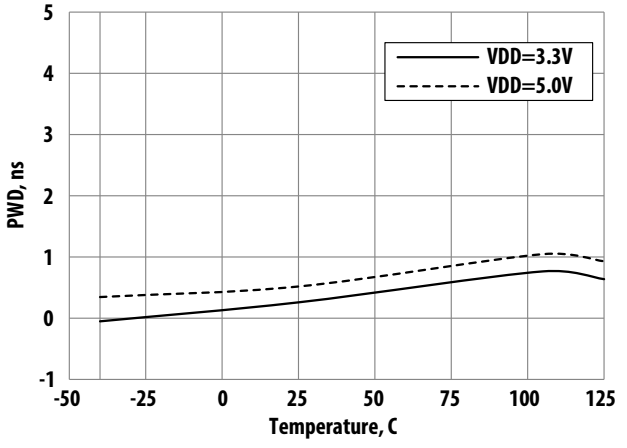
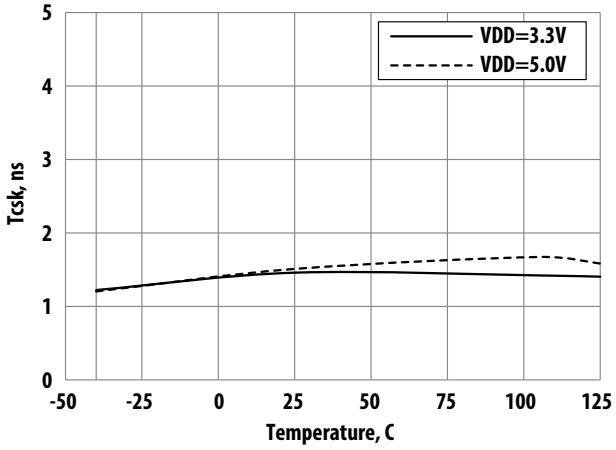


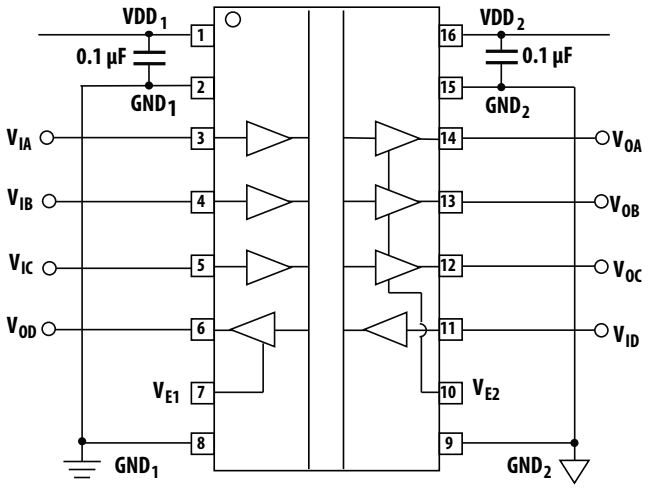

**Figure 8 Typical Propagation Delay Channel Skew $t_{CSK}$ vs Temperature**



## Bypassing and PC Board Layout

The ACCL-9410 digital isolator is easy to use. No external interface circuitry is required because its high speed CMOS IC technology allows CMOS logic to be connected directly to the inputs and outputs. As shown in Figure 9, the external components required for proper operation are two bypass capacitors for decoupling the power supply. Capacitor values should be 0.1 µF and the capacitor be placed as close as possible to the isolator. The total lead length between both capacitor ends and the power supply pins is not more than 20 mm.

**Figure 9 Typical Schematic of ACCL-9410 on PC Board**

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