

# ACPL-M61U-000E

## Wide Operating Temperature 10MBd Digital Optocoupler with R<sup>2</sup>Coupler™ Isolation



### Data Sheet



#### Description

This small outline wide operating temperature, high CMR, high speed, logic gate optocoupler is a single channel device in a five lead miniature footprint.

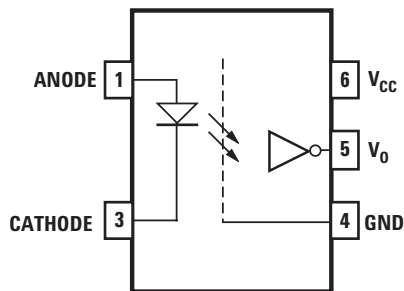
The ACPL-M61U optically coupled gates combine a AlGaAs light emitting diode and an integrated high gain photo detector. The output of the detector IC is an Open-collector Schottky-clamped transistor. The internal shield provides a guaranteed minimum common mode transient immunity specification of 10,000 V/μs at V<sub>CM</sub>=1000V.

This optocoupler is suitable for use in industrial high speed communications logic interfacing with low propagation delays, input/output buffering and is recommended for use in high operating temperature environment.

This unique design provides maximum AC and DC circuit isolation while achieving TTL compatibility. The optocoupler AC and DC operational parameters are guaranteed from -40°C to 125°C.

Avago R<sup>2</sup>Coupler isolation products provide the reinforced insulation and reliability needed for critical in automotive and high temperature industrial applications.

#### Functional Diagram



The connection of a 0.1 μF bypass capacitor between pins 4 and 6 is recommended.

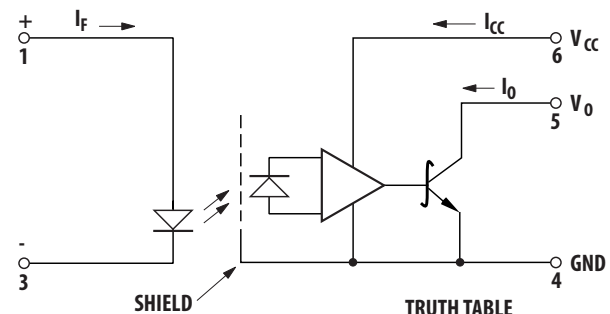
#### Features

- High Temperature and Reliability CANBus communication interface for Industrial Application.
- Min 10 kV/μs High Common-Mode Rejection at V<sub>CM</sub> = 1000V
- Compact, Auto-Insertable SO5 Packages
- Wide Temperature Range: -40°C ~ 125°C
- High Speed: 10MBd (Typical)
- Low LED Drive Current: 6.5mA (typ)
- Low Propagation Delay: 100ns (max)
- Worldwide Safety Approval:
  - UL 1577, 3750 V<sub>RMS</sub>/1 min.
  - CSA File CA88324, Notice #5

#### Applications

- CANBus Communications Interface
- High Temperature Digital Signal Isolation
- Micro-controller Interface
- Digital isolation for A/D, D/A conversion

#### Schematic



USE OF A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 6 AND 4 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Ordering Information

Part number	Option		Surface Mount	Tape & Reel	Quantity
	RoHS Compliant	Package			
ACPL-M61U	-000E	SO-5	X		100 per tube
	-500E		X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-M61U-500E to order product of SO-5 Surface Mount package in Tape and Reel packaging with RoHS compliant.

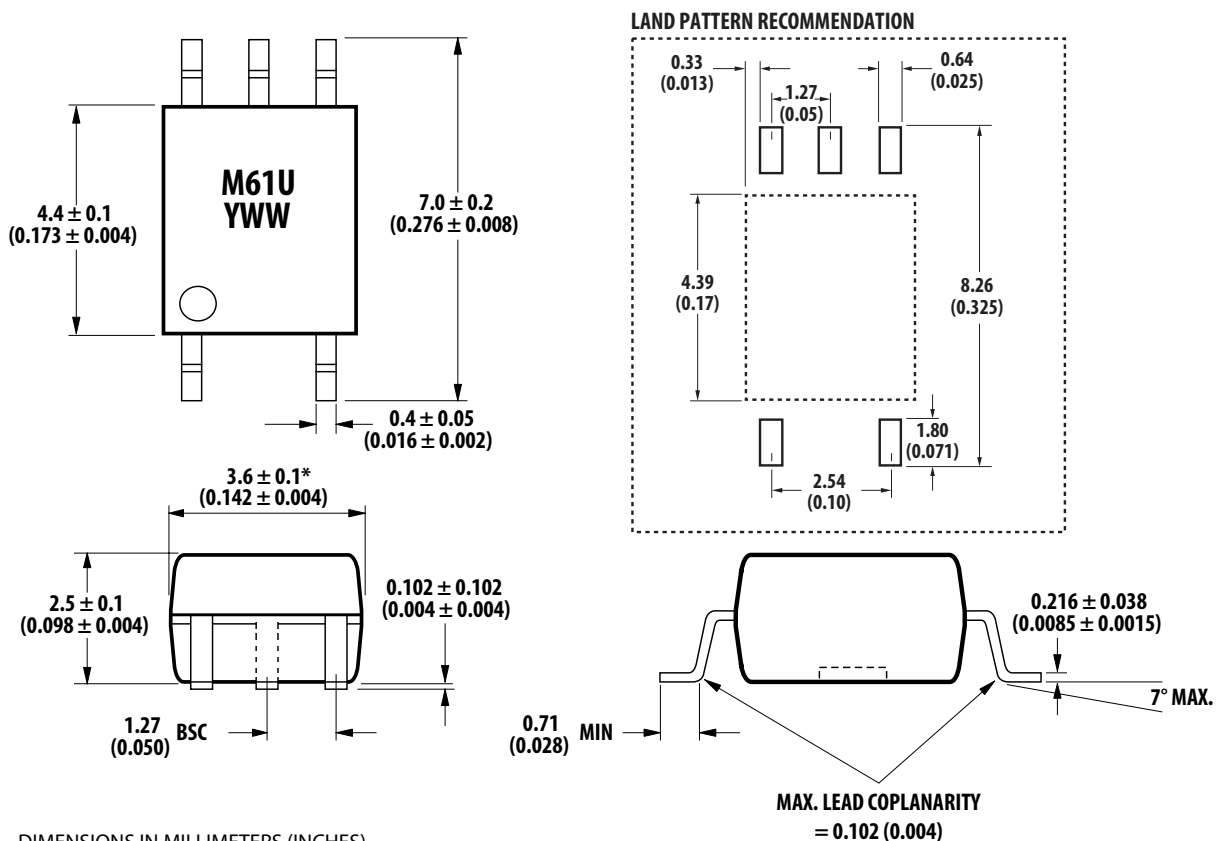
Example 2:

ACPL-M61U-000E to order product of SO-5 Surface Mount package in tube packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings

ACPL-M61U-000E Small Outline SO-5 Package (JEDEC MO-155)



DIMENSIONS IN MILLIMETERS (INCHES)

\* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

## Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

## Regulatory Information

The ACPL-M61U-000E is approved by the following organizations:

<b>UL</b>	Approved under UL 1577, component recognition program up to $V_{ISO} = 3750 V_{RMS}$ .
<b>CSA</b>	Approved under CSA Component Acceptance Notice #5

### IEC/EN/DIN EN 60747-5-5 Insulation Characteristics\* (Option x6xx)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage $\leq 150 V_{rms}$ for rated mains voltage $\leq 300 V_{rms}$ for rated mains voltage $\leq 600 V_{rms}$		I – IV I – III I – II	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	567	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m=1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1063	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m=10$ sec, Partial discharge $< 5$ pC	$V_{PR}$	907	$V_{peak}$
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	6000	$V_{peak}$
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	$T_S$	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	150	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at $T_S, V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

\* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

### Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M61U	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	$\geq 5$	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	$\geq 5$	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_S$	-55	125	°C	
Operating Temperature	$T_A$	-40	125	°C	
Lead Soldering Cycle	Temperature		260	°C	
	Time		10	sec	
Input Current (50% duty cycle, 1ms pulse width) ( $\leq 1\mu\text{s}$ pulse width, 300ps)	Average	$I_{F(\text{avg})}$	20	mA	12
	Peak	$I_{F(\text{peak})}$	40	mA	
	Transient	$I_{F(\text{trans})}$	100	mA	
Reversed Input Voltage	$V_R$		5	V	
Input Power Dissipation	$P_I$		30	mW	13
Output Power Dissipation	$P_O$		85	mW	14
Output Collector Current	$I_O$		50	mA	
Supply Voltage (Pins 6-4)	$V_{CC}$	-0.5	7	V	
Output Voltage (Pins 5-4)	$V_O$	-0.5	7	V	

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	$V_{CC}$	4.5	5.5	V
Operating Temperature	$T_A$	-40	125	°C
Input Current, Low Level	$I_{FL}^*$	0	250	$\mu\text{A}$
Input Current, High Level	$I_{FH}$	5	15	mA
Fan Out ( $R_L = 1\text{k}\Omega$ )	N		5	TTL Loads
Output Pull-Up Resistor	$R_L$	330	4,000	$\Omega$

\* The off condition can also be guaranteed by ensuring that  $V_{F(\text{off})} \leq 0.8\text{Volts}$

## Electrical Specifications (DC)

Over recommended operating Temperature  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions	Fig.	Note
Input Threshold Current	$I_{TH}$		2	5	mA	$V_{CC} = 5.5\text{V}$ , $I_O \geq 13\text{mA}$ , $V_O = 0.6\text{V}$	4	
High Level Output Current	$I_{OH}$		5.5	100	$\mu\text{A}$	$V_{CC} = 5.5\text{V}$ , $V_O = 5.5\text{V}$ , $V_F = 0.5\text{V}$	1	
Low Level Output Voltage	$V_{OL}$		0.4	0.6	V	$V_{CC} = 5.5\text{V}$ , $I_F = 6.5\text{mA}$ $I_{OL}(\text{Sinking}) = 13\text{mA}$	2, 4, 5	
High Level Supply Current	$I_{CCH}$		7.0	10.0	mA	$V_{CC} = 5.5\text{V}$ , $I_F = 0\text{mA}$		
Low Level Supply Current	$I_{CCL}$		9.0	13.0	mA	$V_{CC} = 5.5\text{V}$ , $I_F = 10\text{mA}$ ,		
Input Forward Voltage	$V_F$	1.45	1.5	1.85	V	$T_A = 25^\circ\text{C}$ , $I_F = 10\text{mA}$		
		1.35	1.5	1.95	V	$I_F = 10\text{mA}$		
Input Reversed Breakdown Voltage	$BV_R$	5			V	$I_R = 10\mu\text{A}$		
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$		-1.5		$\text{mV}/^\circ\text{C}$	$I_F = 10\text{mA}$	3, 12	

\*All Typical at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .

## Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V <sub>ISO</sub>	3750			V <sub>rms</sub>	RH ≤ 50%, t = 1 min; T <sub>A</sub> = 25°C		
Input-Output Resistance	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	V <sub>I-O</sub> = 500 Vdc		
Input-Output Capacitance	C <sub>I-O</sub>		0.6		pF	f = 1 MHz; V <sub>I-O</sub> = 0 Vdc		

## Switching Specifications (AC)

Over recommended temperature T<sub>A</sub> = -40°C to 125°C, V<sub>CC</sub> = 5.0 V, I<sub>F</sub> = 6.5mA unless Otherwise Specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Low Output Level	t <sub>PHL</sub>	46	75	100	ns	T <sub>A</sub> =25°C R <sub>L</sub> = 350Ω C <sub>L</sub> = 15pF I <sub>F</sub> = 6.5mA	6, 7, 8	6
Propagation Delay Time to High Output Level	t <sub>PLH</sub>	50	75	100	ns	T <sub>A</sub> =25°C	6, 7, 8	5
Propagation Delay Skew	t <sub>PSK</sub>		40		ns		14, 15	10, 11
Pulse Width Distortion	t <sub>PHL</sub> - t <sub>PLH</sub>	3.5	35		ns		9	10
Output Rise Time (10% - 90%)	t <sub>rise</sub>	24			ns		10	
Output Fall Time (10% - 90%)	t <sub>fall</sub>	10			ns		10	
Common Mode Transient Immunity at High Output Level	CM <sub>H</sub>	15	30		kV/μs	V <sub>CM</sub> =1000Vp-p V <sub>O</sub> (min) = 2V I <sub>F</sub> = 0mA T <sub>A</sub> =25°C R <sub>L</sub> =350Ω	11	7,9
Common Mode Transient Immunity at Low Output Level	CM <sub>L</sub>	15	30		kV/μs	V <sub>CM</sub> =1000Vp-p V <sub>O</sub> (max) = 0.8V I <sub>F</sub> = 6.5mA T <sub>A</sub> =25°C R <sub>L</sub> =350Ω		8,9

\*All Typical at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V.

### Notes:

- By-passing of the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler. The total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
- Peaking circuits may produce transient input currents up to 40 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
- Device considered a two terminal device: pins 1 and 3 shorted together and pins 4, 5 and 6 shorted together.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V<sub>RMS</sub> for 1 second (Leakage detection current limit, I<sub>I-O</sub> ≤ 5 μA).
- The t<sub>PLH</sub> propagation delay is measured from 3.25 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
- The t<sub>PHL</sub> propagation delay is measured from 3.25 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
- CM<sub>H</sub> is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V<sub>OUT</sub> > 2.0V).
- CM<sub>L</sub> is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V<sub>OUT</sub> < 0.8V).
- For sinusoidal voltages, (dV<sub>CM</sub>/dt)<sub>max</sub> = πf<sub>CM</sub>V<sub>CM</sub>(p-p).
- See application section; "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.
- t<sub>PSK</sub> is equal to the worst case difference in t<sub>PHL</sub> and/or t<sub>PLH</sub> that will be seen between units at any given temperature within the worst case operating condition range.
- Input current derates linearly above 85°C free-air temperature at a rate of 0.25 mA/°C.
- Input power derates linearly above 85°C free-air temperature at a rate of 0.375mW/°C.
- Output power derates linearly above 85°C free-air temperature at a rate of 0.475 mW/°C.

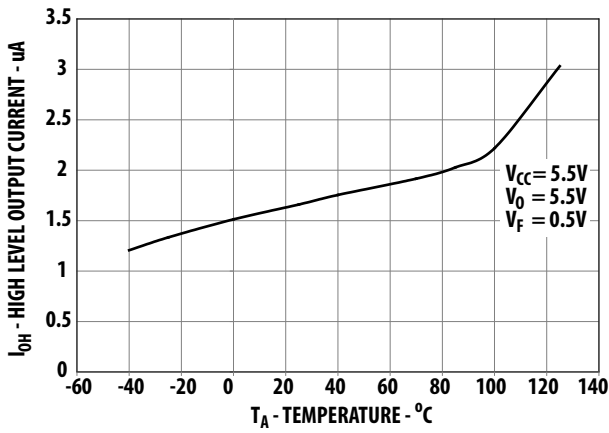


Figure 1. High Level Output Current vs Temperature

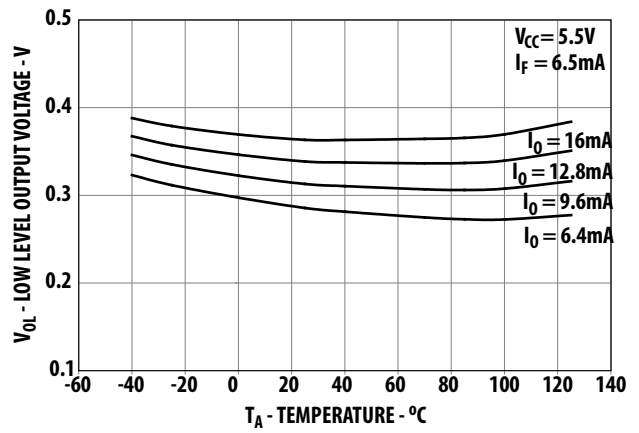


Figure 2. Low Level Output Voltage vs. Temperature

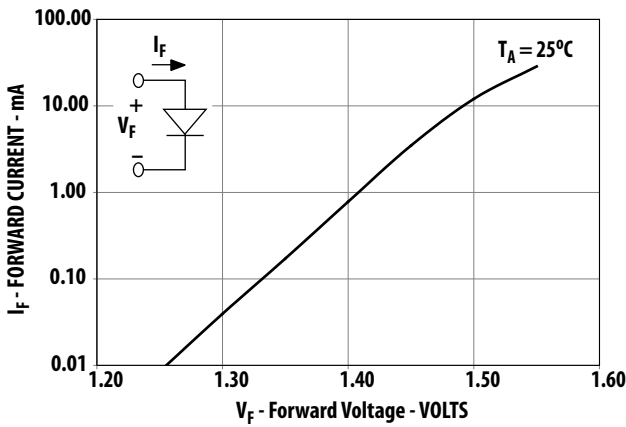


Figure 3. Input Current vs Forward Voltage

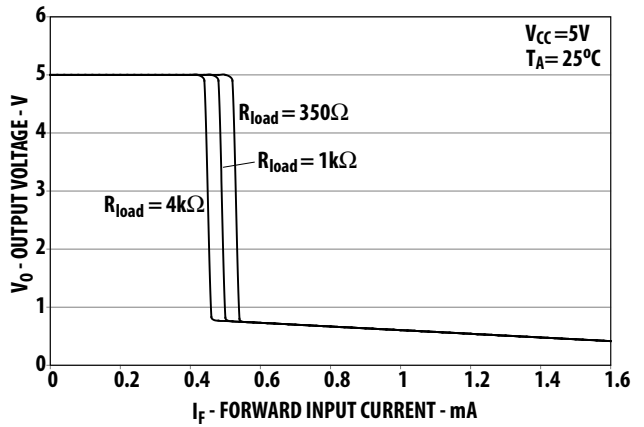


Figure 4. Output Voltage vs Forward Input current

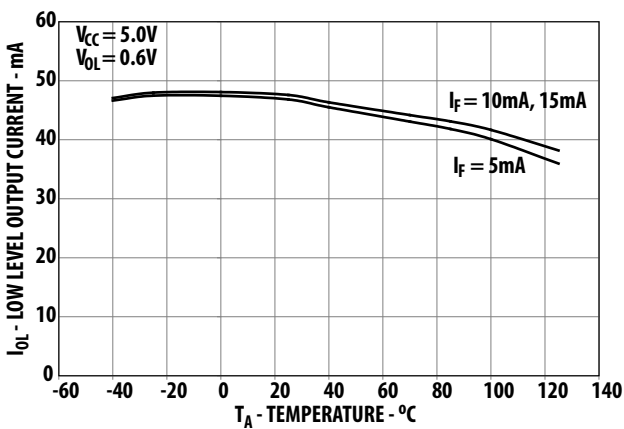


Figure 5. Low Level Output Current vs. Temperature

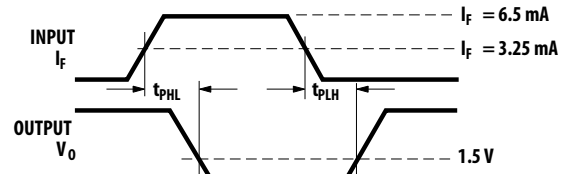
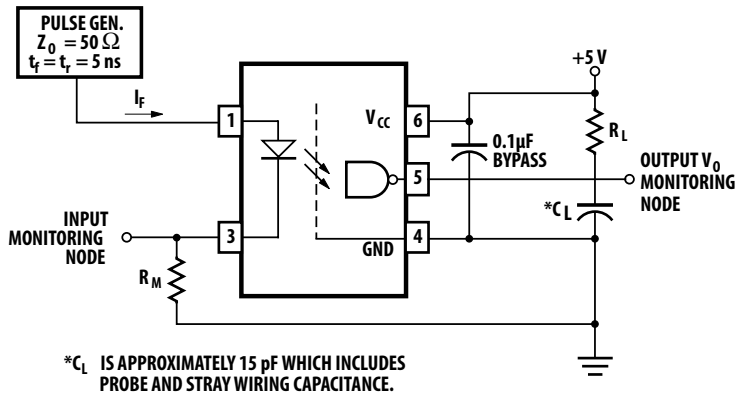


Figure 6. Test Circuit for  $t_{pHL}$  and  $t_{pLH}$

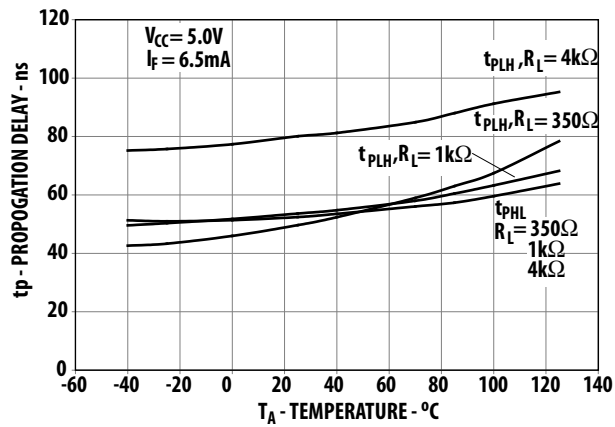


Figure 7. Propagation Delay vs. Temperature

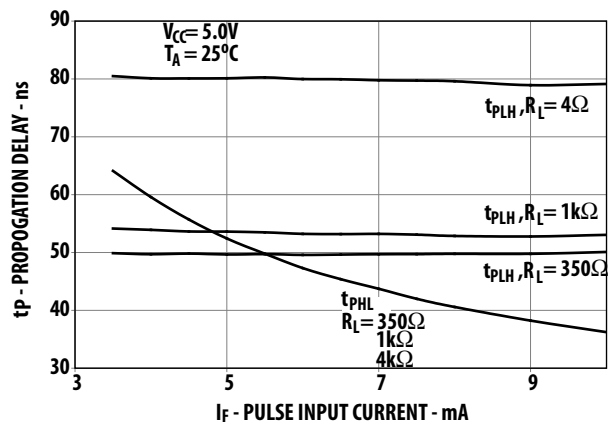


Figure 8. Propagation Delay vs. Pulse Input Current

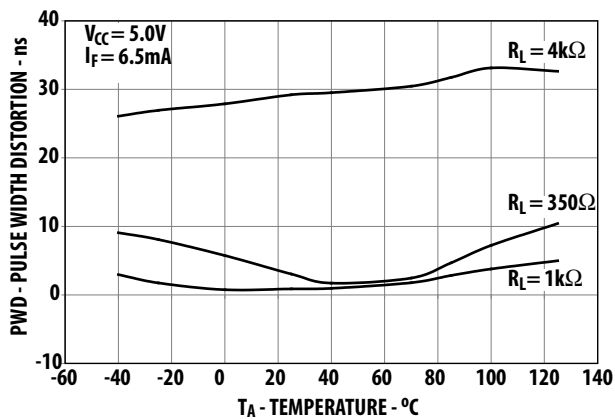


Figure 9. Pulse Width Distortion vs Temperature

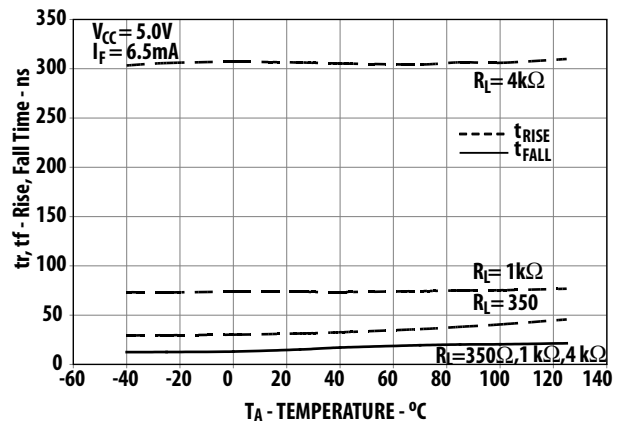


Figure 10. Rise and Fall Time vs. Temperature

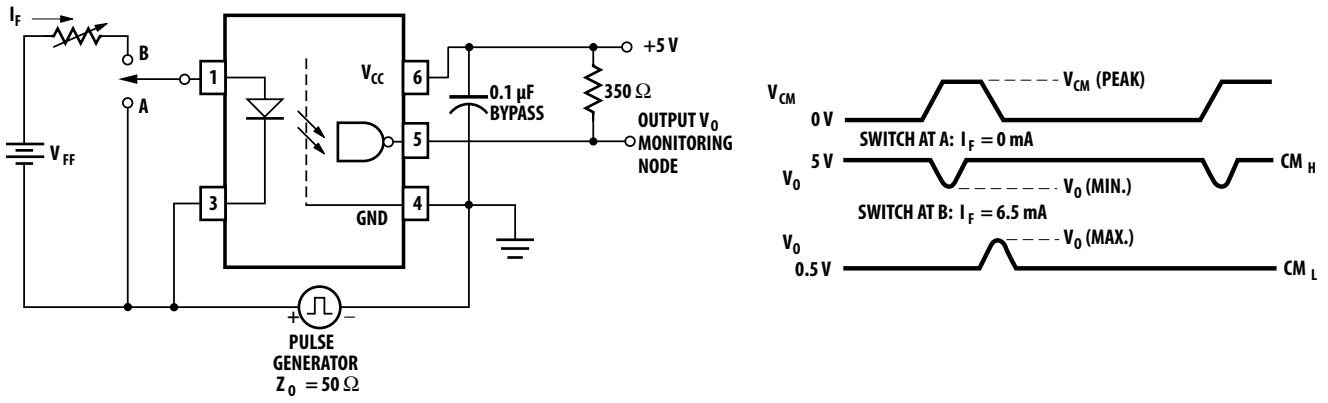


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

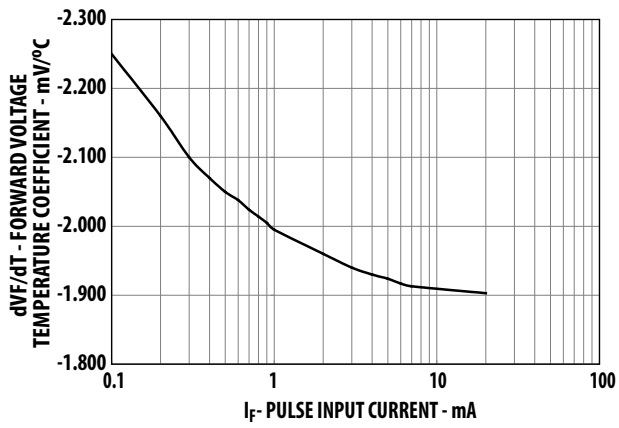


Figure 12. Temperature Coefficient for Forward Voltage vs. Input Current

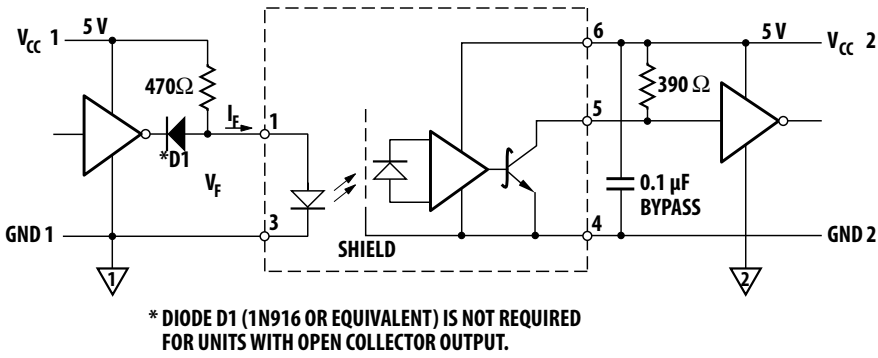


Figure 13. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.



## Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high ( $t_{PLH}$ ) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low ( $t_{PHL}$ ) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when  $t_{PLH}$  and  $t_{PHL}$  differ in value. PWD is defined as the difference between  $t_{PLH}$  and  $t_{PHL}$  and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew,  $t_{PSK}$ , is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either  $t_{PLH}$  or  $t_{PHL}$ , for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and

operating temperature). As illustrated in Figure 14, if the inputs of a group of optocouplers are switched either ON or OFF at the same time,  $t_{PSK}$  is the difference between the shortest propagation delay, either  $t_{PLH}$  or  $t_{PHL}$ , and the longest propagation delay, either  $t_{PLH}$  or  $t_{PHL}$ .

As mentioned earlier,  $t_{PSK}$  can determine the maximum parallel data transmission rate. Figure 15 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 15 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice  $t_{PSK}$ . A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The  $t_{PSK}$  specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and input current, and power supply ranges.

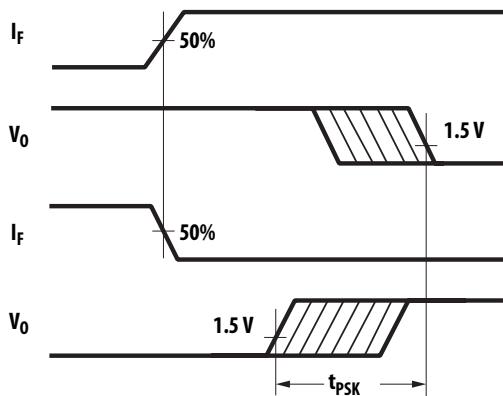


Figure 14. Illustration of Propagation Delay Skew –  $t_{PSK}$

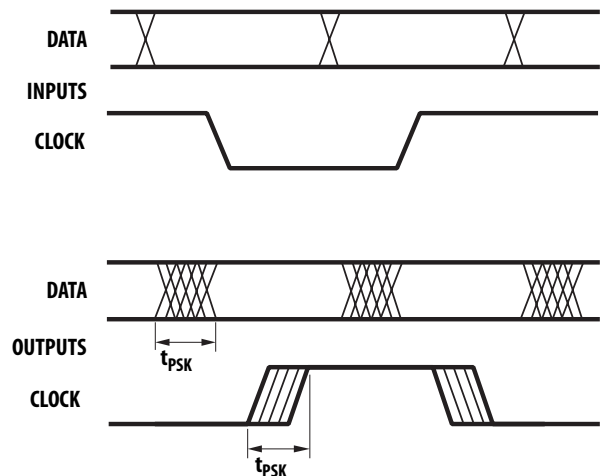


Figure 15. Parallel Data Transmission Example

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