ACPL-P314 and ACPL-W314

0.6-Amp Output Current IGBT Gate Driver Optocoupler

Data Sheet

Description

The ACPL-P314/W314 consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs.

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters
- Inverter for home appliances
- Induction cooker
- Switching power supplies (SPSs)

Features

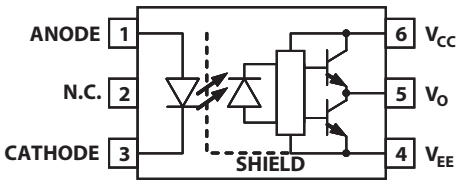
- High-speed response
- Ultra high CMR
- Bootstrappable supply current
- Available in Stretched SO-6 package
- Package clearance/creepage at 8 mm (ACPL-W314)
- Safety approval:
  - UL1577 recognized with 3750 Vrms for 1 minute for ACPL-P314 and 5000 Vrms for 1 minute for ACPL-W314
  - CSA Approved
  - IEC/EN/DIN EN 60747-5-5 Approved
  - V_{IORM} = 891 Vpeak for ACPL-P314
  - V_{IORM} = 1140 Vpeak for ACPL-W314

Specifications

- 0.6-A maximum peak output current
- 0.4-A minimum peak output current
- 0.7-µs maximum propagation delay over temperature range
- $I_{CC(max)}$ = 3-mA maximum supply current
- 25 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1500V
- Wide V_{CC} operating range: 10V to 30V over temperature range
- Wide operating temperature range: –40°C to 100°C

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagram



NOTE A 0.1-µF bypass capacitor must be connected between pins V_{CC} and VEE.

Truth Table	
LED	VO
OFF	LOW
ON	HIGH

Ordering Information

ACPL-P314 is UL Recognized with 3750 Vrms for 1 minute per UL1577. ACPL-W314 is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape and Reel	UL 5000 Vrms / 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant						
ACPL-P314	-000E	Stretched SO-6	X				100 per tube
	-500E		X	X			1000 per reel
	-060E		X			X	100 per tube
	-560E		X	X		X	1000 per reel
ACPL-W314	-000E	Stretched SO-6	X		X		100 per tube
	-500E		X	X	X		1000 per reel
	-060E		X		X	X	100 per tube
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P314-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

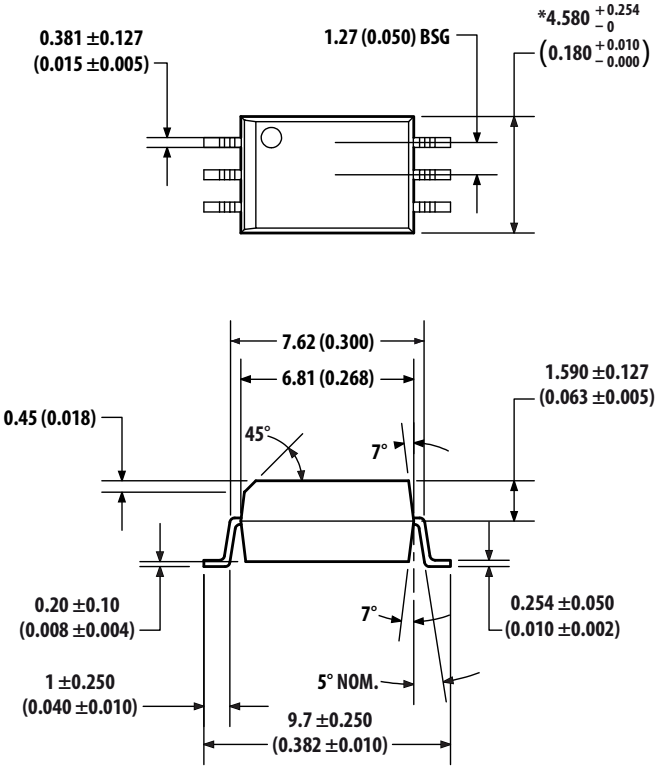
ACPL-P314-000E to order product of Stretched SO-6 Surface Mount package in tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

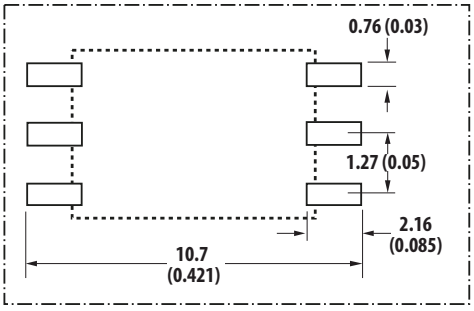
NOTE The notation #XXX is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant option will use -XXXE.

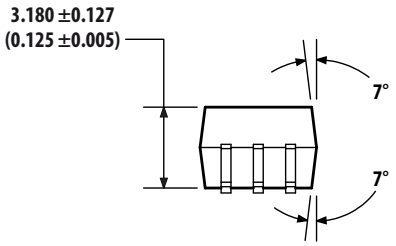
Package Outline Drawings

ACPL-P314 Stretched SO-6 Package



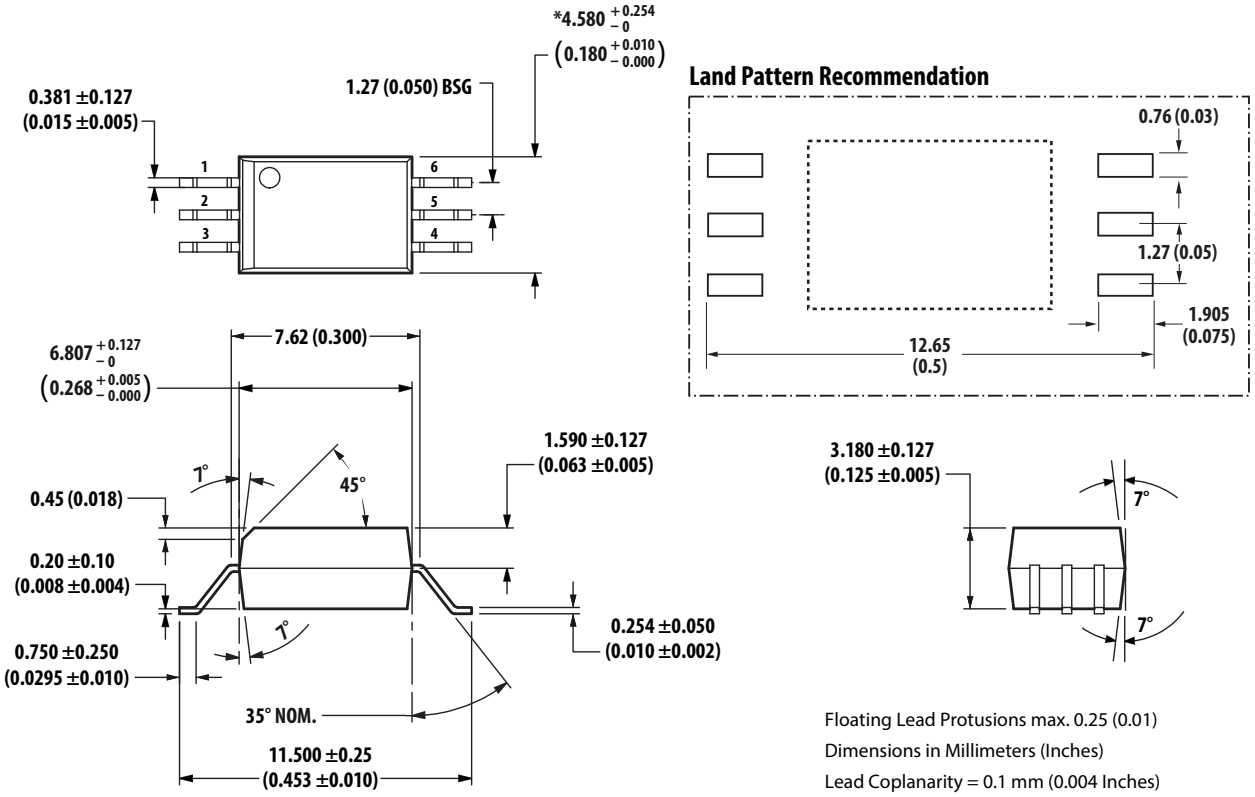
Land Pattern Recommendation





Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)
* Total Package Length (inclusive of mold flash)
4.834 ± 0.254 (0.190 ± 0.010)

ACPL-W314 Stretched SO-6 Package



Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)
* Total Package Length (inclusive of mold flash)
4.834 ± 0.254 (0.190 ± 0.010)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-P314/W314 is approved by the following organizations.

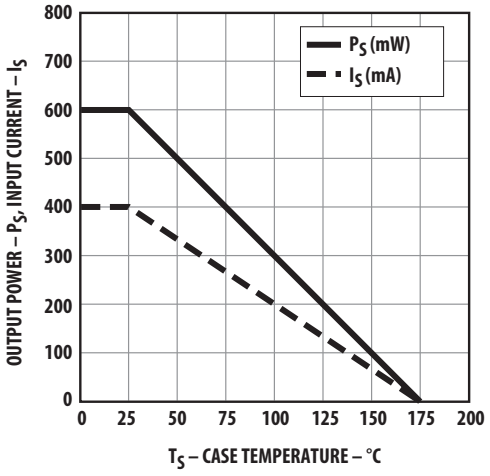
IEC/EN/DIN EN 60747-5-5 (Option 060 only)	Approval under IEC 60747-5-5:2007.
UL	Approval under UL 1577 component recognition program up to V_{ISO} = 3750 V_{RMS} for the ACPL-P314 and V_{ISO} = 5000 V_{RMS} for the ACPL-W314, File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics[a] (ACPL-P314/W314 Option 060)

Description	Symbol	ACPL-W314	ACPL-P314	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1				
For Rated Mains Voltage ≤ 150 Vrms		I-IV	I-IV	
For Rated Mains Voltage ≤ 300 Vrms		I-IV	I-IV	
For Rated Mains Voltage ≤ 450 Vrms		I-IV	I-III	
For Rated Mains Voltage ≤ 600 Vrms		I-IV	I-III	
For Rated Mains Voltage ≤ 1000 Vrms		I-III		
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	1140	891	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1s$, Partial Discharge < 5 pC	V_{PR}	2137	1670	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10s$, Partial Discharge < 5 pC	V_{PR}	1824	1426	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini} = 60s$)	V_{IOTM}	8000	6000	V_{peak}
Safety Limiting Values (maximum values allowed in the event of a failure)				
Case Temperature	T_S	175	175	°C
Input Current[b]	$I_{S,INPUT}$	230	230	mA
Output Power[b]	$P_{S,OUTPUT}$	600	600	mW
Insulation Resistance at T_S, $V_{IO} = 500$ V	R_S	$\leq 10^9$	$\leq 10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits,* AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

b. Refer to the following figure for dependence of P_S and I_S on ambient temperature:



Insulation and Safety-Related Specifications

Parameter	Symbol	ACPL-		Unit	Conditions
		P314	W314		
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		N/A	N/A	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

NOTE All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors, such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	100	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	V_R	—	5	V	
High Peak Output Current	$I_{OH(PEAK)}$	—	0.6	A	b
Low Peak Output Current	$I_{OL(PEAK)}$	—	0.6	A	b
Supply Voltage	$V_{CC} – V_{EE}$	–0.5	35	V	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output Power Dissipation	P_O	—	250	mW	c
Input Power Dissipation	P_I	—	45	mW	d
Lead Solder Temperature	260°C for 10s., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section.				

a. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 ms, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.4A. See Applications Information section for additional details on limiting I_{OL} peak.

c. Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.

d. Input power dissipation does not require derating.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply	$V_{CC} – V_{EE}$	10	30	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.8	V	
Operating Temperature	T_A	–40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
High Level Output Current	I_{OH}	0.2	—	—	A	$V_O = V_{CC} - 4$	2	a
		0.4	0.5	—	A	$V_O = V_{CC} - 10$	3	b
Low Level Output Current	I_{OL}	0.2	0.4	—	A	$V_O = V_{EE} + 2.5$	5	a
		0.4	0.5	—	A	$V_O = V_{EE} + 10$	6	b
High Level Output Voltage	V_{OH}	$V_{CC} - 4$	$V_{CC} - 1.8$	—	V	$I_O = -100$ mA	1	c, d
Low Level Output Voltage	V_{OL}	—	0.4	1	V	$I_O = 100$ mA	4	
High Level Supply Current	I_{CCH}	—	0.7	3	mA	$I_F = 10$ mA	7, 8	e
Low Level Supply Current	I_{CCL}	—	1.2	3	mA	$I_F = 0$ mA	7, 8	e
Threshold Input Current Low to High	I_{FLH}	—		7	mA	$I_O = 0$ mA, $V_O > 5V$	9, 15	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V	$I_O = 0$ mA, $V_O > 5V$		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	$I_F = 10$ mA	16	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	$I_F = 10$ mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	$I_R = 10$ µA		
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, $V_F = 0V$		

a. Maximum pulse width = 50 ms, maximum duty cycle = 0.5%.

b. Maximum pulse width = 10 ms, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.4A. See the Applications section for additional details on limiting I_{OL} peak.

c. In this test, V_{OH} is measured with a DC load current. When driving capacitive load, V_{OH} approaches V_{CC} as I_{OH} approaches zero amps.

d. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

e. The power supply current increases when operating frequency and Q_g of the driven IGBT increases.

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	µs	R_g = 47Ω, C_g = 3 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 8 mA, V_{CC} = 30V	10, 11, 12, 13, 14, 17	a
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.3	0.7	µs			a
Propagation Delay Difference Between Any Two Parts or Channels	PDD	–0.5	—	0.5	µs			b
Rise Time	t_R	—	50	—	ns			
Fall Time	t_F	—	50	—	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	25	—	—	kV/µs	T_A = 25°C, V_{CM} = 1500V	18	c
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	25	—	—	kV/µs		18	d

a. This load condition approximates the gate load of a 1200V/25A IGBT.

b. PDD is the difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test conditions.

c. Common mode transient immunity in the high state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse V_{CM} to ensure that the output remains in the high state (that is, V_O > 6.0V).

d. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to ensure that the output remains in a low state (that is, V_O < 1.0V).

Package Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage	ACPL-P314	V_{ISO}	3750	—	—	Vrms	T_A = 25°C, RH < 50% for 1 min.		a, b
	ACPL-W314		5000	—	—				b, c
Input-Output Resistance		R_{I-O}	—	10^{12}	—		V_{I-O} = 500V		b
Input-Output Capacitance		C_{I-O}	—	0.6	—	pF	Freq = 1 MHz		

a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 4500 V_{rms} for 1 second (leakage detection current limit I_{I-O} < 5 µA). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics[a] (ACPL-P314/W314 Option 060) table, if applicable.

b. The device is considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V_{rms} for 1 second (leakage detection current limit I_{I-O} < 5A). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics[a] (ACPL-P314/W314 Option 060) table, if applicable.

Figure 1 V_{OH} vs. Temperature

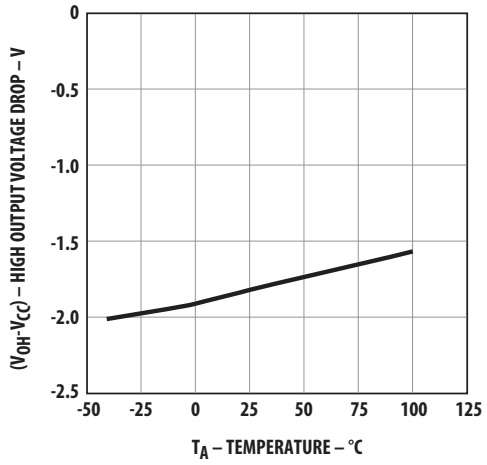


Figure 2 I_{OH} vs. Teperature

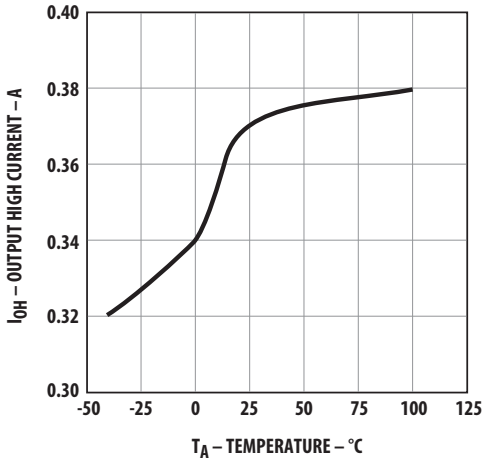


Figure 3 V_{OH} vs. I_{OH}

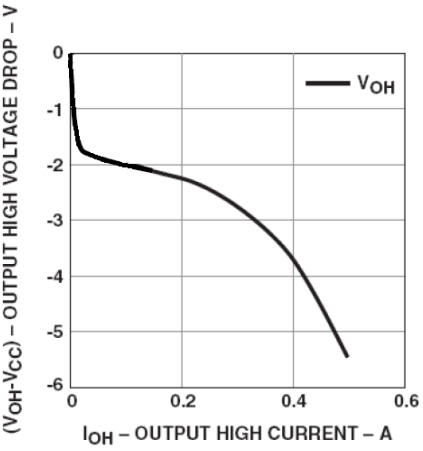


Figure 4 V_{OL} vs. Temperature

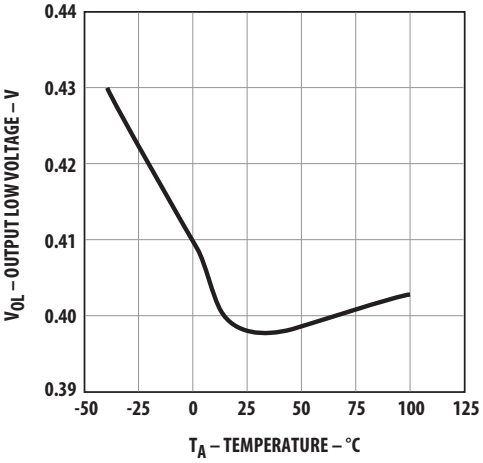


Figure 5 I_{OL} vs. Temperature

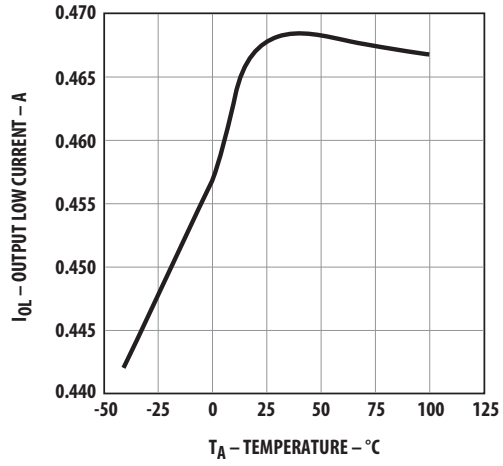


Figure 6 V_{OL} vs. I_{OL}

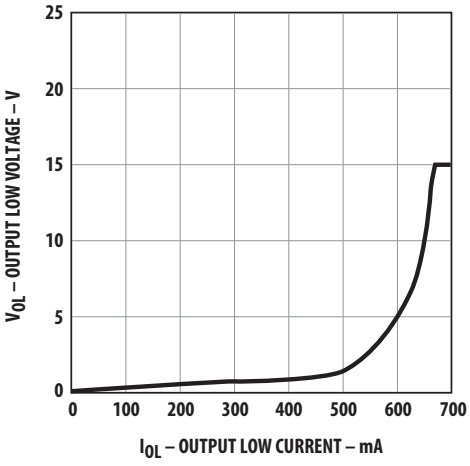


Figure 7 I_{CC} vs. Temperature

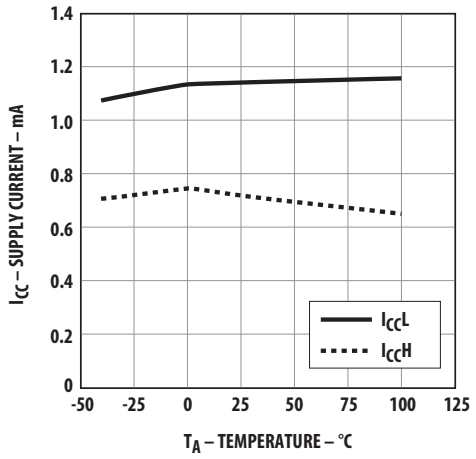


Figure 8 I_{CC} vs. V_{CC}

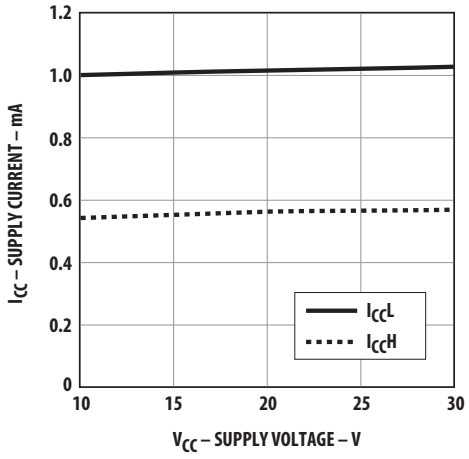


Figure 9 I_{FLH} vs. Temperature

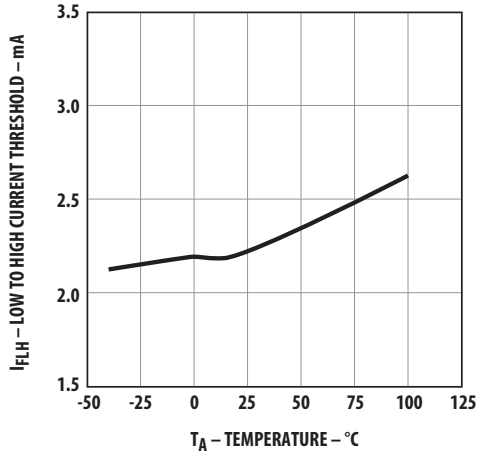


Figure 10 Propagation Delay vs. V_{CC}

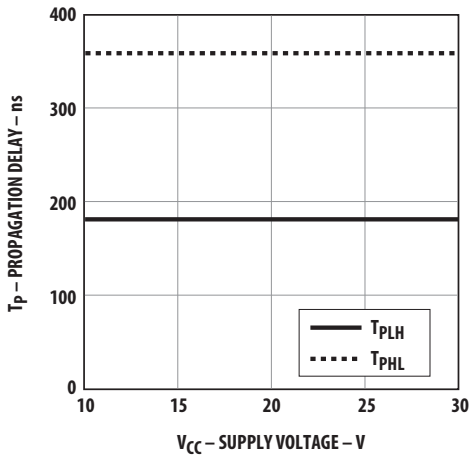


Figure 11 Propagation Delay vs. I_F

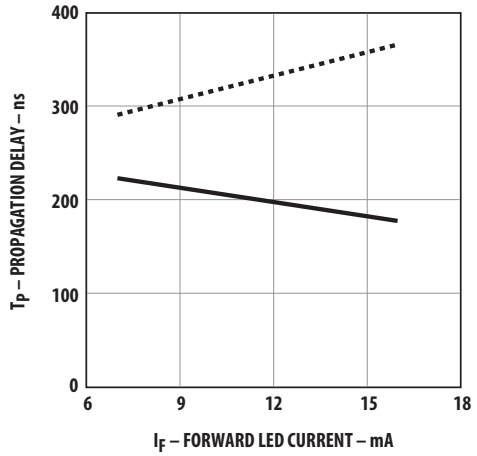


Figure 12 Propagation Delay vs. Temperature

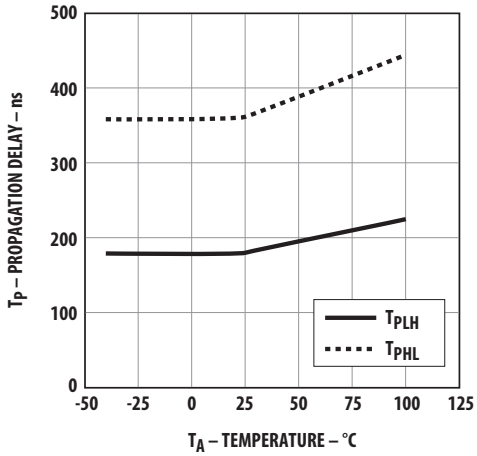


Figure 13 Propagation Delay vs. Rg

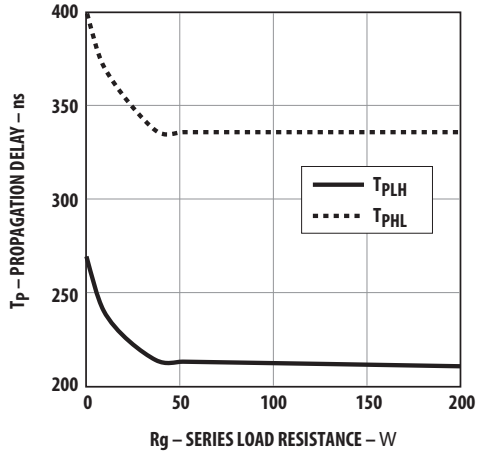


Figure 14 Propagation Delay vs. Cg

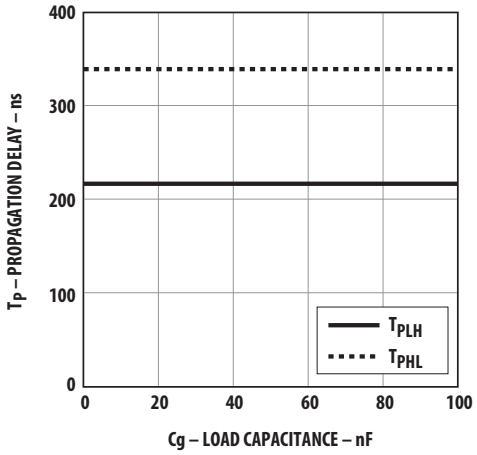


Figure 15 Transfer Characteristics

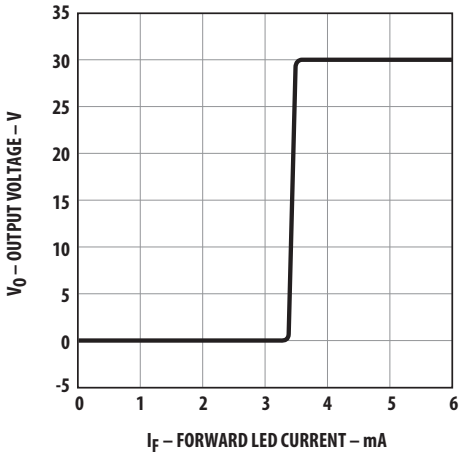


Figure 16 Input Current vs. Forward Voltage

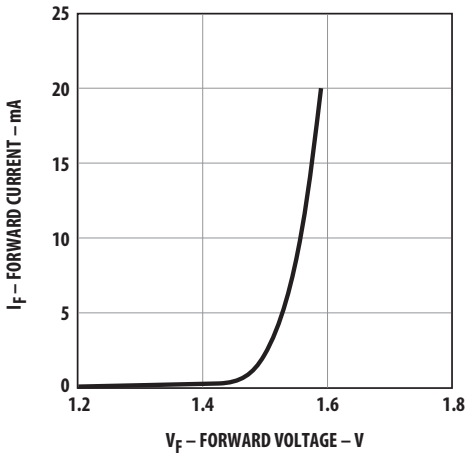
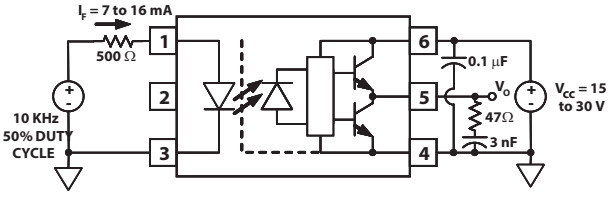


Figure 17 Propagation Delay Test Circuit and Waveforms



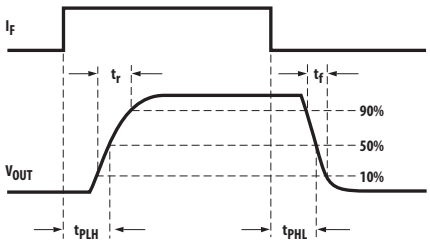
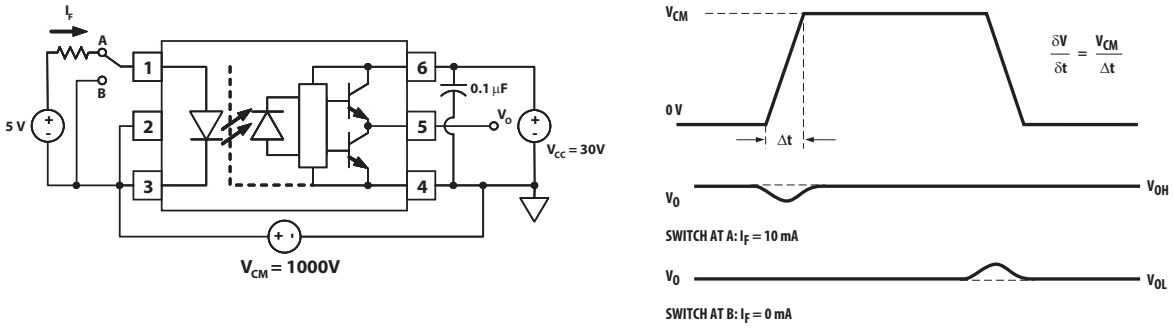


Figure 18 CMR Test Circuit and Waveforms



Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the ACPL-P314/W314 has a very low maximum V_{OL} specification of 1.0V. Minimizing R_g and the lead inductance from the ACPL-P314/W314 to the IGBT gate and emitter (possibly by mounting the ACPL-P314/W314 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 19. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the ACPL-P314/W314 input as this can result in unwanted coupling of transient signals into the input of ACPL-P314/W314 and degrade performance. (If the IGBT drain must be routed near the ACPL-P314/W314 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the ACPL-P314/W314.)

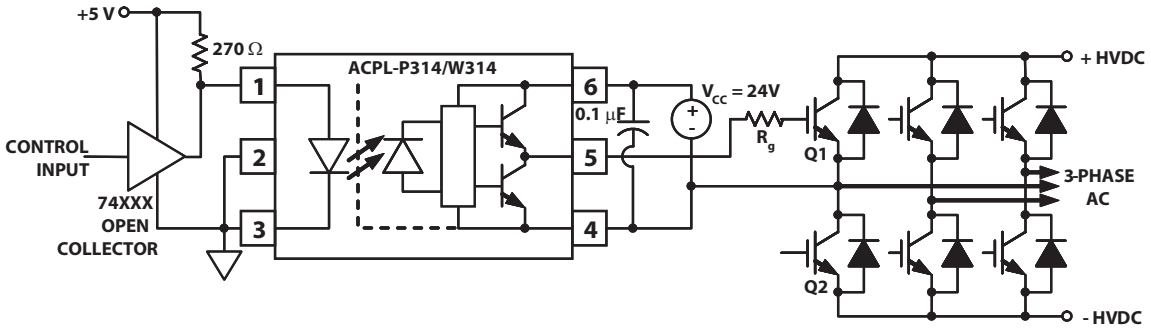
Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The IGBT and Rg in Figure 19 can be analyzed as a simple RC circuit with a voltage supplied by the ACPL-P314/W314.

$$R_g = \frac{V_{CC} - V_{OL}}{I_{OLPEAK}} = \frac{24 - 5}{0.6} = 32\,\Omega$$

The V_{OL} value of 5V in the previous equation is the V_{OL} at the peak current of 0.6A. (See Figure 6).

Figure 19 Recommended LED Drive and Application Circuit for ACPL-P314/W314



Step 2: Check the ACPL-P314/W314 power dissipation and increase R_g if necessary. The ACPL-P314/W314 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$$P_T = P_E + P_O$$

$$P_E = I_F \cdot V_F \cdot \text{DutyCycle}$$

$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \cdot V_{CC} + E_{SW}(R_g; Q_g) \cdot f$$

$$= (I_{CCBIAS} + K_{ICC} \cdot Q_g \cdot f) \cdot V_{CC} + E_{SW}(R_g; Q_g) \cdot f$$

where $K_{ICC} \cdot Q_g \cdot f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 19 with I_F (worst case) = 10 mA, R_g = 32Ω, Max Duty Cycle = 80%, Q_g = 100 nC, f = 20 kHz, and T_{AMAX} = 85°C:

$$P_E = 10\,\text{mA} \cdot 1.8\text{V} \cdot 0.8 = 14\,\text{mW}$$

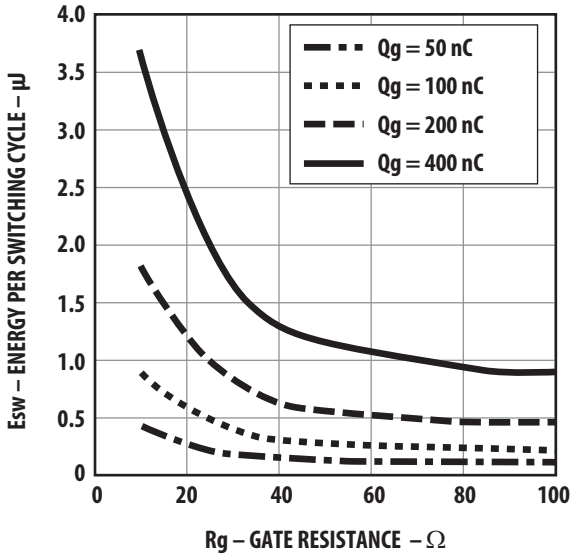
$$P_O = (3\,\text{mA} + (0.001\,\text{mA/nC} \cdot \text{kHz}) \cdot 20\,\text{kHz} \cdot 100\,\text{nC}) \cdot 24\text{V} +$$

$$0.4\,\mu\text{J} \cdot 20\,\text{kHz} = 128\,\text{mW} < 250\,\text{mW}\,(P_{O(MAX)}\ @85\,^\circ\text{C})$$

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over entire operating temperature range.

Since P_O for this case is less than $P_{O(MAX)}$, R_g = 32Ω is alright for the power dissipation.

Figure 20 Energy Dissipated in the ACPL-P314/W314 and for Each IGBT Switching Cycle



LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 21. The ACPL-P314/W314 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5–8 as shown in Figure 22. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 19) can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

Figure 21 Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers

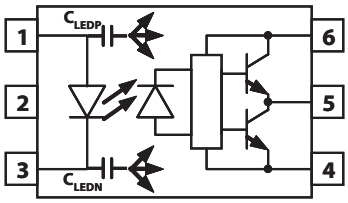
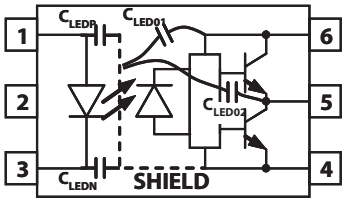


Figure 22 Optocoupler Input to Output Capacitance Model for Shielded Optocouplers



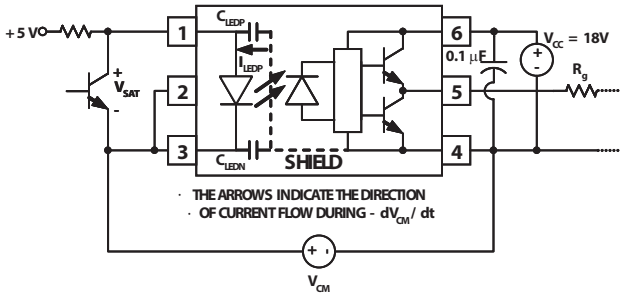
CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 8 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 10 kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 23, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED remains off and no common mode failure occurs.

Figure 23 Equivalent Circuit for Figure 17 During Common Mode Transient



The open collector drive circuit, shown in Figure 24, cannot keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR1 performance. The alternative drive circuit, like the recommended application circuit (Figure 19), achieves ultra high CMR performance by shunting the LED in the off state.

Figure 24 Not Recommended Open Collector Drive Circuit

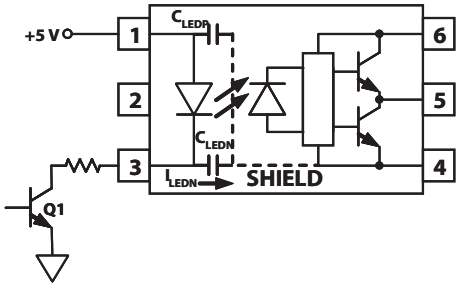
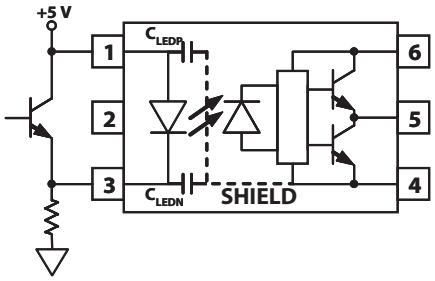


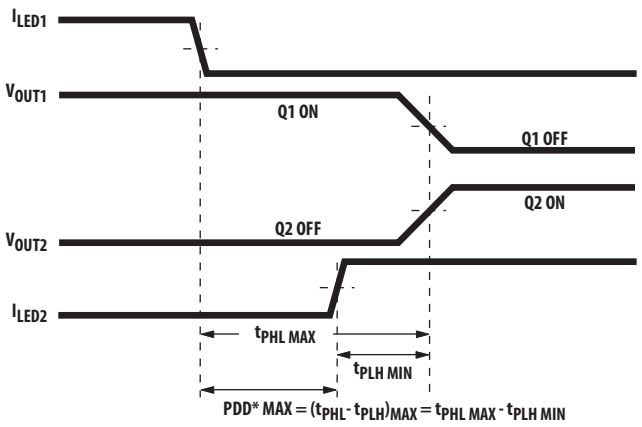
Figure 25 Recommended LED Drive Circuit for Ultra-High CMR



Dead Time and Propagation Delay Specifications

The ACPL-P314/W314 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize *dead time* in their power inverter designs. Dead time is the time high and low side power transistors are off. Any overlap in Ql and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 26. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of –40°C to 100°C.

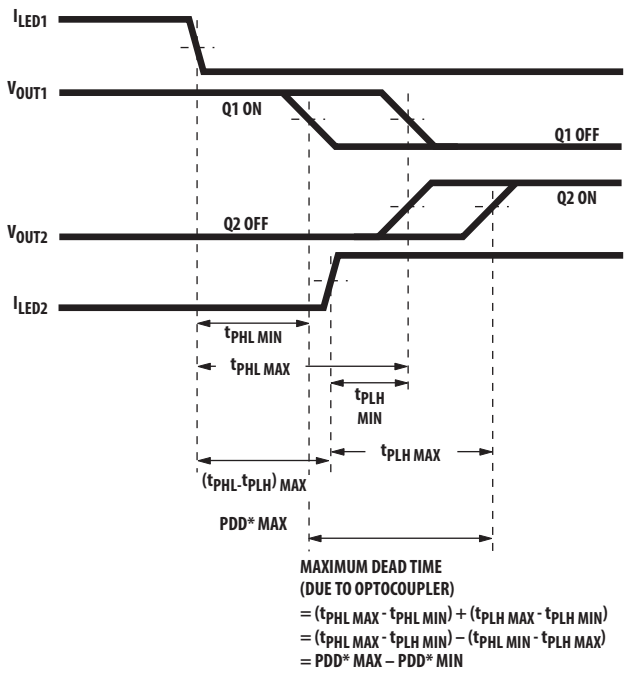
Figure 26 Minimum LED Skew for Zero Dead Time



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 27. The maximum dead time for the ACPL-P314/W314 is 1 µs (= 0.5 µs – (–0.5 µs)) over the operating temperature range of –40°C to 100°C.

Figure 27 Waveforms for Dead Time



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

NOTE The propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Thermal Model for ACPL-P314/W314 Streched-SO6 Package Optocoupler

Definitions

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED.

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC).

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector/Output IC (W).

T_1: Junction temperature of LED (C).

T_2: Junction temperature of Detector (C).

T_a: Ambient temperature.

ΔT_1: Temperature difference between LED junction and ambient (C).

ΔT_2: Temperature deference between Detector junction and ambient.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air.

Description

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm × 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a$ -- (1)

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a$ -- (2)

JEDEC Specifications	R_{11}	R_{12}, R_{21}	R_{22}
Low K board	357	150, 166	228
High K board	249	76, 79	159

NOTE Maximum junction temperature for above parts: 125°C.

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