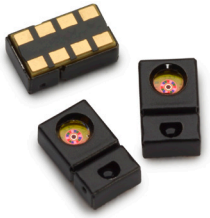
APDS-9950

Digital Proximity, RGB and Ambient Light Sensor

Data Sheet



Description

The APDS-9950 device provides red, green, blue, and clear (RGBC) light sensing and proximity detection. The devices detect light intensity under a variety of lighting conditions and through a variety of attenuation materials, including dark glass. The proximity detection feature allows a large dynamic range of operation for accurate distance detection, such as in a cell phone, for detecting when the user positions the phone close to their ear. IR LED sink current is factory-trimmed to provide consistent proximity response without requiring customer calibrations. An internal state machine provides the ability to put the device into a low power state in between proximity and RGBC measurements, providing very low average power consumption.

The color-sensing feature is useful in applications such as LED RGB backlight control, solid-state lighting, reflected LED color sampler, or fluorescent light color temperature detection. The integrated IR blocking filter makes this device an excellent ambient light sensor and color temperature monitor sensor.

Ordering Information

Part Number	Packaging	Quantity
APDS-9950	Tape & Reel	5000 per reel

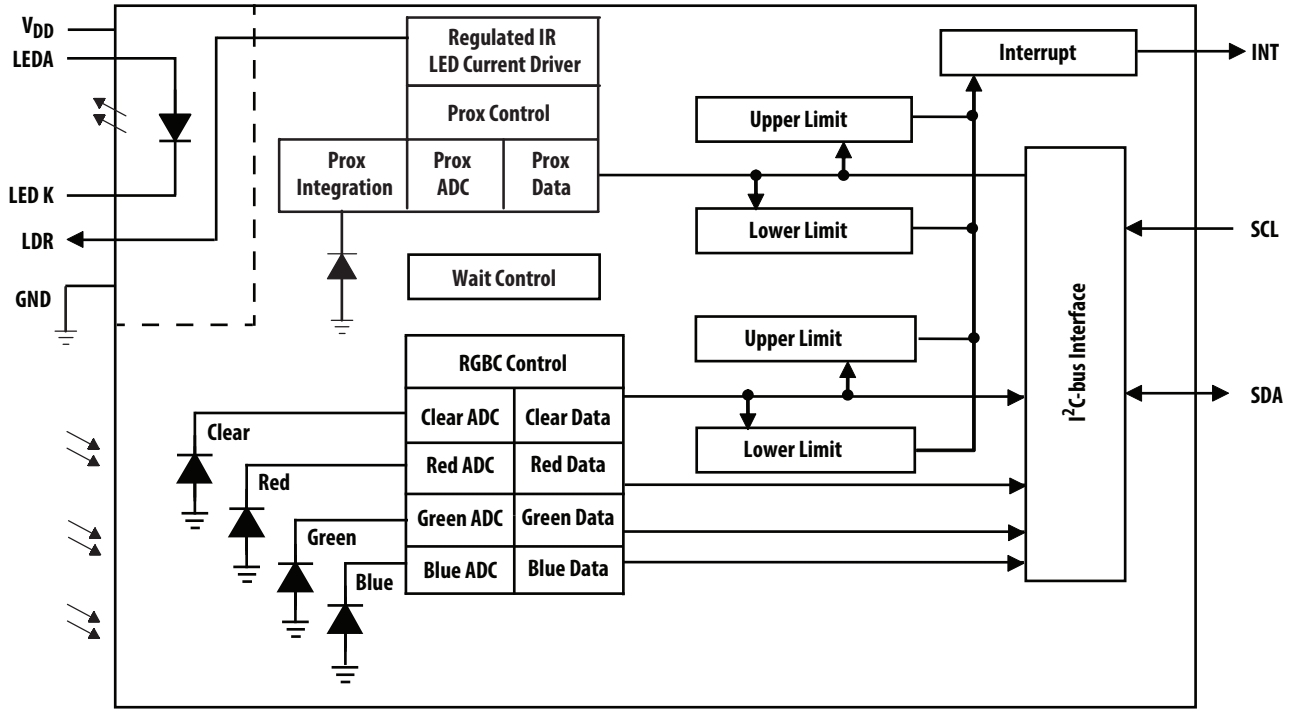
Features

- RGB and Clear Color Sensing and Proximity Detector and IR LED in an Optical Module
- Color Light Sensing with IR Blocking Filter
  - Programmable Analog Gain and Integration Time
  - Very High Sensitivity – Ideally suited for Operation Behind Dark Glass
- Proximity Detection
  - Trimmed for Calibrated 100 mm Detection
  - Ambient Light Rejection
  - Integrated IR LED and LED Driver
- Maskable Light and Proximity Interrupt
  - Programmable Upper and Lower Thresholds with Persistence Filter
- Power Management
  - Low Power – 2.5 µA Sleep State
  - 85 µA Wait State with Programmable Wait State Timer from 2.4 ms to > 7 sec
- I^2C-bus Fast Mode Compatible Interface
  - Data Rates up to 400 kHz
  - Input Voltage Levels Compatible with V_{DD} or 1.8 V V_{BUS}
  - Dedicated Interrupt Pin
- Small Package L 3.94 × W 2.36 × H 1.35 mm

Applications

- OLED Display Control
- RGB LED Backlight Control
- Ambient Light Color Temperature Sensing
- Cell Phone Touch-screen Disable
- Automatic Speakerphone Enable
- Automatic Menu Pop-up
- Mechanical Switch Replacement
- Industrial Process Control

Functional Block Diagram



Description

The APDS-9950 is a next-generation digital color light sensor device containing four integrating analog-to-digital converters (ADCs) that integrate currents from photodiodes. Multiple photodiode segments for red, green, blue, and clear are geometrically arranged to reduce the reading variance as a function of the incident light angle. Integration of all color sensing channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the corresponding data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller.

The APDS-9950 provides a separate pin for level-style interrupts. When interrupts are enabled and a preset value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of a clear channel or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both clear and proximity.

Proximity detection is done using a dedicated proximity photodiode centrally located beneath an internal lens, an internal LED, and a driver circuit. The driver circuit requires no external components and is trimmed to provide a calibrated proximity response. Customer calibrations are usually not required.

The number of proximity LED pulses can be programmed from 1 to 255 pulses. Each pulse has a 14 μs period.

This LED current coupled with the programmable number of pulses provides a 2000:1 contiguous dynamic range.

I/O Pins Configuration

Pin	Name	Type	Description
1	SDA	I/O	I²C serial data I/O terminal - serial data I/O for I²C-bus
2	INT	O	Interrupt - open drain (active low)
3	LDR		LED driver input for proximity IR LED, constant current source LED driver
4	LEDK		LED Cathode, connect to LDR pin when using internal LED driver circuit
5	LEDA		LED Anode, connect to V_{BATT} on PCB
6	GND		Power supply ground. All voltages are referenced to GND
7	SCL	I	I²C serial clock input terminal - clock signal for I²C serial data
8	V_{DD}		Power supply voltage

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)*

Parameter	Symbol	Min	Max	Units	Conditions
Power supply voltage [1]	V_{DD}		3.8	V	
Input voltage range	V_{IN}	-0.5	3.8	V	
Output voltage range	V_{OUT}	-0.3	3.8	V	
Storage temperature range	T_{stg}	-40	85	°C	

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating ambient temperature	T_A	-30		85	°C
Power supply voltage	V_{DD}	2.5		3.5	V
Supply voltage accuracy, V_{DD} total error including transients		-3		+3	%
LED supply voltage	V_{BATT}	2.5		4.5	V

Operating Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
I_{DD} supply current	I_{DD}		235	330	µA	Active – LDR pulses off
			85			Wait State
			2.5	10		Sleep Mode – No I²C activity
V_{OL} INT, SDA output low voltage	V_{OL}	0		0.4	V	3 mA sink current
I_{LEAK} leakage current, SDA, SCL, INT pins	I_{LEAK}	–5		5	µA	
I_{LEAK} leakage current, LDR P\pin	I_{LEAK}	–10		10	µA	
SCL, SDA input high voltage, V_{IH}	V_{IH}	1.25		V_{DD}	V	
SCL, SDA input low voltage, V_{IL}	V_{IL}			0.54	V	

Optical Characteristics, V_{DD} = 3 V, T_A = 25 °C, AGAIN = 16×, AEN = 1 (unless otherwise noted) [1]

Parameter	Red Channel			Green Channel			Blue Channel			Clear Channel			Units	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Irradiance responsitivity	0%		15%	10%		42%	60%		95%	14	17.5	21	counts /µW /cm²	λ_D = 465 nm [2]
	4%		25%	55%		85%	8%		45%	14.96	18.7	22.44		λ_D = 525 nm [3]
	75%		110%	0%		14%	3%		24%	16	20	24		λ_D = 625 nm [4]

Notes:
1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda_{½}$ = 22 nm.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda_{½}$ = 35 nm.
4. The 625 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 625 nm, spectral halfwidth $\Delta\lambda_{½}$ = 15 nm.

RGBC Characteristics, V_{DD} = 3 V, T_A = 25 °C, A_{GAIN} = 16×, AEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Dark ALS count value		0	5	counts	E_e = 0, A_{GAIN} = 60×, A_{TIME} = 0×D6 (100 ms)
ADC integration time step size	2.27	2.4	2.56	ms	A_{TIME} = 0×FF
ADC number of integration steps	1		256	steps	
Full scale ADC counts per step			1023	counts	
Full scale ADC count value			65535	counts	A_{TIME} = 0×C0 (153.6 ms)
Gain scaling, relative to 1× gain setting	3.6	4	4.4		4×
	14.4	16	17.6		16×
	54	60	66		60×

Proximity Characteristics, V_{DD} = 3 V, T_A = 25 °C, PEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions	
I_{DD} supply current – LDR Pulse On		3		mA		
ADC conversion time step size	2.27	2.4	2.56	ms		
ADC number of integration steps		1		steps		
Full scale ADC counts			1023	counts		
LED pulse count	0		255	pulses		
LED pulse period		14.0		µs		
LED pulse width – LED on time		6.3		µs		
LED drive current		100		mA	P_{DRIVE} = 0	I_{SINK} sink current @ 0.6 V, LDR pin
		50			P_{DRIVE} = 1	
		25			P_{DRIVE} = 2	
		12.5			P_{DRIVE} = 3	
Proximity ADC count value, no object		125	250	counts	Dedicated power supply V_{BATT} = 3 V LED driving 8 pulses, P_{DRIVE} = 00, P_{GAIN} = 00, open view (no glass) and no reflective object above the module.	
Proximity ADC count value, 100 mm distance object	350	440	530	counts	Reflecting object – 73 mm × 83 mm Kodak 90% grey card, 100 mm distance, LED driving 8 pulses, P_{DRIVE} = 00, P_{GAIN} = 00, open view (no glass) above the module.	

IR LED Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Peak Wavelength, λ_P		850		nm	I_F = 20 mA
Spectrum Width, Half Power, $\Delta\lambda$		40		nm	I_F = 20 mA
Optical Rise Time, T_R		20		ns	I_F = 100 mA
Optical Fall Time, T_F		20		ns	I_F = 100 mA

Wait Characteristics, V_{DD} = 3 V, T_A = 25 °C, WEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Wait Step Size	2.27	2.4	2.56	ms	W_{TIME} = 0×FF

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted) *

Parameter	Symbol	Min.	Max.	Unit
Clock frequency (I^2C-bus only)	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	µs
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	µs
Data hold time	$t_{HD;DAT}$	0	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	ns
LOW period of the SCL clock	t_{LOW}	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs
Clock/data fall time	t_f	–	300	ns
Clock/data rise time	t_r	–	300	ns
Input pin capacitance	C_i	–	10	pF

* Specified by design and characterization; not production tested.

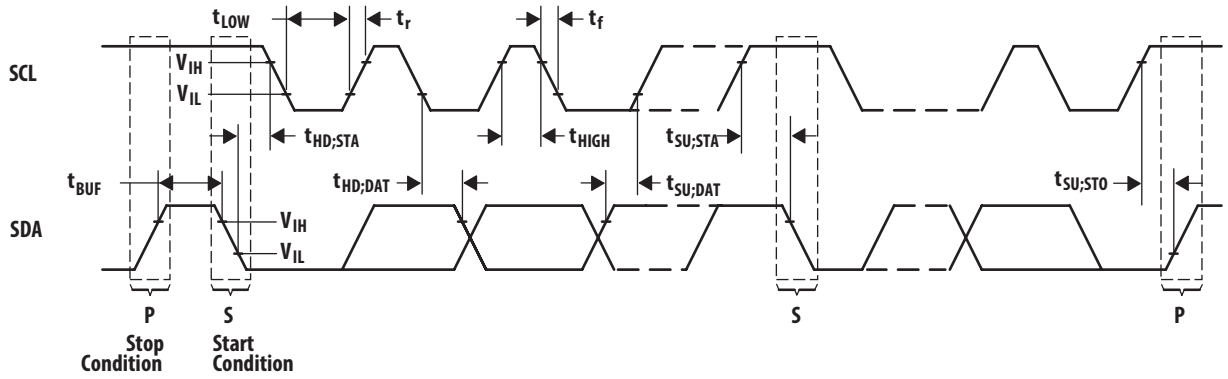


Figure 1. Timing Diagrams

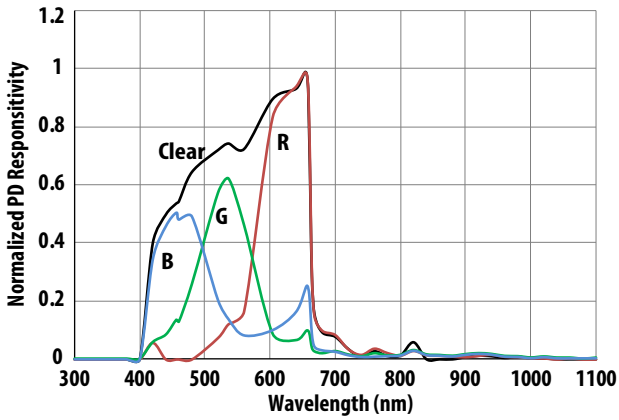


Figure 2. Normalized PD Spectral Response

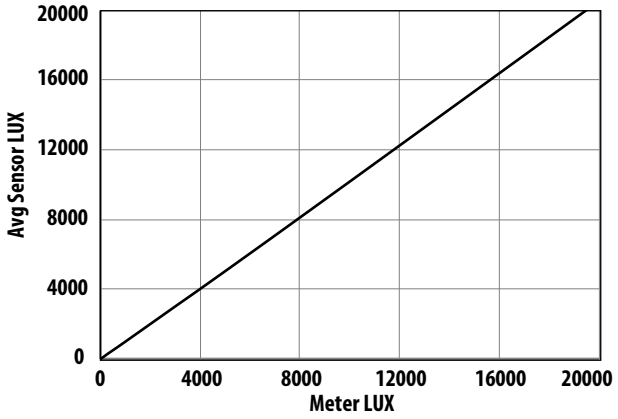


Figure 3. ALS Sensor LUX vs Meter LUX using White Light

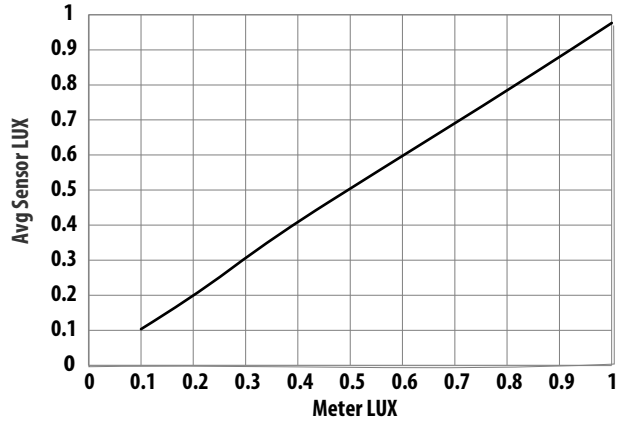


Figure 4. ALS Sensor LUX vs Meter LUX using White Light

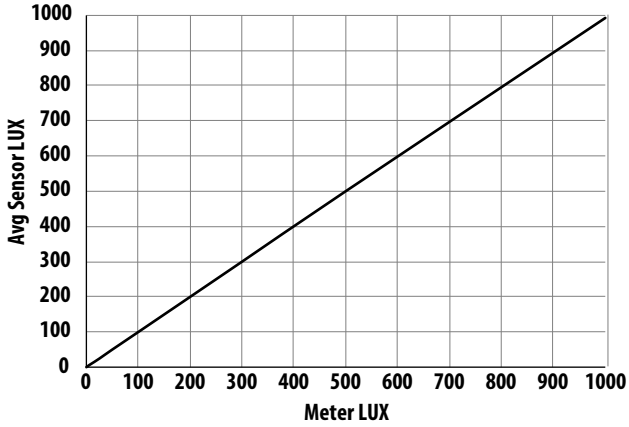


Figure 5. ALS Sensor LUX vs Meter LUX using Incandescent Light

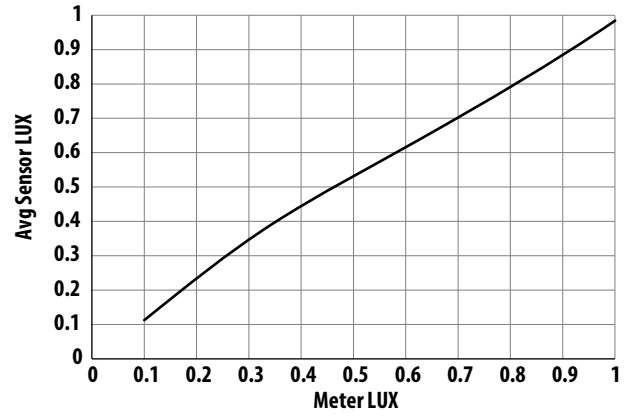


Figure 6. ALS Sensor LUX vs Meter LUX using Incandescent Light

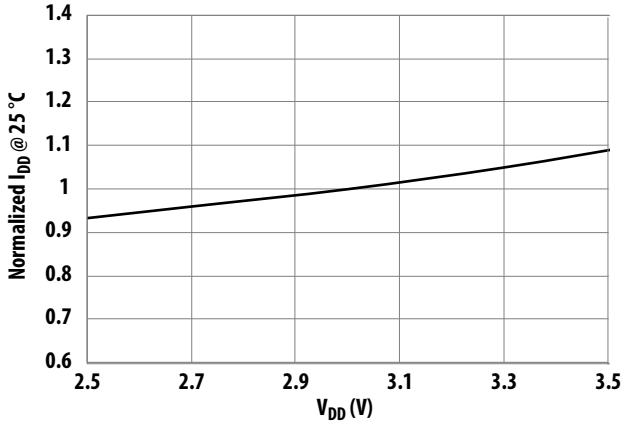


Figure 7. Normalized IDD vs. VDD

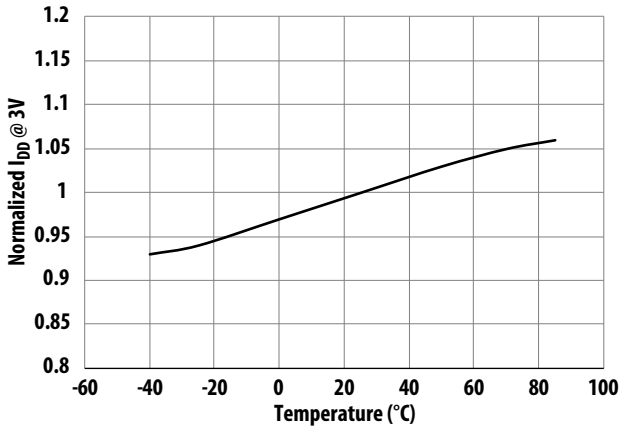


Figure 8. Normalized IDD vs. Temperature

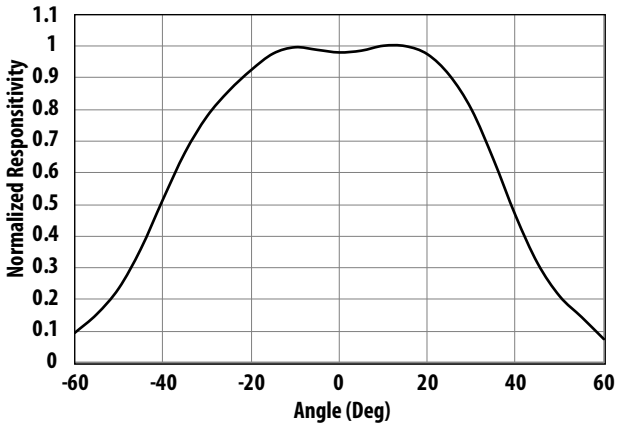


Figure 9. Normalized ALS Response vs. Angular Displacement

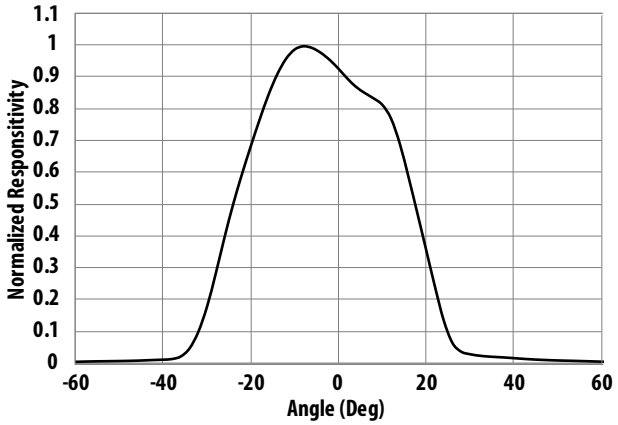


Figure 10. Normalized LED Angular Emitting Profile

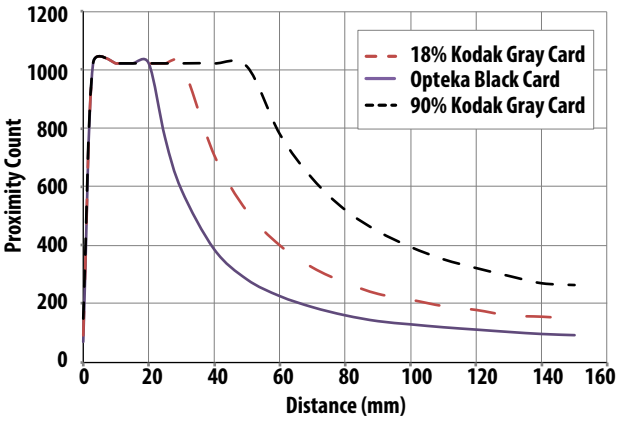


Figure 11a. Proximity Distance Profile (8Pulse, 100 mA, 1×)

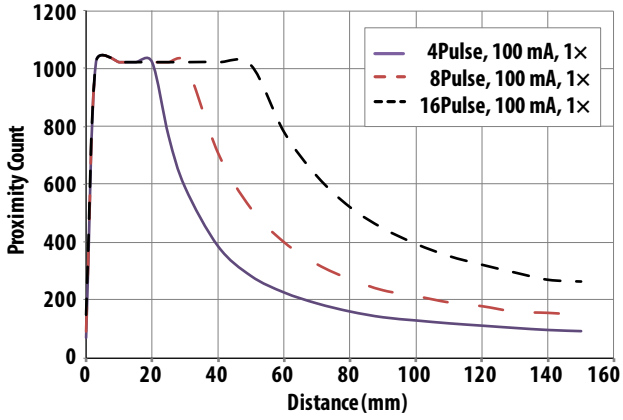


Figure 11b. Proximity Distance Profile (18% Kodak Gray Card)

Principles of Operation

System State Machine

The APDS-9950 provides control of RGBC, proximity detection and power management functionality through an internal state machine. After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Prox, Wait and RGBC states. If these states are enabled, the device will execute each function. If the PON bit is set to a 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

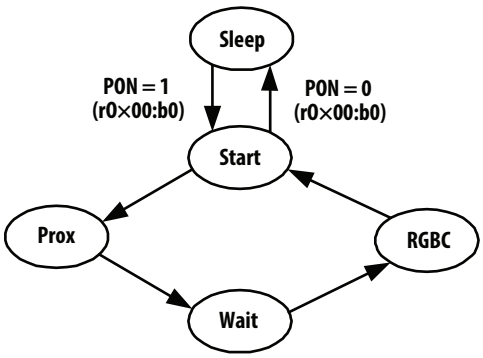


Figure 12. Simplified State Diagram

Note:

In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as PON (r0:b0).

RGBC Operation

The RGBC engine contains RGBC gain control (AGAIN) and four integrating analog-to-digital converters (ADC) for the RGBC photodiodes. The RGBC integration time (ATIME) affects both the resolution and the sensitivity of the RGBC reading. Integration of all four channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the color data registers. This data is also referred to as channel count. The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically moves to the next state in accordance with the configured state machine.

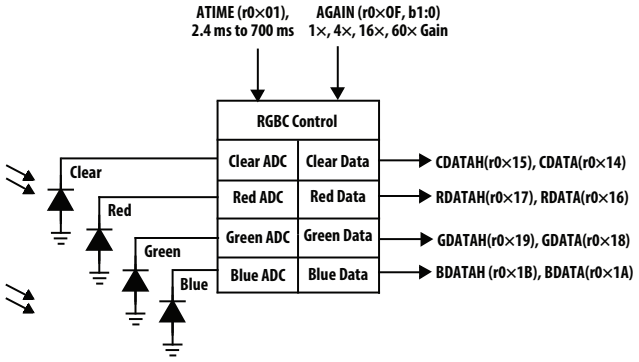


Figure 13. RGBC Operation

The registers for programming the integration and wait times are a 2's complement values. The actual time can be calculated as follows:

A_{TIME} = 256 – Integration Time/2.4 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.4 ms $_v$ (256 – A_{TIME})

For example, if a 100 ms integration time is needed, the device needs to be programmed to:

256 – (100 / 2.4) = 256 – 42 = 214 = 0×D6

Conversely, the programmed value of 0×C0 would correspond to:

(256 – 0×C0) × 2.4 = 64 × 2.4 = 154 ms

Proximity Detection

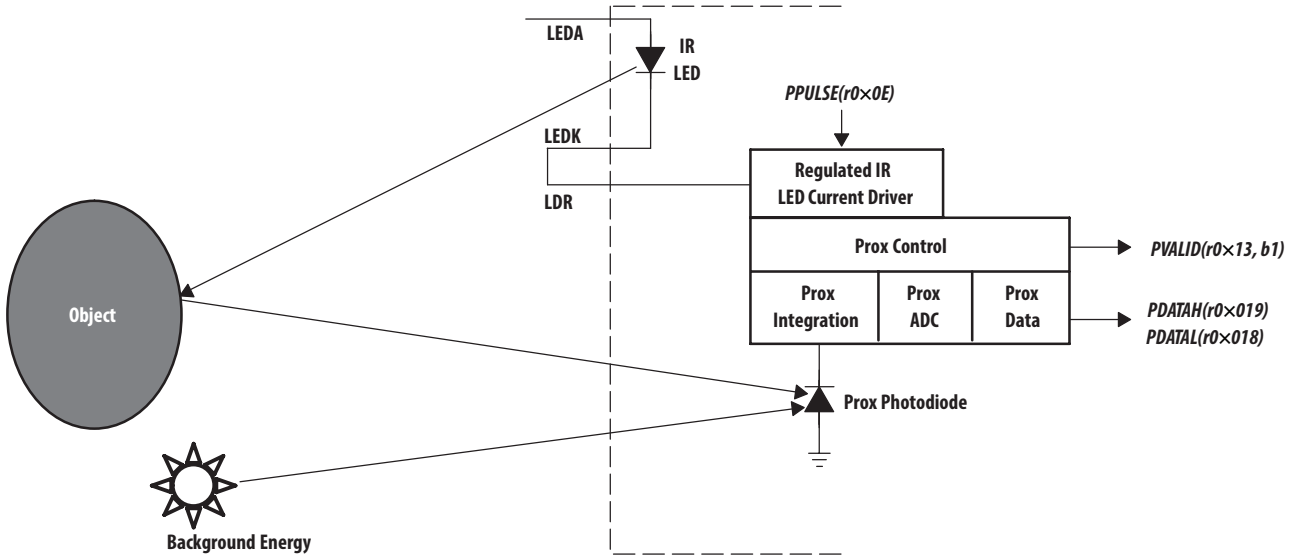


Figure 14. Proximity Detection

Proximity detection measures IR signal energy reflected off a remote object to determine its relative distance. Figure 14 shows light rays emitting from the internal IR LED, reflecting off an object, and being detected by the proximity photodiode. The system response is managed by controlling the number of IR pulses set in P_{PULSE} (Proximity Pulse Count Register).

The internal LED current driver provides a regulated current sink on the LDR terminal that eliminates the need for external components. If even higher LED output is needed, currents can be switched using an external P_{FET}, gated by the LDR pin. The P_{FET} can then sink current from LEDK to ground with an appropriate external current-limiting resistor.

Referring to the Expanded State Diagram (Figure 17), the LED current driver pulses the internal IR LED during the Prox Accum state. Using P_{PULSE}, 1 to 255 proximity pulses can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of P_{PULSE}.

To negate ambient light from the photodiode signal, the background energy is subtracted from the total energy received. Figure 15 illustrates the timing of the LED pulse. The circuitry used to cancel the background energy causes the pulse duty cycle to be asymmetrical as shown. During the LED On time, the reflected signal and the background energy are integrated by the sensor. During the LED Off time, the background energy is subtracted from the integrated value leaving the reflected IR signal to accumulate from pulse to pulse.

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. The PSAT control (Control Register) can be used to assist with detecting analog saturation at the sensor. When PSAT = 1 the PDATA output registers will show the dark current value (< 5) if saturation is determined to be likely. When PSAT = 0 the PDATA registers will contain the ADC output but if a saturation event happened the results will be inaccurate.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit (Status Register) will be set and remain set until the proximity detection function is disabled (PEN).

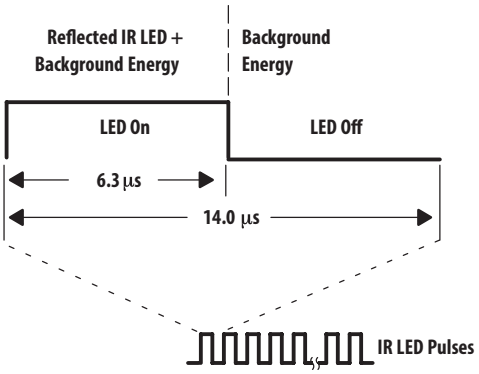


Figure 15. Proximity LED Current Driver Waveform

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0×13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or Clear interrupt enable (AIEN) fields in the enable register (0×00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the Clear data (CDATA) falls outside of the desired light level range, as determined by the values in the Clear interrupt low threshold registers (AILTx) and Clear interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

Note: The thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range Clear or proximity occurrences before an interrupt is generated. The persistence register (0×0C) allows the user to set the Clear persistence (APERS) and the proximity persistence (PPERS) values. See the persistence register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

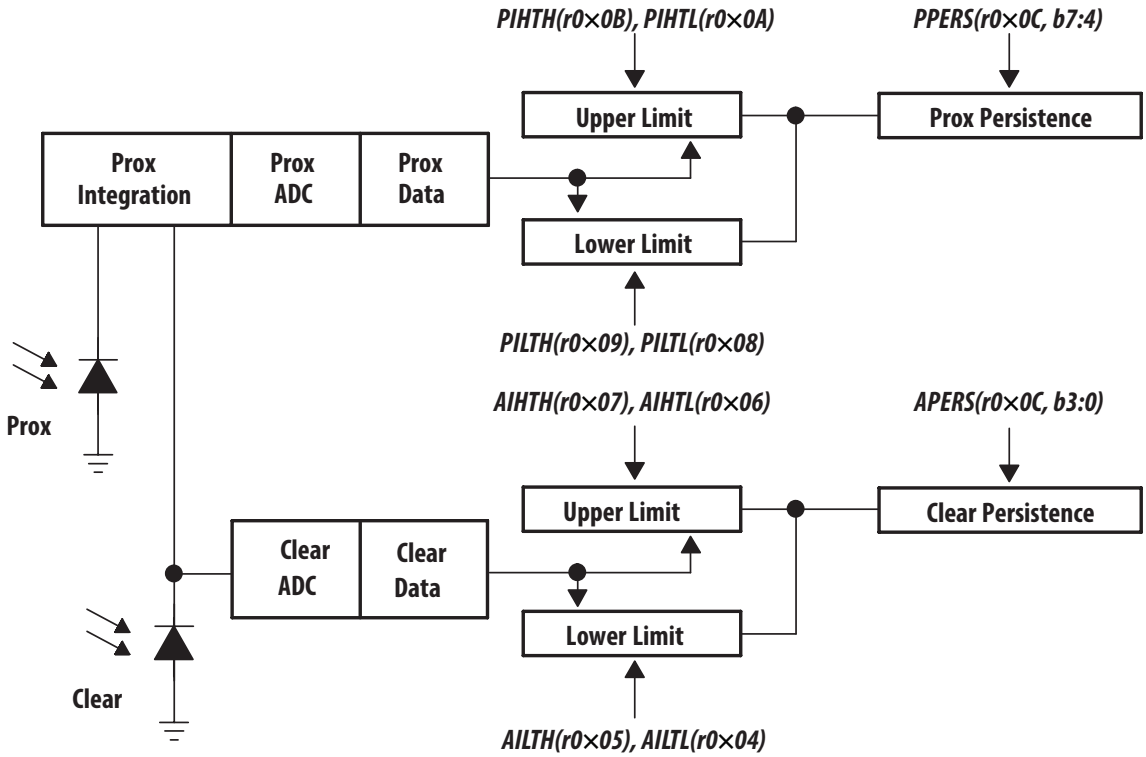


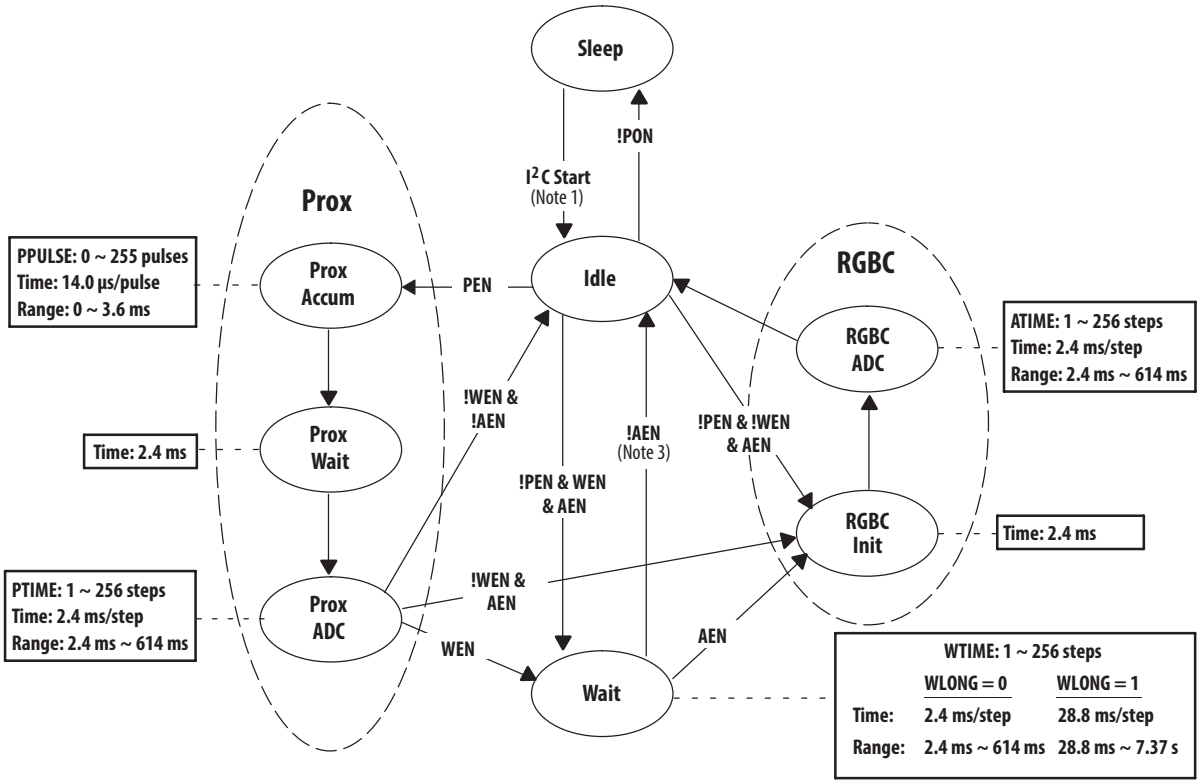
Figure 16. Programmable Interrupt

State Diagram

Figure 17 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.4 ms delay will occur before entering the start state. If the PEN bit is set, the state machine will step through the proximity states of proximity accumulate and then proximity ADC conversion. As soon as the conversion is complete, the state machine will move to the following state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12 over normal operation. When the wait counter terminates, the state machine will step to the RGBC state.

The AEN should always be set, even in proximity-only operation. In this case, a minimum of 1 integration time step should be programmed. The RGBC state machine will continue until it reaches the terminal count, at which point the data will be latched in the RGBC register and the interrupt set, if enabled.



Notes:
1. There is a 2.4 ms warm-up delay if PON is enabled. If PON is not enabled, the device will return to the Sleep state, as shown.
2. PON, PEN, WEN, AEN, and SAI are fields in the Enable register (0x00).
3. PON=1, PEN-1, WEN-1, AEN=0 is unsupported and will lead to erroneous proximity readings.

Figure 17. Expanded State Diagram

I²C Protocol

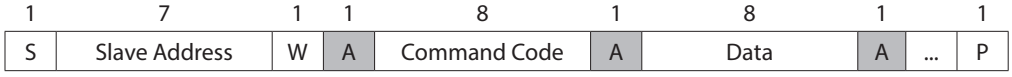
Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The device supports a single slave address of 0×39 Hex using 7-bit addressing protocol. (Contact factory for other addressing options.)

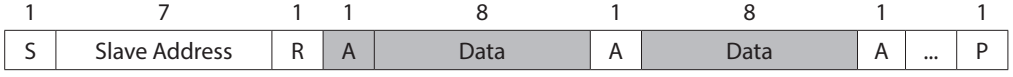
A	Acknowledge (0)
N	Not Acknowledged (1)
P	Stop Condition
R	Read (1)
S	Start Condition
Sr	Repeated Start Condition
W	Write (0)
…	Continuation of protocol
☐	Master-to-Slave
▒	Slave-to-Master

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol. During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

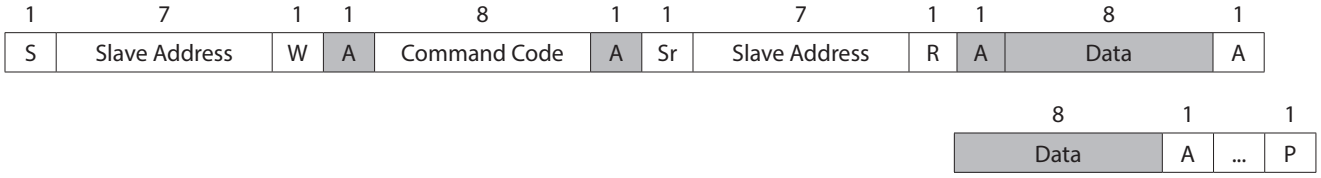
The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.



I²C Write Protocol



I²C Read Protocol



I²C Read Protocol - Combined Format

Register Set

The APDS-9950 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Address	Register Name	R/W	Register Function	Reset Value
––	COMMAND	W	Specifies register address	0×00
0x00	ENABLE	R/W	Enable of states and interrupts	0×00
0x01	ATIME	R/W	RBGC time	0×FF
0x03	WTIME	R/W	Wait time	0×FF
0x04	AILTL	R/W	Clear interrupt low threshold low byte	0×00
0x05	AILTH	R/W	Clear interrupt low threshold high byte	0×00
0x06	AIHTL	R/W	Clear interrupt high threshold low byte	0×00
0x07	AIHTH	R/W	Clear interrupt high threshold high byte	0×00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0×00
0x09	PILTH	R/W	Proximity interrupt low threshold hi byte	0×00
0x0A	PIHTL	R/W	Proximity interrupt hi threshold low byte	0×00
0x0B	PIHTH	R/W	Proximity interrupt hi threshold hi byte	0×00
0x0C	PERS	R/W	Interrupt persistence filters	0×00
0x0D	CONFIG	R/W	Configuration	0×00
0x0E	PPULSE	R/W	Proximity pulse count	0×00
0x0F	CONTROL	R/W	Gain control register	0×00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0×00
0x14	CDATAL	R	Clear ADC low data register	0×00
0x15	CDATAH	R	Clear ADC high data register	0×00
0x16	RDATAL	R	Red ADC low data register	0×00
0x17	RDATAH	R	Red ADC high data register	0×00
0x18	GDATAL	R	Green ADC low data register	0×00
0x19	GDATAH	R	Green ADC high data register	0×00
0x1A	BDATAL	R	Blue ADC low data register	0×00
0x1B	BDATAH	R	Blue ADC high data register	0×00
0x1C	PDATAL	R	Proximity ADC low data register	0×00
0x1D	PDATAH	R	Proximity ADC high data register	0×00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

	7	6	5	4	3	2	1	0	
COMMAND	COMMAND	TYPE		ADD					--

Field	Bits	Description	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		Field Value	**Integration Time**
		00	Repeated byte protocol transaction
		01	Auto-Increment protocol transaction
		10	Reserved — Do not use
		11	Special function – See description below
		Byte protocol will repeatedly read the same register with each data access. Block protocol will provide auto-increment function to read successive bytes.	
ADD	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write or read transactions. The field values listed below apply only to special function commands:	
		Field Value	**Read Value**
		00000	Normal — no action
		00101	Proximity interrupt clear
		00110	Clear interrupt clear
		00111	Proximity and Clear interrupt clear
		other	Reserved – Do not write
		Clear / Proximity Interrupt Clear. Clears any pending Clear / Proximity interrupt. This special function is self-clearing.	

Enable Register (0×00)

The ENABLE register is used primarily to power the APDS-9950 device on and off, and enable functions and interrupts.

	7	6	5	4	3	2	1	0	Address
ENABLE	Reserved	Reserved	PIEN	AIEN	WEN	PEN	AEN	PON	0×00

Field	Bits	Description
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity Interrupt Enable. When asserted, permits proximity interrupts to be generated.
AIEN	4	Ambient Light Sensing (ALS) Interrupt Enable. When asserted, permits ALS interrupts to be generated.
WEN [1][2]	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN [1][2]	2	Proximity Enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN [1][2]	1	RGBC Enable. This bit activates the RGBC function. Writing a 1 enables RGBC. Writing a 0 disables RGBC.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of the PON.

Notes:
1 The PON bit must be set = 1 for these functions to operate.
2. WEN = 1, PEN = 1, AEN = 0 is unsupported and will lead to erroneous proximity readings.

RGBC Time Register (0×01)

The RGBC timing register controls the internal integration time of the RGBC clear and IR channel in the ADCs in 2.4 ms increments. Upon power up, the RGBC time register is set to 0xFF.

Field	Bits	Description			
ATIME	7:0	**VALUE**	**INTEG_CYCLES**	**TIME**	**MAX COUNT**
		0xFF	1	2.4 ms	1024
		0xF6	10	24 ms	10240
		0xD6	42	101 ms	43008
		0xAD	64	154 ms	65535
		0x00	256	614 ms	65535

Wait Time Register (0×03)

Wait time is set 2.4 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the Wait time register is set to 0×FF.

Field	Bits	Description			
WTIME	7:0	**REGISTER VALUE**	**WAIT TIME**	**TIME (WLONG = 0)**	**TIME (WLONG = 1)**
		0xFF	1	2.4 ms	0.029 sec
		0xAB	85	204 ms	2.45 sec
		0x00	256	614 ms	7.4 sec

Note: The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

Clear Interrupt Threshold Registers (0×04 – 0×07)

The Clear interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by the clear channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Register	Address	Bits	Description
AILTL	0×04	7:0	Clear channel low threshold lower byte
AILTH	0×05	7:0	Clear channel low threshold upper byte
AIHTL	0×06	7:0	Clear channel high threshold lower byte
AIHTH	0×07	7:0	Clear channel high threshold upper byte

Proximity Interrupt Threshold Registers (0×08 – 0×0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Register	Address	Bits	Description
PILTL	0x08	7:0	Proximity ADC channel low threshold lower byte
PILTH	0x09	7:0	Proximity ADC channel low threshold upper byte
PIHTL	0x0A	7:0	Proximity ADC channel high threshold lower byte
PIHTH	0x0B	7:0	Proximity ADC channel high threshold upper byte

Persistence Register (0×0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and the clear channel.

	7	6	5	4	3	2	1	0	
PERS	PPERS				APERS				0×0C

Field	Bits	Description		
PPERS	7:4	Proximity Interrupt persistence. Controls rate of proximity interrupt to the host processor.		
		Field Value	**Meaning**	**Interrupt Persistence Function**
		0000	Every	Every proximity cycle generates an interrupt
		0001	1	1 consecutive proximity values out of range
		0010	2	2 consecutive proximity values out of range
		…	…	…
		1111	15	15 consecutive proximity values out of range
APERS	3:0	Clear Interrupt persistence. Controls rate of Clear interrupt to the host processor.		
		Field Value	**Meaning**	**Interrupt Persistence Function**
		0000	Every	Every RGBC cycle generates an interrupt
		0001	1	1 consecutive clear channel values out of range
		0010	2	2 consecutive clear channel values out of range
		0011	3	3 consecutive clear channel values out of range
		0100	5	5 consecutive clear channel values out of range
		0101	10	10 consecutive clear channel values out of range
		0110	15	15 consecutive clear channel values out of range
		0111	20	20 consecutive clear channel values out of range
		1000	25	25 consecutive clear channel values out of range
		1001	30	30 consecutive clear channel values out of range
		1010	35	35 consecutive clear channel values out of range
		1011	40	40 consecutive clear channel values out of range
		1100	45	45consecutive clear channel values out of range
		1101	50	50 consecutive clear channel values out of range
		1110	55	55 consecutive clear channel values out of range
		1111	60	60 consecutive clear channel values out of range

Configuration Register (0×0D)

The configuration register sets the wait long time.

	7	6	5	4	3	2	1	0	
CONFIG	Reserved						WLONG	Reserved	0×0D

Field	Bits	Description
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Proximity Pulse Count Register (0×0E)

The proximity pulse count register sets the number of proximity pulses that will be transmitted.

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								0×0E

Field	Bits	Description
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0×0F)

The Gain register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		PGAIN		AGAIN		0×0F

Field	Bits	Description	
PDRIVE	7:6	**LED Drive Strength**	
		Field Value	**LED Strength**
		00	100 mA
		01	50 mA
		10	25 mA
		11	12.5 mA
PDIODE	5:4	**Proximity Diode Select**	
		Field Value	**LED Strength**
		00	**Reserved**
		01	Reserved
		10	Proximity uses the IR Diode
		11	Reserved
PGAIN	3:2	**Proximity Gain Control**	
		Field Value	**LED Strength**
		00	1× Gain
		01	Reserved
		10	Reserved
		11	Reserved
AGAIN	1:0	**RGBC Gain Control**	
		Field Value	**RGBC Gain Value**
		00	1× Gain
		01	4× Gain
		10	16× Gain
		11	60× Gain

ID Register (0×12)

The ID register provides the value for the part number. The ID is a read-only register.

	7	6	5	4	3	2	1	0	
ID	ID								0×12

Field	Bits	Description
ID	7:0	Part number identification
		0×69 = APDS-9950

Status Register (0×13)

The Status Register provides the internal status of the device. This register is read-only.

	7	6	5	4	3	2	1	0	
STATUS	Reserved	Reserved	PINT	AINT	Reserved	Reserved	PVALID	AVALID	0×13

Field	Bits	Description
Reserved	7:6	Reserved.
PINT	5	Proximity Interrupt.
AINT	4	Clear Interrupt.
Reserved	3:2	Reserved.
PVALID	1	Proximity Valid. Indicates that a proximity cycle has completed since PEN was asserted
AVALID	0	RGBC Valid. Indicates that a RGBC cycle has completed since AEN was asserted

RGBC DATA Register (0×14 – 0×1B)

Clear, red, green, and blue data is stored as 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Register	Address	Bits	Description
CDATAL	0×14	7:0	Clear data low byte
CDATAH	0×15	7:0	Clear data high byte
RDATAL	0×16	7:0	Red data low byte
RDATAH	0×17	7:0	Red data high byte
GDATAL	0×18	7:0	Green data low byte
GDATAH	0×19	7:0	Green data high byte
BDATAL	0×1A	7:0	Blue data low byte
BDATAH	0×1B	7:0	Blue data high byte

Proximity DATA Register (0×1C – 0×1D)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two byte read I^2C transaction should be utilized with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Register	Address	Bits	Description
PDATAL	0×1C	7:0	Proximity data low byte
PDATAH	0×1D	7:0	Proximity data high byte

Application Information Hardware

In a proximity sensing system, the included IR LED can be pulsed by the APDS-9950 with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. If V_{BATT} does not exceed the maximum specified LDR pin voltage (including when the battery is being recharged), LEDA can be directly tied to V_{BATT} for best proximity performance.

In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the VDD pin and the noisy supply to the LED, the key goal can be meet. Place a 1 μF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LED anode, and a 22 μF capacitor at the output of the LED voltage regulator to supply the 100 mA current surge.

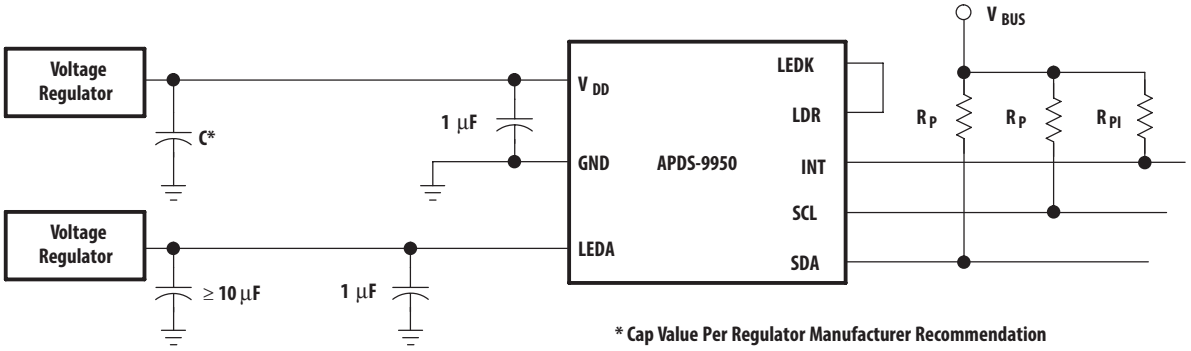


Figure 18a. Circuit Implementation using Separate Power Supplies

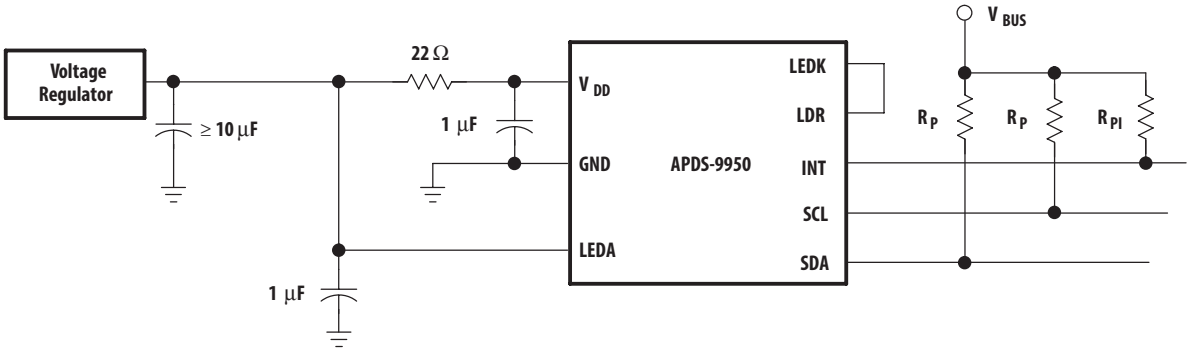


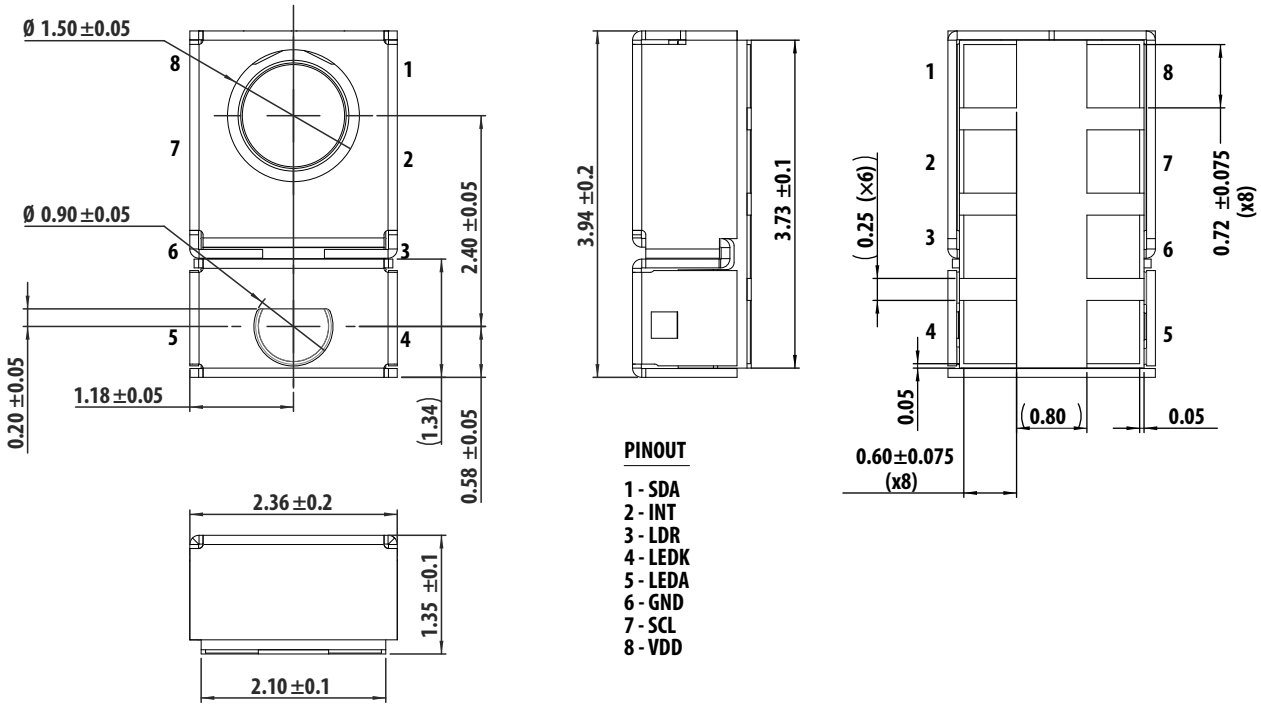
Figure 18b. Circuit Implementation using Single Power Supply

If operating from a single supply, use a 22 Ω resistor in series with the V_{DD} supply line and a 1 μF low ESR capacitor to filter any power supply noise. The previous capacitor placement considerations apply.

V_{BUS} in the above figures refers to the I²C-bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I²C-bus voltage shown in the Available Options table for the specific device being used.

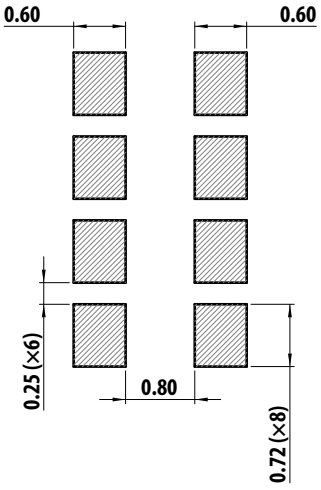
The I²C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (RP) value is a function of the I²C-bus speed, the I²C-bus voltage, and the capacitive load. A 10 kΩ pull-up resistor (RPI) can be used for the interrupt line.

Package Outline Dimensions



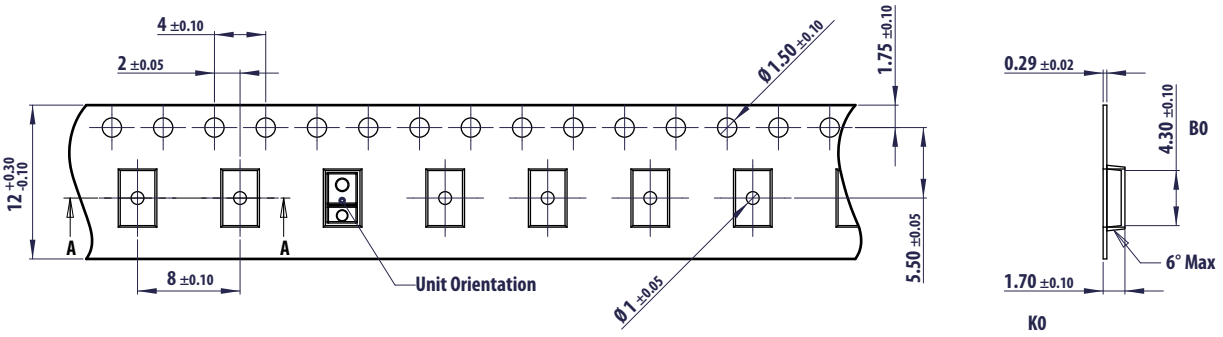
PCB Pad Layout

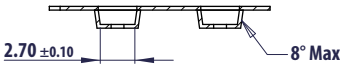
Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are shown below.



Note: All linear dimensions are in mm.

Tape Dimensions

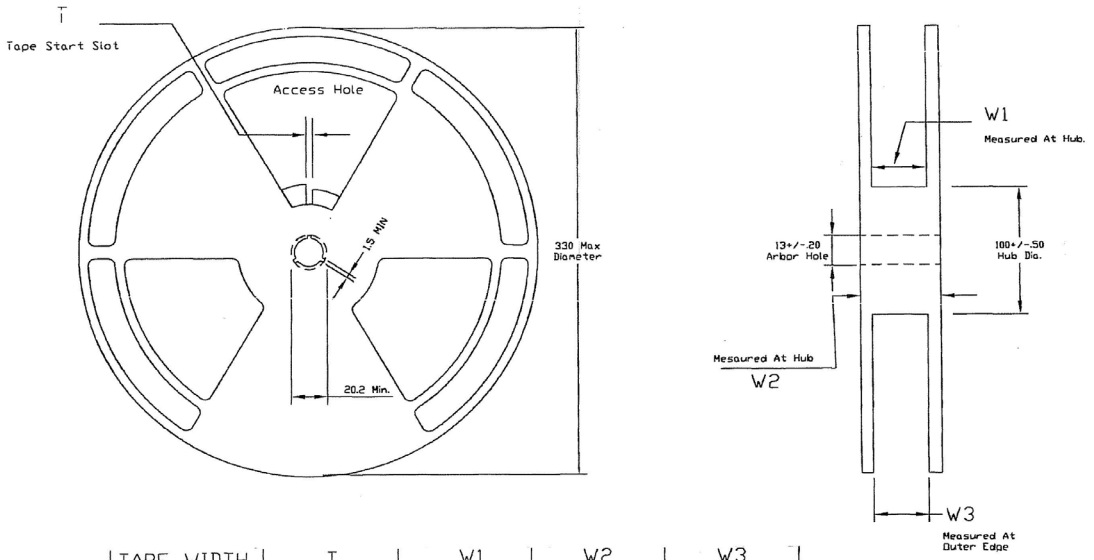




A0

Note: All linear dimensions are in mm.

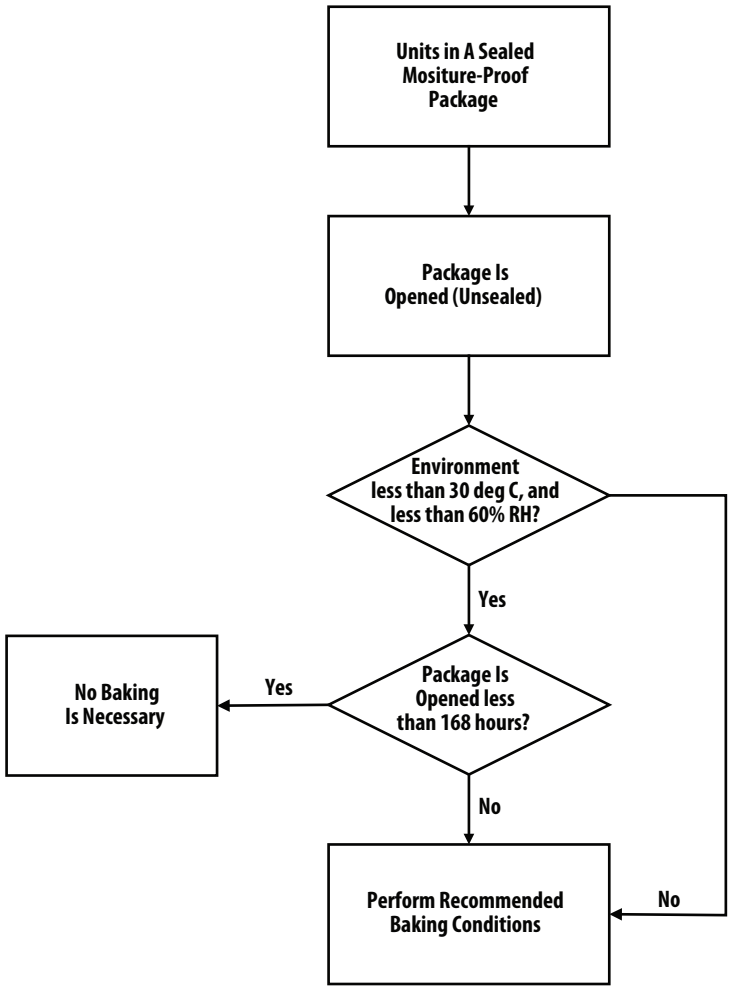
Reel Dimensions



TAPE WIDTH	T	W1	W2	W3
12MM	4+/-.50	12.4+2.0 -0.0	18.4 MAX	11.9MIN 15.4MAX

Moisture Proof Packaging

All APDS-9950 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

Package	Temperature	Time
In Reel	60 °C	48 hours
In Bulk	100 °C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

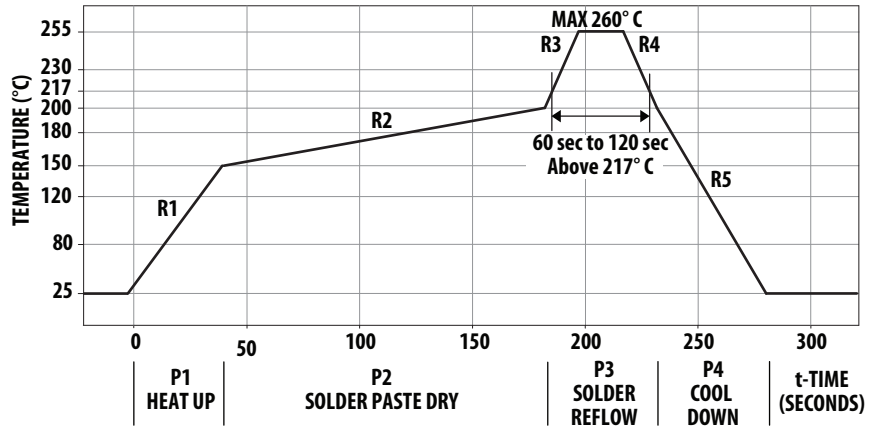
Recommended Storage Conditions

Storage Temperature	10 °C to 30 °C
Relative Humidity	below 60% RH

Time from unsealing to soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25 °C to 150 °C	3 °C/s
Solder Paste Dry	P2, R2	150 °C to 200 °C	100 s to 180 s
Solder Reflow	P3, R3	200 °C to 260 °C	3 °C/s
	P3, R4	260 °C to 200 °C	-6 °C/s
Cool Down	P4, R5	200 °C to 25 °C	-6 °C/s
Time maintained above liquidus point , 217 °C		> 217 °C	60 s to 120 s
Peak Temperature		260 °C	–
Time within 5 °C of actual Peak Temperature		> 255 °C	20 s to 40 s
Time 25 °C to Peak Temperature		25 °C to 260 °C	8 mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and component pins are heated to a temperature of 150 °C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3 °C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260 °C (500 °F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 120 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25 °C (77 °F) should not exceed 6 °C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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