Data Sheet

BCM53125S

Multiport Gigabit Ethernet Switches

GENERAL DESCRIPTION

The Broadcom® BCM53125S is a highly integrated, cost-effective smart-managed Gigabit switch. The switch design is based on the field-proven, industry-leading ROBO architecture. This device combines all the functions of a high-speed switch system including packet buffers, PHY transceivers, media access controllers (MACs), address management, port-based rate control, and a nonblocking switch fabric into a single 65-nm CMOS device. Designed to be fully compliant with the IEEE 802.3 and IEEE 802.3x specifications, including the MAC-control PAUSE frame, the BCM53125S provides compatibility with all industry-standard Ethernet, fast Ethernet, and Gigabit Ethernet (GbE) devices.

The BCM53125S has a rich feature set suitable for not only standard GbE connectivity for desktop and laptop PCs, but also for next-generation gaming consoles, set-top boxes, networked DVD players, and home theater receivers. It is also specifically designed for next-generation SOHO/SMB routers and gateways.

The BCM53125S contains five full-duplex 1000Base-T/100Base-TX/10Base-T Ethernet transceivers. In addition, the BCM53125S has one GMII/RGMII/MII/RvMII/TMII/RvTMII interface for the CPU or a router chip, providing flexible

10/100/1000 Mbps connectivity. A GMII/RGMII/MII/RvMII/TMII/RvTMII interface for the WAN port can be configured as an IMP port.

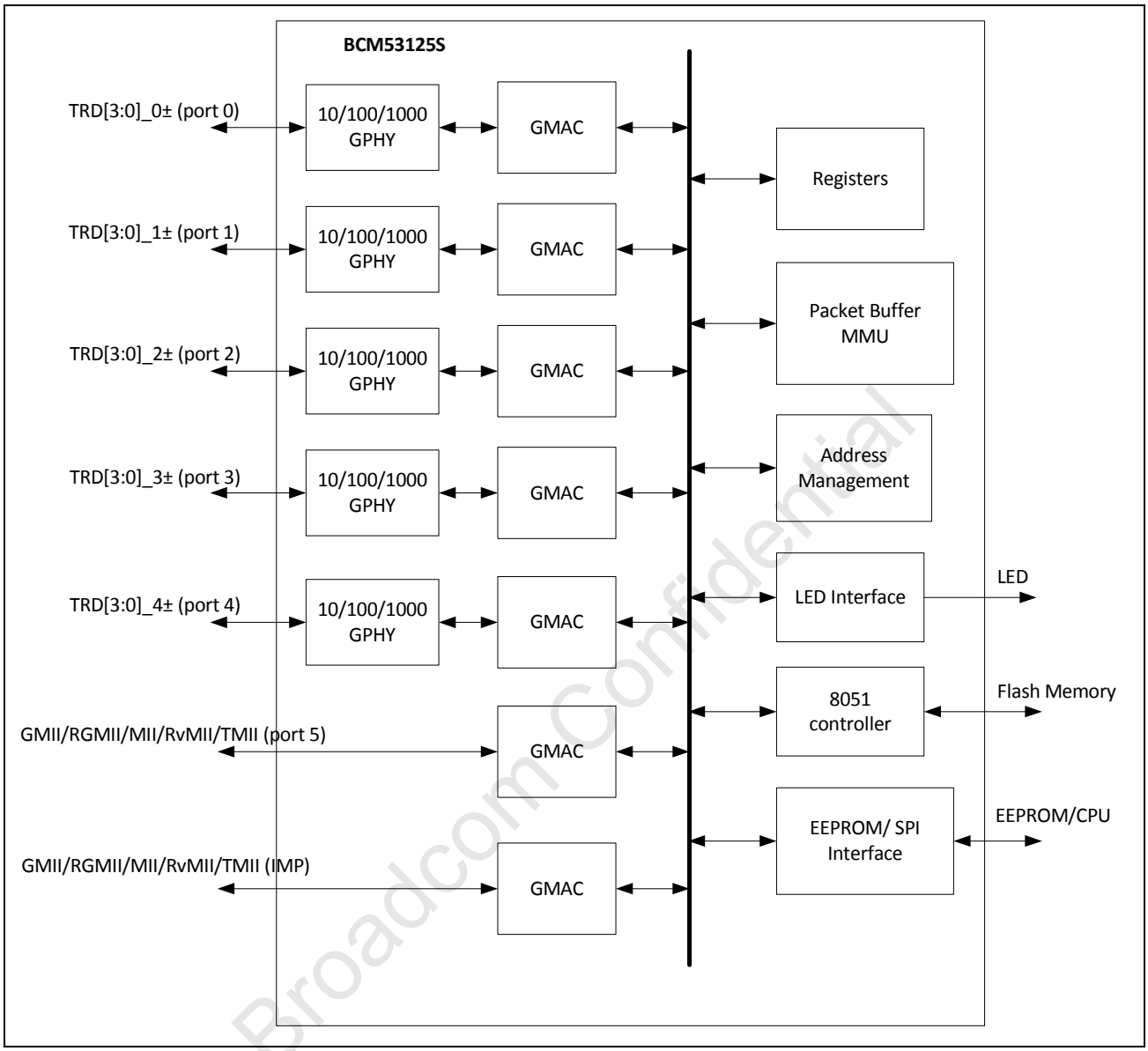
The BCM53125S provides 70+ on-chip MIB counters to collect receive and transmit statistics for each port.

The BCM53125S is available in industrial temperature (I-Temp) and commercial temperature (C-Temp) rated packages. The BCM53125S is available in one package type, a 186-pin multirow MLF (MML) package.

FEATURES

- Seven 10/100/1000 media access controllers
- Five-port 10/100/1000 transceivers for TX
- One GMII/RGMII/MII/RvMII/TMII/RvTMII interface for an inband management port (IMP) for connection to a CPU/management entity without PHY
- One GMII/RGMII/MII/RvMII/TMII/RvTMII interface for WAN management port
- Dual IMP ports support, WAN interface (port 5) to be management port-capable
- IEEE 802.1p, MAC Port, ToS, and DiffServ QoS for four queues, plus two time-sensitive queues
- Port-based VLAN
- IEEE 802.1Q-based VLAN with 4K entries
- MAC-based trunking with automatic link failover
- Port-based rate control
- Port mirroring
- BroadSync® HD for IEEE 802.1AS support
  - Timestamp tagging at MAC interface
  - Time-aware egress scheduler
- DoS attack prevention
  - Support IPv6
  - Ingress mirroring
- IGMP snooping, MLD snooping support
- Spanning tree support (multiple spanning trees, up to eight)
- Embedded CPU (8051) processor for cable diagnostics, and green power saving mode.
- CableChecker™ with unmanaged mode support
- Double tagging/QinQ
- Egress VID remarking
- IEEE 802.az EEE (Energy Efficient Ethernet™) support
- IEEE 802.1AS support
- IEEE 802.3x programmable per-port flow control and backpressure, with IEEE 802.1x support for secure user authentication
- EEPROM, MDC/MDIO, and SPI Interface
- Serial Flash Interface for accessing embedded CPU (8051)
- 4K entry MAC address table with automatic learning and aging
- 128 KB packet buffer (1 KB = 1024 bytes)
- 128 multicast group support
- Jumbo frame support up to 9720 byte
- 1.2V for core and 3.3V for I/O
- RGMII with option of 2.5V or 1.5V
- JTAG support
- 186-pin multirow MLF (MML) package

Figure 1: Functional Block Diagram



Revision History

Revision	*Date*	*Change Description*
53125S-DS06-R	3/11/16	Note: Page numbers referenced are valid for this revision of the document only. **Updated:** • Section 12: “Ordering Information,” on page 307 **Added:** • “JTAG Interface” on page 300
53125S-DS05-R	04/27/11	**Updated:** • “TMII (TURBO MII) and RvTMII (Reverse TMII) Interface” on page 96: removed the Note stating “The BCM53125S does not support RvTMII (Reverse TMII) mode." • Table 33: “Signal Descriptions,” on page 131: corrected the typo of the FCS_B signal name. • Table 286: “Absolute Maximum Ratings,” on page 293: changed V_{ESD} Maximum value to 1800V.
53125S-DS04-R	01/19/11	**Added:** • “BroadSync HD Egress Time Stamp Status Registers (Page 90h: Address D0h)” on page 283 • “BroadSync HD Link Status Register (Page 90h: Address E0h–E1h)” on page 284 • Figure 63: “MDC/MDIO Timing (Master Mode),” on page 309

Revision	Date	Change Description
		Updated: • "Multicast Addresses" on page 63 • "Address Aging" on page 66 • Figure 45: "Write Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path," on page 122 • Figure 50: "Internal Digital Regulator Controller," on page 129 • Table 33: "Signal Descriptions," on page 131 • "MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)" on page 162 • "Software Reset Control Register (Page 00h: Address 79h)" on page 166 • "VLAN Table Entry Register (Page 05h: Address 83h–86h)" on page 198 • "PHY Identifier Register (Page 10h–14h: Address 04h)" on page 205 • "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 264 • "Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)" on page 267 • Table 287: "Recommended Operating Conditions," on page 294 • Table 299: "RGMII Output Timing (Normal Mode)," on page 302 • Table 300: "RGMII Output Timing (Delayed Mode)," on page 303 • Table 304: "GMII Input Timing," on page 307 • Table 306: "MDC/MDIO Timing (Master Mode)," on page 309 • "SPI Timings" on page 311 **Removed:** • Figure "SPI Timings, SS Asserted During SCK Low"
53125S-DS03-R	09/20/10	**Added** • Table 286: "Internal Voltage Regulator Electrical Characteristics," on page 291 • Figure 67: "186-Pin Package (1 of 3) - Top View," on page 312 • Figure 68: "186-Pin Package (2 of 3) - SectionC-C," on page 313 • Figure 69: "186-Pin Package (3 of 3) - Bottom View," on page 314

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53125S-DS03-R (continued)		**Updated:** • Features on page 2 • “Deep Green Mode” on page 64 • Table 30: “20 LED Display Mode (GMII_LED_SEL=1),” on page 120 • Table 31: “10 LED Display Mode (GMII_LED_SEL=0),” on page 120 • Table 32: “Dual Input Configuration/LED Output Function,” on page 123 • “Internal Digital Regulator Controller” on page 124 • Figure 50: “Internal Digital Regulator Controller,” on page 125 • Table 34: “Signal Descriptions,” on page 127 • “LED Interfaces” on page 119 • “Pin List by Pin Number” on page 138 • “Pin List by Signal Name” on page 141 • Table 85: “Broadcom Tag Control Register (Page 02h: Address 03h),” on page 171 • Table 96: “Egress Mirror MAC Address Register (Page 02h: Address 40h),” on page 176 • Table 87: “Aging Time Control Register (Page 02h: Address 06h–09h),” on page 172 • Table 200: “Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h),” on page 252 • “Absolute Maximum Ratings” on page 289 • “Recommended Operating Conditions” on page 289 • “Electrical Characteristics” on page 290 • Table 285: “Electrical Characteristics,” on page 290 • Section 10: “Thermal Characteristics,” on page 309 • Figure 67: “186-Pin Package (1 of 3) - Top View,” on page 312 • Figure 51: “Reset and Clock Timing,” on page 292 • “BCM53125MKMML 2-Layer PCB Package Without a Heat Sink” on page 310 • “BCM53125MKMML 2-Layer PCB Package With a Heat Sink” on page 309 • “BCM53125MKMML 4-Layer PCB Package Without a Heat Sink” on page 311

Revision	*Date*	*Change Description*
53125S-DS03-R (continued)		**Removed:** • Table 238: Loop Detection Control Register (Page 72h) • Table 239: Loop Detection Control Registers (Page 72h: Address 00h-01h) • Table 239: Loop Detection Control Registers (Page 72h: Address 00h-01h) • Table 240: Discovery Frame Timer Control Registers (Page 72h: Address 02h) • Table 241: LED Warning Port Map registers (Page 72h: Address 03h-04h) • Table 242: Module ID 0 Registers (Page 72h: Address 05h-0Ah) • Table 243: Module ID 1 Registers (Page 72h: Address 0Bh-10h) • Table 244: Loop Detect Source Address Registers (Page 72h: Address 11h-16h) • Figure 67: 186-Pin Package • Figure 68: BCM53125S Pin Number Orientation
53125S-DS02-R	05/18/10	**Added:** • Table 65: “RGMII Timing Delay Register for IMP Port (Page 00h: Address 60h),” on page 162 • Table 66: “RGMII Timing Delay Register for Port 5 (Page 00h, Address 65h),” on page 163 • Note after Table 284: “Recommended Operating Conditions,” on page 289

Revision	*Date*	*Change Description*
53125S-DS02-R (continued)		**Updated:** • Figure 1: “Functional Block Diagram,” on page 2 • “Double Tagging” on page 39 • “WAN Port” on page 43 • “Ingress Rate Control” on page 44 • “Reserved Multicast Addresses” on page 60 • “LED Interfaces” on page 119 • Table 85: “Broadcom Tag Control Register (Page 02h: Address 03h),” on page 171 • Default values in Table 130: “MII Control Register (Page 10h–14h: Address 00h–01h),” on page 199, Table 134: “Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h),” on page 201, Table 139: “1000BASE-T Control Register (Page 10h–14h: Address 12h–13h),” on page 205, Table 213: “Global Rate Control Register (Page 41h: Address 00h–03h),” on page 259, Table 215: “Port Rate Control Register (Page 41h: Address 10h–33h),” on page 261 • Table 259: “EEE Enable Control Register (Page 92h: Address 00h),” on page 281 • Table 260: “EEE LPI Assert Register (Page 92h: Address 02h),” on page 282 • Table 261: “EEE LPI Indicate Register (Page 92h: Address 04h),” on page 282 • Table 262: “EEE RX Idle Symbol Register (Page 92h: Address 06h),” on page 283 • Table 263: “EEE Pipeline Timer Register (Page 92h: Address 0Ch),” on page 283 • Table 277: “EEE TXQ Congestion Threshold Register (Page 92h: Address C6h),” on page 286 • Table 278: “EEE TXQ Congestion Threshold Register (Page 92h: Address C6h–D1h),” on page 287 • I_{DD} in Table 285: “Electrical Characteristics,” on page 290 **Removed:** • Table 151: “Expansion Register Access Register (Page 10h–14h: Address 2Eh–2Fh)” • Table 152: “Expansion Register Select Values” • “Expansion Registers”

Revision	*Date*	*Change Description*
53125S-DS01-R	01/13/10	**Updated:** • “TMII (TURBO MII) and RvTMII (Reverse TMII) Interface” on page 57: TMII SPEED setting register. • “SCK: Serial Clock” on page 60: Maximum operating frequency. • “Internal Digital Regulator Controller” on page 89: Voltage values. • Table 27, ”Dual Input Configuration/LED Output Function,” on page 88: LED[1] input pins. • Table 29, ”Signal Descriptions,” on page 92: IMP_TXCLK, SCK/SK, LED1 LED5, LED6 definitions. • Table 291, ”Electrical Characteristics,” on page 245: I_{DD} conditions and input and output voltages. • Table 292, ”Reset and Clock Timing,” on page 246: RESET rise time maximum. • Table 310, ”SPI Timings,” on page 259: SCK clock period and SCK high/low time values. • Figure 67, ”BCM53125S Pin Number Orientation,” on page 263: Ring labels.
53125S-DS00-R	11/16/09	Initial release

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About This Document

Purpose and Audience

This document describes the Broadcom® BCM53125S, a highly integrated, cost-effective smart-managed Gigabit switch. The switch design is based on the field-proven, industry-leading ROBO architecture.

This document is for designers interested in integrating the BCM53125S switches into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM53125S switches.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Notational Conventions

The following notational conventions are used in this document:

- Signal names are shown in uppercase letters (such as DATA).
- A bar over a signal name indicates that it is active-low (such as CE).
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m. For example, [7:0] indicates bits 7 through 0, inclusive.
- The use of R or Reserved indicates that a bit or a field is reserved by Broadcom for future use. Typically, R is used for individual bits and Reserved is used for fields.
- Numerical modifiers such as K or M follow traditional usage. For example, 1 KB means 1,024 bytes, 100 Mbps (referring to fast Ethernet speed) means 100,000,000 bps, and 133 MHz means 133,000,000 Hz).

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	*Number*	*Source*
Broadcom Items		
[1] Energy Efficient Ethernet™	53125-AN2xx-R	CSP
[2] Layout and Design Guidelines	53125-AN100-R	CSP
Other Items		
[3] Motorola SPI spec	MC68HC08AS20-Rev. 4.0.	

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Overview

The BCM53125S is a single-chip, seven-port Gigabit Ethernet (GbE) switch device. It provides the following:

- A seven-port nonblocking 10/100/1000 Mbps switch controller
- Five ports with 1000Base-T/100Base-TX/10Base-T-compatible transceivers
- Seven integrated gigabit MACs (GMACs)
- One GMII/RGMII/MII/RvMII/TMII/RvTMII port for PHY-less connection to the management agent (only available in full duplex mode)
- One GMII/RGMII/MII/RvMII/TMII/RvTMII interface for a WAN management port (only available in full-duplex mode)
- An integrated Motorola SPI-compatible interface
- A high-performance, integrated packet buffer memory
- An address resolution engine
- A set of management information base (MIB) statistics registers

The GMACs support full-duplex and half-duplex modes for 10 Mbps and 100 Mbps and full-duplex for 1000 Mbps. Flow control is supported in the half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is supported. The GMACs are IEEE 802.3™-compliant and support maximum frame sizes of 9720 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for learning up to 4K unicast addresses. Addresses are added to the table after receiving error-free packets.

The MIB statistics registers collect receive and transmit statistics for each port and provide direct hardware support for the Etherlike MIB, MIB II (interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the Serial Peripheral Interface (SPI) port by an external microcontroller.

Section 2: Features and Operation

Overview

The BCM53125S switches include the following features:

The following sections discuss each feature in detail.

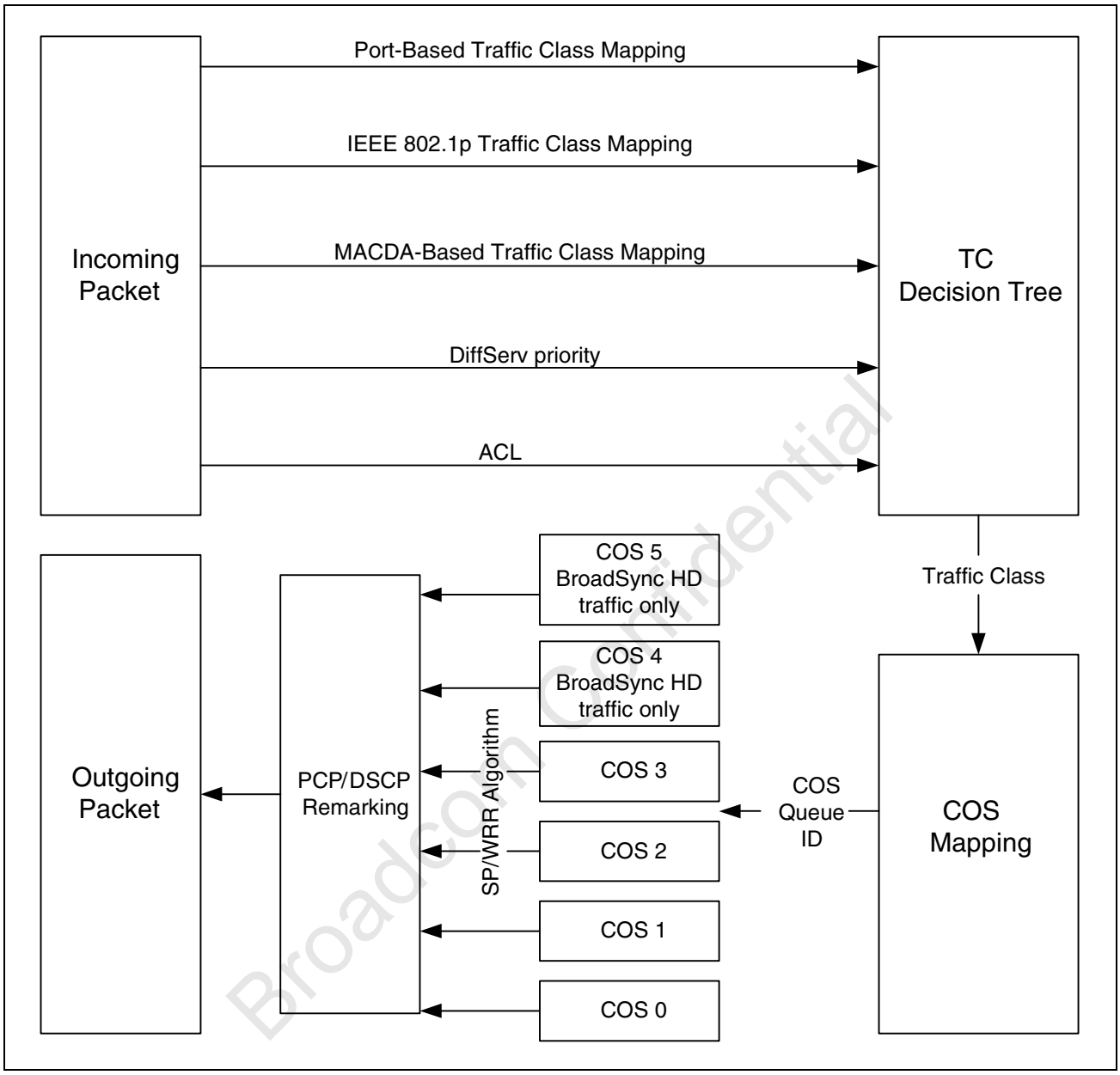
Quality of Service

The Quality of Service (QoS) feature provides up to six internal queues per port to support eight different traffic classes (TCs). The traffic classes can be programmed so that higher-priority TCs in the switch experiences less delay than lower-priority TCs under congested conditions. This can be important in minimizing latency for delay-sensitive traffic. The BCM53125S switches can assign the packet to one of the six egress transmit queues according to information in:

- “Port-Based QoS” on page 37 (ingress port ID)
- “IEEE 802.1p QoS” on page 37
- “MACDA-Based QoS” on page 37
- “ToS/DSCP QoS” on page 38
- “TC Decision Tree” on page 38
- “Queuing Class (COS) Determination” on page 39

The “TC Decision Tree” on page 38 identifies which priority system is used based on three programmable register bits, which are detailed in Table 1: “TC Decision Tree Summary,” on page 38. The corresponding traffic class is then assigned to one of the six queues on a port-by-port basis.

Figure 2: QoS Program Flow



Egress Transmit Queues

Each Ethernet egress port has six transmit queues (COS0–COS5). The COS4 and COS5 queues are dedicated to BroadSync HD traffic only and cannot be shared with other traffic. Each COS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purposes. Every Ethernet (ingress) port has its own set of counters to measure the buffer occupancy and the arrival rate of traffic received from the port.

The IMP (egress) port serves four queues (COS0–COS3) and the traffic generated by the Local Management Packet Generator which generate management report messages back to CPU, e.g., the Time Sync TX time stamp packets.

Each COS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. The IMP (ingress) port also has its own set of counters to measure the buffer occupancy and the arrival rated to the traffic received from the port, but should be used only if it is configured as a regular Ethernet port.

All incoming frames are assigned to an egress transmit queue depending on their assigned TC. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port transmits packets from each of the queues according to a programmable algorithm, with the higher TC queues being given greater access than the lower TC queues. Queue 0 is the lowest-TC queue.

The COS0–COS3 queues are dedicated to non-BroadSync HD traffic only. The BCM53125S uses strict priority (SP) and a weighted round robin (WRR) algorithm for COS0–COS3 queues scheduling. The scheduling is configurable as one of the following combination of SP and WRR:

- 4SP, 4WRR
- 1SP, 3WRR
- 2SP, 2WRR

The WRR algorithm weights for each queue can be programmed using registers.

Port-Based QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with the TC configured for the corresponding port. The mapping mechanism is globally enabled and disabled using register programming. When disabled, the TC that results from this mapping is 000.

IEEE 802.1p QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC configured for the corresponding IEEE 802.1p priority code point (PCP). When disabled, or if the incoming packet is not tagged, the TC that results from this mapping is 000.

MACDA-Based QoS

MAC destination address (MACDA)-based QoS is enabled when IEEE 802.1p QoS is disabled using the 802_1P_EN bit. When using MACDA-based QoS, the destination address and VLAN ID is used to index the address resolution logic (ARL) table, as described in “Address Management” on page 57. The matching ARL entry contains a 3-bit TC field as shown in Table 7 on page 60. These bits set the MACDA-based TC for the frame. The MACDA-based TC is assigned to the TC bits depending on the result shown in Table 1 on page 38. The TC bits for a learned ARL entry default to 0. For more information about the egress transmit queues, see “Egress Transmit Queues” on page 36.

ToS/DSCP QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC configured for the corresponding IP ToS/DSCP. When disabled or the incoming packet is not of IPv4/v6 type, the TC resulted from this mapping is 000.

TC Decision Tree

Non-BroadSync HD Frame

The TC decision tree determines which priority system is assigned to TC-mapping bits for the given frame. As summarized in the preceding sections, the TC bits for the frame can be determined according to the ingress port-based TC, IEEE 802.1p TC, MACDA-based TC, or DiffServ TC. The decision of which TC mapping to use is based on the Port_QoS_En bit and the QoS_Layer_Sel bits. Table 1 summarizes how these programmable bits affect the derived TC. The DiffServ and IEEE 802.1p QoS TC are available only if the respective QoS is enabled and the received packet has the appropriate tagging.

Table 1: TC Decision Tree Summary

Port_QoS_En	*QoS_Layer_Sel*	*Value of TC Bits*
0	00	IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping.
0	01	DiffServ TC mapping if available; otherwise, TC = 000.
0	10	DiffServ TC mapping for IP frame; otherwise, IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping.
0	11	Highest available TC of the following: IEEE 802.1p TC mapping, DiffServ TC mapping, or MACDA-based TC mapping.
1	00	Port-based TC mapping.
1	01	Port-based TC mapping.
1	10	Port-based TC mapping.
1	11	Highest available TC of the following: Port-based TC mapping, IEEE 802.1p TC mapping, DiffServ TC mapping, or MACDA-based TC mapping.

For the packets received from an Ethernet port when the ACL rules generate a TC-change request, the ACL derived TC overwrites the priority generated by the Table 1 TC-mapping mechanisms.

BroadSync HD Frame

For the BroadSync HD packet from an Ethernet port, the TC is determined directly from the explicit IEEE 802.1Q/P tag carried in the BroadSync HD packets (BroadSync HD packets are expected to always be tagged), which is independent of the Table 1 TC mapping (including ACL-based mapping). The conditions that determine whether an incoming packet is a BroadSync HD packet are as follows:

- The port from which the packet is received is configured as AV-enabled.

- The packet received is either VLAN-tagged or priority-tagged. The priority value can be any value as long as it matches the programmed value. The switch default setting of BroadSync HD priority values are 4 for class 4 and 5 for class 5.
- The MACDA can be either a multicast or unicast address as long as the MAC address matches the configured (registered) BroadSync HD MAC addresses in the switch.

Note: BroadSync HD cannot be received from the IMP port.

Queuing Class (COS) Determination

The BCM53125S supports the COS mapping through the following mapping mechanisms:

- TC to COS mapping: The queuing class to forward a packet to an Ethernet port is mapped from the TC determined for the packet.
- BroadSync HD to COS mapping: The queuing class to forward a BroadSync HD packet to an AV-enabled Ethernet port is mapped from the PCP carried by the packet. PCP5 is mapped to COS5 and PCP4 is mapped to COS4.
- CPU to COS mapping: The queuing class to forward a packet to the external CPU through the IMP port is determined based on the reasons to forward (copy or trap) the packet to CPU.

Note: When the BCM53125S is configured in the aggregation mode where the IMP operates as the uplink port to the upstream network processor, the COS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operates as the interface to the management CPU, and the COS is decided based on the reasons for forwarding the packet to the CPU.

Table 2 shows the reasons for forwarding a packet to the CPU.

Table 2: Reasons to Forward a Packet to the CPU

ToCPU Reason	*Description*	*ToCPU COS*
Mirroring	The packet is forwarded (copied) through the IMP port because it must be mirrored to the CPU as the capturing device.	0
SA Learning	The packet is forwarded (copied) through the IMP port because its SA must be learned by the CPU. The SW_LEARN_CNTL bit of the Software Learning register must be enabled.	0
Switching	The packet is forwarded through the IMP port either because the CPU is one of the intended destination hosts of the packet.	0
Protocol Termination	The packet is forwarded (trapped) through the IMP port because it implies an IEEE 802.1 defined L2 protocol that must be terminated by the CPU.	0
Protocol Snooping	The packet is forwarded (copied) through the IMP port because it implies an L3 or application level protocol that must be monitored by the CPU for network security or operation efficiency.	0

Table 2: Reasons to Forward a Packet to the CPU (Cont.)

ToCPU Reason	*Description*	*ToCPU COS*
Exception Processing/Flooding	The packet is forwarded (trapped) through the IMP port for some special processing even though the CPU is not the intended destination, or because the switch makes the flooding decision to reach all potential destinations.	0

The ToCPU COS values listed in Table 2 are the default setting and are configurable. In order to prevent out of order delivery of the same packet flow to the CPU, the COS for the mirroring and SA learning reasons must be programmed with a value that is lower than or equal to the value of the other reasons.

A packet could be forwarded to the CPU for more than one reason, therefore the COS selection is based on the highest COS values among all the reasons for the packet.

Port-Based VLAN

The port-based virtual LAN (VLAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM53125S provide flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to nonprivate domain ports. For each received packet, the ARL resolves the destination address (DA) and obtains a forwarding vector (list of ports to which the frame will be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the nonprivate domain ports. The frame is only forwarded to those ports that meet the ARL table criteria, as well as the port-based VLAN criteria.

IEEE 802.1Q VLAN

The BCM53125S support IEEE 802.1Q VLAN and up to approximately 4000 VLAN table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller, the BCM53125S autonomously handles all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tag, depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups, in addition to MAC L2 lookups.

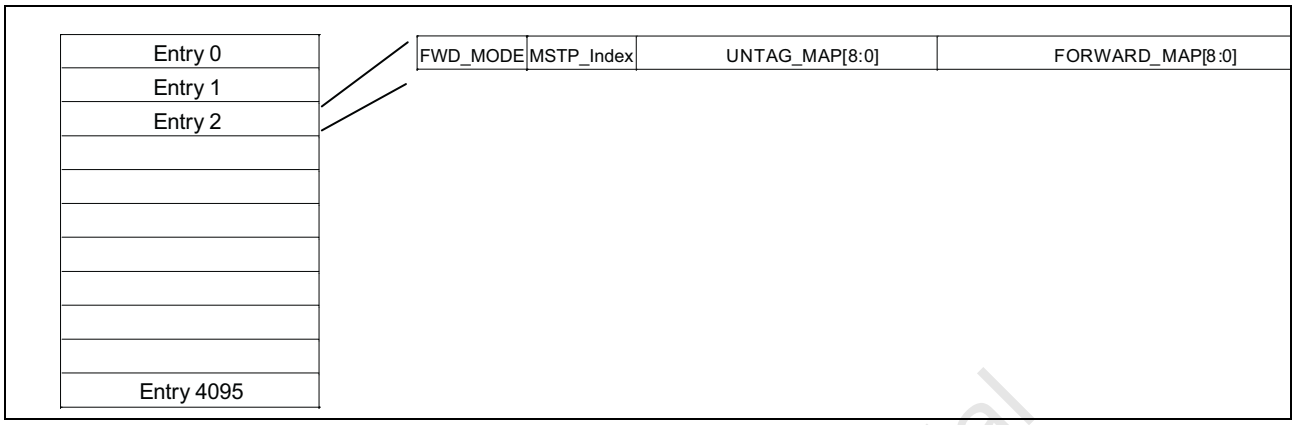
IEEE 802.1Q VLAN Table Organization

Each VLAN table entry, also referred to as a VLAN ID, has untag map and a forward map.

- The untag map controls whether the egress packet is tagged or untagged.
- The forward map defines the membership within a VLAN domain.
- The FWD_MODE indicates whether packet forwarding should be based on VLAN membership or on ARL flow.

The untag map and forward map include bit-wise representation of all the ports.

Figure 3: VLAN Table Organization



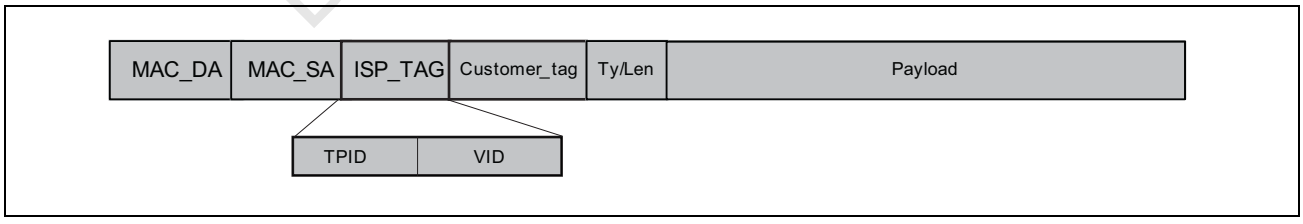
Note: If the MII port is configured as a management port, then the tag is not stripped even if the untag bit is set.

Double Tagging

The BCM53125S provides a double-tagging feature, which is useful for ISP applications. When the ISP aggregates incoming traffic from each individual customer, the extra tag (double tag) can provide an additional layer of tagging to the existing IEEE 802.1Q VLAN. The ISP tag (extra tag) is a way of distinguishing one customer from another. Using the IEEE 802.1Q VLAN tag, an individual customer's traffic can be identified on a per-port basis.

When the double-tagging feature is enabled (register page 34h, address 05h, bits [3:2]) and IEEE 802.1Q is enabled (register page 34h, address 00h, bit 7), users can expect two VLAN tags in a frame: The tag close to MAC_SA is the ISP tag and the one that follows it is the customer tag, as shown in Figure 4.

Figure 4: ISP Tag Diagram



The switch uses the ISP tag for ARL and VLAN table accesses and uses the customer tag as an IEEE 802.1Q tag. There is a per-chip programmable Double Tagging TPID register for the ISP tag (default = 9100'h). All ISP tags are qualified by this Tag Protocol ID (TPID) value.

When the double-tagging feature is enabled, all switch ports are separated into two groups: ISP ports and customer ports. The BCM53125S performs the normalization process for all ingress frames in both IDT and DT modes, whether from the ISP port or the customer port. The normalization process inserts an ISP tag, customer tag, or ISP + customer tag (depending whether the ingress frame is without tags or with one tag) to allow all ingress frames with double tags. But if the ingress frames have double tags (ISP + customer tag) and the ISP tag TPID matches the TPID specified in the Double Tagging TPID register, the normalization process is not performed. The ISP ports are defined in the ISP Port Selection Portmap register. When the port(s) corresponding bit(s) are set, that port(s) should be connected to the ISP; otherwise it should be connected to customers. Each switch device can have multiple ports assigned as ISP ports, and each ISP is uniquely identified using different VLAN forward maps or the port-based VLAN feature.

ISP Port

It is possible for the ISP port to receive three different types of frames: untagged, ISP-tagged, and ISP + customer-tagged frames.

When the double-tagging feature is enabled and the received frame is untagged (or the TPID does not match with ISP TPID specified in Double Tagging TPID register, the default ISP tag and customer tag are added, and VLAN ID of ISP tag receives it from the port default VID. The frames are forwarded according to the VLAN table. However, if the Port-Based VLAN Control register is enabled, the egress ports specified in the port-VLAN control register override the VLAN table settings. If the received frame is ISP-tagged (its TPID matches the ISP tag VLAN ID specified in the double-tagging TPID register), the following occurs:

1. The default customer tag (8100 + default PVID) is added.
2. The ISP VID is used to access the ARL table.
3. The ISP tag can be stripped on the way out according to the untagged bit setting in the VLAN table.

In addition, the ISP port frame can be forwarded to the destination port directly based on the forward port map of the VLAN table, by setting the FWD_MODE bit to 1 in the VLAN Table Entry register.

The VLAN ID is generated from the ISP tag, and TC is generated from the ingress frame outer tag.

Customer Port

It is also possible for the customer port to receive two different types of frames: untagged and customer-tagged frames.

When the double-tagging feature is enabled, all the ingress frames preform the normalization process to insert a ISP tag or ISP + Customer tag (depending whether the ingress frame is without tags or with one tag) to allow all ingress frames with double tags. The VLAN ID of ISP tag receives it from the port default VID.

The VLAN ID is generated from the ISP tag, and the TC is generated from the ingress frame outer tag.

Note: It is illegal to strip out the ISP tag on the ISP egress port by using the untagged bit setting in the VLAN table.

Note: Only VLAN-tagged or untagged packets are expected for the ingress of the customer ports. The customer does not add the ISP tags.

There are two possible traffic scenarios: one from a customer port to an ISP port and one from an ISP port to a customer port.

Uplink Traffic (from Customer Port to ISP)

Data traffic is traffic received from the customer port without tags or a customer tag, and the frame is destined for an ISP port. The customer ingress port performs a normalization process to allow ingress frames with double tags (ISP + Customer tag), and the ISP tag VID is based on the port default VID tag.

However, if the ingress frame is with an 802.1p tag, the VID of 802.1p tag is changed by the VID of port default VID tag after the customer port normalization process. The TC do not change.

Control traffic frames can be forwarded to the CPU first and then the CPU forwards to the ISP port if the switch management mode is enabled and if the RESV_MCAST_FLOOD bit=0 in the Global VLAN Control 4 register. In this case, an ISP tag is added to the control frame by the ingress port and the frame is forwarded to the CPU. The CPU can then forward it to the ISP port with or without the ISP tag by using the egress-direct feature.

Downlink Traffic (from ISP to Customer Port)

Data traffic frame received from ISP port may or may not have an ISP tag attached. When the received frame does not have an ISP tag and customer tag, the ISP ingress port does a normalization process to insert double tags (ISP + Customer tag), and the ISP tag VID is based on the port default VID tag. All ARL and VID table access should be based on the new tag. The traffic is then forwarded to the customer port through proper VLAN configuration. Usually, the software configures so the customer Egress port continuously removes the ISP tag. However, it is based on how the untagged map is configured.

Moreover, if the ingress frame is with an 802.1p tag, the VID of 802.1p tag is changed by the VID of port default VID tag after the ISP port normalization process. The TC will not change.

The Control traffic is forwarded to the CPU when the switch management mode is enable and if the RESV_MCAST_FLOOD bit=0 in the Global VLAN Control 4 register. The BCM53125S can also support multiple ISP port configurations by enabled the FWD_MODE bit of VLAN Table Entry register.

There are also two ways to separate traffic that belongs to two different ISP customers:

1. Each group (ISP and customer) is assigned to the same VLAN group, so that traffic does not leak to other ISPs.
2. The Port-based VLAN features is used to separate traffic that belongs to a different ISP.

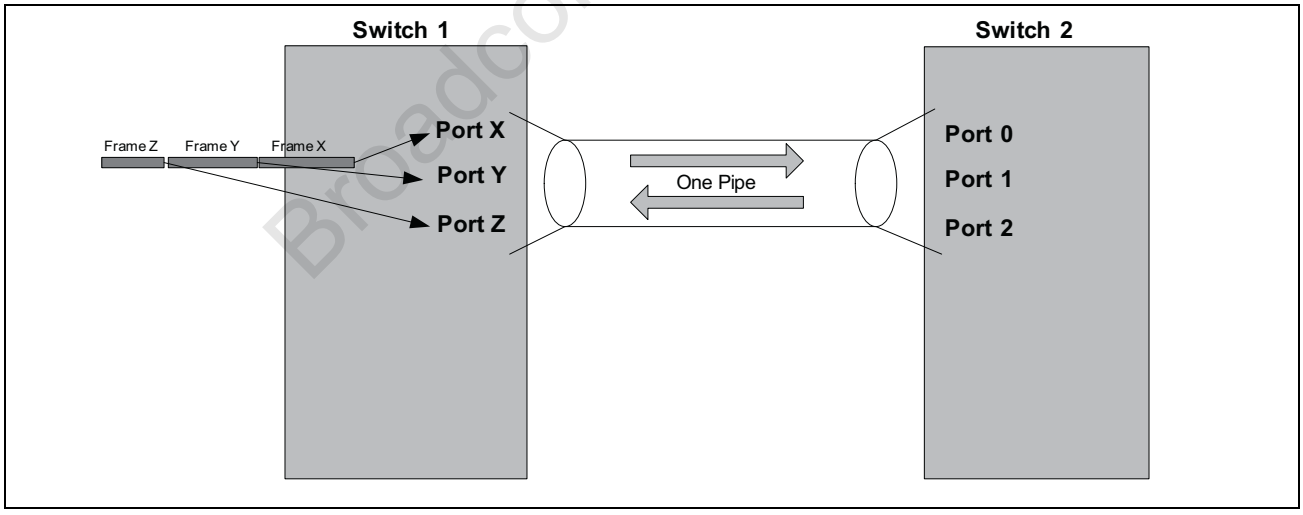
Jumbo Frame Support

The BCM53125S can receive and transmit frames of extended length on ports linked at gigabit speed. Referred to as jumbo frames, these packets are longer than the standard maximum size, but shorter than 9720 bytes. Jumbo packets can only be received or forwarded to 1000BASE-T linked ports that are jumbo-frame enabled. Up to 38 buffer memory pages are required for storing the longest allowed jumbo frame. While there is no physical limitation to the number of ports that can be jumbo-enabled, it is recommended that no more than two be enabled simultaneously to maintain acceptable system performance. There is no performance penalty for enabling additional jumbo ports beyond the potential strain on memory resources that can occur due to accumulated jumbo packets at multiple ports.

Port Trunking/Aggregation

The BCM53125S supports MAC-based trunking. The trunking feature allows up to four ports to be grouped together as a single-link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. The BCM53125S allow up to two trunk groups. Trunks are composed of predetermined ports and can be enabled using the Trunking Group 0 register. Ports within a trunk group must be of the same link speed. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the trunk is forwarded to one of the valid ports within the trunk group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within a trunk. In addition, the MAC-based algorithm provides dynamic failover. If a port within a trunking group fails, the other port within the trunk automatically assumes all traffic designated for the trunk. It allows for a seamless, automatic redundancy scheme. This hashing function can be performed using DA, SA, or DA/SA.

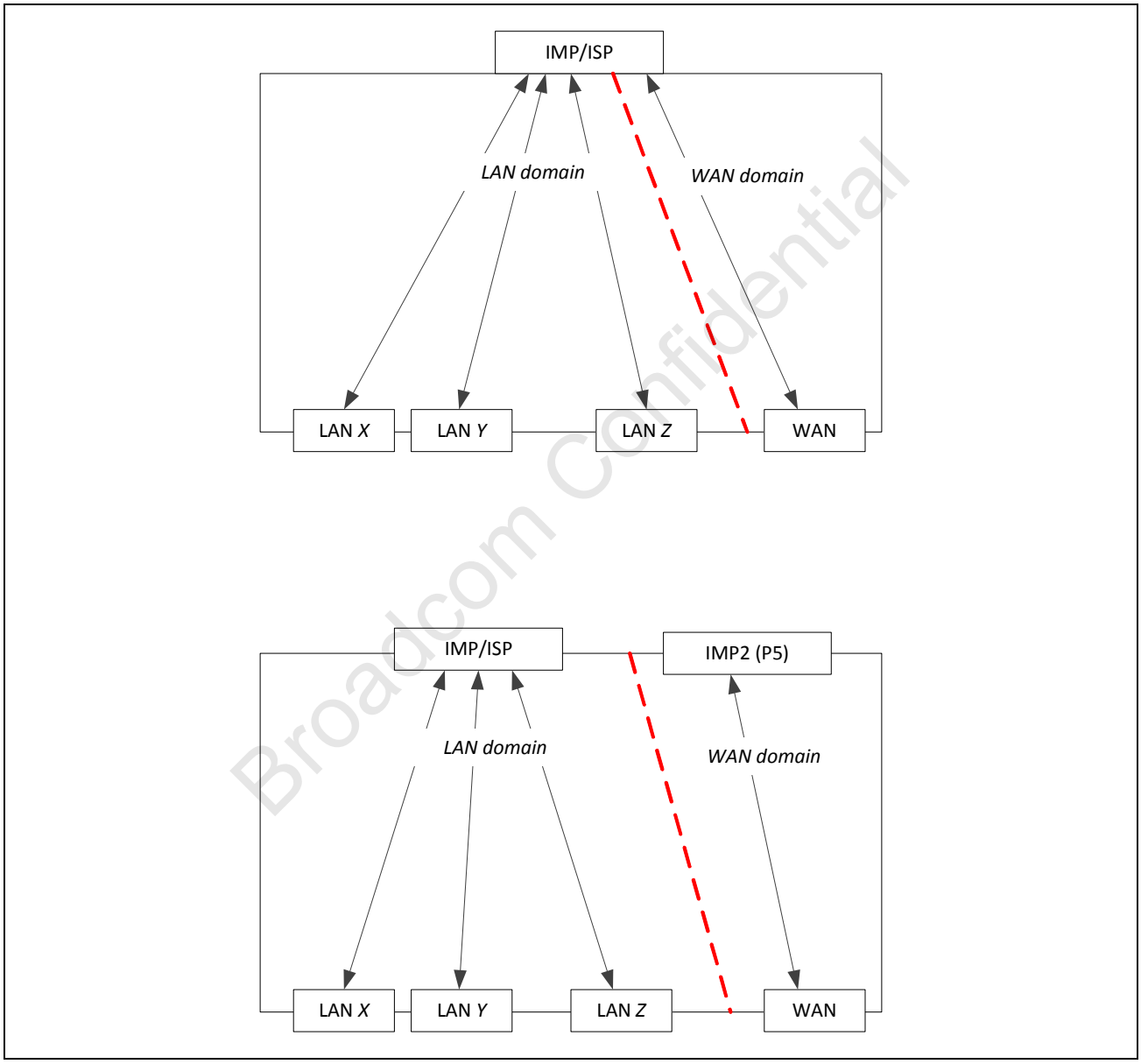
Figure 5: Trunking



WAN Port

The BCM53125S offers a programmable WAN port feature: It has a WAN Port Select register (page 00h, address 26h). Select a port as a WAN port, then all that port's traffic is forwarded to the CPU port only. The non-WAN port traffic from all other local ports does not flood to the WAN port. Figure 6 shows the WAN and LAN domain separation when WAN port is selected.

Figure 6: WAN and LAN Domain Separation When WAN Port Is Selected



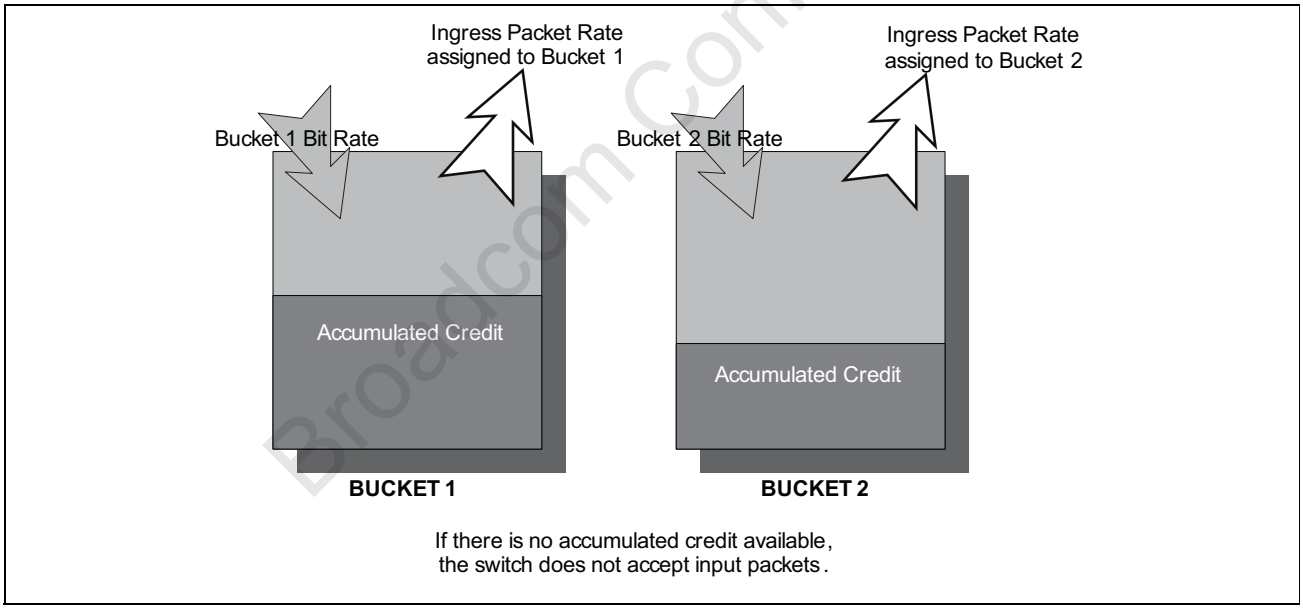
Rate Control

Ingress Rate Control

Forwarding broadcast traffic consumes switch resources, which can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an overabundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped.

The broadcast storm suppression mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see Figure 7 on page 46). Credit is continually added to the bucket at a programmable bucket bit rate. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit becomes drained. When the bucket is emptied, incoming traffic is constrained to the bucket bit rate (the rate at which credit is added to the bucket). At this point, excess packets are either dropped or deterred using flow control, depending upon the Suppression Drop mode.

Figure 7: Bucket Flow



Two-Bucket System

For added flexibility, the BCM53125S employs two buckets to track the rate of ingressed packets. Each of the two buckets (Bucket 0 and Bucket 1) can be programmed to monitor different packet types. For example, Bucket 0 could monitor broadcast packets while Bucket 1 monitors multicast packets. Multiple packet types can be monitored by each bucket, and a packet type can be monitored by both buckets.

The rates of each bucket can be individually programmed. For example, the broadcast packets of Bucket 0 could have a maximum rate of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps. The size of each bucket can be programmed. This determines the maximum credit than can accumulate in each bucket. The Rate Count and Bucket Size can be individually programmed for each port, providing another level of flexibility. Suppression control can be enabled or disabled on a per-port basis. This system allows the user to control dual packet-type rates on a per-port basis.

Egress Rate Control

The BCM53125S monitor the rate of egress traffic per port. Unlike the Ingress traffic rate control, the Egress Rate Control provides only the per-port rate control regardless of traffic types. This feature only uses one bucket to track the rate of egressed packets. The Egress Rate Control feature only support absolute bit rate mode (Bit Rate Mode = 0) and the bucket bit rate calculation is shown in Table 3.

Bucket Bit Rate

The relative ingress rates of each bucket can be programmed on a per-port basis. Each port has a programmable Rate Count value for Bucket 0 and Bucket 1. Additionally, the bit rate mode is programmed on a chip basis. If this bit is 1, the packet rate is automatically scaled according to the port link speed. Ports operating at 1000 Mbps would be allotted a 100 times higher ingress rate than ports linked at 10 Mbps. Together, the Rate Count value and the bit rate mode determine the bucket bit rate, which is a reflection of how quickly data can be ingressed (Kbps) at the given port for a given bucket. The Rate Count values are specified in Table 3. Values outside these ranges are not valid entries.

Table 3: Bucket Bit Rate

Rate Count (RC)	*Bit Rate Mode*	*Link Speed*	*Bucket Bit Rate Equation*	*Approximate Computed Bucket Bit Rate Values (as a function of RC)*
1–28	0	Any	= (RC x 8 x 1M)/125	64 KB, 128 KB, 192 KB, …1.792 MB
29–127	0	Any	= (RC – 27) x 1M	2 MB, 3 MB, 4 MB, …100 MB
128–240	0	Any	= (RC – 115) x 1M x 8	104 MB, 112 MB, 120 MB, …1000 MB
1–125	1	10 Mbps	= (RC x 8 x 1M)/100	0.08 MB, 0.16 MB, 0.24 MB, …10 MB
1–125	1	100 Mbps	= (RC x 8 x 1M)/10	0.8 MB, 1.6 MB, 2.4 MB, …100 MB
1–125	1	1000 Mbps	= RC x 8 x 1M	8 MB, 16 MB, 24 MB, …1000 MB

Note: 1M represents 1 x 10^6.

IMP Port Egress Rate Control

The IMP port egress is configurable of rate limiting at packet-per-second (PPS) granularity, in addition to bits-per-second (BPS) granularity.

Protected Ports

The Protected Ports feature allows certain ports to be designated as protected. All other ports are unprotected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. Several applications that can benefit from protected ports:

- Aggregator: For example, all the available ports are designated as protected ports except a single aggregator port. No traffic incoming to the protected ports is sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- To prevent unsecured ports from monitoring important information on a server port, the server port and unsecured ports are designated as protected. The unsecured ports will not be able to receive traffic from the server port.

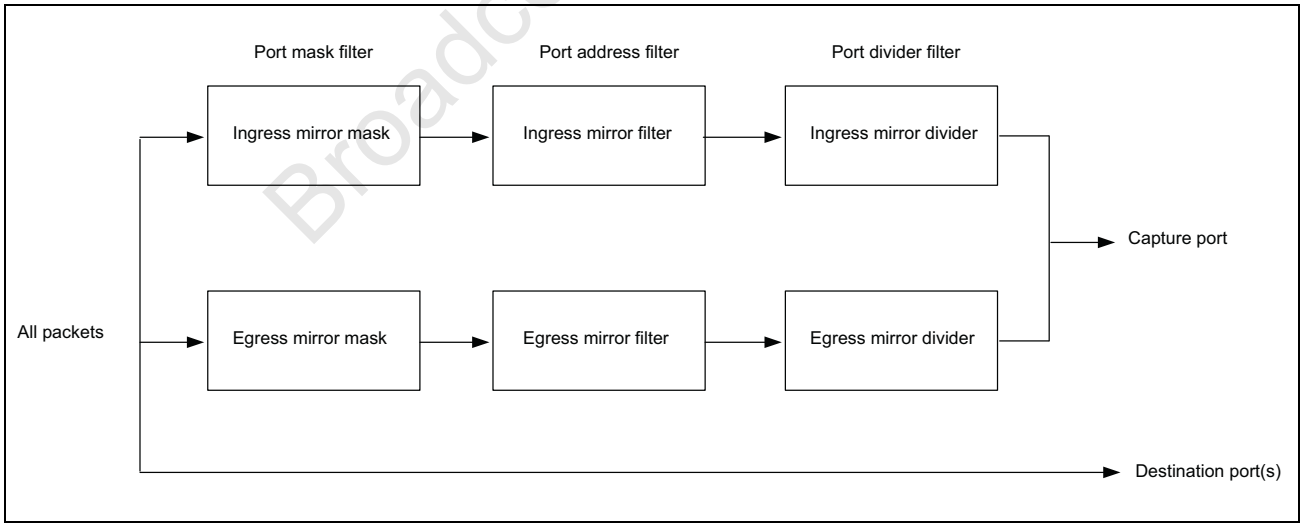
Port Mirroring

The BCM53125S support Port Mirroring, allowing ingress and/or egress traffic to be monitored by a single port designated as the mirror capture port. The BCM53125S can be configured to mirror the ingress traffic and/or egress traffic of any other port (s). Mirroring multiple ports is possible, but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

Enabling Port Mirroring

Port Mirroring is enabled by setting the Mirror Enable bit.

Figure 8: Mirror Filter Flow



Capture Port

The capture port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the Capture port according to the mirror filtering rules described in the next section.

Mirror Filtering Rules

Mirror filtering rules consist of a set of three filter operations (Port Mask, Packet Address, and Packet Divider) that are applied to traffic ingressed and/or egressed at a switch port.

Port Mask Filter

The IN_MIRROR_MASK bits define the receive ports that are monitored. The OUT_MIRROR_MASK bits define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one-mirror capture port should be taken into account to avoid congestion or packet loss.

Packet Address Filter

The type of filtering that is applied to frames received on the mirrored ports is configurable. The IN_MIRROR_FILTER bits select among the following:

- Mirror all received frames
- Mirror received frames with DA = x
- Mirror received frames with SA = x

where x is the 48-bit MAC address. Likewise, The type of filtering that is applied to frames transmitted on the egressed mirrored ports.

Packet Divider Filter

The IN_DIV_EN bit allows further statistical sampling. When IN_DIV_EN = 1, the receive frames passing the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value. Only one out of every n frames is forwarded to the mirror capture port, where n = IN_MIRROR_DIV +1. This allows the following additional capabilities:

- Mirror every n^{th} received frame.
- Mirror every n^{th} received frame with DA = x.
- Mirror every n^{th} received frame with SA = x.

Note: When multiple ingress ports have been enabled in the IN_MIRROR_MASK, the cumulative total packet count received from all ingress ports is divided by the value of IN_MIRROR_DIV to deliver the n^{th} receive frame to the mirror capture port. Egressed frames are governed by the OUT_MIRROR_MASK bit and the OUT_MIRROR_DIV bit.

IGMP Snooping

The BCM53125S supports IP-layer IGMP Snooping, which includes IGMP unknown, query, report, and leave messages.

An IGMP frame has a value of 2 in the IP header protocol field. These frames are forwarded to the CPU port. The management CPU can then determine from the IGMP control packets which port should participate in the multigroup session. The management CPU proactively programs the multicast address in the ARL table or the multiport address entries. If the IGMP_UKN_FWD_MODE, IGMP_QRY_FWD_MODE, IGMP_RPTLVE_FWD_MODE is enabled, IGMP frames are trapped to the CPU port only.

MLD Snooping

The BCM53125S supports IP layer MLD Snooping includes MLD query, report and done message. For each of the query and report/done message types, four options are available: discard, forward normally, forward to CPU, or forward normally and copy to CPU. The CPU is then expected to interpret those messages and configure the address table accordingly.

IEEE 802.1x Port-Based Security

IEEE 802.1x is a port-based authentication protocol. By receiving and extracting special frames, the CPU can control whether the ingress and egress ports should forward packets or not. If a user port wants service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process. The BCM53125S detect EAPOL frames by checking the destination address of the frame. The Destination addresses should be either a multicast address as defined in IEEE 802.1x (01-80-C2-00-00-03) or a user-predefined MAC (unicast or multicast) address. When EAPOL frames are detected, the frames are forwarded to the CPU so it can send them to the authenticator server. Eventually, the CPU determines whether the requestor is qualified based on its MAC_Source addresses, and frames are either accepted or dropped. The per-port EAP can be programmed in the register.

BCM53125S provides three modes for implementing the IEEE 802.1x feature. Each mode can be selected by setting the appropriate bits in the register.

The Basic Mode (when EAP Mode = 00'b) is the standard mode, where the EAP_BLK_MODE bit is set before authentication to block all incoming packets. Upon authentication, the EAP_BLK_MODE bit is cleared to allow all incoming packets. In this mode, the Source Address of incoming packets is not checked.

In Extended Mode (when EAP Mode = 10'b), an extra filtering mechanism is implemented after the port is authenticated. If the Source MAC address is unknown, the incoming packets are dropped and the unknown SA is not learned. However if the incoming packet is an IEEE 802.1x packet, or special frames, the incoming packets are forwarded. The definition of the Unknown SA in this case is when the switch cannot match the incoming Source MAC address to any of the addresses in ARL table, or the incoming Source MAC address matches the address in ARL table but the port number is mismatched.

The third mode is Simplified Mode (when EAP Mode = 11'b). In this mode, the unknown Source MAC address packets are forwarded to the CPU rather than dropped. Otherwise, it is same as the Extended Mode operation.

Note: The BCM53125S check only the destination addresses to qualify EAPOL frames. Ethernet type fields, packet type fields, and non-IEEE 802.1Q frames are not checked.

DoS Attack Prevention

The BCM53125S supports the detection of the following DoS (Denial of Service) attack types based on a register setting, which can be programmed to drop or not to drop each type of DoS packet.

Table 4: DoS Attacks Detected by BCM53125S

DoS Attack Type	*Description*
IP_LAND	IPDA = IPSA in an IPv4/IPv6 datagram.
TCP_BLAT	DPort = SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.
UDP_BLAT	DPort = SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.
TCP_NULLScan	Seq_Num = 0 and all TCP_FLAGs = 0 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.
TCP_XMASScan	Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.
TCP_SYNFINScan	SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.
TCP_SYNError	SYN = 1, ACK = 0, and SRC_Port<1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.
TCP_ShortHDR	The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size.
TCP_FragError	The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data.
ICMPv4_Fragment	The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram.
ICMPv6_Fragment	The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram.
ICMPv4_LongPing	The ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header.
ICMPv6_LongPing	The ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size.

- MIN_TCP_Header_Size is programmable between 0 and 255 bytes, inclusive. The default value is 20 bytes (TCP header without options).
- MAX_ICMPv4_Size is programmable between 0 and 9.6 KB, inclusive. The default value is 512 bytes.
- MIN_TCP_Header_Size is programmable between 0 and 9.6 KB, inclusive. The default value is 512 bytes.
- The default control setting for all types of DoS attacks is not to drop the DoS attack packet.

- The ping flooding or SYN/ACK flooding types of DoS attack can be detected.
- It is globally configurable whether to perform the SA learning operation with the received packets of the DoS attack type defined in the registers, regardless of the individual DoS attack types.
- When a packet is detected as a DoS attack type that must be dropped, the packet is dropped regardless of ARL forwarding decisions, but its forwarding based on the mirroring function is not affected.

MSTP Multiple Spanning Tree

The BCM53125S support up to eight multiple spanning tree instances. When the EN_RX_BPDU bit = 1, the BCM53125S forwards BPDU packets to the management port only.

Software Reset

The BCM53125S provides Software Resets. Software Resets can be triggered by register settings.

BroadSync™ HD

BroadSync HD is the enhancement to IEEE 802.3 MAC and IEEE 802.1D bridges to support the kind of low-latency, isochronous services and guaranteed quality of service (QoS) that is required for many consumer electronics applications.

BCM53125S provides the BroadSync HD feature. The BCM53125S always forwards BPDU and Multiple Registration Protocol (MRP) packets to the CPU for BroadSync HD applications, and handles the IEEE 802.1 Time Sync Protocol.

The BCM53125S can identify a packet as a BroadSync HD packet if its MAC DA value matches the programmed (registered and configured based on MRP protocols) MAC address. A MAC address can be a multicast or unicast address. The priority code point (PCP) value of the incoming BroadSync HD packet can be any value that is programmed. The default values are 4 and 5. Two queues are dedicated queues for BroadSync HD Class 5 and Class 4 traffic per egress port. The BCM53125S enhances shaping and scheduling for BroadSync HD operation.

Time Base and Slot Generation

For BroadSync HD applications, the BCM53125S maintains a time base (32-bit counter) running at a granularity of 1 ns, which can be adjusted by the CPU for synchronization with the BroadSync HD time master unit (switch or host) through the IEEE 802.1 Time Synchronized (TS) protocol (to be standardized). The TS protocol is implemented by the CPU, which requires the BCM53125S to perform the following operations:

- A received TS protocol packet is time stamped at the ingress port when the first byte (of MACDA) arrives, and is transferred along with the receiving time stamp to the CPU.

- A TS protocol packet initiated by the CPU (to be transmitted at an egress port) is time stamped at the egress port when the first byte (of MACDA) is transmitted, and the transmit time stamp recorded at the egress port is reported back to CPU.

It is required that the time synchronization point peers over an Ethernet link is chosen such that the link delay is perceived as constant, and the protocol exchange occurs at least every 10 ms over every link.

The CPU may be required to speed up or slow down the timebase maintained in BCM53125S based on the TS protocol execution. The BCM53125S provides the time base adjustment mechanism for graceful time changes based on CPU instructions.

In addition, the BCM53125S maintains counter mechanism to generate the time slot for BroadSync HD traffic scheduling.

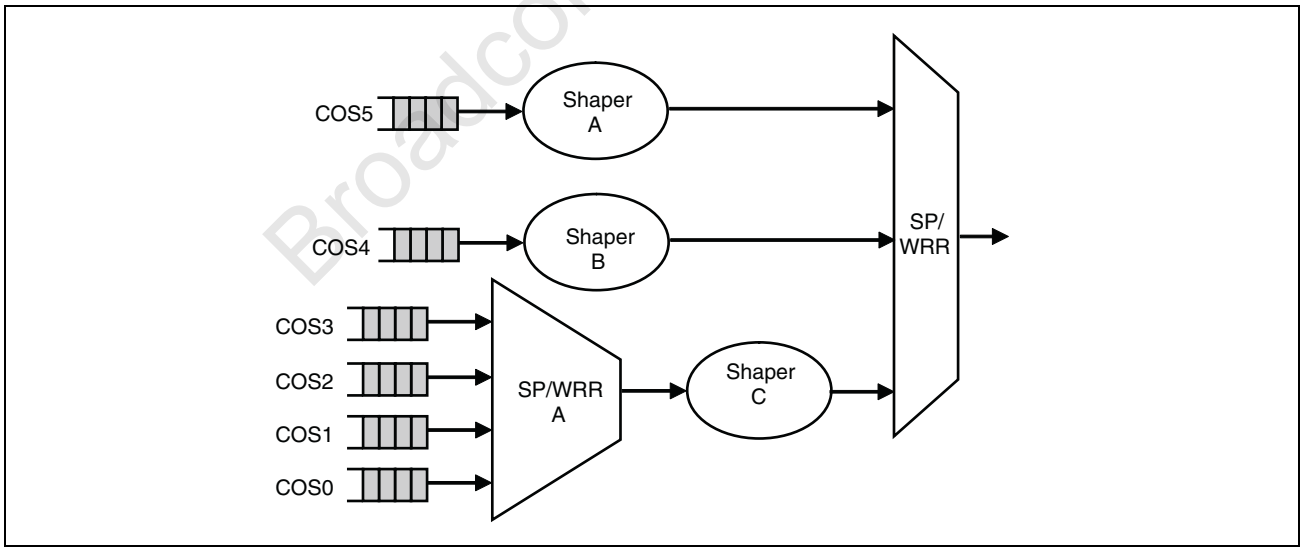
- A Slot is defined as 125 µs. It is used to pace the BroadSync HD Class5 traffic, which has tight jitter requirements.
- A MacroSlot is configurable as 1 ms, 2 ms, or 4 ms (binary number of Slots). It is used to pace the BroadSync HD Class4 traffic, which has relaxed jitter requirements.

The CPU may be required to make the Slot wider or narrower based on the TS protocol execution. The BCM53125S provides the Slot adjustment mechanism for graceful Slot width changes based on CPU instructions.

Transmission Shaping and Scheduling

Packets queued at each Ethernet (egress) port is subject to the scheduling behavior as shown in Figure 9 on page 53.

Figure 9: BroadSync HD Shaping and Scheduling



BroadSync HD Class5 Media Traffic

The COS5 queue is dedicated for BroadSync HD Class 5 traffic only, and a COS5 packet is always the highest priority to be scheduled for transmission if it is allowed by the Shaper A. The Shaper A is an emulation of fixed bandwidth pipe for Class5 BroadSync HD traffic, with tight jitter to adaptively handle interference from non-BroadSync HD or Class4 BroadSync HD traffic. Note that the preamble and IPG transmission are not taken into account for the pipe operation.

Tunable parameters for the Shaper A are listed as follows.

- MaxAVPacketSize indicates the maximum packet size allowed on an AV-Enabled port. It is a global setting using BroadSync HD Max Packet Size register.
- Class5_BW indicates the reserved bandwidth for Class 5 BroadSync HD traffic at granularity of Byte (per Slot, 125 µs). It is a per-port setting.
- Class5_Window indicates the jitter control for Class5 BroadSync HD transmission. It is a per-port setting.

At the start of each Slot:

- Reset the credit in the shaping bucket to Class5_BW if the queue is empty.
- Reset the credit in the shaping bucket to Class5_BW if the queue is not empty and Class5_Window is set to 0.
- Reset the credit in the shaping bucket to Class5_BW if the queue is not empty, Class5_Window is set to 1, and the credit remained in the shaping bucket is greater than MaxAVPacketSize.
- Add Class5_BW to the credit in the shaping bucket if the queue is not empty, Class5_Window is set to 1, and the credit remained in the shaping bucket is less than or equal to MaxAVPacketSize.

The credit in the shaping bucket decrements for every byte transmitted for the Class 5 BroadSync HD traffic through the port. If the credit reaches 0 before the end of the current Slot while transmitting a Class 5 BroadSync HD packet, the ongoing packet transmission is not interrupted, and the credit stays at 0 until being reset at the start of next Slot. The credit decrements resumes at the next Slot if the ongoing transmission continues. As long as the credits in the shaping bucket is greater than 0, a Class 5 BroadSync HD packet is allowed to be scheduled for transmission.

BroadSync HD Class4 Media Traffic

The COS4 queue is dedicated for BroadSync HD Class 4 traffic only, and a COS4 packet always yield to COS5 traffic (if allowed to be scheduled), but takes precedence over the traffic from COS0–COS3 queues or follow the weight ratio between COS4 and COS0–COS3 for transmission scheduling, if it is allowed by the Shaper B. The Shaper B is an emulation of fixed bandwidth pipe for Class 4 BroadSync HD traffic with relaxed jitter to adaptively handle interference from non-BroadSync HD or Class 5 BroadSync HD traffic. It also statistically levels the Class 4 BroadSync HD transmission bursts towards the next hop switch to reduce the buffering requirements, by using Slot (instead of MacroSlot) as the pacing mechanism. The preamble and IPG transmission are not accounted for in the pipe operation.

Tunable parameters for the Shaper B are listed as follows:

- MacroSlot_Period indicates the periodic cycle time to shape the Class4 traffic. It is a global setting to indicate 1 ms, 2 ms, or 4 ms.
- MaxAVPacketSize indicates the maximum packet size allowed on an AV-Enabled port. It is a global setting. (same as for BroadSync HD Class 5 setting).

- Class4_BW indicates the evenly divided bandwidth share per Slot, which is derived from dividing the reserved bandwidth for Class 4 BroadSync HD traffic at granularity of Byte (per MacroSlot) by the number of Slots within a MacroSlot. It is a per-port setting.

At the start of each Slot:

- If the Slot is the first one for the current MacroSlot, reset the credit bucket to Class4_BW+MaxAVPacketSize; (MaxAVPacketSize is used as the deficit base).
- Otherwise, add Class4_BW to the credit in the shaping bucket.

The shaping credit bucket decrements for every byte transmitted for the Class 4 BroadSync HD traffic. As long as the credits in the shaping bucket is greater than or equal to MaxAVPacketSize, a Class 4 BroadSync HD packet is allowed to be scheduled for transmission

CableChecker™

The BCM53125S provides the cable diagnostic capabilities for unmanaged environments. The actual cable diagnostic feature lies in the PHY functional block. The BCM53125S devices let the user monitor the cable diagnostic results through the LED display by setting the appropriate bits in the LED refresh registers.

The BCM53125S uses the existing LED display (which is already assigned to various functions) to indicate the cable diagnostic results. Table 5 shows the cable diagnostic result output for each LED function where 1 and 0 represent the LED indication pin status: 1 indicates active and 0 indicates inactive.

Notes:

- The best way for a user to visualize the cable diagnostic test result through LEDs is to bring out the LINK status bit to the LED display along with other functions to be displayed per port. In this way, the user can observe the cable diagnostic result from the flashing (or lit) LED of other functions while LINK LED is off. The switch turns off the LINK status LED during the cable diagnostic mode.
- The cable diagnostic is expected to be most effective when the user cannot establish the link with the partner.

Table 5: Cable Diagnostic Output

LED Function in LED Function Register	*Cable Diagnostic Output*
PHYLED4	1 = Cable diagnostic failed. 0 = Cable diagnostic passed.
LNK	No output during the cable diagnostic mode.
DPX	1 = Passed. 0 = Failed.
ACT	1 = Passed. 0 = Failed.

Table 5: Cable Diagnostic Output (Cont.)

LED Function in LED Function Register	*Cable Diagnostic Output*
COL	1 = Passed. 0 = Failed.
LNK/ACT	No output during the cable diagnostic mode.
DPX/COL	1 = Passed. 0 = Failed.
SPD10M	1 = Failed. 0 = Passed.
SPD100M	In LED function0 map: 1 = Cable diagnostic passed. 0 = Failed. In LED function1 map: 1 = Cable diagnostic failed. 0 = Passed.
SPD1G	1 = Passed. 0 = Failed.
10M/ACT	1 = Failed. 0 = Passed.
100M/ACT	In LED function0 map: 1 = Cable diagnostic passed. 0 = Failed. In LED function1 map: 1 = Cable diagnostic failed. 0 = Passed.
10–100M/ACT	1 = Failed. 0 = Passed.
1G/ACT	1 = Passed. 0 = Failed.
PHYLED3	1 = Failed. 0 = Passed.

Egress PCP Remarking

The BCM53125S provides an egress PCP remarking feature of the outer tag at each egress port, which includes the CFI and PCP field modification based on either the internal ARL-generated or the TC-generated Rate Violation (RV) status. The Egress PCP remarking process applies to Ethernet ports only. Each Ethernet port can provide a 16-entry mapping table indexed by {RV, TC} to map to the {New CFI, New PCP} field for the outgoing packet.

Note: For the AV-enabled egress port, the egress PCP for the non-BroadSync HD class of traffic must never be programmed with values of 100 and 101.

Address Management

The BCM53125S Address Resolution Logic contains the following features:

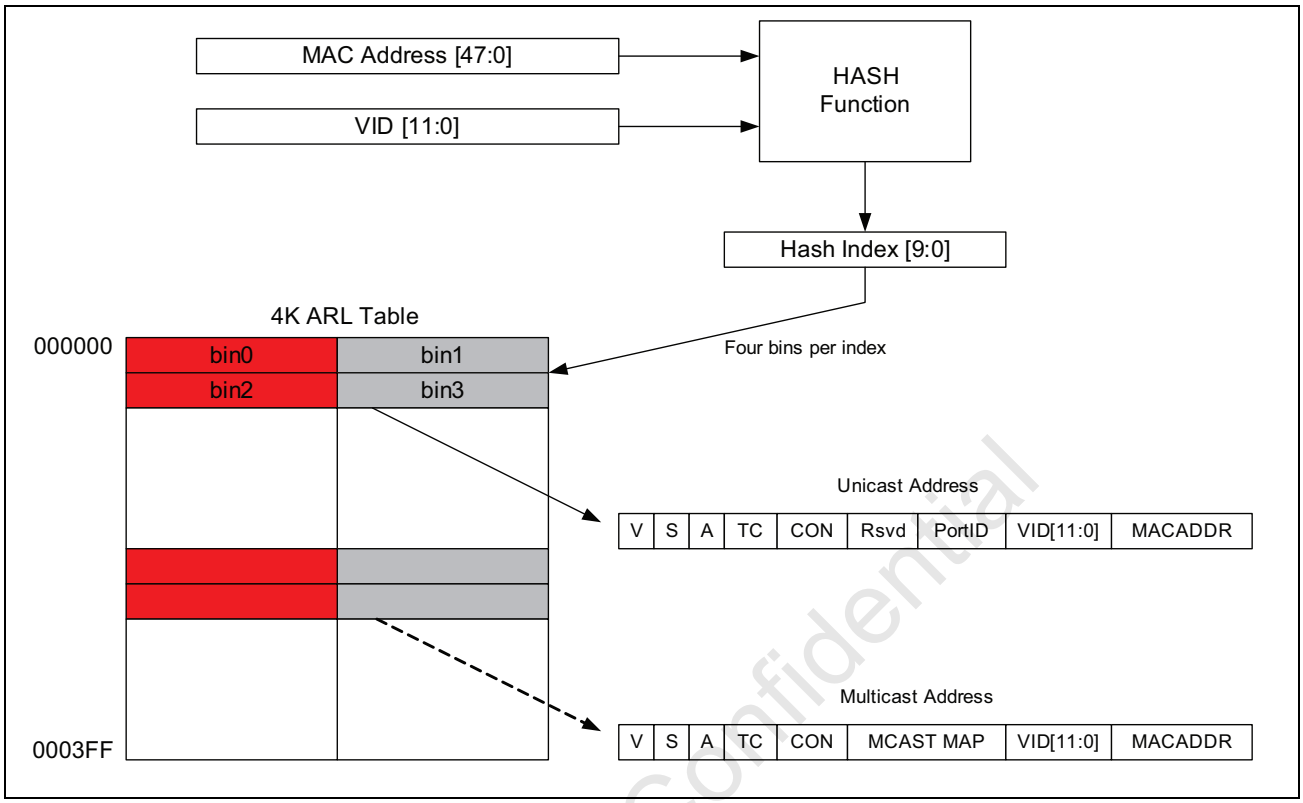
- Four-bins-per-bucket address table configuration.
- Hashing of the MAC/VID address to generate the address table point.

The address management unit of the BCM53125S provides wire speed learning and recognition functions. The address table supports 4K unicast/multicast addresses using on-chip memory.

Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains four entries or bins. The address table has 1K buckets with four entries in each bucket. This allows up to four different MAC addresses with the same hashed index bits to be simultaneously mapped into the address table. In the ARL DA/SA lookup process, it hashes a 10-bit search index and reads out bin0 and bin1 in the first cycle, and reads out bin2 and bin3 in the second cycle. These four entries are used for ARL routing and learning.

Figure 10: Address Table Organization



The index to the address table is computed using a hash algorithm based on the MAC address and the VLAN ID (VID) if enabled.

Note: In the Enable IEEE 802.1Q and VLAN Learning Mode, both the MAC address and the VLAN ID (VID) are used to compute the hashed index. See "IEEE 802.1Q VLAN" on page 40 for more information.

The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits [9:0] of the hash are used as an index to the approximately 4K locations of the address table.

The CRC-CCITT polynomial is $x^{16} + x^{12} + x^5 + 1$.

Address Learning

Information is gathered from received unicast packets and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process, the frame information (such as the Source Address [SA] and VID) is saved until completion of the packet. An entry is created in the ARL table memory when the following conditions are met:

- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE 802.1Q VLAN, the packet is from an SA that belongs to the indicated VLAN domain.

- The packet does not have a reserved multicast destination address. This condition can be disabled using register settings.
- Free space is available in the memory pointed to by the hashed index.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See Table 7 on page 60 for a description of a unicast ARL entry.

Multicast addresses are not learned by the ARL table, but must be written using one of the "Programming Interfaces" on page 94.

Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written to the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The destination address (DA) and VID of the received packet are used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The specifics of address resolution and frame forwarding are described in "Unicast Addresses" on page 59 and "Multicast Addresses" on page 60.

Unicast Addresses

Frames containing a unicast destination address are assigned a forwarding field corresponding to a single port. Listed below is the unicast address-resolution algorithm:

- If the multiport addressing feature is enabled and the DA matches one of the programmed multiport addresses, then it is forwarded accordingly. See "Power Savings Modes" on page 64.
- The lower 10 bits of the hashed index key are used as a pointer into the address table memory, and the entry is retrieved.
- If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet.
- If the destination port matches the source port, the packet is not forwarded.
- If the address resolution function fails to return a matching valid ARL entry and the unicast DLF forward bit is set, the frame is forwarded according to the port map.
- Otherwise, the packet is flooded to all appropriate ports.

See Table 6 for definitions of the unicast index key and the assigned forwarding field. The forwarding field for a unicast packet is the port ID contained in the matching ARL entry. See Table 7 for a description of a unicast ARL entry.

Table 6: Unicast Forward Field Definitions

EN_1QVLAN	*Index Key*	*Forwarding Field*
1	DA and VID	Port ID
0	DA	Port ID

Table 7: Address Table Entry for Unicast Address

Field	Description
VID	VLAN ID associated with the MAC address.
Valid	1 = Entry is valid. 0 = Entry is empty.
Static	1 = Entry is static—Should not be aged out and is written and updated by software. 0 = Entry is dynamically learned and aged.
Age	1 = Entry has been accessed or learned since last aging process. 0 = Entry has not been accessed since last aging process.
TC	MACDA-based TC (only valid for static entries). See “Quality of Service” on page 35 for more information.
Reserved	–
Reserved	Only 00 is valid.
PortiD	Port identifier. The port associated with the MAC address.
MAC Address	48-bit MAC address.

Multicast ARL table entries are described in Table 8 on page 61.

Multicast Addresses

Frames containing a multicast destination address are assigned a forwarding field that corresponds to multiple ports specified in a port map. If no matching ARL entry is found, the packet is flooded to all appropriate ports.

The multicast address resolution algorithm is listed below:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in Table 9 on page 61.
- If the multiport addressing feature is enabled and the DA matches one of the programmed Multiport Addresses, it is forwarded accordingly. See “Multiport Control Register (Page 04h: Address 0Eh–0Fh)” on page 179.
- Otherwise, the lower 10 bits of the hashed index key are used as a pointer into the ARL table memory, and the entry is retrieved.
- If the Valid indicator is set, and the address stored at the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- If the address resolution function fails to return a matching valid ARL entry and the multicast DLF forward bit is set (see “Port Forward Control Register (Page 00h: Address 21h)” on page 152), the frame is forwarded according to the port map. Two types of multicast address groups are handled by two separate Lookup Fail Forward registers:
  - When the ARL table lookup fails for an address in the multicast address range = 01-00-5e-xx-xx-xx, called IP Multicast (IPMC), the frames are forwarded to the ports according to the “MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)” on page 156.
  - When ARL table lookup fails for all other multicast addresses, the frames are forwarded to the ports according to the “Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)” on page 156.

- Otherwise, all other multicast and broadcast packets are flooded to all appropriate ports.

The forwarding field for a multicast packet is the port map contained in the matching ARL entry. See Table 8 for a description of a multicast ARL entry. See "Accessing the ARL Table Entries" on page 62 for more information.

Table 8: Address Table Entry for Multicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address.
Valid	1 = Entry is valid. 0 = Entry is empty.
Static	1 = Entry is static—This entry is not aged out and is written and updated by software. 0 = Not defined.
Age	The AGE bit is ignored for static ARL table entries.
TC	MACDA-based TC (only valid for static entries). See "Quality of Service" on page 35 for more information.
Reserved	–
IPMC0 [8:0]	Multicast forwarding mask. 1 = Forwarding enable. 0 = Forwarding disable.
MAC Address	48-bit MAC address.

Unicast ARL table entries are described in Table 7 on page 60.

Reserved Multicast Addresses

Table 9 summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions.

Table 9: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*IEEE 802.1 Specified Action*	*Unmanaged Mode Action*	*Managed Mode Action*
01-80-C2-00-00-00	Bridge group address	Drop frame.	Flood frame.	Forward frame to IMP only.
01-80-C2-00-00-01	IEEE 802.3x MAC control frame	Drop frame.	Receive MAC determines if it is a valid pause frame and then acts accordingly.	Receive MAC determines if valid pause frame and acts accordingly.
01-80-C2-00-00-02	Reserved	Drop frame.	Drop frame.	Forward to frame management port only.
01-80-C2-00-00-03	IEEE 802.1x port-based network access control	Drop frame.	Drop frame.	Forward frame to management port only.
01-80-C2-00-00-04– 01-80-C2-00-00-0F	Reserved	Drop frame.	Drop frame.	Forward frame to management port only.

Table 9: Behavior for Reserved Multicast Addresses (Cont.)

MAC Address	Function	IEEE 802.1 Specified Action	Unmanaged Mode Action	Managed Mode Action
01-80-C2-00-00-10	All LANs bridge management group address	Forward frame.	Flood frame.	Forward frame to all ports including management port.
01-80-C2-00-00-11–01-80-C2-00-00-1F	Reserved	Forward frame.	Flood frame.	Forward frame to all ports excluding management port.
01-80-C2-00-00-20	GMRP address	Forward frame.	Flood frame.	Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 4 of page 34, offset 04h register).
01-80-C2-00-00-21	GVRP address	Forward frame.	Flood frame.	Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 5 of page 34, offset 04h register).
01-80-C2-00-00-22–01-80-C2-00-00-2F	Reserved	Forward frame.	Flood frame[a].	Forward frame to all ports excluding management port.

a. Frames flood to all ports. Certain exclusions apply, such as VLAN restrictions.

Note: Managed mode is set using register page 00h, address 0Bh, bit 0. A management port can be selected using register page 02h, address 00h. The management (IMP) port often has to be forced to link using the IMP Port State Override register page 00h, address 0Eh.

Static Address Entries

The BCM53125S supports static ARL table entries that are created and updated using one of the “Programming Interfaces” on page 94. These entries can contain either unicast or multicast destinations. Static entries do not automatically learn MAC addresses or port associations and are not aged out by the automatic internal aging process.

Accessing the ARL Table Entries

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL read/write control, which allows an address-entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

Searching the ARL Table

The second method to access the ARL table is through the ARL search control. The entire ARL table is searched sequentially, revealing each valid ARL entry.

The ARL search and ARL read/write operations execute in parallel with other register accesses. This allows the host processor to start a read, write, or search process and then read/write other registers, returning periodically to see if the operation has completed.

Address Aging

The BCM53125S offers two types of address aging processes: normal aging and fast aging. When address entries are marked as “static” in the ARL table, the normal aging process does not apply (i.e., the address entries can removed only by the user, the fast-aging process, or a reset).

Normal Aging

The normal aging process removes a dynamically learned address entry in the ARL table if the entry is not accessed (i.e., no packets are destined to its MAC address) for the user-configurable time period specified in the “Aging Time Control Register (Page 02h: Address 06h)” on page 169. The default aging time is 300 seconds.

The user also can accelerate the aging time by enabling the AGE_Accelerate bit (bit 2) of the “Global ARL Configuration Register (Page 04h: Address 00h)” on page 179. When this bit is set, the aging time is reduced to 1/128 of the current aging time.

Fast Aging

The fast aging process removes the address entries in the ARL table selectively, as specified by the “Fast-Aging Control Register (Page 00h: Address 88h)” on page 161. The fast aging function can be enabled per port or per VLAN ID.

The user can select the type of entries to be removed in the Fast-Aging Control Register:

- Multicast entries—Multicast cannot be selected while Port ID is selected.
- Spanning tree ID
- VLAN ID—Specified in the “Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)” on page 161
- Port ID—Specified in the “Fast-Aging Port Control Register (Page 00h: Address 89h)” on page 161
- Dynamic entries
- Static entries

The user can trigger the fast aging process by setting the Fast-Age-Start bit in the “Fast-Aging Control Register (Page 00h: Address 88h)” on page 161. When the Fast-Aging process is triggered, the process goes through each entry in the ARL table and removes the selected type of entry (i.e., entries stored in the lower address are removed first, as the process sequences through the entire ARL table).

Power Savings Modes

The BCM53125S offers different power savings modes for different operating states. All the power saving schemes are implemented without requiring an external CPU.

The various power savings modes are:

- Auto power-down mode: This is a stand-alone PHY feature which is enabled by a register bit setting. The PHY shuts off the analog portion of the circuitry when cable is not connected or the link partner power is down.
- Energy Efficient Ethernet (EEE) mode: Energy Efficient Ethernet is IEEE 802.1az, an extension of the IEEE 802.3 standard. IEEE defines support for the PHY to operate in Low Power Idle (LPI) mode. When enabled, this mode supports QUIET times during low link utilization, allowing the both sides of link to disable portions of each PHY's operating circuitry and save power.
- Short-cable mode (Green mode): This mode requires the CPU to run the cable diagnostics, and the CPU enables power savings mode based on the cable length measurement result.
- Deep green mode: This mode also requires the CPU to recognize the long period power-down time and shut off the PHY power and the PLL to the PHY core. The CPU wakes up the PHY when a signal is detected at the PHY input.

Auto Power-Down Mode

Auto power-down mode saves PHY power consumption while the link is down. When the user enables the auto power-down mode through a PHY register bit setting, the PHY goes into the power savings mode automatically whenever it is in link-down state. During the Power Down state, the PHY wakes up every 2.7 or 5.4 seconds, depending on the register settings, and checks for a link signal. If no link signal is detected, then the PHY goes back to Power Down state, or the PHY wakes up and resumes the link process.

Automatic Power Down mode applies to the following conditions:

1. The cable is plugged in, but the link partner is shut down (for example, when a PC is off), so the port is in link down state.
2. The cable is unplugged, so the port is in link down state.

Energy Efficient Ethernet Mode

Energy Efficient Ethernet (EEE) power savings mode saves PHY consumption while the link is up but when extended idle periods may exist between packet traffic. In EEE power savings mode PHY power consumption is scalable to the actual bandwidth utilization. The PHY can go in to “Quiet” mode (low-power idle mode) when there is no data to be transmitted. This feature is based on the latest IEEE 802.3az standard. The link partner must support EEE capability for this feature to work. The discovery of this capability is during auto-negotiation through the Link Layer Discovery Protocol (LLDP). This EEE feature is an embedded PHY feature and no external CPU is required.

In this mode, the MAC determines when to enter low-power mode by examining the state of the transmit queues associated with each MAC. Four simple adjustments (settings) are used to trigger (optimize) the behavior of EEE control policy. These adjustments are as follows:

- Global Buffer occupancy threshold
- Two-part sleep delay timer
- Minimum low-power idle duration timer
- Wake transition timer

The two-way communication between the PHY and its link partner is required for the PHY to achieve the power savings on both sides. The transmit PHY sends a sleep symbol to the link partner, and the link partner enters low-power state. When the transmit PHY sends a wake symbol, the regular packet transfer mode resumes.

For details on how the mode works and how to set up the conditions, refer to the 53125-AN2*xx*-R Application Note, Energy Efficient Ethernet™ in the BCM53125 product area.

Note: The BCM53125S supports the EEE feature for external PHYs connected on the IMP port and GMII (port 5) port only through the GMII interface.

Short Cable Mode (Green Mode)

The Short Cable Power Saving mode (called Green mode) requires a CPU. In the BCM53125S, a dedicated embedded 8051 processor is used to implement this feature. Software running in the 8051 triggers the cable diagnostic routine on a schedule programmed by the user (for example, upon every power up or every new link-up). The diagnostic routine obtains the length of the cable connected to the port. Then, the CPU reduces the PHY Receiver power based on the measured cable length.

Deep Green Mode

The Deep Green Power Saving mode is a step deeper than the Auto Power Down Power Saving mode. The Deep Green Power Saving mode can be enabled through the internal 8051 microcontroller by setting the EN_8051 strap pin high (default state). The Auto Power Down Power Saving mode is per port, but the Deep Green Power Saving mode is for all ports with a common PLL. When all ports that are sharing a PLL are linked down, the Auto Power Down mode is enabled (Register Page 10h – 14h, Address 38h, Shadow 01010b [this is required]), and the DLL Auto Power-Down mode is enabled (Register Page 10h – 14h, Address 38h, Shadow 00101b), then the PHYs enter the Deep Green Power Saving mode. In this mode, all the PHY circuits are powered down except the energy detection circuit, and the energy detection circuit constantly monitors the energy on the line. Upon signal energy detection, the microcontroller turns on the PLL along with PHY power to start the auto negotiation process. The Deep Green Power Saving mode is most effective when the user expects no activities on the line for a long period of time.

Interrupt

The BCM53125S has an interrupt feature that can be programmed to generate two types of interrupts. One type of interrupt is a same type of interrupt that the BCM53115 offers. This type of interrupt is generated whenever link status change occurs in any of the ports. The second type of interrupt is generated when there is a packet(s) in IMP transmit queue to the CPU using the IMP port. The new type of interrupt is called IMP Sleep interrupt. The two types of interrupts can be enabled through Interrupt_Enable_Register (page 03h, address 08h), and both types of interrupts can be enabled together per port. However, the Link Status Change interrupts are normally used on Port[4:0], and IMP Sleep interrupts are only available on Port 5 and the IMP port.

The purpose of the second type of interrupt is to wake up the external CPU connected to the IMP port before the switch to transmit the queued-up packet to the CPU. This interrupt can be used in any system with the CPU/switch combination. When there is no traffic to be sent to CPU, the CPU can go into sleep mode to conserve power. However, the CPU must be able to wake up when there is a packet(s) to be received, without losing any packets. For this situation, the BCM53125S can send out an interrupt to wake up the CPU and hold the packet(s) until the CPU is ready to accept the packets and process. The time to hold the packets to the CPU is programmable by the specific CPU based on its wakeup time requirement. The packet hold time (IMP sleep time) can be programmed through the register (page 03h, address 10h (for IMP port), address 14h (for Port 5).

Once the interrupt is generated to wake up the CPU, the switch holds the packet(s) in the transmit queue till the IMP-sleep timer expires. The IMP-sleep timer is also programmable depending on the wakeup time required by the CPU.

The CPU has an option to enable each different type of interrupt through the Interrupt-Enable register. Once an interrupt is generated, the CPU can find out the source of the interrupt by reading the Interrupt Status register.

Section 3: System Functional Blocks

Overview

The BCM53125S include the following blocks:

Each of these is discussed in more detail in the following sections.

Media Access Controller

The BCM53125S contains six 10/100/1000 GMACs, and one MAC.

The MAC automatically selects the appropriate speed (CSMA/CD or full-duplex) based on the PHY auto-negotiation result. In full-duplex mode, IEEE 802.3x PAUSE frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3-, IEEE 802.3u-, and IEEE 802.3x-compliant.

Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than standard max frame size or 9,720 bytes for jumbo-enabled ports

Note: Frames longer than standard max frame size are considered oversized frames. When jumbo-frame mode is enabled, only the frames longer than 9,720 bytes are bad frames and dropped.

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled using register settings.

Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and interpacket gap enforcement.

In 10/100 Mbps half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted, and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame, and the 96-bit times of IPG have been observed. Transmit functions can be disabled using register settings.

Flow Control

The BCM53125S implement an intelligent flow-control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM53125S initiate flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes.

10/100 Mbps Half-Duplex

In 10/100 half-duplex mode, the MAC back-pressures a receiving port by transmitting a 96-bit time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow-control state.

10/100/1000 Mbps Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow-control frames are recognized and, when properly received, set the flow-control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the BCM53125S are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner flow control (IEEE 802.3x) capability. See Table 10 on page 69 for detailed information.

Table 10: Flow Control Modes

Link Partner Flow Control (IEEE 802.3x)	*Control Input ENFDXFLOW*	*Control Input ENHDXFLOW*	*Auto-negotiated Link Speed*	*Flow Control Mode*
X	X	0	Half-duplex	Disabled
X	X	1	Half-duplex	Jam pattern
0	0	X	Full-duplex	Disabled
0	1	X	Full-duplex	Disabled
1	0	X	Full-duplex	Disabled
1	1	X	Full-duplex	IEEE 802.3x flow control

Integrated 10/100/1000 PHY

There are five integrated PHY blocks in the BCM53125S. For more information see “Copper Interface” on page 91. The following sections describe the operations of the internal PHY block.

Encoder

There are five integrated PHY blocks in the BCM53125S. The PHY is the Ethernet transceiver that appropriately processes data presented by the MAC into an analog data stream to be transmitted at the MDI interface, which performs the reverse process on data received at the MDI interface. The registers of the PHY are read using the “Programming Interfaces” on page 94. The following sections describe the operations of the internal PHY block. For more information, see “Copper Interface” on page 91.

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs preequalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM53125S transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in “Stream Cipher” on page 72. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the BCM53125S simultaneously transmits and receives a continuous data stream on all 4 pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2 bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn-to-zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM53125S asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails, or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. Decoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets is disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state, and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state and the transmission and reception of data packets are disabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM53125S achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1 x 10–12 for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

Cross Talk Canceler

The BCM53125S transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

Analog-to-Digital Converter

Each receive channel has its own 125 MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High power-supply noise rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM53125S automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and therefore, produces very low noise transmit signals.

Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit-wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit-wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit-wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53125S enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that interpacket gaps containing idles or frame extensions are received at expected intervals. When the BCM53125S detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM53125S is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM53125S has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM53125S) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable.
- Polarity errors caused by the swapping of wires within a pair.

The BCM53125S also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM53125S can tolerate delay skews of up to 64 ns long. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100 Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

Automatic MDI Crossover

During copper auto-negotiation, one end of the link must perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53125S can perform an automatic media-dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM53125S normally transmits and receives on the TRD pins.

When connecting to another device that does not perform MDI crossover, the BCM53125S automatically switches its TRD in pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the BCM53125S swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function cannot be disabled when in 1000BASE-T mode. During 10BASE-T and 100BASE-TX operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default only works when auto-negotiation is enabled. This function can be disabled during auto-negotiation using a register write.

Note: This function only operates when the copper auto-negotiation is enabled.

10BASE-T/100BASE-TX Forced Mode Auto-MDIX

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for at least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100Tx idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4.

Note: This function only operates when the copper auto-negotiation is disabled.

Resetting the PHY

The BCM53125S provides a hardware reset pin, RESET, which resets all internal nodes to a known state. Hardware reset is accomplished by holding the RESET pin low for at least 1 ms. Once RESET is brought high, the PHY will complete its reset sequence within 5 ms. All outputs will be inactive until the PHY has completed its reset sequence. The PHY will keep the inputs inactive for 5 ms after the deassertion of hardware reset. The hardware configuration pins and the PHY address pins will be read on the deassertion of hardware reset.

The BCM53125S also has a software reset capability. To enable the software reset, a 1 must be written to the bit. This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit. Mode pins that are labeled sample on reset (SOR) are latched during hardware reset. Similarly, software resets also latch new values for the SOR mode pins.

PHY Address

The BCM53125S has five unique PHY addresses for MII management of the internal PHYs. The PHY addresses for each port are as follows:

- PHY address for Port 0 is 0
- PHY address for Port 1 is 1
- PHY address for Port 2 is 2
- PHY address for Port 3 is 3
- PHY address for Port 4 is 4

Super Isolate Mode

When in Super Isolate mode, the transmit and receive functions on the Copper Media Dependent Interface are disabled (No link will be established with the PHY's copper link partner). Any data received from the switch will be ignored by the BCM53125S and no data will be sent from the BCM53125S.

Standby Power-Down Mode

The BCM53125S can be placed into standby power-down mode using software commands. In this mode, all PHY functions except for the serial management interface are disabled. To enter standby power-down mode, set MII Control register (page 10h–14h: address 00h), bit 11 = 1. There are three ways to exit standby power-down mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software RESET bit 15, MII Control register (page 10h–14h: address 00h).
- Assert the hardware RESET pin.

Read or write operations to any MII register, other than MII Control register, while the device is in the standby power-down mode returns unpredictable results. Upon exiting standby power-down mode, the BCM53125S remains in an internal reset state for 40 µs and then resumes normal operation.

Auto Power-Down Mode

The BCM53125S can be placed into auto power-down mode. Auto power-down mode reduces device power when the signal from the copper link partner is not present. The auto power-down mode works whether the device is in Auto-negotiation Enabled or Forced mode. This mode is enabled by setting bit 5 =1 of Auto Power-Down register. When auto power-down mode is enabled, the BCM53125S automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. The energy-detect circuit is always enabled even when a port is in low-power mode. When the BCM53125S is in auto power-down mode, it wakes up after 2.7s or 5.4s, which determined by bit 4 of Auto Power-Down register, and sends link pulses to the link partner. The BCM53125S enters normal operation and establishes a link if energy is detected.

Note: Auto power-down mode is a Broadcom proprietary feature and is based on IEEE standard.

External Loopback Mode

The External Loopback mode allows in-circuit testing of the BCM53125S as well as the transmit path through the magnetics and the RJ-45 connector. External loopback can be performed with and without a jumper block. External loopback with a jumper block tests the path through the magnetics and RJ-45 connector. External loopback without the jumper block only tests the BCM53125S's transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1----------3
2----------6
4----------7
5----------8

The following six tables describe how the external loopback is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

Table 11: 1000BASE-T External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 1800h to 1000BASE-T Control register	Enable 1000BASE-T Master Mode.
Write 0040h to MII Control register	Enable Force 1000BASE-T.
Write 8400h to Auxiliary Control register	Enable External Loopback Mode with external loopback plug.

Table 12: 1000BASE-T External Loopback Without External Loopback Plug

Register Writes	*Comments*
Write 1800h to 1000BASE-T Control register	Enable 1000BASE-T Master Mode.
Write 0040h to MII Control register	Enable Force 1000BASE-T.
Write 8400h to Auxiliary Control register	Enable External Loopback Mode.
Write 0014h to Auxiliary Control register	Enable External Loopback Mode without external loopback plug.

Table 13: 100BASE-TX External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 2100h to MII Control register	Enable Force 100BASE-TX full-duplex mode.

Table 14: 100BASE-TX External Loopback Without External Loopback Plug

Register Writes	*Comment*
Write 2100h to MII Control register	Enable Force 100BASE-TX full-duplex mode.
Write 0014h to Auxiliary Control register	Enable external loopback mode without external loopback plug.

Table 15: 10BASE-T External Loopback With External Loopback Plug

Register Writes	Comments
Write 0100h to MII Control register	Enable Force 10BASE-T full-duplex mode.

Table 16: 10BASE-T External Loopback Without External Loopback Plug

Register Writes	Comments
Write 0100h to MII Control register	Enable Force 10BASE-T full-duplex mode
Write 0014h to Auxiliary Control register	Enable external loopback mode without external. loopback plug.

Note: To exit the External Loopback mode, a software or hardware reset is recommended.

Full-Duplex Mode

The BCM53125S supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

Copper Mode

When auto-negotiation is disabled, full-duplex operation can be enabled using register settings.

When auto-negotiation is enabled, the full-duplex capability is advertised for one of the following, depending on register settings:

- 10BASE-T
- 100BASE-TX
- 1000BASE-T

Master/Slave Configuration

In 1000BASE-T mode, the BCM53125S and its link partner perform loop timing. One end of the link must be configured as the timing master, and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. Each end generates an 11-bit random seed if the two settings are equal, and the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the BCM53125S sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register, and auto-negotiation is restarted. This is used to set the BCM53125S to manual master/slave configuration or to set the advertised repeater/DTE configuration.

Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the BCM53125S and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM53125S is configured to advertise 1000BASE-T capability.

The BCM53125S also supports software controlled Next Page exchanges. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM53125S automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM53125S is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM53125S is not configured to advertise 1000BASE-T capability, the BCM53125S does not advertise Next Page ability.

Frame Management

The BCM53125S provides a Frame Management block that works in conjunction with one of the GMII ports operating in IMP mode as the full-duplex packet streaming interface to the external CPU, with in-band messaging mechanism for management purpose.

Note: The BCM53125S supports the EEE feature for external PHYs connected on the IMP and GMII (port 5) port only through the GMII interface.

In-Band Management Port

The BCM53125S provides two PHY-less interface ports and supports a dual IMP ports (IMP port and Port 5) feature. One (IMP port) or both PHY-less ports (IMP port and Port 5) can be configured as the management port using register settings. In the dual IMP feature, all traffic to the CPU from LAN ports will be forwarded to IMP port, and all traffic to the CPU from WAN ports will be forwarded to Port 5. When the PHY-less interface port is defined as the Frame Management Port, it is referred to as the in-band management port (IMP).

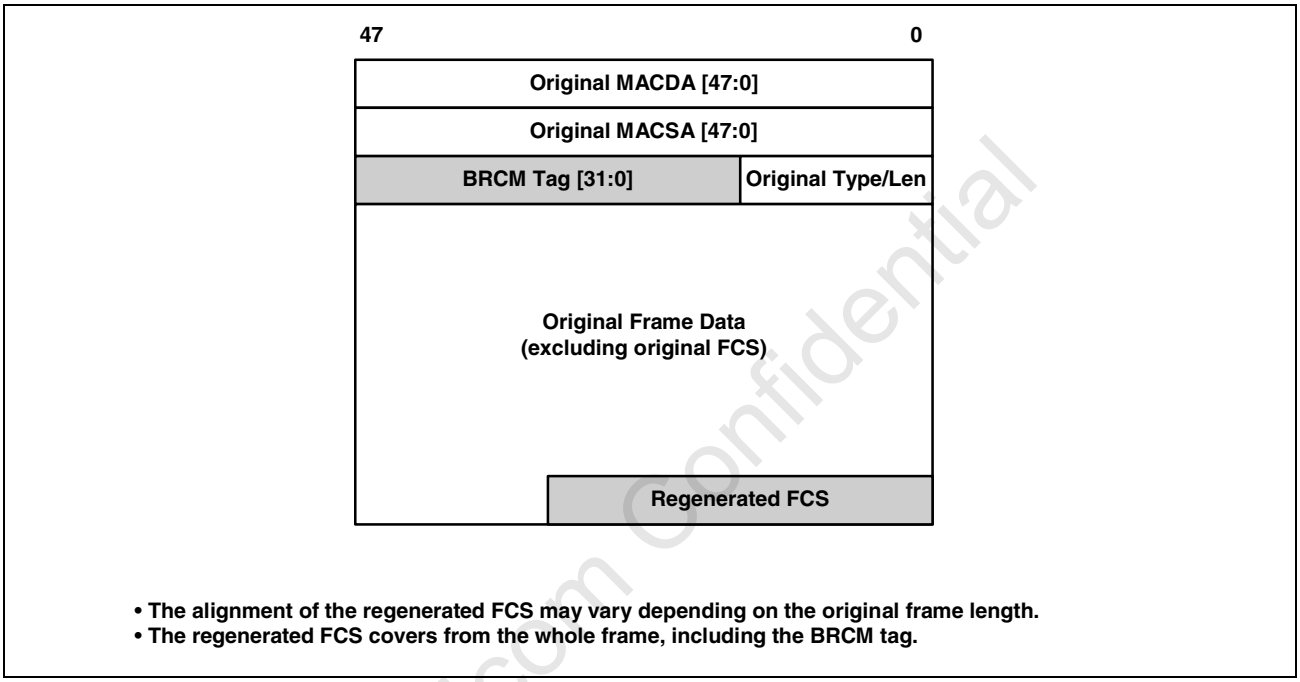
The IMP can be used as a full-duplex 10/100/1000 Mbps port, which can be used to forward management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other static address entries that have been identified as a special interest to the management system. Two interfaces only support Full Duplex mode.

Note: The signals of the IMP port are named as IMP_xxx in the Signal Description section. The signals of the WAN(port5) port are name as GMII_xxx.

As IMP is defined as the frame management port, normal frame data is forwarded to the port based on register settings. If these bits are cleared, no frame data will be forwarded to the Frame Management Port, with the exception that frames meeting the mirror ingress/egress rules criteria, will always be forwarded to the designated frame management port.

Packets transferred over the IMP port are tagged with the Broadcom proprietary header to carry the necessary information which is of interest to the management entity running on the CPU, as shown below, except for the PAUSE frame. The IMP port must support normal Ethernet pause based flow control mechanism.

Figure 11: IMP Packet Encapsulation Format



The BRCM tag is designed for asymmetric operation across the IMP port. The information carried from the switching device to the CPU is different from the information carried from the CPU to the switching device.

Similarly, the host system must insert the BRCM tag fields into frames it wished to send into the management port, to be routed to specific egress ports. The OPCODE within the tag field determines how the frame is handled, and allows frames to be forwarded using the normal address lookup using a port ID designation within the Tag.

The BRCM tag are transmitted with the convention of highest significant octet first, followed by the next lowest significant octet, and so on, with the least significant bit of each octet transmitted out from the MAC first. So, for the BRCM tag field in Table 17, the most significant octet would be transmitted first (bits [24:31]), with bit 24 being the first bit transmitted.

Broadcom Tag Format for Egress Packet Transfer

When a packet is forwarded by the switching device to the external CPU for processing, the BRCM tag is formatted as shown below.

Table 17: Egress Broadcom Tag Format (IMP to CPU)

31–29	***28–24***	***23–16***	***15–8***	***7–5***	***4–0***
OPCODE=000	Reserved	Reserved	REASON_CODE [7:0]	TC[2:0]	SRC_PID[4:0]
63–61		***60–38***		***37***	***36–32***
OPCODE=001		Reserved		T/R	T/R_PID[4:0]
		31–0			
		TIME_STAMP[31:0]			

- OPCODE 000

  This indicates the packet transfer with explicit reasons to help the external CPU to direct the packet for the appropriate packet processing entities.
- REASON_CODE [7:0]

  This indicates the reasons why the packet is forwarded to the external CPU so that the CPU can identify the appropriate software routines for packet processing.
- Bit [0] indicates mirroring.
- Bit [1] indicates SA learning.
- Bit [2] indicates switching.
- Bit [3] indicates protocol termination.
- Bit [4] indicates protocol snooping.
- Bit [5] indicates flooding/exception processing.
- Bit [6] and Bit [7] are reserved.
- TC [2:0]

  This indicates the traffic class classified by the switching device when forwarding the packet to the CPU.
- SRC_PID [4:0]

  This indicates the ingress port of the switching device where the packet is received.
- OPCODE 001

  This indicates a packet transfer with explicit time stamp recorded at the port where it was transmitted or received (indicated by the T/R_PID) for IEEE 802.1AS protocol implementation.
- T/R

  This indicates the type of time stamp. 0 indicates the time stamp recorded when the packet was received through the port (indicated by the T/R_PID); 1 indicates the time stamp recorded when the packet was transmitted through the port (indicated by the T/R_PID).
- T/R_PID [4:0]

  This indicates the port through which the packet was transmitted when T/R = 1, or the port through which the packet was received when T/R = 0.

- TIME_STAMP [31:0]

  This carries the time stamp recorded at the port through which the packet was transmitted when T/R = 1, or the time stamp recorded at the port through which the packet was received when T/R = 0.

Broadcom Tag Format for Ingress Packet Transfer

For packet transfer from the external CPU to the switching device, the BRCM tag is formatted as shown below.

Table 18: Ingress BRCM Tag (CPU to IMP)

31–29	***28–26***	***25–24***	***23–0***	
OPCODE=000	TC[2:0]	TE[1:0]	Reserved	
31–29	***28–26***	***25–24***	***23***	***22–0***
OPCODE=001	TC[2:0]	TE[1:0]	TS	DST_MAP[22:0]

- OPCODE 000

  It indicates that the external CPU is not dictating how the packet is forwarded, and the packet is forwarded by the switching device based on the original Ethernet packet information.
- OPCODE 001

  This indicates the packet is forwarded to multiple (or single) egress ports by the switching device based on the explicit direction of the external CPU.
- DST_MAP [22:0]

  This indicates the egress port bit map to which the external CPU intends to forward the packet. Bits [5:0] = Port[5:0], Bit 8 = IMP port.
- TC [2:0]

  This indicates the traffic class with which the external CPU intends to forward the packet.
- TS (time stamp request)

  This indicates whether the transmit time stamped at the egress port should be reported back to the external CPU.
- TE (tag enforcement)

  This indicates the 802.1Q/P tagging/untagging encapsulation enforcement for the packet transmission.

  00 = No enforcement (follow VLAN untag mask rules)

  01 = Untag enforcement

  10 = Tag enforcement

  11 = Reserved

MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM53125S implement 70-plus MIB counters on a per-port basis. MIB counters can be categorized into three groups: receive-only counters, transmit-only counters, and receive or transmit counters. This latter group can, as a group, be selectively steered to the receive or transmit process on a per-port basis. The section below describes each individual counter.

The BCM53125S offers the MIB snapshot feature per port. A snapshot of a selected port MIB registers can be captured and available to the users while MIB counters are continuing to count.

MIB Counters Per Port

Total number of counters per port = 45.

Table 19: Receive-Only Counters (19)

Receive-Only Counter	*Description*
RxDropPkts (32 bit)	Number of good packets received by a port that were dropped due to a lack of resources (e.g., lack of input buffers) or were dropped due to a lack of resources before a determination of the validity of the packet was able to be made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters.
RxOctets (64 bit)	Number of data bytes received by a port (excluding preamble, but including FCS), including bad packets.
RxBroadcastPkts (32 bit)	Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. The maximum packet size can be programmed.
RxMulticastPkts (32 bit)	Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. The maximum packet size can be programmed.
RxSAChanges (32 bit)	Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. The maximum packet size can be programmed.
RxUndersizePkts (32 bit)	Number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).
RxOversizePkts (32 bit)	Number of good packets received by a port that are greater than standard max frame size. The maximum packet size can be programmed.
RxFragments (32 bit)	Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.

Table 19: Receive-Only Counters (19) (Cont.)

Receive-Only Counter	*Description*
RxJabbers (32 bit)	Number of packets received by a port that are longer than standard max frame size and have either an FCS error or an alignment error.
RxUnicastPkts (32 bit)	Number of good packets received by a port that are addressed to a unicast address. The maximum packet size can be programmed.
RxAlignmentErrors (32 bit)	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.
RxFCSErrors (32 bit)	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size inclusive, and have a bad FCS with an integral number of bytes.
RxGoodOctets (64 bit)	Total number of bytes in all good packets received by a port (excluding framing bits, but including FCS). The maximum packet size can be programmed.
JumboPktCount (32 bit)	Number of good packets received by a port that are greater than the standard maximum size and less than or equal to the jumbo packet size, regardless of CRC or alignment errors.
RxPausePkts (32 bit)	Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88–08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE opcode (00–01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.
RxSymbolErrors (32 bit)	Total number of times a valid-length packet was received at a port and at least one invalid data symbol was detected. The counter only increments once per carrier event and does not increment on detection of a collision during the carrier event.
RxDiscard (32 bit)	Number of good packets received by a port that were discarded by the Forwarding Process.
InRangeErrors (32 bit)	Number of packets received with good CRC and one of the following: • The value of length/type field is between 46 and 1500 inclusive, and does not match the number of (MAC client data + PAD) data octets received. • The value of length/type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).
OutOfRangeErrors (32 bit)	Number of packets received with good CRC and the value of length/type field is greater than 1500 and less than 1536.

Table 20: Transmit-Only Counters (19)

Transmit-Only Counter	*Description*
TxDropPkts (32 bit)	This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.
TxOctets (64 bit)	Total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
TxBroadcastPkts (32 bit)	Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
TxMulticastPkts (32 bit)	Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
TxCollisions (32 bit)	Number of collisions experienced by a port during packet transmissions.
TxUnicastPkts (32 bit)	Number of good packets transmitted by a port that are addressed to a unicast address.
TxSingleCollision (32 bit)	Number of packets successfully transmitted by a port that have experienced exactly one collision.
TxMultipleCollision (32 bit)	Number of packets successfully transmitted by a port that have experienced more than one collision.
TxDeferredTransmit (32 bit)	Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. This only applies to the Half Duplex mode, while the Carrier Sensor Busy.
TxLateCollision (32 bit)	Number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
TxExcessiveCollision (32 bit)	Number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.
TxPausePkts (32 bit)	Number of PAUSE events at each port.
TxFrameInDisc (32 bit)	Number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (not maintained or reported in the MIB counters). Located in the Congestion Management registers (Page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM53125S internal flow-control/buffering scheme has been configured incorrectly.
TxQ0PKT(32 bit)	Total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.
TxQ1PKT(32 bit)	Total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.
TxQ2PKT(32 bit)	Total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.
TxQ3PKT(32 bit)	Total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.
TxQ4PKT(32 bit)	Total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.
TxQ5PKT(32 bit)	Total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.

Table 21: Transmit or Receive Counters (10)

Transmit or Receive Counter	Description
Pkts64Octets (32 bit)	Number of packets (including error packets) that are 64 bytes long.
Pkts65to127Octets (32 bit)	Number of packets (including error packets) that are between 65 and 127 bytes long.
Pkts128to255Octets (32 bit)	Number of packets (including error packets) that are between 128 and 255 bytes long.
Pkts256to511Octets (32 bit)	Number of packets (including error packets) that are between 256 and 511 bytes long.
Pkts512to1023Octets (32 bit)	Number of packets (including error packets) that are between 512 and 1023 bytes long.
Pkts1024toMaxPktOctets (32 bit)	Number of packets that (include error packets) are between 1024 and the standard maximum packet size inclusive.

Table 22: EEE Counters

EEE Counter	Description
LPI Idle count (32 bit)	EEE low-power idle event. In asymmetric mode, this is simply a count of the number of times that the lowPowerAssert control signal has been asserted for each MAC. In symmetric mode, this is the count of the number of times both lowPowerAssert and the lowPowerIndicate (from the receive path) are asserted simultaneously.
LPI Duration count (32 bit)	EEE low-power idle duration. This counter accumulates the number of microseconds that the associated MAC/PHY is in the low-power idle state. The unit is 1 µs.

Table 23 identifies the mapping of the BCM53125S MIB counters and their generic mnemonics to the specific counters and mnemonics for each of the key IETF MIBs that are supported. Direct mappings are defined. However, there are several additional statistics counters, which are indirectly supported that make up the full complement of the counters required to fully support each MIB. These are shown in Table 24 on page 87.

Finally, Table 25 on page 88 identifies the additional counters supported by the BCM53125S and references the specific standard or reason for the inclusion of the counter.

Table 23: Directly Supported MIB Counters

BCM53125S MIB	Ethernet-Like MIB RFC 1643	Bridge MIB RFC 1493	MIB II Interface RFC 1213/1573	RMON MIB RFC 1757
RxDropPkts	dot3StatsInternalMACReceiveErrors	dot1dTpPortInDiscards	ifInDiscards	–
RxOctets	–	–	ifInOctets	etherStatsOctets
RxBroadcastPkts	–	–	ifInBroadcastPkts	etherStatsBroadcastPkts
RxMulticastPkts	–	–	ifInMulticastPkts	etherStatsMulticastPkts

Table 23: Directly Supported MIB Counters (Cont.)

BCM53125S MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxSAChanges	Note 2	Note 2	Note 2	Note 2
RxUndersizePkts	–	–	–	etherStatsUndersize Pkts
RxOversizePkts	dot3StatsFrameToo Longs	–	–	etherStatsOverrsize Pkts
RxFragments	–	–	–	eytherStatsFragment s
RxJabbers	–	–	–	etherStatsJabbers
RxUnicastPkts	–	–	ifInUcastPkts	–
RxAlignmentErrors	dot3StatsAlignment Errors	–	–	–
RxFCSErrors	dot3StatsFCSErrors	–	–	–
RxGoodOctets	–	–	–	–
RxExcessSizeDisc	Note 2	Note 2	Note 2	Note 2
RxPausePkts	Note 2	Note 2	Note 2	Note 2
RxSymbolErrors	Note 2	Note 2	Note 2	Note 2
Note 1	–	–	ifInErrors	–
Note 1	–	–	ifInUnknownProtos	–
Note 1	–	dot1dTpPortInFrames	–	–
TxDropPkts	dot3StatsInternal MACTransmitErrors	–	ifOutDiscards	–
TxOctets	–	–	ifOutOctets Note 3	–
Note 1	–	dot1dTpPortOutFrame s	–	–
TxBroadcastPkts	–	–	ifOutBroadcastPkts	–
TxMulticastPkts	–	–	ifOutMulticastPkts	–
TxCollisions	–	–	–	etherStatsCollisions
TxUnicastPkts	–	–	ifOutUcastPkts	–
TxSingleCollision	dot3StatsSingle CollisionFrames	–	–	–
TxMultipleCollision	dot3StatsMultiple CollisionFrames	–	–	–
TxDeferredTransmit	dot3StatsDeferred Transmissions	–	–	–
TxLateCollision	dot3StatsLate Collision	–	–	–
TxExcessiveCollision	dot3StatsExcessive Collision	–	–	–
TxFrameInDisc	Note 2	Note 2	Note 2	Note 2
TxPausePkts	Note 2	Note 2	Note 2	Note 2

Table 23: Directly Supported MIB Counters (Cont.)

BCM53125S MIB	Ethernet-Like MIB RFC 1643	Bridge MIB RFC 1493	MIB II Interface RFC 1213/1573	RMON MIB RFC 1757
Note 4	dot3StatsCarrier SenseErrors	–	–	–
Note 1	–	–	ifOutErrors	–
Pkts64Octets	–	–	–	etherStatsPkt64 Octets
Pkts65to127Octets	–	–	–	etherStatsPkt65to 127Octets
Pkts128to255Octets	–	–	–	etherStatsPkt128to 255Octets
Pkts256to511Octets	–	–	–	etherStatsPkt256to 511Octets
Pkts512to1023Octets	–	–	–	etherStatsPkt512to 1023Octets
Pkts1024toMaxPkt Octets	–	–	–	etherStatsPkt1024to MaxPktOctets
Note 1	–	–	–	etherStatsDrop Events
Note 1	–	–	–	etherStatsPkts
Note 1	–	–	–	etherStatsCRCAlign Errors
Note 4	dot3StatsSQETest Errors	–	–	–

Notes:

Note 1: Derived by summing two or more of the supported counters. See Table 24 on page 87 for specific details.

Note 2: Extensions required by recent standards developments or BCM53125S operation specifics.

Note 3: The MIB II interfaces specification for if OutOctets includes preamble/SFD and errored bytes. Because IEEE 802.3-compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets counter maintained by the BCM53125S is consistent with good bytes transmitted, excluding preamble, but including FCS. The count can be adjusted to more closely match the if OutOctets definition by adding the preamble for TxGoodPkts and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.

Note 4: The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM53125S. These attributes were originally defined to support coax-based AUI transceivers. The BCM53125S integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of 0 (not supported).

Table 24: Indirectly Supported MIB Counters

BCM53125S MIB	Ethernet-Like MIB RFC 1643	Bridge MIB RFC 1493	MIB II Interface RFC 1213/1573	RMON MIB RFC 1757
RxErrorPkts = RxAlignmentErrors + RxFCSErrors + RxFragments + RxOversizePkts + RxJabbers	–	–	ifInErrors	–

Table 24: Indirectly Supported MIB Counters (Cont.)

BCM53125S MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
–	–	–	ifInUnknownProtos	–
RxGoodPkts = RxUnicastPkts + RxMulticastPkts + RxBroadcastPkts	–	dot1dTpPortIn Frames	–	–
DropEvents = RxDropPkts + TxDropPkts	–	–	–	etherStatsDrop Events
RxTotalPkts = RxGoodPkts + RxErrorPkts	–	–	–	etherStatsPkts
RxCRCAlignErrors = RxCRCErrors + RxAlignmentErrors	–	–	–	etherStatsCRCAlign Errors
–	dot3StatsSQETest Errors	–	–	–
RxFramesTooLong = RxOversizePkts + RxJabber	dot3StatsFrameToo Longs	–	–	–
TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts	–	dot1dTpPortOut Frames	–	–
TxErrorPkts = TxExcessiveCollision + TxLateCollision Note 1	–	–	ifOutErrors	–

Note: The number of packets transmitted from a port that experienced a late collision or excessive collisions. While some media types operate in half-duplex mode, frames that experience carrier sense errors are also summed in this counter. The BCM53125S integrated design means this error condition is eliminated.

Table 25: BCM53125S Supported MIB Extensions

BCM53125S MIB	*Appropriate Standards Reference*
RxSAChanges	IEEE 802.3u Clause 30—Repeater Port Managed Object Class aSourceAddressChanges.
RxExcessSizeDisc	The BCM53125S cannot store packets in excess of 1536 bytes (excluding preamble/SFD, but inclusive of FCS). This counter indicates packets that were discarded by the BCM53125S due to excessive length.
RxPausePkts	IEEE 802.3x Clause 30—PAUSE Entity Managed Object Class aPAUSEMACCtrlFramesReceived.
RxSymbolErrors	IEEE 802.3u Clause 30—Repeater Port Managed Object Class aSymbolErrorDuringPacket.

Table 25: BCM53125S Supported MIB Extensions (Cont.)

BCM53125S MIB	*Appropriate Standards Reference*
TxFrameInDisc	Internal diagnostic use for optimization of flow control and buffer allocation algorithm.
TxPausePkts	Number of PAUSE events at a given port.

Integrated High-Performance Memory

The BCM53125S embed a 128 KB high-performance SRAM for storing:

- Packet data
- The ARL table
- The VLAN table
- The TX queues
- Descriptors

This eliminates the need for external memory and allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves nonblocking performance for stand-alone 5-port applications.

Switch Controller

The core of the BCM53125S devices is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

Buffer Management

The frame buffer memory is divided into pages (units of data consisting of 256 bytes each). Each received packet may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, the VLAN lookup, learning and aging functions, egress descriptor update, and output-port queue managers. These processes are arbitrated to provide fair access to the memory and minimize the latency of critical processes to provide a fully nonblocking solution.

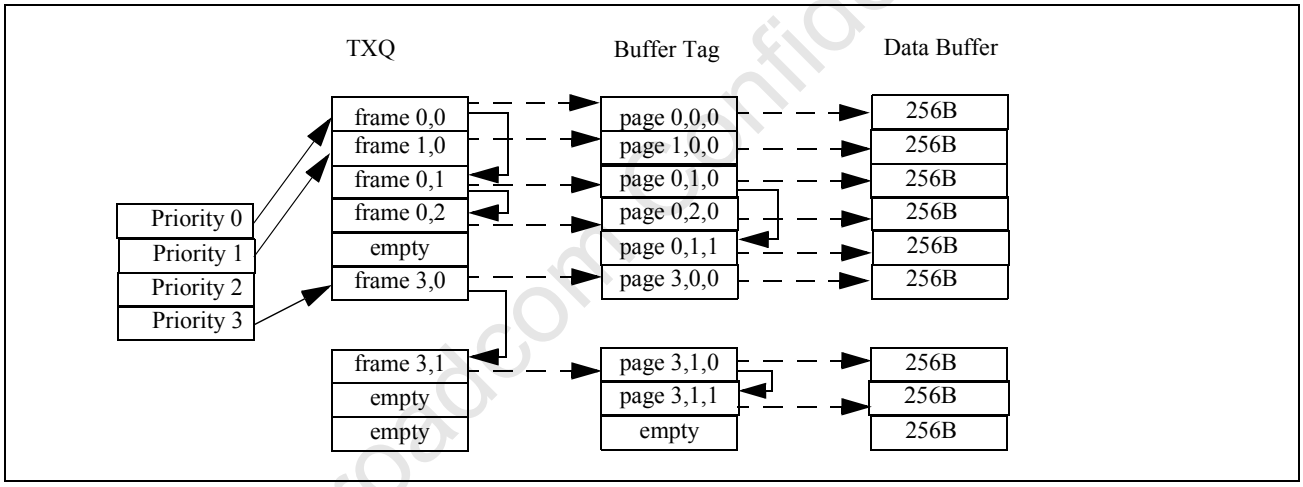
Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (see Figure 12). The first level is the TXQ linked list, and the second level is the buffer tag linked list. The TXQ linked list is used to maintain frame TC order for each port. For each frame, the buffer tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

Each egress port supports up to six transmit queues for servicing Quality of Service (QoS). All six transmit queues share the 512 entries of the TXQ table. The TXQ table is maintained as a linked list, and each node in the TXQ uses one entry in the TXQ table. The TXQ size for each priority can be programmed to up to 512 entries.

When the QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per-port individual internal memory. Each node in the queue represents a pointer that points to a frame buffer tag. Each buffer tag includes frame information and a pointer to the next buffer tag. Each buffer tag has an associated page allocated in the frame buffer. For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. For instance, a 9720-byte jumbo frame requires 38 buffer tags for handling the frame.

Figure 12: TXQ and Buffer Tag Structure



Section 4: System Interfaces

Overview

The BCM53125S include the following interfaces:

Each interface is discussed in detail in these sections.

Copper Interface

The internal PHYs transmit and receive data using the analog copper interface. This section discusses the following topics:

Auto-Negotiation

The BCM53125S negotiate a mode of operation over the copper media using the auto-negotiation mechanism defined in the IEEE 802.3u and IEEE 802.3ab specifications. When the auto-negotiation function is enabled, the BCM53125S automatically choose the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53125S can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex
- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be disabled by software control, but is required for 1000BASE-T operation.

Lineside (Remote) Loopback Mode

The lineside loopback mode allows the testing of the copper interface from the link partner. This mode is enabled by setting bit 15 of the Miscellaneous Test register. The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the internal MAC interface.

Frame Management Port Interface

The dedicated frame management port provides high-speed connection to transfer management packets to an external management agent. For more information about frame management, see “Frame Management” on page 78. The port is configurable to MII, Reverse MII (RvMII), GMII, or RGMII using strap pins or software configuration.

Note: The Frame Management port interface supports only full duplex mode.

MII Interface

The Media Independent Interface (MII) serves as a digital data interface between the BCM53125S and an external 10/100 Mbps management entity or a PHY entity. The BCM53125S provides an IEEE 802.3u-compatible MII interface.

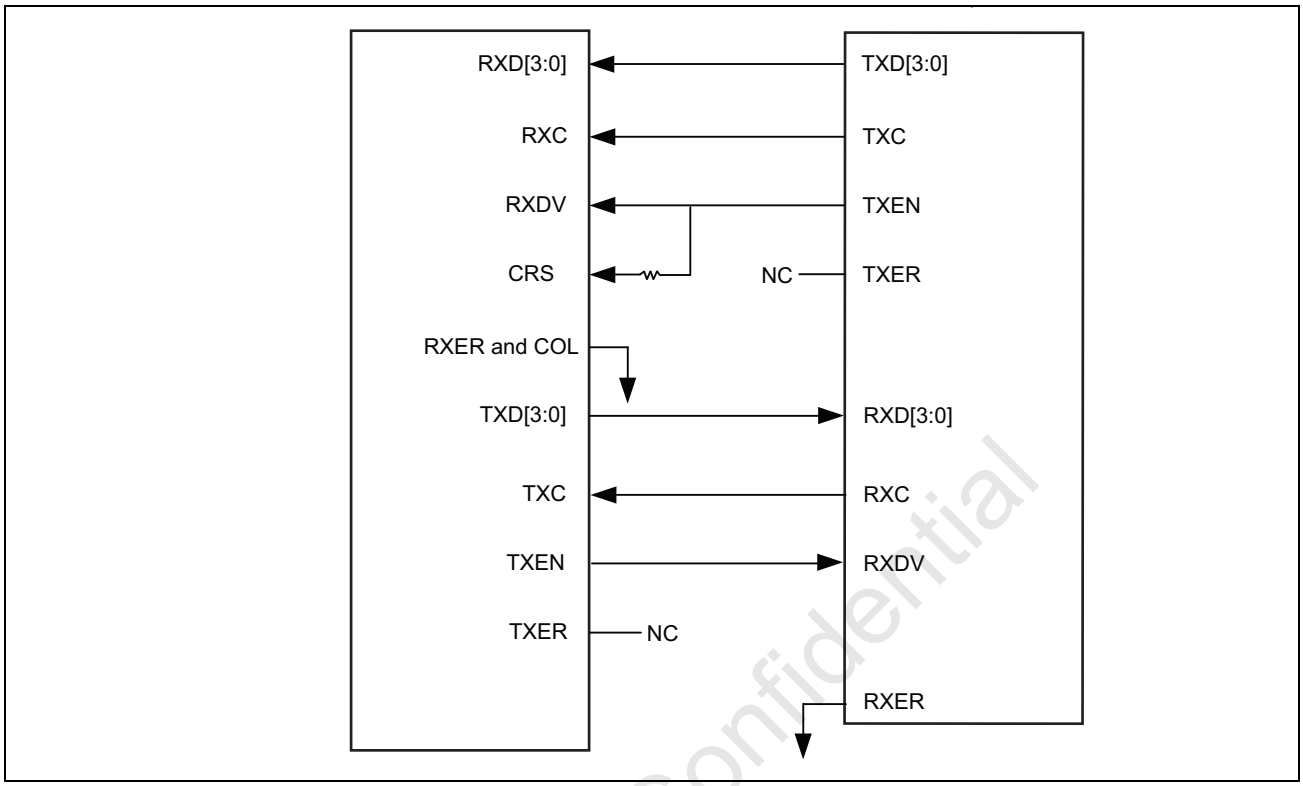
TMII (TURBO MII) and RvTMII (Reverse TMII) Interface

The TMII and RvTMII interfaces use the same hardware interface signals as the MII interface. The TMII mode requires the SPEED setting bits in the register (page 00h, address 0Eh, bits [3:2]) to be set. TMII mode supports 200 Mbps data rate over the existing MII interface by running the interface at (up to) 50 MHz. The original MII timing is designed such that it can support 50 MHz clocking over the existing design.

Reverse MII Interface (RvMII)

The media independent interface (MII) serves as a digital data interface between the BCM53125S and an external 10/100 Mbps management entity. Reverse MII notation reflects the MII port interfacing to a MAC-based external agent. The RvMII contains all the signals required to transmit and receive data at 100 Mbps and 10 Mbps operation. The interface supports full duplex operation only. See Figure 13 for connection information.

Figure 13: RvMII Port Connection



GMII Interface

The Gigabit Media Independent Interface (GMII) serves as a digital data interface between the BCM53125S and an external gigabit management entity. Transmit and receive data is clocked on the rising edge of the clocks. The GMII transmits data synchronously using the TXD[7:0] and RXD[7:0] data signals.

RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM53125S and an external management entity or an external PHY to provide additional data port capacity. Transmit and receive data is clocked on the rising and falling edge of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data transmission rate. The RGMII transmits data synchronously using the TXD[3:0] and RXD[3:0] data signals. The BCM53125S offers either 2.5V or 1.5V RGMII interface with an external device.

WAN Interface

The BCM53125S provides one GMII/RGMII/MII/RvMII/TMII/RvTMII interface (Port 5) for WAN port or integrated gateways application. Port 5 is IMP port-capable; the BCM53125S provides dual-IMP (both IMP port and Port 5) feature.

Port 5 can be configured as IMP port in BCM53125S dual-IMP enabled only.

Note: The BCM53125S supports the EEE feature for external PHYs connected on the IMP port and GMII (port 5) port only through the GMII interface.

Configuration Pins

Initial configuration of the BCM53125S takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes, and the pin transitions to normal operation. Pull-up or pull-down resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pull-down configuration. See “Signal Descriptions” on page 125 for more information.

Programming Interfaces

The BCM53125S can be programmed using the SPI interface or the EEPROM interface. The interfaces share a common pin set that is configured using the CPU_EPROM_SEL strap pin. The “SPI-Compatible Programming Interface” on page 94 provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM53125S register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the “EEPROM Interface” on page 109 can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM53125S devices is broken into a number of pages. Each page groups a logical set of registers associated with a specific function. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

An explanation follows for using the serial interface with an SPI-compatible CPU (“SPI-Compatible Programming Interface” on page 94) or an EEPROM (“EEPROM Interface” on page 109). Either mode can be selected with the strap pin, CPU_EPROM_SEL. Either mode has access to the same register space.

SPI-Compatible Programming Interface

One way to access the BCM53125S internal registers is to use the serial peripheral interconnect (SPI) compatible interface. This four-pin interface is designed to support a fully functional, bi-directional Motorola serial peripheral interface (SPI) for register read/write accesses. The maximum speed of operation is 25 MHz. The SPI interface shares pins with the EEPROM interface. To select the SPI interface, pull up or float the CPU_EPROM_SEL pin. (The internal pull-up resistor defaults SPI interface over EEPROM interface.)

The SPI is a four-pin interface comprises the following:

- Device select (SS: slave select, input to BCM53125S)
- Device clock (SCK: Operates at speeds up to 25 MHz, input to BCM53125S)
- Data write line (MOSI: Master Out/Slave In, input to BCM53125S)
- Data read line (MISO: Master In/Slave Out, output from BCM53125S)

Note: All the RoboSwitch™ SPI interfaces are designed to operate in slave mode. Therefore, the SCK and SS signals are driven by the external master host device when accessing the BCM53125S registers. For more detailed descriptions reader may refer to the *Motorola SPI spec MC68HC08AS20-Rev. 4.0*.

Note: The internal SPI bus can be in the busy state, not allowing an external device to access the switch registers during power-up. The SPI bus is held busy while the internal 8051 controller is being initialized. This busy period can be as long as 350 ms from the deasserting of the RESET line.

SS: Slave Select

The SS signal is used to select a slave device and to indicate the beginning of transmission. The BCM53125S SPI interface operates in the clock phase one (CPHA = 1) transmission format. In this format, the SS signal is driven active low while the SCK signal is high, and remains low throughout the transmission including multiple-byte transfers. The minimum time requirement between SS operation is 200 ns.

SCK: Serial Clock

The serial clock SCK maximum operating frequency is 25 MHz for the BCM53125S family of devices. The SCK is used to clock data into and out of the Slave ROBO device. The SCK signal is expected to remain high when the interface is idle. This is because the BCM53125S SPI design is based on CPOL = 1 (Clock Polarity = 1). This is not programmable on BCM53125S. The BCM53125S is designed so that data is driving by the falling edge and sampling by the rising edge of the SCK clock. This clock is not a free-running clock, it is generated only during a data transaction, and remains high when the clock is idle.

MOSI: Master Output Slave Input

The MOSI signal is used by the master device to transmit the data to the slave device. The data is put on the bus and is expected to be clocked in by a rising edge of the SCK clock signal. This line is used to issue a command and to set the register page and address value of read/write operations.

MISO: Master Input Slave Output

The MISO signal is used by the Slave device to output the data to the master device. The data is put on the bus and is expected to be clocked out by a rising edge of the SCK clock signal. This line is used to transmit the status and the content of the register of read operation.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM53125S. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM53125S slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms, normal SPI and fast SPI, determined by the content of the command byte. Figure 14 shows the normal SPI command byte, and Figure 15 shows the Fast SPI command byte. These two mechanisms should not be mixed in an implementation; the CPU should always initiate transfers consistently with only one of the two mechanisms.

0	1	1	MODE = 0	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 14: Normal SPI Command Byte

Byte Offset (MSB)	Byte Offset	Byte Offset (LSB)	MODE = 1	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 15: Fast SPI Command Byte

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is a 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b. If bit 4 is a 1, bits 7:5 indicate a fast SPI command byte, and bits 7:5 indicate the byte offset into the register that the BCM53125S starts to read from (byte offsets are not supported for write operations).

In command bytes, bits [3:1] indicate the CHIP ID to be accessed. Because the BCM53125S operates as a single-chip system, the CHIP ID is 000.

Note: The SS# signal must also be active for any BCM53125S device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block data from a register to be stored/read in a single transmission. When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits 7:5 of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Noncontiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The SS signal must remain low for the entire read or write transaction, as shown in Figure 16 on page 97 and Figure 17 on page 97, with the transaction terminated by the deassertion of the SS line by the master.

Figure 16: SPI Serial Interface Write Operation

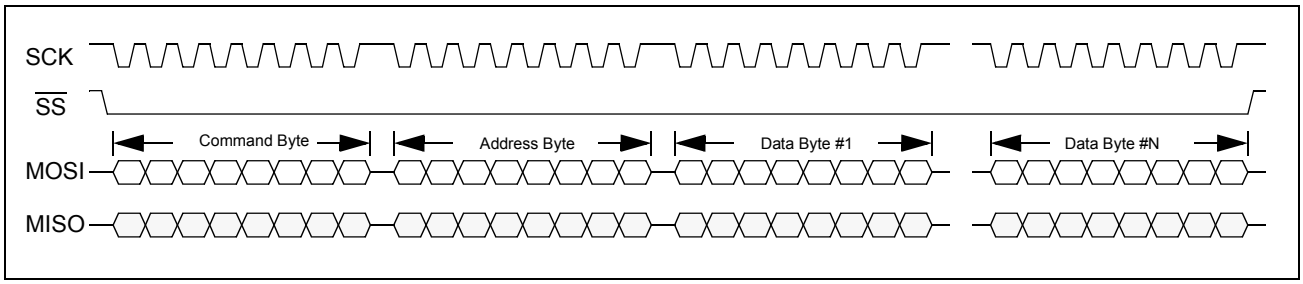
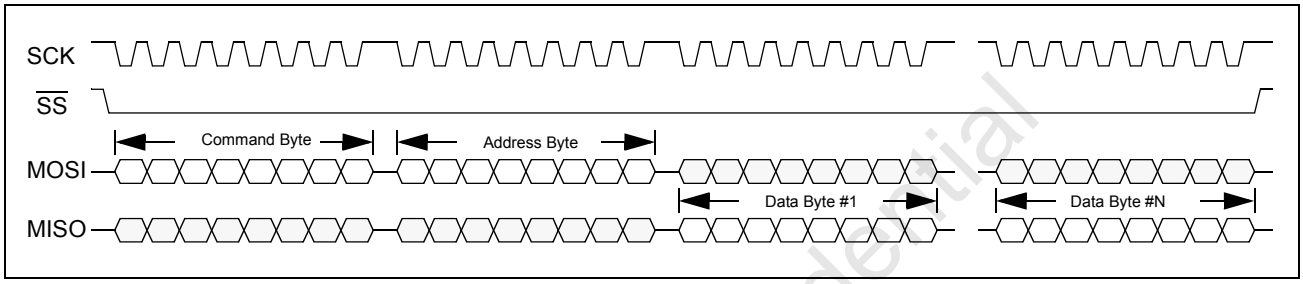


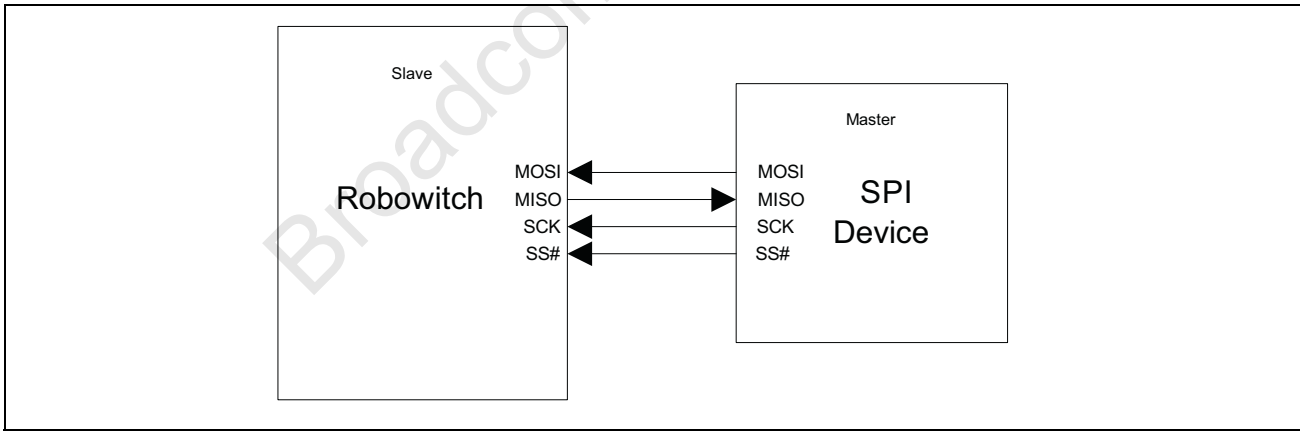
Figure 17: SPI Serial Interface Read Operation



The following diagram shows the typical connection block diagram for SPI interface with/without external PHY devices.

Without External PHY

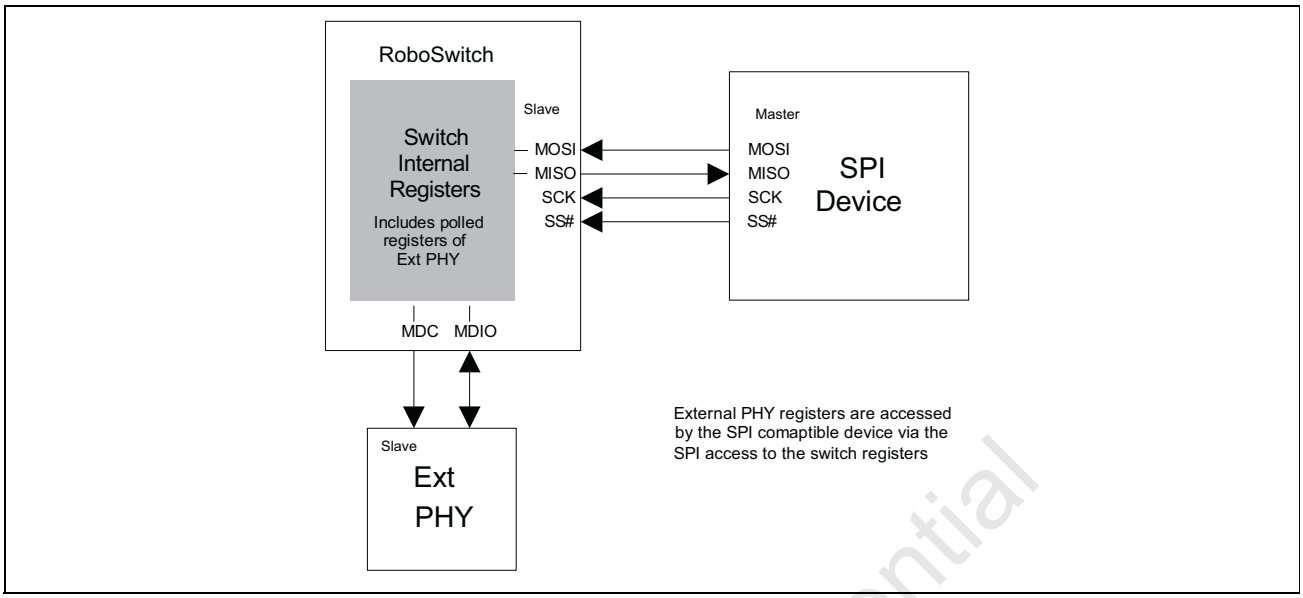
Figure 18: SPI Interface Without External PHY Device



External PHY Registers

The BCM53125S also uses the MDIO/MDC interface for polling registers of an external PHY. In this case, the MDIO/MDC interface polls the external PHY registers pulling the data internal to the BCM53125S. Then, the external PHYs and retrieved from the register data using the SPI interface. The MDIO/MDC interface is not used as a method to access internal PHY registers. This must be done using the SPI interface.

Figure 19: Accessing External PHY Registers



Reading and Writing BCM53125S Registers Using SPI

BCM53125S internal register read and write operations are executed by issuing a command followed by multiple accesses of the SPI registers in the BCM53125S. There are three SPI interface registers in the BCM53125S that are used by the master device to access the internal switch registers. The SPI interface registers are:

- SPI Page register (page: global, address: FFh): Used to specify the value of the specific register pages.
- SPI Data I/O register (page: global, address: F0h): Used to write and read the specific register's content.
- SPI Status register (page: global, address: FEh): Used to check for an operation completion:
- Bit 7 = SPIF, SPI read/write complete flag
- Bit 6 = Reserved
- Bit 5 = RACK, SPI read data ready acknowledgment
- Bit 4:3 = Reserved
- Bit 2 = MDIO_Start, Start/Done MDC/MDIO operation
- Bit 1 = Reserved
- Bit 0 = Reserved

The BCM53125S SPI interface supports the following operating modes:

- Normal read mode
- Fast read mode
- Normal write mode

Note: The RoboSwitch family does not support fast-write mode.

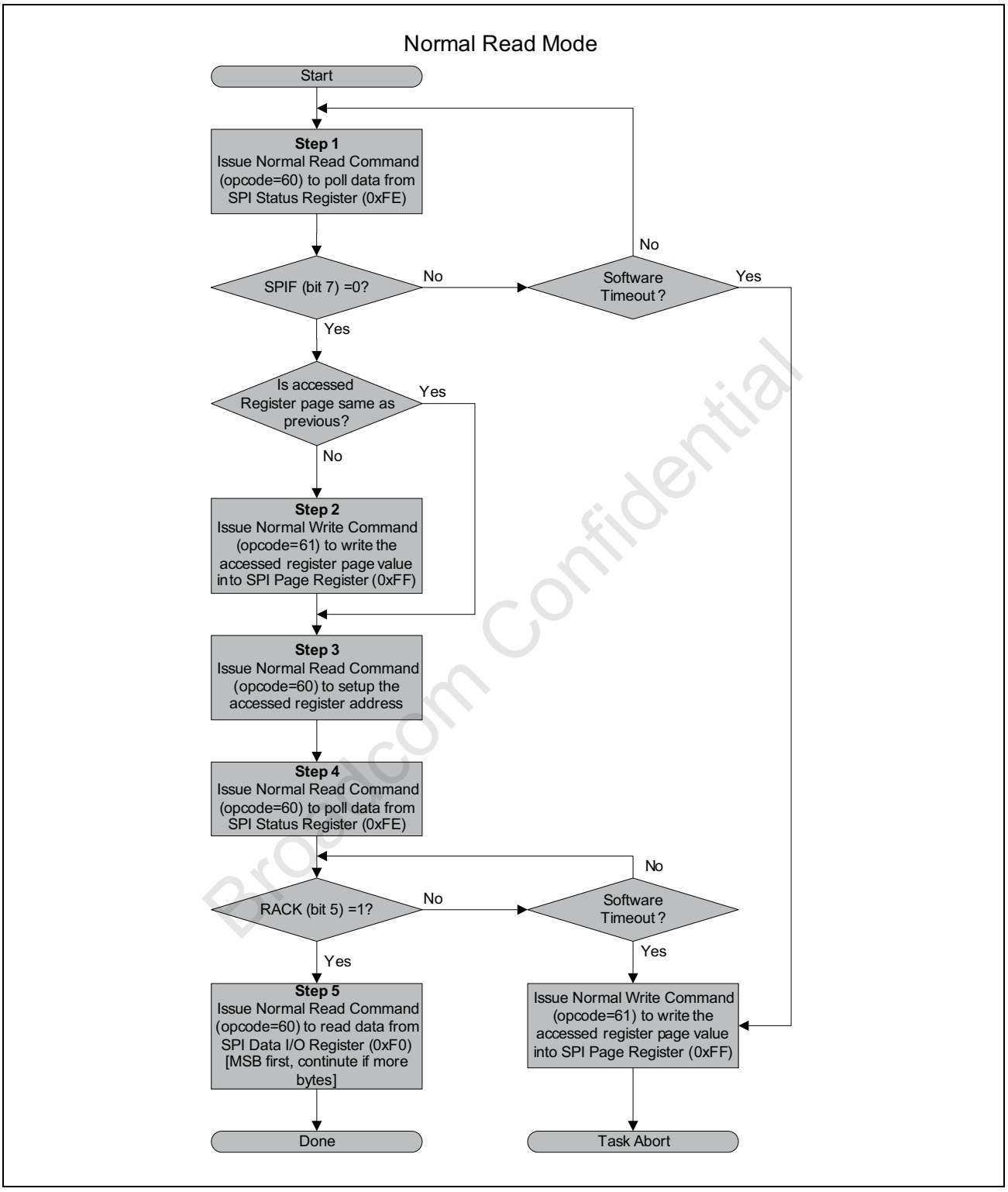
The details of each modes are described in the following paragraphs.

Normal Read Operation

Normal read operation consists of five transactions (five SS operations):

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a normal write command (opcode = 0x61) to write the register page value into the SPI Page register 0xFF.
3. Issue a normal read command (opcode = 0x60) to setup the required RoboSwitch register address.
4. Issue a normal read command (opcode = 0x60) to poll the RACK bit in the SPI status register (0xFE) to determine the completion of read (register content gets loaded in SPI Data I/O register).
5. Issue a normal read command (opcode = 0x60) to read the specific registers' content placed in the SPI Data I/O register (0xF0).

Figure 20: Normal Read Operation

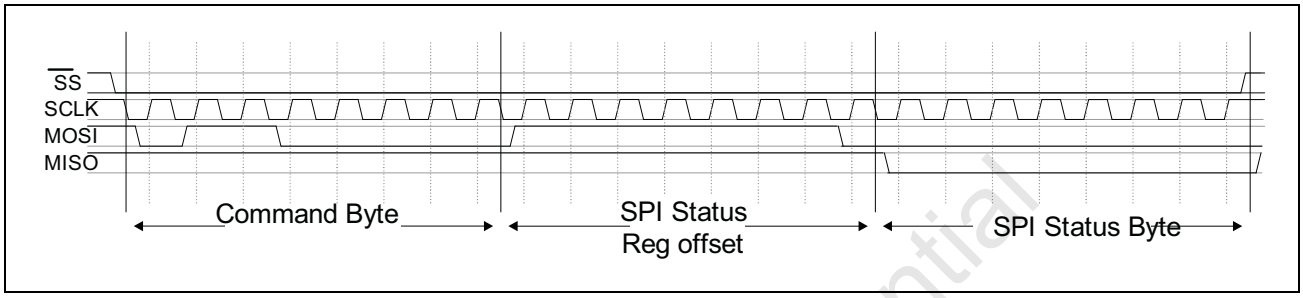


Example: Read from 1000BASE-T Control register (page 10h, offset 12h).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).

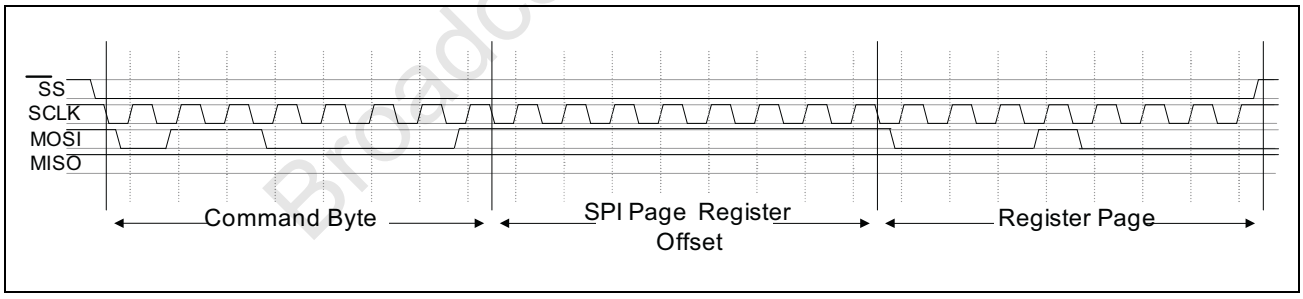
- Assert SS while SCK is high idle state.
- Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60).
- Clock in the SPI Status register address (0xFE).
- Clock out the SPI Status register value: 0 0 0 0 0 0 0 0 (SPIF bit 7 = 0).
- Deassert SS while SCK is high idle state.

Figure 21: Normal Read Mode to Check the SPIF Bit of SPI Status Register



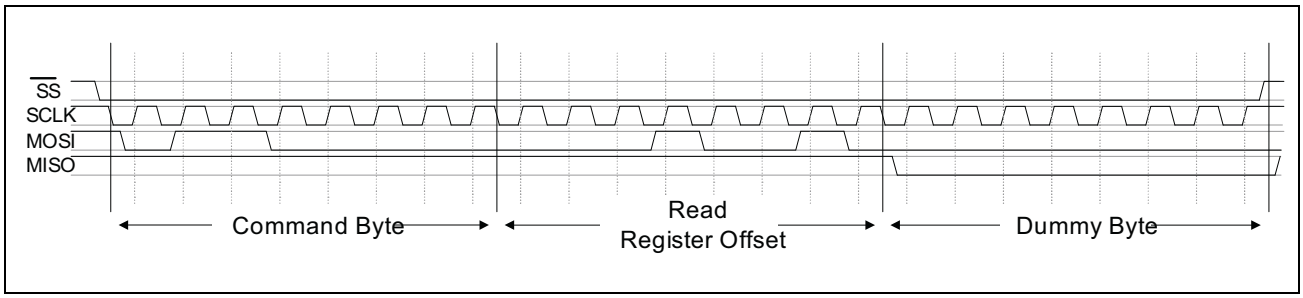
1. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into SPI Page Reigster(0xFF)—this step is required only if previous read/write was not to/from Page 10h.
   - Assert SS while SCK is high idle state.
   - Clock in a normal write command byte: 0 1 1 0 0 0 0 1 (opcode = 0x61).
   - Clock in offset of Page register (0xFF).
   - Clock in the accessed register page value: 0 0 0 1 0 0 0 0 (Page register: 0x10).
   - Deassert SS while SCK is high idle state.

Figure 22: Normal Read Mode to Setup the Accessed Register Page Value



2. Issue a normal read command (opcode = 0x60) and write the accessed register address value 0x12, and clock out 8 bits to complete the read cycle, but discard result (this is where the state machine triggers a internal data transfer from Address 0x12 to the SPI Data I/O register).
   - Assert SS while SCK is high idle state.
   - Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60).
   - Clock in the address of accessed register address value (0x12).
   - Clock out eight clocks for the dummy read, and discard results on MISO.
   - Deassert SS while SCK is high idle state.

Figure 23: Normal Read Mode to Setup the Accessed Register Address Value (Dummy Read)

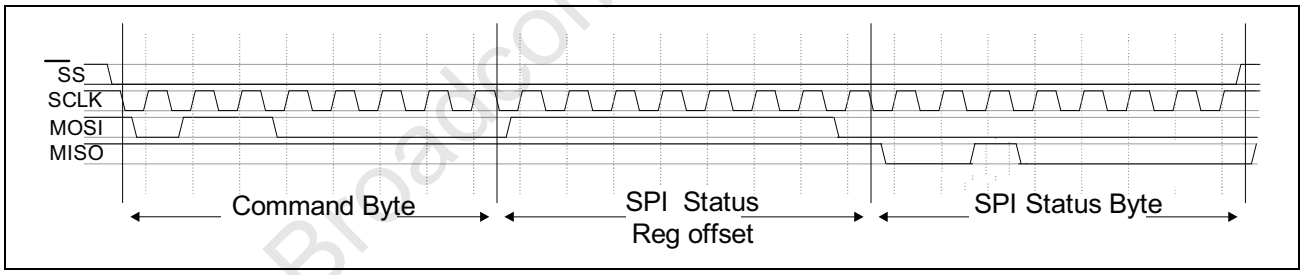


Note: This dummy read is always eight clock cycles, whether or not it is an 8-bit register.

3. Issue a normal read command (opcode = 0x60) to read the SPI Status to check the RACK bit for completion of the register content transfer to the SPI Data I/O register. (This step may be repeated until the proper bit set is read.)

- Assert SS while SCK is high idle state.
- Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60).
- Clock in offset for SPI Status Register (0xFE): 1 1 1 1 1 1 1 0.
- Clock out the content of SPI Status bits.
- Repeat the polling until the content of SPI Status Register value: 0 0 1 0 0 0 0 0 (RACK bit 5 = 1).
- Deassert SS while SCK is high idle state.

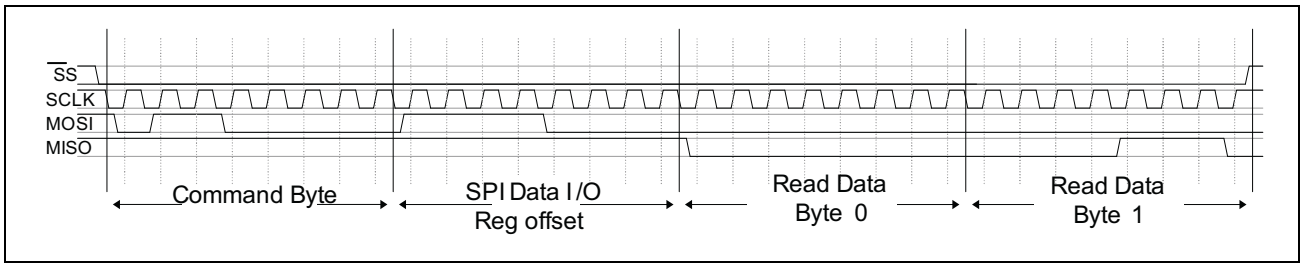
Figure 24: Normal Read Mode to Check the SPI Status for Completion of Read



4. Issue a normal read command (opcode = 0x60) to read the data from the SPI Data I/O register:

- Assert SS while SCK is high idle state.
- Clock in command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60).
- Clock in offset of SPI Data I/O register (0xF0).
- Clock out first data byte on MISO line: 0 0 0 0 0 0 0 0 (byte 0: bit 7 to bit 0: MSB to LSB).
- Clock out next byte (in this case, last) on MISO line: 0 0 0 0 1 1 1 0 (byte 1: bit 15 to bit 8).
- [Continue if more bytes].
- Deassert SS while SCK is high idle state.

Figure 25: Normal Read Mode to Obtain the Register Content



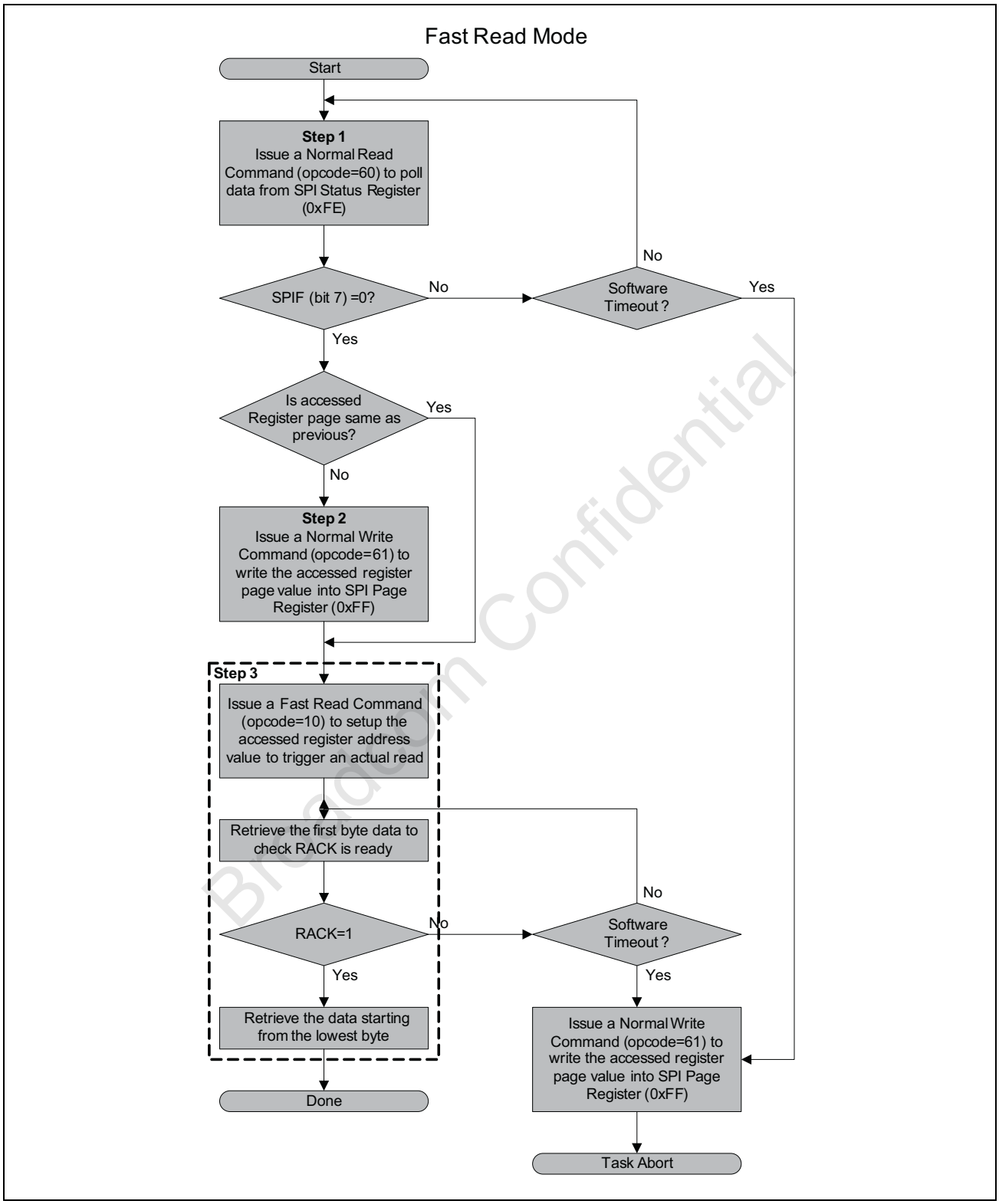
Fast Read Operation

Fast Read operation consists of 3 transactions (three SS operations):

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status Register (0xFE) to determine the operation can start.
2. Issue a Fast Read command (opcode = 0x10) to setup the accessed Register Page value into the Page register (0xFF).
3. Issue a Fast Read command (opcode = 0x10) to setup the accessed register address value, to trigger an actual read, and retrieve the accessed register content till the completion.

Fast Read mode process is different from normal read mode, once the switch receives a fast read command followed by the register page and address information, the status and the data (register content) will be put on the MISO line without going through the SPI Status register or SPI Data I/O register. Once RACK bit of the bytes following the Fast Read command with Address information is recognized the register content will be put on MISO line immediately following the byte with RACK bit set. The Fast Read process is described in the following paragraphs with a flowchart followed by a step by step description.

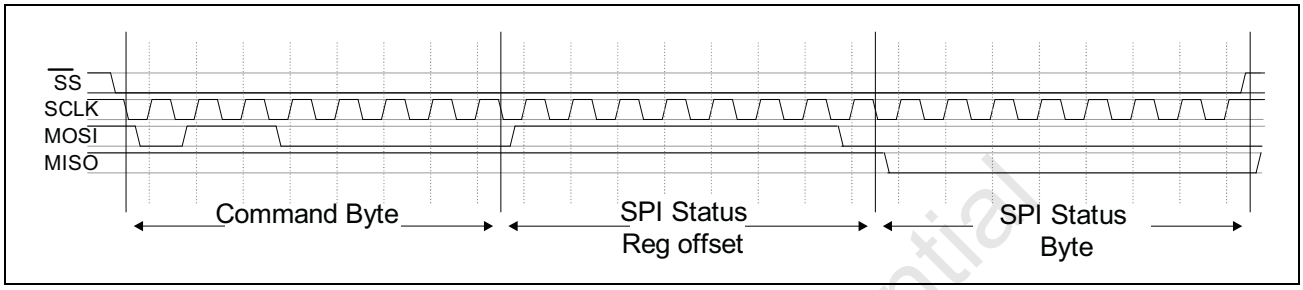
Figure 26: Fast Read Operation



Example: Read from 1000BASE-T Control register (Page 10h, Offset 12h).

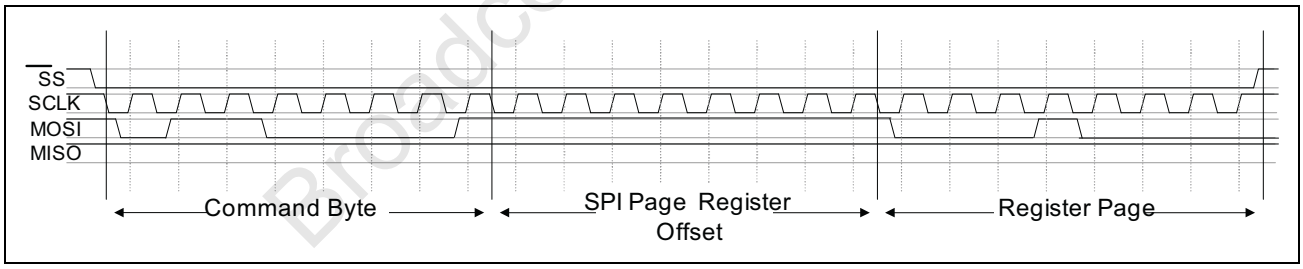
1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
   - Assert SS while SCK is high idle state.
   - Clock in a normal read command byte: 0 1 1 0 0 0 0 0(opcode = 0x60).
   - Clock in the SPI Status register address (0xFE).
   - Clock in the accessed register page value: 0 0 0 0 0 0 0 0 (SPIF bit 7 = 0).
   - Deassert SS while SCK is high idle state.

Figure 27: Normal Read Mode to Check the SPIF Bit of SPI Status Register



2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 in to SPI Page Reigster(0xFF)—this step is required only if previous read/write was not to/from Page 10h.
   - Assert SS while SCK is high idle state.
   - Clock in a Fast Read command byte: 0 11 0 0 0 0 0 1 (opcode = 0x61).
   - Clock in offset of Page register (0xFF).
   - Clock in the accessed register page value: 0 0 0 1 0 0 0 0 (Page register: 0x10).
   - Deassert SS while SCK is high idle state.

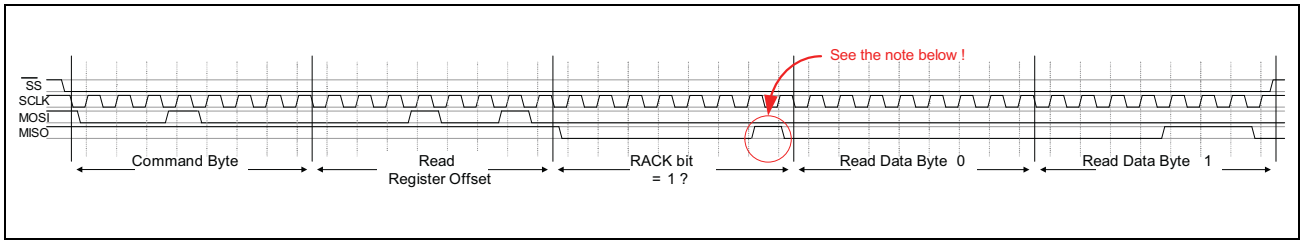
Figure 28: Fast Read Mode to Setup New Page Value



3. Issue a Fast Read command (opcode = 0x10), followed by the Address of the accessed register (0x12), check for a read completion by checking the RACK bit in the SPI Status register, and finally clock out the read data.
   - Assert SS while SCK is high idle state.
   - Clock in a Fast Read command byte: 0 0 0 1 0 0 0 0 0 (opcode = 0x10).
   - Clock in the address of accessed register (0x12).
   - Clock out bytes until bit 0 or bit 1 = 1 : 0 0 0 0 0 0 0 1 (RACK bit 0 = 1).
   - Clock out first data byte: 0 0 0 0 0 0 0 0 (byte 0: bit 7 to bit 0).
   - Clock out next data (in this case, last) byte: 0 0 0 0 1 1 1 0 (byte 1: bit 15 to bit 8).

- [Continue if more bytes].
- Deassert SS while SCK is high idle state.

Figure 29: Fast Read to Read the Register



Note: There is an errata on the RACK output timing in Fast Read mode. The RACK (bit 0) must be sampled prior to toggling the clock to shift out the bit 0.

Normal Write Operation

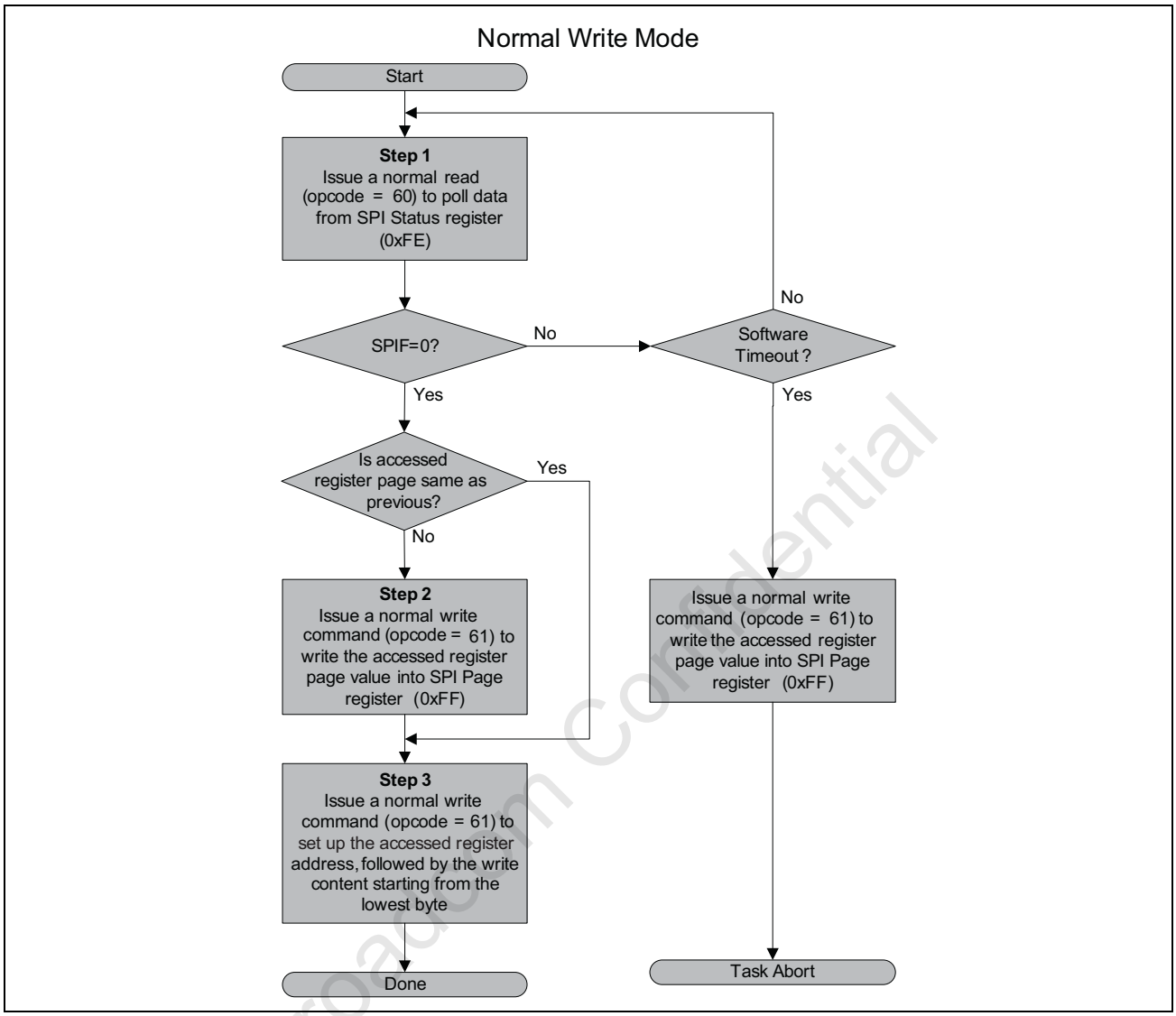
Normal write operation consists of 3 transactions (three SS operations):

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a normal write command (opcode = 0x61) to setup the accessed register page value into the page register (0xFF).
3. Issue a normal write command (opcode = 0x61) to setup the accessed register address value, followed by the write content starting from a lower byte.

The normal write Mode process is described in the following paragraphs with a flowchart followed by a step by step description.

Note: The RoboSwitch does not support Fast Write Mode.

Figure 30: Normal Write Operation

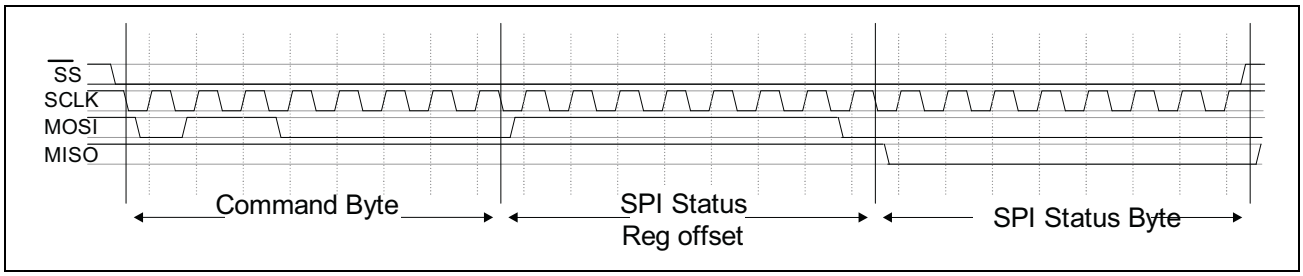


Example: 0x1600h is written to 1000BASE-T Control register (page 0x10, offset 0x12).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).

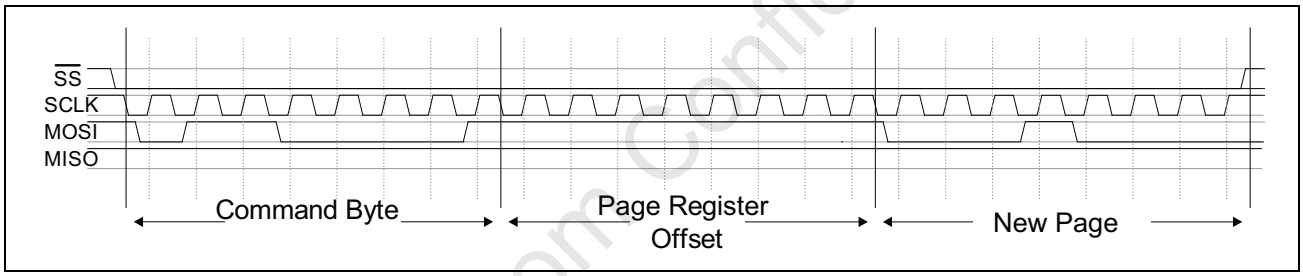
- Assert SS while SCK is high idle state.
- Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60).
- Clock in the SPI Status register address (0xFE).
- Clock in the accessed register page value,: 0 0 0 0 0 0 0 0 (SPIF bit 7 = 0).
- Deassert SS while SCK is high idle state.

Figure 31: Normal Read Mode to Check the SPIF Bit of SPI Status Register



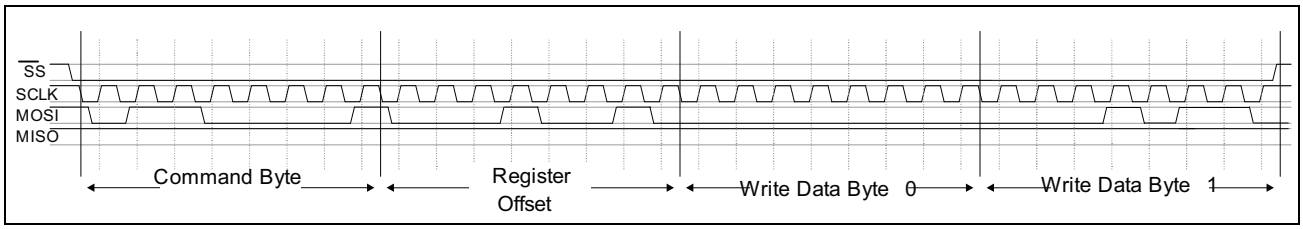
2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into SPI Page register (0xFF)—this step is required only if previous read/write was not from/to Page 0x10.
   - Assert SS while SCK is high idle state.
   - Clock in a normal write command byte: 0 1 1 0 0 0 0 1 (opcode = 0x61).
   - Clock in offset of Page register (0xFF).
   - Clock in 1 byte of the accessed register page value (Page register 0x10).
   - Deassert SS while SCK is high idle state.

Figure 32: Normal Write to Setup the Register Page Value



3. Issue a normal write command (opcode = 0x61) and write the Address of the accessed register followed by the write content starting from a lower byte.
   - Assert SS while SCK is high idle state.
   - Clock in a normal write command byte: 0 1 1 0 0 0 0 1 (opcode = 0x61).
   - Clock in offset of address of accessed register (0x12).
   - Clock in lower data byte first: 0 0 0 0 0 0 0 0 (byte 0: bit 7 to bit 0).
   - Clock in upper data byte next: 0 0 0 1 0 1 1 0 (byte 1: bit 15 to bit 8).
   - [Continue if more bytes].
   - Deassert SS while SCK is high idle state.

Figure 33: Normal Write to Write the Register Address Followed by Written Data

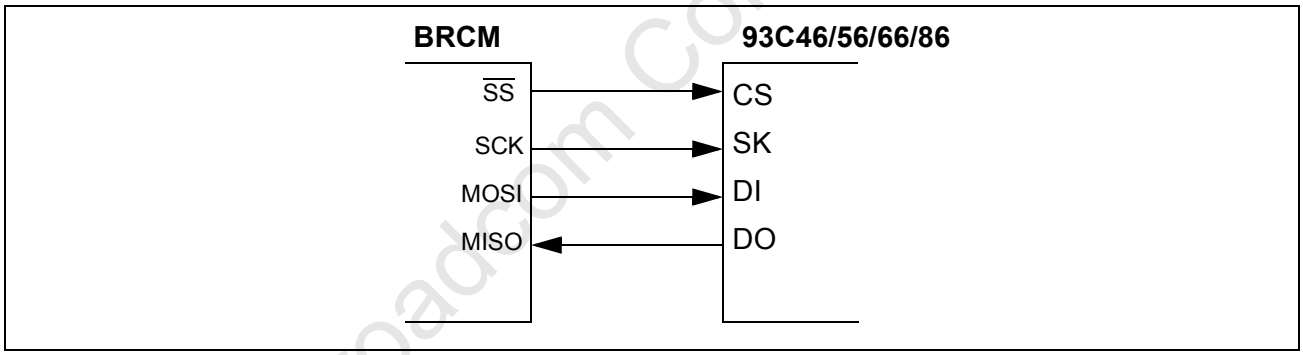


EEPROM Interface

The BCM53125S can be connected using the serial interface to a low-cost external serial EEPROM, enabling it to download register-programming instructions during power-on initialization. For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

During the chip-initialization phase, the switch identifies automatically the type of EEPROM it is connected to, then the data is sequentially read-in from the EEPROM after the internal memory has been cleared. The first data read-in is the HEADER and it matches a predefined magic code. In the case where the HEADER data does not match the instruction fetch, the process stops, and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the HEADER.

Figure 34: Serial EEPROM Connection



EEPROM Format

The EEPROM should be configured to x16 word format. The header contains key and length information as shown in Table 26 on page 110. The actual data stored in the EEPROM is byte-swapped as shown in Table 27 on page 110.

- Upper 5 bits are magic code 15h, which indicates that valid data follows.
- Bit 10 is for speed indication. A 0 means normal speed. A 1 indicates speedup. The default is 0.
- Lower 10 bits indicate the total length of all entries. For example:
- 93C46 up to 64 words
- 93C56 up to 128 words
- 93C66 up to 256 words
- 93C86 up to 1024 words

Table 26: EEPROM Header Format

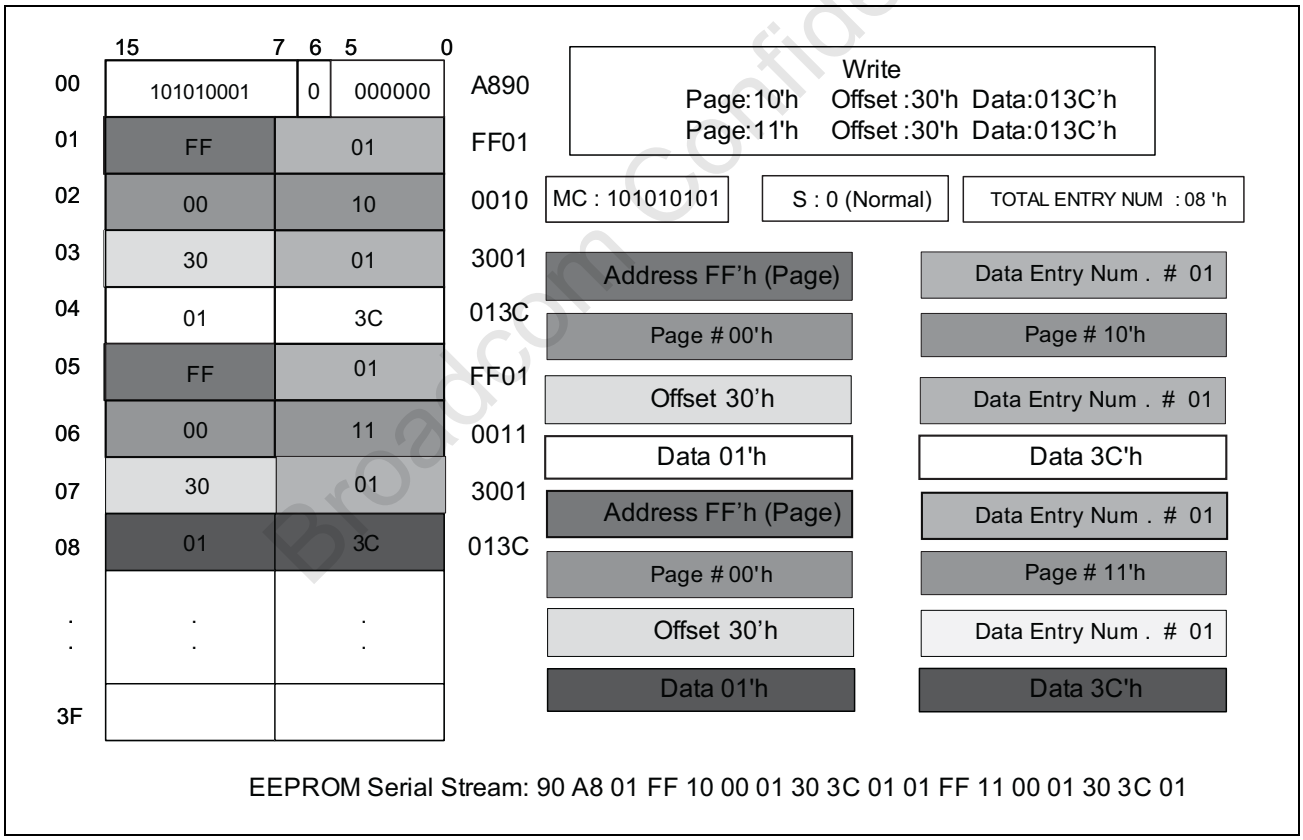
Bits [15:11}	*Bit 10*	*Bits [9:0]*
Magic code, 15h	Speed	Total entry number 93C46 = 0–63 93C56 = 0–127 93C66 = 0–255 93C86 = 0–1023

Table 27: EEPROM Contents

Bits [7:0]	*Bits [15:11]*	*Bit 10*	*Bits [9:8]*
Total entry number	Magic code, 15h	Speed	Total entry number

Figure 35 on page 110 shows an EEPROM programming example.

Figure 35: EEPROM Programming Example



Serial Flash Interface

The BCM53125S offers a serial flash interface to store program code for the internal microcontroller (BCM8051 processor). The BCM53125S detects a flash memory device automatically and downloads the memory contents upon power-up. The main purpose of the stored code is to configure and run the power savings mode, such as Green mode or any application that the user wishes to run that can fit in the internal BCM8051 memory. The embedded BCM8051 microcontroller has 32 KB of SRAM and 16 KB of ROM. The interface comprises four signal pins: chip select (FCS), Flash clock (FCLK), Flash serial out (FSO), and Flash serial in (FSI).

MDC/MDIO Interface

The BCM53125S offers an MDC/MDIO interface for accessing the switch registers as well as the PHY registers. An external management entity can access the switch registers through this interface when the SPI interface is not used. (i.e., when the SPI clock is in idle mode.) The switch registers are accessed through the Pseudo PHY interface, and the PHY registers are accessed directly by using PHY addresses.

An external PHY can be connected to the GMII interface of the IMP port and Port 5. Through the SPI interface, by accessing the Page 88h and Page 85h, the external PHY MII registers can be accessed.

Note: The PHY registers are not accessible through the Pseudo PHY operation.

MDC/MDIO Interface Register Programming

The BCM53125S are designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MDC pin of the BCM53125S sources a 2.5 MHz clock. Serial bidirectional data transmitted using the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction is initiated by the BCM53125S and contains the following:

- Preamble (PRE). To signal the beginning of an MII instruction after reset, at least 32 consecutive 1-bits must be written to the MDIO pin. A preamble of 32 1-bits is required only for the first read or write following reset. A preamble of fewer than 32 1-bits causes the remainder of the instruction to be ignored.
- Start of Frame (ST). A 01 pattern indicates that the start of the instruction follows.
- Operation Code (OP). A read instruction is indicated by 10, while a write instruction is indicated by 01.
- PHY Address (PHYAD). A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- Register Address (REGAD). A 5-bit register address follows, with the MSB transmitted first.
- Turnaround (TA). The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM53125S chip during these two bit times. When a read operation is being performed, the MDIO pin of the BCM53125S must be put in a high-impedance state during these bit times. The external PHY drives the MDIO pin to 0 during the second bit time.
- Data. The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM53125S. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

Pseudo-PHY

The MDC/MDIO can be used by an external management entity to read/write register values internal to the BCM53125S. This mode offers an alternative programming interface to the chip. The BCM53125S operate in slave mode with a PHY address of 30d. The following figures show the register setup flow chart for accessing the registers using the MDC/MDIO interface.

Figure 36: Pseudo-PHY MII Register Definitions

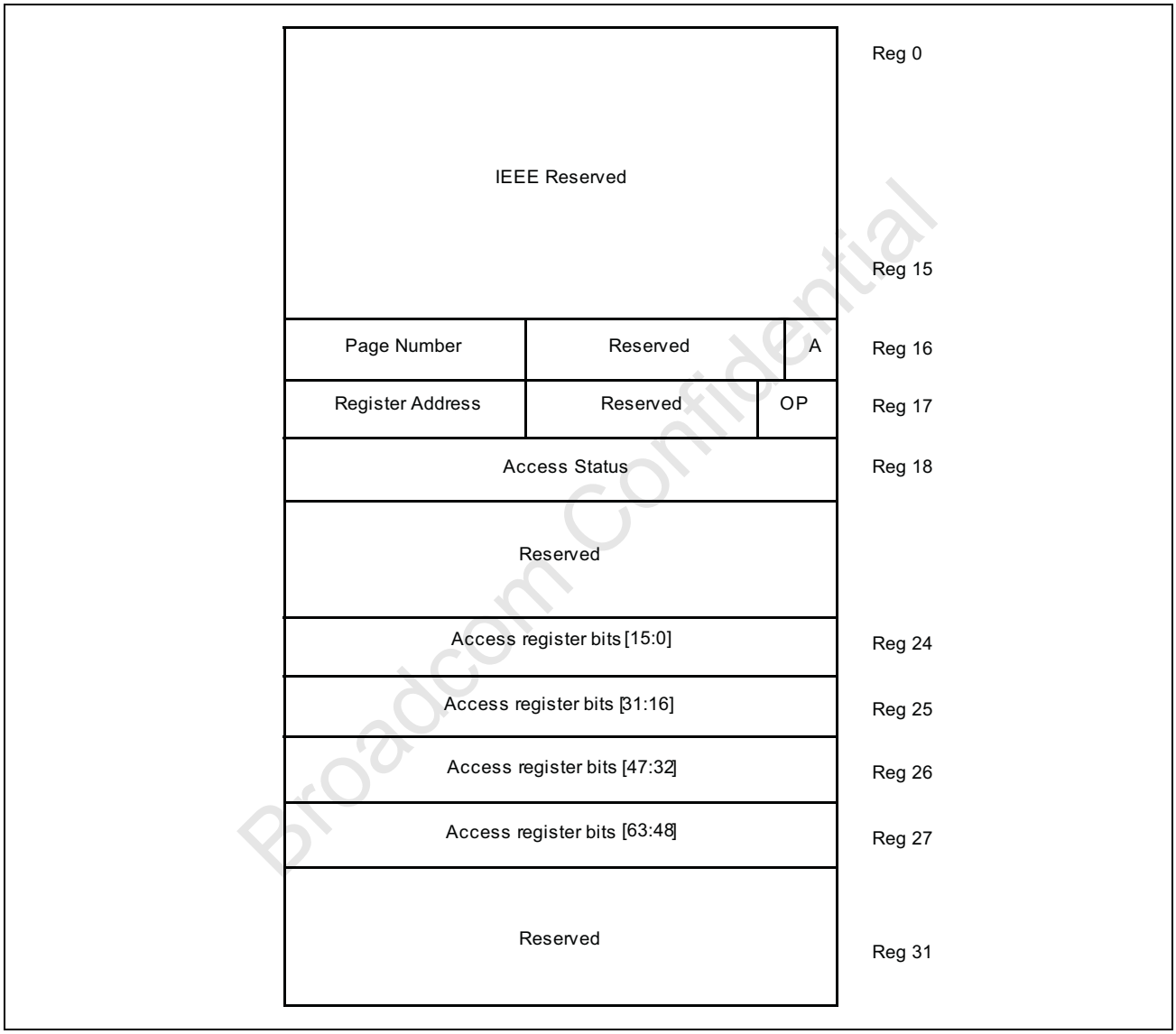
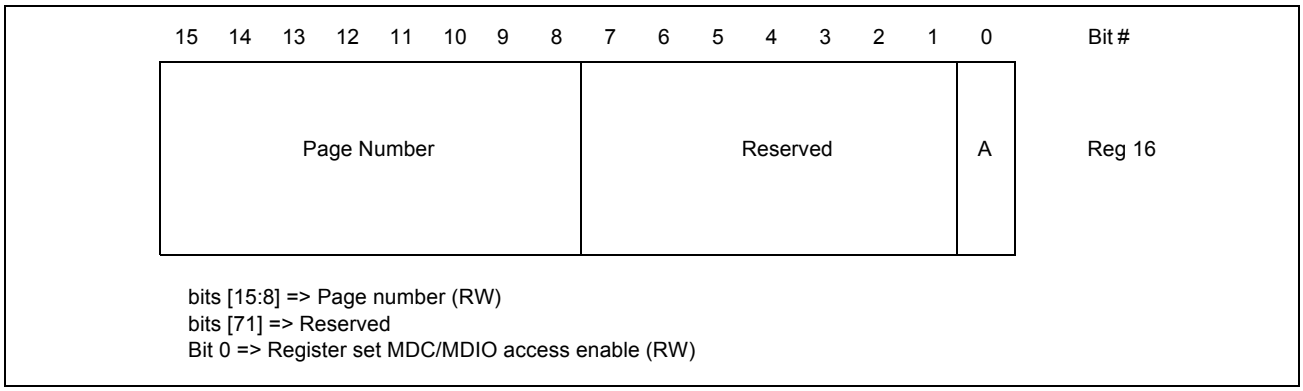


Figure 37: Pseudo-PHY MII Register 16: Register Set Access Control Bit Definition



Note: The bit 0 (MDC/MDIO Access Enable) in register 16 should be released (set to 0) after a transaction is completed. This allows the SPI interface to access the switch register if required.

Figure 38: Pseudo-PHY MII Register 17: Register Set Read/Write Control Bit Definition

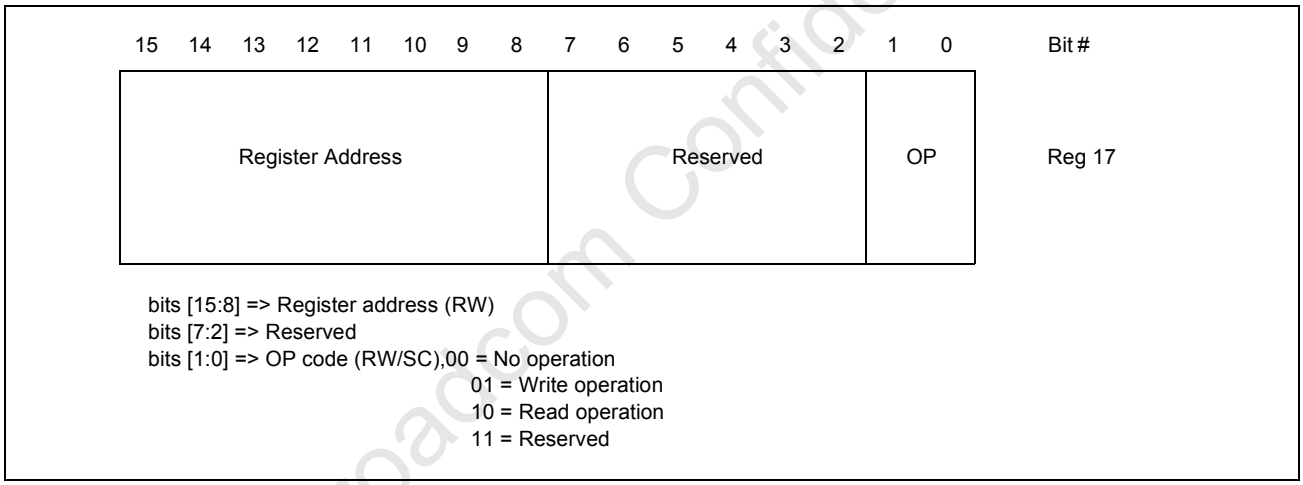


Figure 39: Pseudo-PHY MII Register 18: Register Access Status Bit Definition

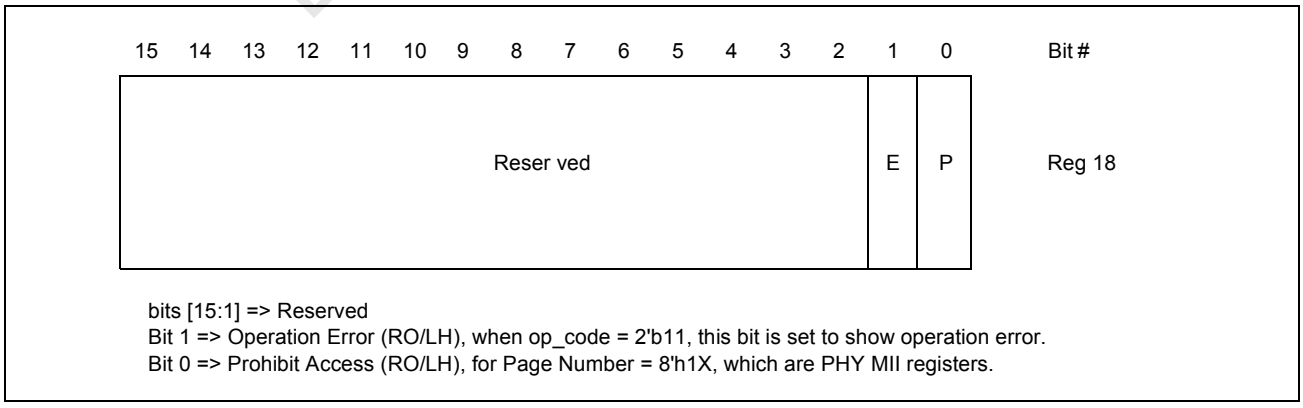


Figure 40: Pseudo-PHY MII Register 24: Access Register Bit Definition

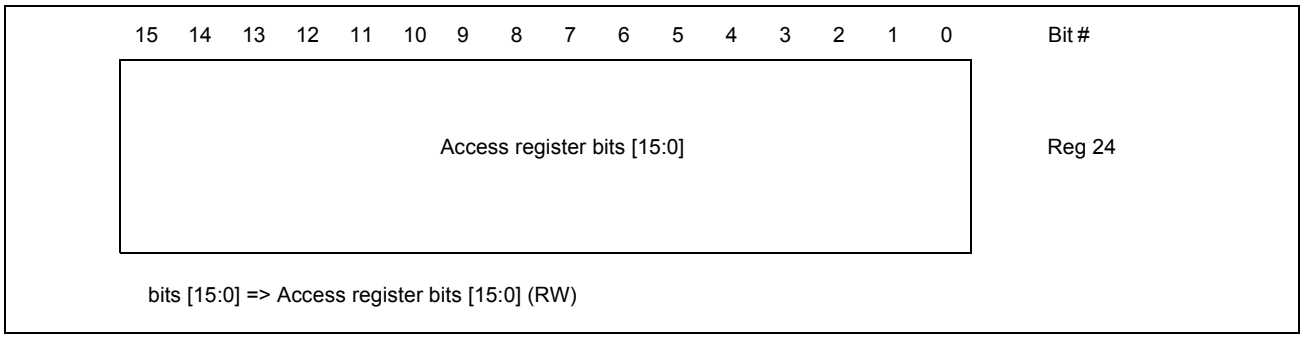


Figure 41: Pseudo-PHY MII Register 25: Access Register Bit Definition

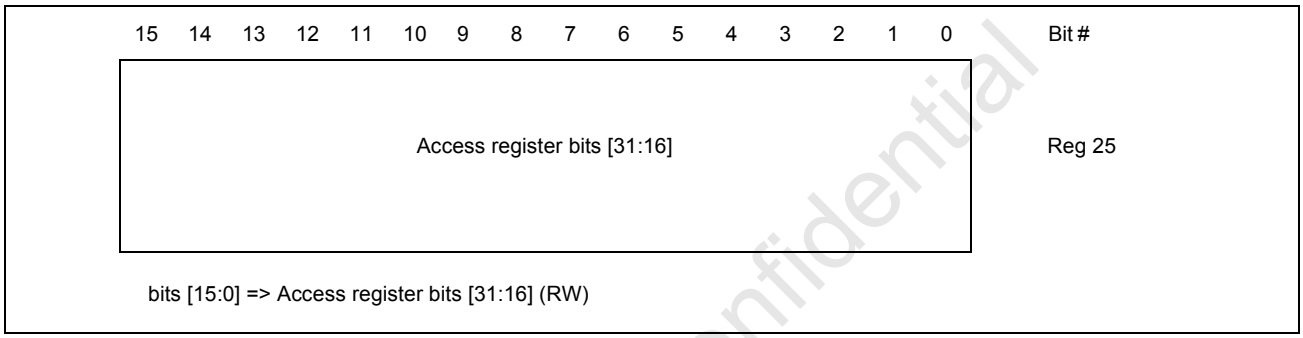


Figure 42: Pseudo-PHY MII Register 26: Access Register Bit Definition

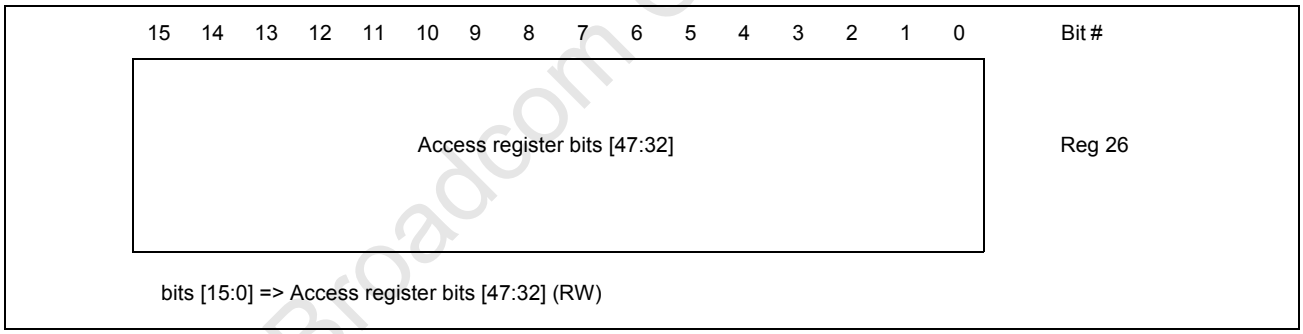


Figure 43: Pseudo-PHY MII Register 27: Access Register Bit Definition

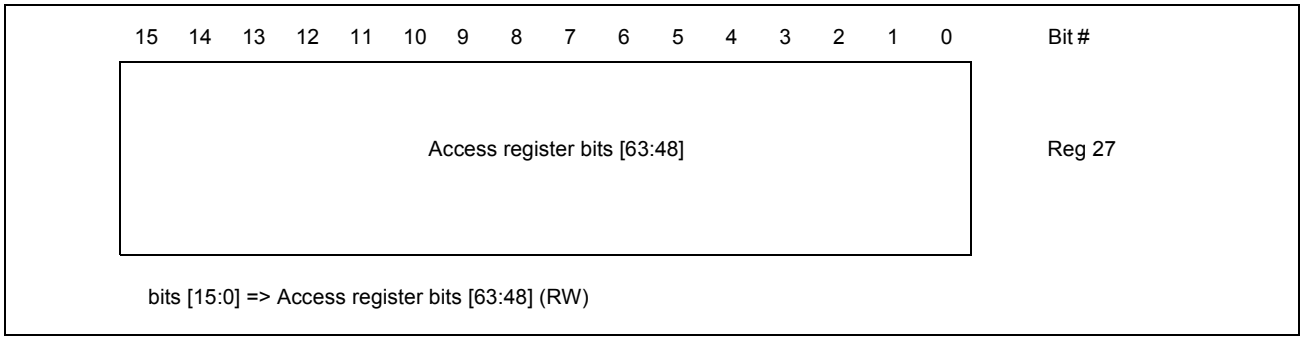


Figure 44: Read Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

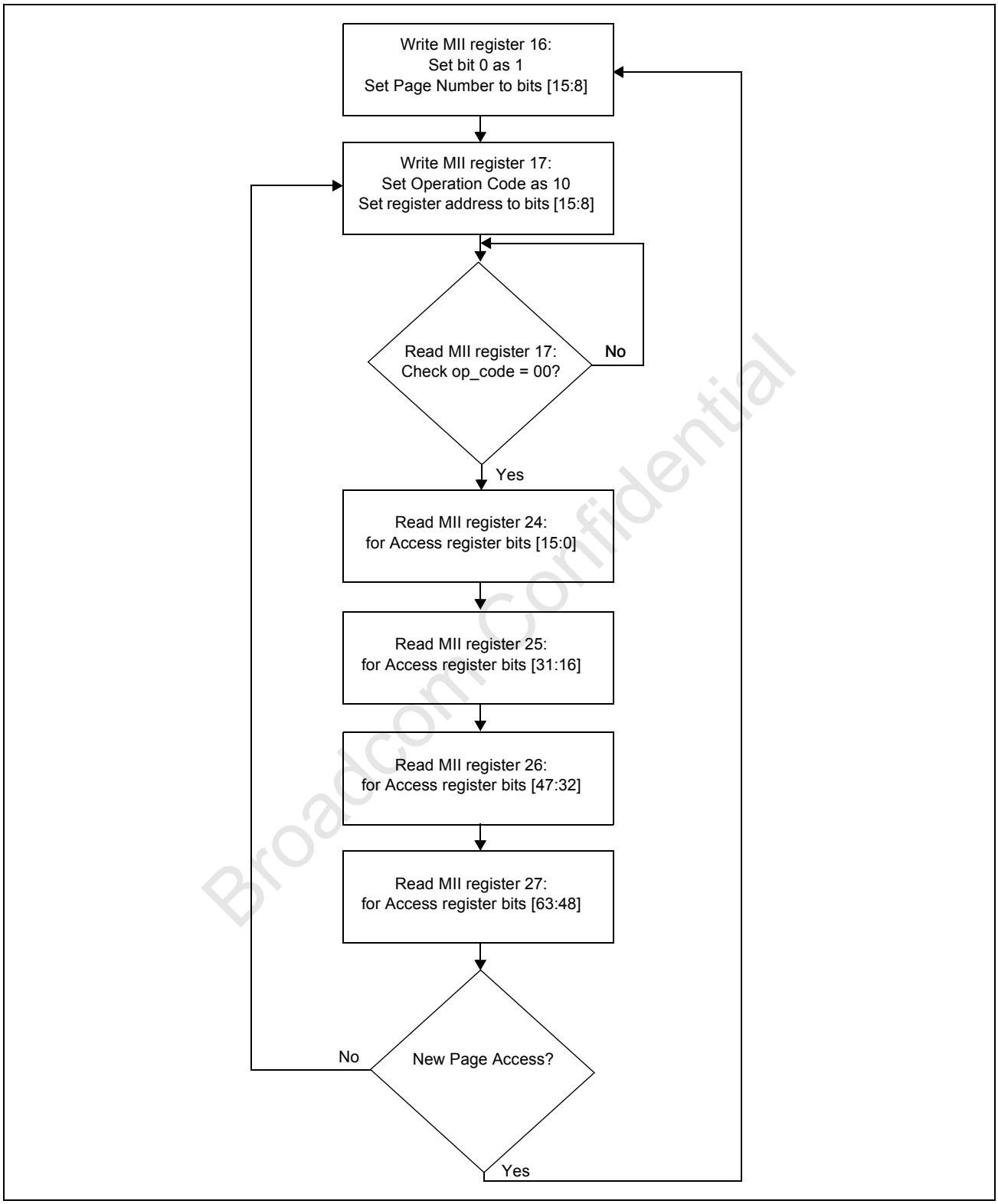


Figure 45: Write Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

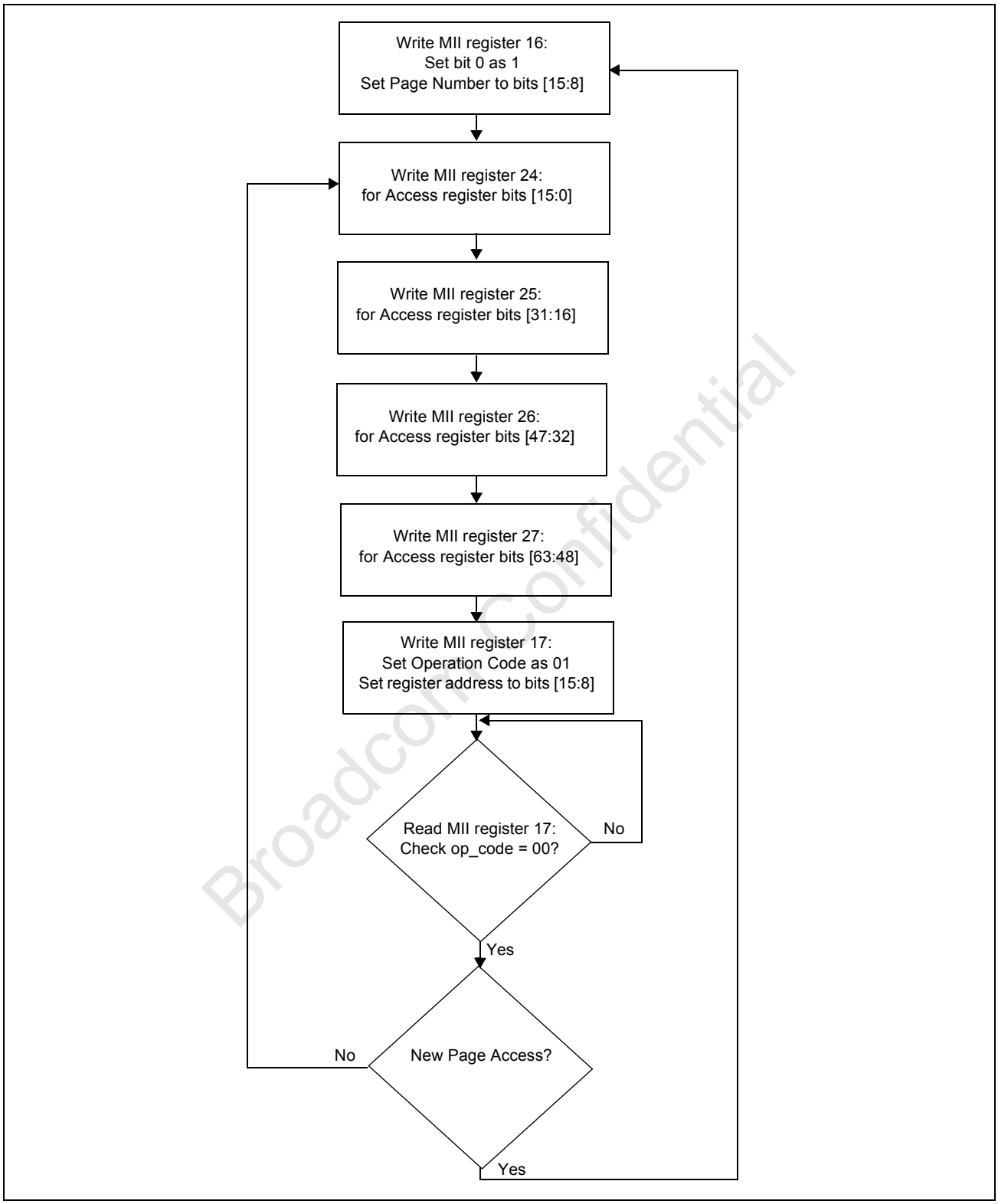


Table 28 summarizes the complete management frame format.

Table 28: MII Management Frame Format

Operation	PRE	ST	OP	PHYAD	REGAD	TA	Data	Direction
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ	Z ... Z	Driven by master
						Z0	D ... D	Driven by slave
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to master

See "MDC/MDIO Interface" on page 111 for more information regarding the timing requirements.

LED Interfaces

The BCM53125S provides flexible programmable per-port status of various functions. The user can select predefined LED displays per port by setting the LED_MODE strap pins, or the user can program different display functions for different ports by programming the LED Control registers. When the GMII (port 5) port is not used, the BCM53125S offers a total of 20 LED displays, four functions per port. When the GMII interface is used, the BCM53125S offers a total of 10 LED displays, two functions per port. The LED interface offers options to display different functions.

The following options are available for the LED display:

- Number of displays per port based on the GMII_LED_SEL strap pin option
- GMII_LED_SEL = 1: Total of 20 LED displays, four display functions per port
- GMII_LED_SEL = 0: Total of 10 LED displays, two display functions per port

Note: This mode is forced when the GMII (port 5) is used for the data interface.

When the GMII (port 5) is used, the 20 LED display option is not available.

The LED[xx] signal allocation for each port is shown in Table 29 and Table 30 on page 118.

- Different function displays per port
- Default display settings using strap pins LED_MODE[1:0]

  The different display-per-LED_MODE settings are shown in Table 29 and Table 30 on page 118. Each LED[xx] signal is assigned to a specific port. For example, if port 4, port 3, and port 2 LED displays are disabled (register page 00h, address 16h = 0003), port 0 and port 1 LED display are still from LED pins LED[16:19] (port 0), LED[12:15] (port 1), just as if all five ports were used. If port 1 and port 0 LED displays are disabled (register page 00h, address 16h = 001C), port 2, port 3, and port 4 are still from LED pins LED[8:11] (port 2), LED[4:7] (port 3), and LED[0:3] (port 4), again as if all five ports were used.

  All ports display the same set of functions based on the strap pin settings. The display is fixed per port and per pin as shown in Table 29 and Table 30 on page 118.

- Displaying one of two different display settings by programming the LED configuration registers

  Enable LED display per port using register page 00h, address 16h).

  Two sets of display options can be set using the LED Function Control register 0 and 1 (register page 00h, address 10h, and 12h).

Each port can select one of two display functions (register page 00h, address 14h).

Note: Refer to 53125-AN100-R, *Layout and Design Guidelines*, for a more detailed description of how to program LED-related registers.

- Different LED lighting behavior (register page 00h, address 18h, and 1Ah)
- Automatic mode: All mode indicators are in steady state, except for the activity indicator, which is blinking.
- Blink mode: All status indicators are blinking. The blinking rate can be set using register page 00h, address 0Fh, bit [2:0].
- ON mode: Forces the LED to be on

The status of enabled ports is sent out from a higher port number to the lowest port number. The output order in the shift-out is from LED[0], LED[1], LED[2], …LED[19]. The output port order for LED is from high port number to low port number, and the output bit order within the port LED is from MSB to LSB.

Table 29: 20 LED Display Mode (GMII_LED_SEL=1)

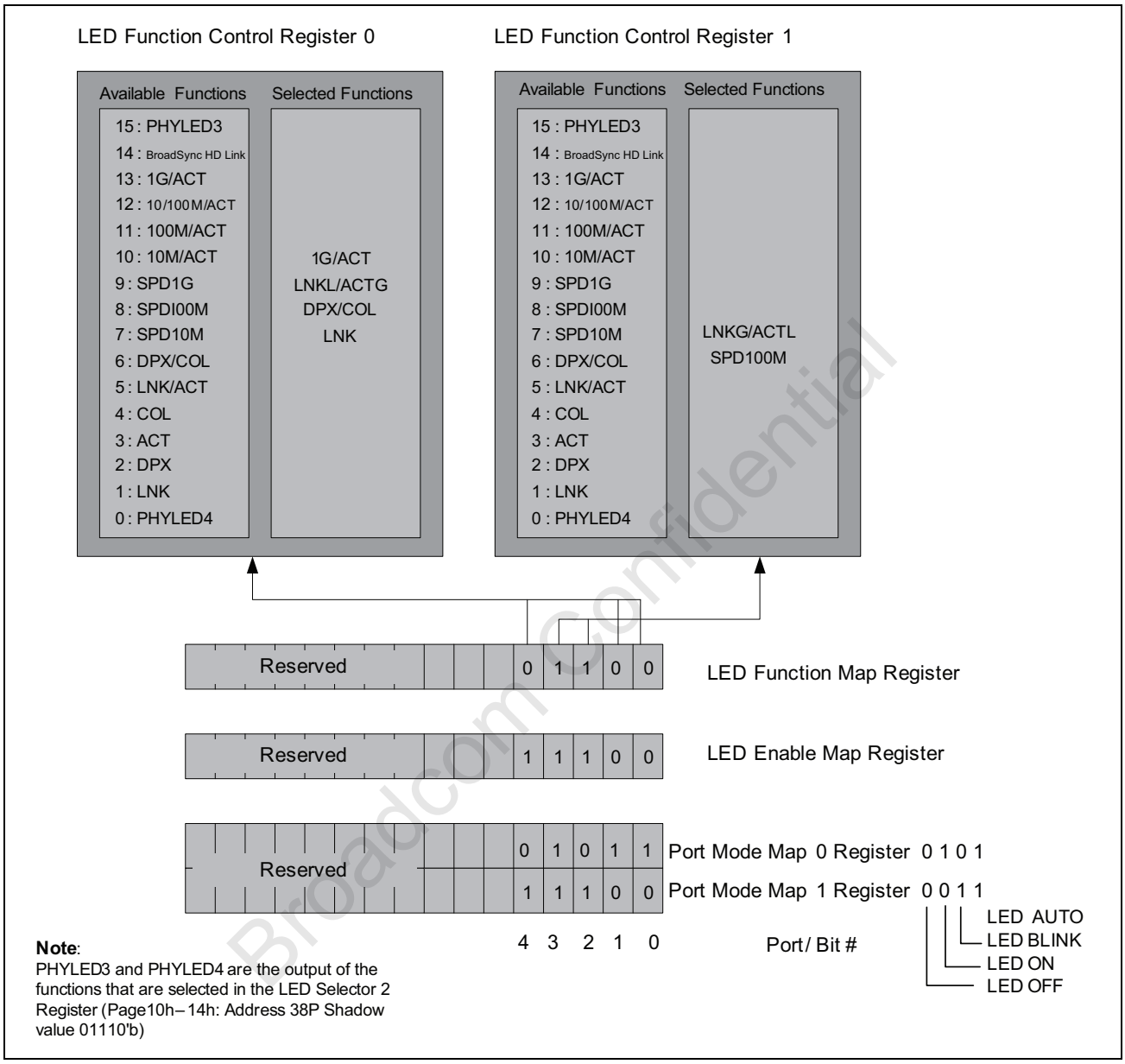
Port					***LED_Function Reg 1 (Default)***			
0	***1***	***2***	***3***	***4***	***'b11***	***'b10***	***'b01***	
LED[16]	LED[12]	LED[08]	LED[04]	LED[00]	1G/ACT	SPD1G	1G/ACT	SPD1G
LED[17]	LED[13]	LED[09]	LED[05]	LED[01]	100M/ACT	SPD100M	10_100/ACT	SPD100M
LED[18]	LED[14]	LED[10]	LED[06]	LED[02]	10M/ACT	LNK/ACT	DPX/COL	LNK/ACT
LED[19]	LED[15]	LED[11]	LED[07]	LED[03]	DPX	DPX	PHYLED4	PHYLED4

Table 30: 10 LED Display Mode (GMII_LED_SEL=0)

Port					***LED_Function Reg 1 (Default)***			
0	***1***	***2***	***3***	***4***	***'b11***	***'b10***	***'b01***	***'b00***
LED[08]	LED[06]	LED[04]	LED[02]	LED[00]	1G/ACT	SPD1G	1G/ACT	SPD1G
LED[09]	LED[07]	LED[05]	LED[03]	LED[01]	100M/ACT	SPD100M	10/100M/ACT	SPD100M

Figure 46 shows the LED Interface register structure.

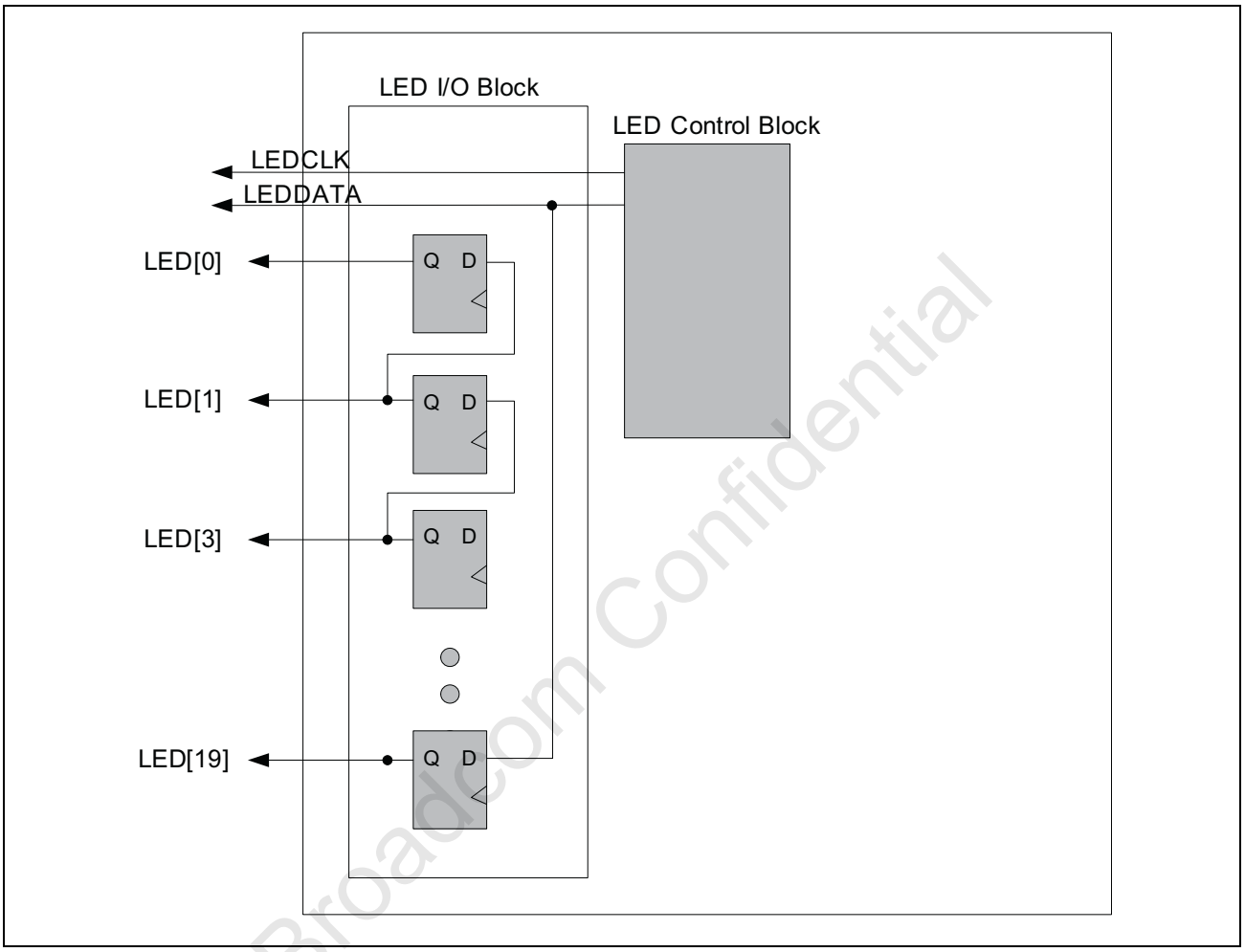
Figure 46: LED Interface Register Structure Diagram



The BCM53125S offer two LED Interfaces, parallel LED interface and serial interface. As shown in Figure 47, the source of LED status stream is the same for both interfaces; the status bit stream is based on the programmed register settings. The Parallel LED Interface provides all the shifting and storing of the status internally, so that it does not require any external shift registers, but it requires more I/O pins to be connected on the part. The active level of the LED DATA signal can be low or high depending on the strap pin configuration of the each LED signal in the parallel LED interface output. The determination of the active state is shown in "Dual-Input Configuration/LED Output Function" on page 121.

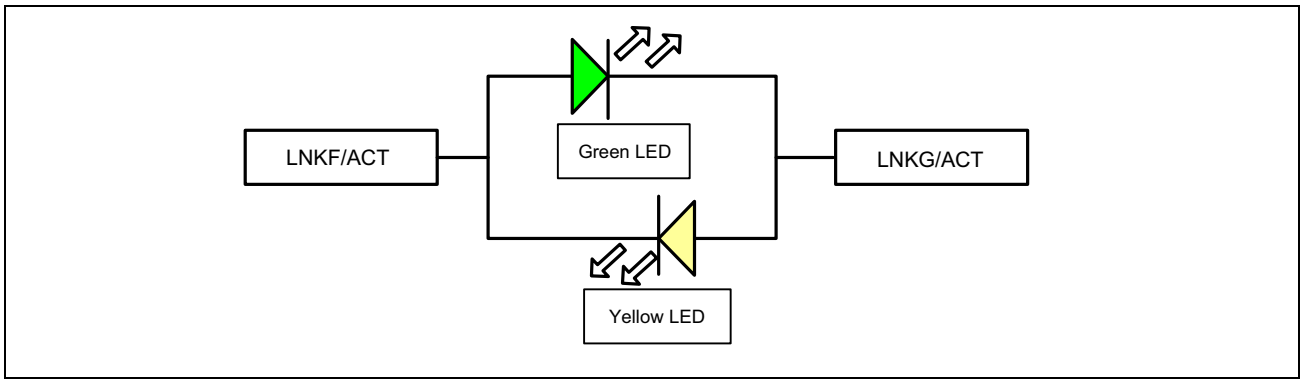
The serial LED interface is being output through two pins (LEDDATA, LEDCLK). This approach minimizes the number of I/O pins but requires the user to design using the external shift registers. The serial LED interface provides the LED display of ports 0–5. The active level of the LEDDATA signal is low for all status in the serial LED interface output.

Figure 47: LED Interface Block Diagram



Dual LED is used for displaying more than one status using one LED cell. By packing two different colors LED into one holder, dual LED can display more than two states in one cell. Figure 48 shows a typical dual LED usage. Green LED is to display LNKG/ACT status, while Yellow LED is to display LNKF/ACT status.

Figure 48: Dual LED Usage Example



Dual-Input Configuration/LED Output Function

There are 10 LED pins that have secondary functions. These pins serve as input pins during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active-low. The user must first decide, based on the individual application, the values of the input configuration pin shown in Table 31 to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or active-high LED output.

Table 31: Dual Input Configuration/LED Output Function

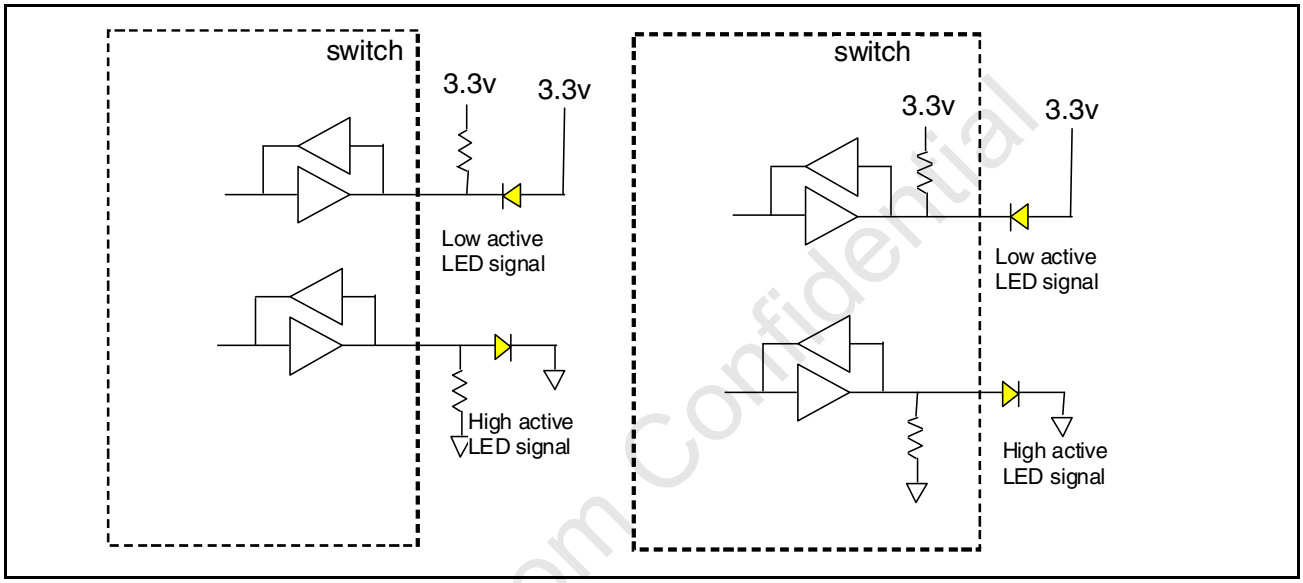
LED Output Pins	*Input Configuration Pins*	*Internal Default Pull Up/Down*	*Active State*
LED [0]	MII_DUMB_FWDG_EN	Pull up	Opposite of strap pin state.
LED [1]	No configuration	Pull up	Active low.
LED [2]	LED_MODE[1]	Pull up	Opposite of strap pin state.
LED [3]	SYSFREQ[1]	Pull up	Opposite of strap pin state.
LED [4]	GMII_MODE[0]	Pull up	Opposite of strap pin state.
LED [5]	GMII_MODE[1]	Pull up	Opposite of strap pin state.
LED [6]	IMP_MODE[0]	Pull up	Opposite of strap pin state.
LED [7]	IMP_MODE[1]	Pull up	Opposite of strap pin state.
LED [8]	CPU_EEPROM_SEL	Pull up	Opposite of strap pin state.
LED [9]	HW_FWDG_EN	Pull up	Opposite of strap pin state.
LED [10]	GMII_RXD[0]	Pull down	LED Active state is always low.
LED [11]	GMII_RXD[1]	Pull down	LED Active state is always low.
LED [12]	GMII_RXD[2]	Pull down	LED Active state is always low.
LED [13]	GMII_RXD[3]	Pull down	LED Active state is always low.
LED [14]	GMII_RXD[4]	Pull down	LED Active state is always low.
LED [15]	GMII_RXD[5]	Pull down	LED Active state is always low.
LED [16]	GMII_RXD[6]	Pull down	LED Active state is always low.

Table 31: Dual Input Configuration/LED Output Function (Cont.)

LED Output Pins	*Input Configuration Pins*	*Internal Default Pull Up/Down*	*Active State*
LED [17]	GMII_RXD[7]	Pull down	LED Active state is always low.
LED [18]	GMII_RXDV	Pull down	LED Active state is always low.
LED [19]	GMII_RXER	Pull down	LED Active state is always low.

Note: For LEDs whose active state is “opposite of strap pin state,” if the signal is pulled up/down, the LED is active low/high.

Figure 49: Dual Input Configuration/LED Output Function



Note: When LED signal pins are pulled up or down through an external or an internal termination due to the strap pin configuration, the active states of LED signals are:

- If the signal is pulled up, the LED is active low.
- If the signal is pulled low, the LED is active high.

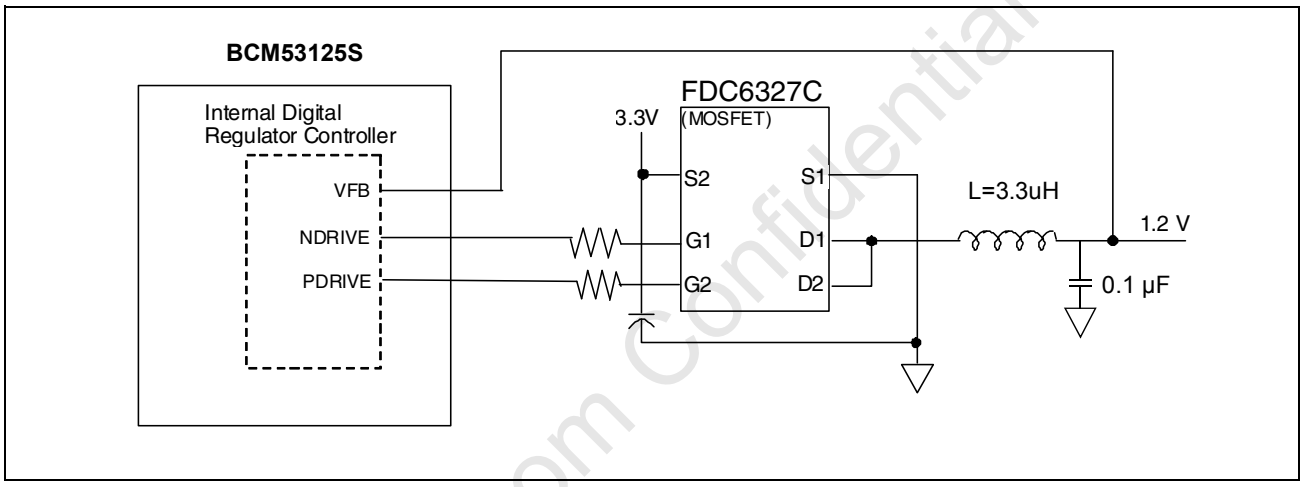
Internal Digital Regulator Controller

The BCM53125S has an Internal Digital Regulator Controller. You can use Regulator Controller to control an external regulator to generate 1.2V power supply. This feature can help to avoid extra circuitry required to generate 1.2V power supply if only required by the BCM53125S in the system. The internal digital regulator block involves three I/O signals. All other necessary signals are internally connected.

- NDRIVE: External NMOS gate control
- PDRIVE: External PMOS gate control
- VFB: External target voltage feedback

Figure 50 on page 123 shows how these signals can be used to generate a 1.2V power supply.

Figure 50: Internal Digital Regulator Controller



Section 5: Hardware Signal Definition Table

I/O Signal Types

The following conventions are used to identify the I/O types shown in the following table. The I/O pin type is useful in referencing the DC-pin characteristics.

Table 32: I/O Signal Type Definitions

Abbreviation	*Description*
XYZ	Active low signal
3T	3.3V tolerant
A	Analog pin type
B	Bias pin type
CS	Continuously sampled
D	Digital pin type
DNC	Do not connect
GND	Ground
I	Input
I/O	Bidirectional
IPU	Input with internal pull-up
O_{3S}	Tristated Signal
O_{DO}	Open-drain output
O	Output
PD	Internal pull-down
SOR	Sample on reset
PWR	Power pin supply
PU	Internal pull-up
XT	Crystal pin type

Signal Descriptions

Table 33: Signal Descriptions

Signal Name	Type	Description
PHY Interface		
TRD0_0±	–	**Transmit/Receive Pairs. In TRD [pair number]_[port number]± 1000BASE-T mode, differential data from the media is transmitted and received on all four signal pairs. In auto-negotiation and 10BASE-T and 100BASE-TX modes, the BCM53125S normally transmits on TRD[0]_[port number]± and receives on TRD[1]_{port number}±. Auto-MDIX operation can reverse the pairs TRD[0]_{4:0}± and TRD[1]_{4:0}±.**
TRD1_0±	–	
TRD2_0±	–	
TRD3_0±	–	
TRD0_1±	–	
TRD1_1±	–	
TRD2_1±	–	
TRD3_1±	–	
TRD0_2±	–	
TRD1_2±	–	
TRD2_2±	–	
TRD3_2±	–	
TRD0_3±	–	
TRD1_3±	–	
TRD2_3±	–	
TRD3_3±	–	
TRD0_4±	–	
TRD1_4±	–	
TRD2_4±	–	
TRD3_4±	–	
Clock/Reset		
RESET	I,Pu	**Hardware Reset Input.** Active low Schmitt-triggered input. Resets the BCM53125S.
XTALI	I,XT	**25 MHz Crystal Oscillator Input/Output.** A continuous 25 MHz reference clock must be supplied to the BCM53125S by connecting a 25 MHz crystal between these two pins or by driving XTALI with an external 25 MHz oscillator clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected. The maximum XTALI input voltage is 3.3V.
XTALO	O,XT	

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
IMP Interface		
IMP_TXCLK	I,O Pd	**MII/TMII Transmit Clock.** This is an input pin in MII mode, or GMII mode but speed is 100Mbps/10Mbps. It synchronizes the TXD[3:0] and connects to the PHY Entity TXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. In 200 Mbps mode (TMII), this is 50 MHz. **RvMII/RvTMII Receive Clock.** This is an output pin in RvMII mode. It synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/Management Entity RXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. This output pin has an internal 25Ω series termination resistor. In 200 Mbps mode (TMII), this is 50 MHz. This clock is not use in the other conditions.
IMP_TXD[0]	O,Pd	**GMII Transmit Data Output (first nibble).** Data bits TXD[3:0] are clocked on the rising edge of TXCLK. **RGMII Transmit Data Output.** For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mbps and 100 Mbps, data bits TXD[3:0] are clocked on the rising edge of TXCLK. **RvMII/RvTMII Receive Data Output.** Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/Management entity. **MII/TMII Transmit Data Output.** Clocked on the rising edge of TXCLK supplied by MAC/Management entity. These output pins have internal 25Ω series termination resistor.
IMP_TXD[1]	O,Pd	
IMP_TXD[2]	O,Pd	
IMP_TXD[3]	O,Pd	
IMP_TXD[4]	O,Pd	**GMII Transmit Data Output (second nibble).** Data bits [7:4] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω series termination resistor.
IMP_TXD[5]	O,Pd	
IMP_TXD[6]	O,Pd	
IMP_TXD[7]	O,Pd	
IMP_TXEN	I Pd	**GMII/MII/TMII Transmit Enable.** Active high. TXEN indicates the data on the TXD pins are encoded and transmitted. **RGMII Transmit Control.** On the rising edge of TXCLK, TXEN indicates that a transmit frame is in progress, and the data present on the TXD[3:0] output pins is valid. On the falling edge of TXCLK, TXEN is a derivative of GMII mode TXEN and TXER signals. **RvMII/RvTMII Receive Data Valid. Active high.** Connected to RXDV pin of MAC/Management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid. This output pin has an internal 25Ω series termination resistor.
IMP_TXER	O,Pd	**GMII/MII/TMII Transmit Error.** Active high. Asserting TXER when TXEN is high indicates a transmission error. TXER is also used to indicate Carrier Extension when operating in half-duplex mode. This output pin has an internal 25Ω series termination resistor.

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
IMP_RXCLK	I, Pd	**GMII Receive Clock.** 125 MHz for 1000 Mbps operation. **RGMII Receive Clock.** 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK. **MII Receive Clock.** 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. **TMII Receive Clock.** 50 MHz for 200 Mbps operation.
	O	**RvMII/RvTMII Transmit Clock.** Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/Management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode. This output pin has an internal 25Ω series termination resistor. **RvMII Transmit Clock.** 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. **RvTMII Transmit Clock.** 50 MHz for 200 Mbps operation.
IMP_RXD[0]	I,Pd	**GMII Receive Data Inputs (first nibble).** Data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RGMII Receive Data Inputs.** For 1000 Mbps operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RvMII/RvTMII Transmit Data Inputs.** Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/Management entity. **MII/TMII Receive Data Input.** Data bits RXD[3:0] are clocked on the rising edge of RXCLK.
IMP_RXD[1]	I,Pd	
IMP_RXD[2]	I,Pd	
IMP_RXD[3]	I,Pd	
IMP_RXD[7:4]/	I,O,Pd	**GMII Receive Data Inputs (second nibble).** Data bits RXD[7:4] are clocked out on the rising edge of RXCLK.
IMP_RXDV	I,Pd	**GMII/MII/TMII Receive Data Valid.** Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid. **RGMII Receive Data Valid.** Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on the falling edge of RXCLK. **RvMII/RvTMII Transmit Enable.** Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/Management entity.
IMP_RXER	I,Pd	**GMII/MII/TMII Receive Error. Indicates an error during the receive frame.**
IMP_GTXCLK	O,Pd	**GMII Transmit Clock.** This clock is driven to synchronize the transmit data in 1000 Mbps speed in GMII mode. **RGMII Transmit Clock.** This clock is driven to synchronize the transmit data in RGMII mode(125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0]. IMP_GTXCLK is used in RGMII and 1000 Mbps speed in GMII mode. IMP_TXCLK is used for MII mode, and 10/100 Mbps speed in GMII mode. This output pin has an internal 25Ω series termination resistor.

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
IMP_VOL_SEL[1]	I,Pd	**IMP_VOL_SEL[1] is used to set the voltage level of the IMP port (port 8) RGMII interface.** 0 = 2.5V (default) 1 = 1.5V ***Note:*** IMP_VOL_SEL signal is to set the voltage level of the IMP port (port 8) RGMII interface.
GMII_GTXCLK/NC	O,Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII Transmit Clock.** This clock is driven to synchronize the transmit data in 1000 Mbps speed in GMII mode. **RGMII Transmit Clock.** This clock is driven to synchronize the transmit data in RGMII mode (125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0]. • GMII_GTXCLK is used in RGMII and 1000 Mbps speed in GMII mode. • GMII_TXCLK is used for MII mode, and 10/100 Mbps speed in GMII mode. This output pin has an internal 25Ω series termination resistor. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** No connect.
GMII_TXCLK/NC	O,Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **MII/TMII Transmit Clock.** This is an input pin in MII mode, or GMII mode but speed is 100 Mbps/10 Mbps. It synchronizes the TXD[3:0] and connects to the PHY Entity TXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. **RvMII/RvTMII Receive Clock.** This is an output pin in RvMII mode. It synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/ Management Entity RXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. This output pin has an internal 25Ω series termination resistor, and in 200 Mbps mode (RvTMII), this is 50 MHz. This clock is not uses in the other conditions. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** No connect.
GMII_TXEN/NC	O,Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII/MII/TMII Transmit Enable.** Active high. TXEN indicates the data on the TXD pins are encoded and transmitted. **RvMII/RvTMII Receive Data Valid.** Active high. Connected to RXDV pin of MAC/Management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid. This output pin has an internal 25Ω series termination resistor. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** No connect.

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
GMII_TXER/NC/	I,O,Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII/MII/TMII Transmit Error.** Active high. Asserting TXER when TXEN is high indicates a transmission error. TXER is also used to indicate Carrier Extension when operating in half-duplex mode. This output pin has an internal 25Ω series termination resistor. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** No connect.
GMII_TXD[0]/NC	O,Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII Transmit Data Output (first nibble).** Data bits TXD[3:0] are clocked on the rising edge of TXCLK. **RGMII Transmit Data Output.** For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mbps and 100 Mbps, data bits TXD[3:0] are clocked on the rising edge of TXCLK. **RvMII/RvTMII Receive Data Output.** Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/Management entity. **MII/TMII Transmit Data Output.** Clocked on the rising edge of TXCLK supplied by MAC/Management entity. These output pins have internal 25Ω series termination resistor. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** No connect.
GMII_TXD[1]/NC	O,Pd	
GMII_TXD[2]/NC	O,Pd	
GMII_TXD[3]/NC	O,Pd	
GMII_TXD[4]/NC	O,Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII Transmit Data Output (second nibble).** Data bits [7:4] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω series termination resistor. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** No connect.
GMII_TXD[5]/NC	O,Pd	
GMII_TXD[6]/NC	O,Pd	
GMII_TXD[7]/NC	O,Pd	
GMII_RXCLK	I,Pd	**GMII Receive Clock.** 125 MHz for 1000 Mbps operation. **RGMII Receive Clock.** 125 MHz for 1000 Mbps operation, 25 MHz for 100Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK. **MII/TMII Receive Clock.** 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. 50 MHz input for 200 Mbps TMII operation.
	O	**RvMII/RvTMII Transmit Clock.** Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/Management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode. This output pin has an internal 25Ω series termination resistor and 50 MHz for 200 Mbps mode (RvTMII).

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
GMII_RXDV/LED[18]	I,O Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII/MII/TMII Receive Data Valid.** Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid. **RGMII Receive Data Valid.** Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on the falling edge of RXCLK. **RvMII/RvTMII Transmit Enable.** Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/Management entity. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** GMII_RXDV is used as LED[18]
GMII_RXER/LED[19]	I,O Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** GMII/MII/TMII Receive Error. Indicates an error during the receive frame. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** GMII_RXER is used as LED[19].
GMII_RXD[0]/LED[10]	I,O Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII Receive Data Inputs (first nibble).** Data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RGMII Receive Data Inputs.** For 1000 Mbps operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RvMII/RvTMII Transmit Data Inputs.** Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/Management entity. **MII/TMII Receive Data Input.** Data bits RXD[3:0] are clocked on the rising edge of RXCLK. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** **GMII_RXD[3:0] are used as LED[13:10].**
GMII_RXD[1]/LED[11]	I,O Pd	
GMII_RXD[2]/LED[12]	I,O Pd	
GMII_RXD[3]/LED[13]	I,O Pd	
GMII_RXD[4]/LED[14]	I,O Pd	**When GMII_LED_SEL =1b'0 (2 x PHY-less ports are used).** **GMII Receive Data Inputs (second nibble).** Data bits RXD[7:4] are clocked out on the rising edge of RXCLK. **When GMII_LED_SEL =1b'1 (1 x PHY-less port (IMP) is used).** GMII_RXD[7:4] are used as LED[17:14].
GMII_RXD[5]/LED[15]	I,O Pd	
GMII_RXD[6]/LED[16]	I,O Pd	
GMII_RXD[7]/LED[17]	I,O Pd	
RGMII_VOL_SEL[1]	Pd, SOR	**RGMII_VOL_SEL[1] is used to select RGMII Interface voltage.** 0 = 2.5V (default) 1 = 1.5V ***Note:*** RGMII_VOL_SEL signal is set to set the voltage level of the WAN port (port 5) RGMII interface.
GMII_LED_SEL	I,Pd	**Select signals to be selected for LED output, or WAN (GMII) interface.** Enable WAN port used as LED output. 1 = GMII interface signals of WAN port used as LED output 0 = Used as original WAN port (default)
MDC/MDIO Interface		

Table 33: Signal Descriptions (Cont.)

Signal Name	*Type*	*Description*
MDIO	I/O,Pd	**Management Data I/O.** In master mode, this serial input/output data signal is used to read from and write to the MII registers of the external transceivers. In slave mode, it is used by an external entity to read/write to the switch registers using the pseudo-PHY. See "MDC/MDIO Interface" on page 111 for more information.
MDC	I/O,Pd	**Management Data Clock.** In master mode, this 2.5 MHz clock sourced by BCM53125S to the external PHY device. In slave mode, it is sourced by an external entity.
Test Interface		
TCK	I,Pu	**JTAG Test Clock Input.** Clock Input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
TDI	I,Pu	**JTAG Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
TDO/EN_8051	O,Pu SOR	**JTAG Test Data Output.** **TDO is used for the strap pin for EN_8051.** Enable the embedded BCM8051 microcontroller. The embedded BCM8051 microcontroller is enabled by default. 0 = Disabled. 1 = Enable (default).
TMS	I,Pu	**JTAG Mode Select Input.**
TRST	I,Pd	**JTAG Test Reset**. Active low. Resets the JTAG controller. This signal must be pulled low during normal operation.

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
LED Interface		
LED[0]/ MII_DUMB_FWDG_EN	O,PuSOR	**Parallel LED Indicators.** • LED[19:0]: Five ports x 4 LEDs = 20 (exclude IMP) • LED[9:0]: Five ports x 2 LEDs = 10 (when port5(GMII port) is connected to an external entity.) LED[19:10] are used for GMII interface. **LED[0] is used for the strap pin for MII_DUMB_FWDG_EN.** IMP port in blocking state for managed mode. 0 = Blocking for managed mode 1 = Forwarding for dumb mode (unmanaged mode) When this pin is pulled up, the IMP port is not in management mode, the IMP port is in a regular port. No Broadcom header is required for ingress, and egress.
LED[1]	O,PuSOR	**LED[1] is not used for a configuration.**
LED[2]/LED_MODE[1]	O,PuSOR	**LED[2] is used for the strap pin for LED_MODE[1].** See detailed description for LEDCLK/LED_MODE[0] on the following page.
LED[3]/SYSFREQ[1]	O,PuSOR	**LED[3] is used for the strap pin for SYSFREQ[1].** See detailed description in LEDDATA//SYSFREQ[0] on the following page.
LED[4]/ GMII_MODE[0]	O,PuSOR	**LED[5:4] are used for the strap pin for GMII_MODE[1:0].** GMII Port mode. Sets the mode of the GMII port based on the value of the pins at power-on reset. 00 = RGMII mode 01 = MII/TMII mode 10 = RvMII/RvTMII mode 11 = GMII mode (default)
LED[5]/ GMII_MODE[1]	O,PuSOR	
LED[6]/IMP_MODE[0]	O,PuSOR	**LED[7:6] are used for the strap pin for IMP_MODE[1:0].** IMP Port mode. Sets the mode of the IMP port based on the value of the pins at power-on reset. 00 = RGMII mode 01 = MII/TMII mode 10 = RvMII/TMII mode 11 = GMII mode (default)
LED[7]/IMP_MODE[1]	O,PuSOR	
LED[8]/ CPU_EEPROM_SEL	O,PuSOR	**LED[8] is used for the strap pin for CPU_EEPROM_SEL.** CPU or EEPROM interface selection. • CPU_EEPROM_SEL = 0: Enable EEPROM interface • CPU_EEPROM_SEL = 1: Enable SPI Interface (default) The SPI interface must be selected (CPU_EEPROM_SEL=1) for Pseudo-PHY accesses through the MDC/MDIO Interface. See "Programming Interfaces" on page 94 for more information.
LED[9]/ HW_FWDG_EN	O,PuSOR	**LED[9] is used for the strap pin for HW_FWDG_EN.** Forwarding enable. Active high. • When this pin is pulled high (default) at power-up, traffic is forwarded without any register settings, based on default register settings. • When this pin is pulled low at power-up, frame forwarding is disabled. Traffic forwarding is enabled through Software Register bit set.
LED[19:10]: see GMII RXDV, GMII RXER, and GMII RXD signals	–	

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
LEDCLK/ LED_MODE[0]	O,Pd, SOR	**LEDCLK is LED Shift Clock.** This clock is periodically active to enable LEDDATA to shift into external registers.
LEDDATA// SYSFREQ[0]	O,Pd, SOR	**LEDDATA is Serial LED Data Output.** Serial LED data for all ports is shifted out when LEDCLK is active. LEDMODE[1:0] pins set the serial data content. See "LED Interfaces" on page 117 for a functional description of this signal. **LED[2] and LEDCLK are used for the strap pin for LED MODE[1:0].** Users can select predefined functions to be displayed for each port by setting the bits accordingly. ***Note:*** When GMII_LED_SEL =0, GMII port is connected to an external CPU entity, only 2 LED function displays are available. The functions in bold, italic fonts are the ones will be displayed when GMII_LED_SEL = 0. • When LED MODE[1:0] = 00: GbE Configuration SPD1G SPD100M LNK/ACT PHYLED4 • When LED MODE[1:0] = 01: GbE Configuration 1G/ACT 10/100M/ACT DPX/COL PHYLED4 • When LED MODE[1:0] = 10 (default): GbE Configuration SPD1G SPD100M LNK/ACT DPX • When LED MODE[1:0] = 11: FE Configuration / GbE Configuration 100M/ACT / 1G/ACT 10M/ACT / 100M/ACT DPX / 10M/ACT DPX **LED[3] and LEDDATA are used for the strap pin for SYS_FREQ[1:0].** System clock selection. Determines rate of system clock: 00 = 83 MHz 01 = 91 MHZ 10 = 100 MHz (normal operation) 11 = 111 MHz

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
Serial Flash Interface		
FCK	O,Pd	**Flash Memory Serial Clock.** The clock output for serial Flash memory.
FCS_B	I,Pd	**Flash Memory Chip Select.** Active low signal. Chip select to serial Flash memory device.
FSI	I,Pd	**Serial Data Input.** Serial data input from serial Flash memory.
FSO	O,Pd	**Serial Data Output.** Serial data output to drive serial Flash memory.
SPI/EEPROM Programming Interfaces		
SCK/SK	I,O Pd	**SPI Serial Clock.** The clock input to the BCM53125S SPI interface is supplied by the SPI master, which supports up to 25 MHz, and is enabled if CPU_EPROM_SEL is high during power-on reset. **EEPROM Serial Clock.** The clock output to an external EEPROM device, and is enabled if CPU_EPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 94 for more information.
SS/CS	I,O Pu	**SPI Slave Select.** Active low signal which enables an SPI interface read or write operation. Enable if CPU_EPROM_SEL is high during power-on reset. **EEPROM Chip Select.** Active high control signal that enables a read operation from an external EEPROM device. Enable if CPU_EPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 94 for more information.
MOSI/DI	I,O Pu	**SPI Master-Out/Slave-In.** Input signal which receives control and address information for the SPI interface, as well as serial data during write operations. Enabled if CPU_EPROM_SEL is high during power-on reset. **EEPROM Data In.** Serial data input to an external EEPROM device. Enabled if CPU_EPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 94 for more information.
MISO/DO/EN_EEE	I,O,Pu, SOR	**SPI Master-In/Slave-Out.** Output signal which transmits serial data during an SPI interface read operations. Enabled if CPU_EPROM_SEL is high during power-on reset. **EEPROM Data Out.** Serial data output to an external EEPROM device. Enable if CPU_EPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 94 for more information. **MISO is used for the strap pin for EN_EEE (Energy Efficient Ethernet).** Enable EEE feature for switch MAC: 1 = Enable (default) 0 = Disable
Interrupt Pin		
INT	O,Pu	**Interrupt.** This interrupt pin generates an interrupt based on the configuration in the Interrupt Enable register. It can be programmed to generate based on link status change of any port, or to generate an interrupt to a CPU entity when there is a packet(s) queued in the IMP transmit queue.
Bias		
QGPHY1_RDAC	–	A 1.24 kΩ resistor to GND is required.

Table 33: Signal Descriptions (Cont.)

Signal Name	Type	Description
QGPHY2_RDAC	–	A 1.24 kΩ resistor to GND is required.
EGPHY_RDAC	–	A 1.24K Ω resistor to GND is required.
Power Interfaces		
AVDDL	–	1.2V analog power, power ring 0.
OVDD	–	3.3/2.5/1.5V digital IMP port power, power ring 1.
OVDD3	–	3.3/2.5/1.5V digital WAN (port5) port power, power ring 2.
AVDDL	–	1.2V analog power, power ring 4.
OVDD2	–	3.3V digital I/O power, power ring 5.
AVDDH	–	3.3V analog I/O power.
DVDD	–	1.2V digital core power.
OTP_VDD	–	3.3V OTP power.
EGPHY_BVDD	–	3.3V bias power for GPHY.
QGPHY1_BVDD	–	3.3V bias power for GPHY.
QGPHY2_BVDD	–	3.3V bias power for GPHY.
EGPHY_PLLVDD	–	1.2V PLL power for GPHY.
SWREG_VDDO	–	3.3V regulator power.
XTAL_AVDD	–	3.3V XTAL power.
PLL_AVDD	–	1.2V system PLL power.
QGPHY1_PLLVDD	–	1.2V PLL power for GPHY.
QGPHY2_PLLVDD	–	1.2V PLL power for GPHY.
IMP_VOL_REF	–	• When 3.3V GMII interface is used, IMP_VOL_REF should be connected to VSSC (Ground). • When 2.5V RGMII interface is used, IMP_VOL_REF should be connected to VSSC (Ground). • When 1.5V RGMII interface is used, IMP_VOL_REF should be connected VDDO/2 which is 0.75V.
GMII_VOL_REF	–	• When 3.3V GMII interface is used, GMII_VOL_REF should be connected to VSSC (Ground). • When 2.5V RGMII interface is used, GMII_VOL_REF should be connected to VSSC (Ground). • When 1.5V RGMII interface is used, GMII_VOL_REF should be connected VDDO/2 which is 0.75V.
Internal Regulator Interface		
NDRIVE	O	NMOS gate signal.
PDRIVE	O	PMOS gate signal.
VFB	I	Output voltage feedback signal.

Section 6: Pin Assignment

Pin List by Pin Number

Pin	Signal
A03	NC
A05	TDP_2_2
A07	TDN_0_2
A09	QGPHY1_PLLVDD
A11	TDN_0_1
A13	TDP_2_1
A15	TDN_3_1
A17	EGPHY_PLLVDD
A19	TDN_0_0
A21	TDP_2_0
A23	TDN_3_0
A25	NC
A27	NC
AA01	DVDD
AA03	LED[4]/GMII_MODE[0]
AA27	GMII_TXCLK/NC
AA29	GMII_GTXCLK/NC
AB02	LED[5]/GMII_MODE[1]
AB05	LED[8]/CPU_EEPROM_SEL
AB25	GMII_TXD[1]/NC
AB28	GMII_TXD[4]/NC
AC01	LED[6]/IMP_MODE[0]
AC03	LED[7]/IMP_MODE[1]
AC27	GMII_TXD[5]/NC
AC29	GMII_TXD[0]/NC
AD02	LED[9]/HW_FWDG_EN
AD05	NC
AD17	PLL_AVDD
AD25	GMII_TXER/NC
AD28	GMII_TXD[6]/NC
AE01	MDC
AE03	MDIO
AE06	NC
AE08	AVDDH
AE10	AVDDH
AE12	QGPHY2_RDAC
AE14	AVDDH
AE18	DVDD
AE20	GMII_RXD[5]/LED[15]
AE22	GMII_RXER/LED[19]
AE24	GMII_VOL_REF
AE27	GMII_TXD[7]/NC
AE29	GMII_TXD[2]/NC
AF02	RESET
AF28	GMII_TXD[3]/NC
AG01	NC
AG05	NC
AG07	TDP_2_3
AG09	NC
AG11	QGPHY2_PLLVDD
AG13	TDN_1_4
AG15	AVDDH
AG17	NC
AG19	GMII_RXD[7]/LED[17]
AG21	GMII_RXD[6]/LED[16]
AG23	GMII_RXD[4]/LED[14]
AG25	DVDD
AG29	NC
AH04	TDP_3_3
AH06	TDN_2_3
AH08	TDN_1_3
AH10	TDP_0_3
AH12	TDP_0_4
AH14	TDP_1_4
AH16	TDN_2_4
AH18	TDP_3_4
AH20	GMII_RXD[3]/LED[13]
AH22	GMII_RXD[1]/LED[11]

Pin	Signal
AH24	GMII_RXCLK
AH26	NC
AJ03	NC
AJ05	TDN_3_3
AJ07	TDP_1_3
AJ09	TDN_0_3
AJ11	QGPHY2_BVDD
AJ13	TDN_0_4
AJ15	TDP_2_4
AJ17	TDN_3_4
AJ19	NC
AJ21	GMII_RXD[2]/LED[12]
AJ23	GMII_RXD[0]/LED[10]
AJ25	GMII_RXDV/LED[18]
AJ27	NC
B04	TDN_2_2
B06	TDP_1_2
B08	TDP_0_2
B10	QGPHY1_RDAC
B12	TDN_1_1
B14	TDN_2_1
B16	TDP_3_1
B18	TDP_0_0
B20	TDP_1_0
B22	TDN_2_0
B24	TDP_3_0
B26	NC
C01	NC
C03	TDP_3_2
C05	TDN_3_2
C07	TDN_1_2
C09	QGPHY1_BVDD
C11	TDP_0_1
C13	TDP_1_1
C15	EGPHY_BVDD
C17	NC
C19	TDN_1_0
C21	NC
C23	PDRIVE
C25	NDRIVE

Pin	Signal
C29	NC
D02	NC
D28	NC
E01	IMP_VOL_SEL[1]
E03	RGMII_VOL_SEL[1]
E08	AVDDH
E10	AVDDH
E12	NC
E14	AVDDH
E16	EGPHY_RDAC
E18	AVDDH
E20	DVDD
E22	NC
E27	IMP_TXD[4]
E29	IMP_TXD[0]
ePAD	PLL_VSS
ePAD	PLL_VSS
ePAD	QGPHY1_BGND
ePAD	QGPHY1_PLLGND
ePAD	QGPHY2_BGND
ePAD	QGPHY2_PLLGND
ePAD	VSS
ePAD	XTAL_AVSS
ePAD	SWREG_AVSS
ePAD	SWREG_VSSO
F02	NC
F05	NC
F21	SWREG_VDDO
F23	VFB
F25	NC
F28	IMP_TXD[5]
G01	LEDCLK/LED_MODE[0]
G03	VSS
G06	NC
G27	IMP_TXD[1]
G29	IMP_TXD[6]
H02	GMII_LED_SEL
H05	LEDDATA/SYS_FREQ[0]
H25	NC
H28	IMP_TXD[2]

Pin	Signal
J01	FCLK
J03	NC
J27	IMP_TXD[7]
J29	IMP_GTXCLK
K02	FCS_B
K05	FSI
K25	IMP_TXD[3]
K28	IMP_TXEN
L01	INT
L03	FSO
L27	IMP_TXER
L29	IMP_TXCLK
M02	NC
M05	DVDD
M25	IMP_VOL_REF
M28	DVDD
N01	TRST
N03	TMS
N27	IMP_RXER
N29	IMP_RXDV
P02	TDO/EN_8051
P05	TDI
P25	IMP_RXCLK
P28	IMP_RXD[4]
PWRing0	AVDDL
PWRing1	OVDD
PWRing2	OVDD3
PWRing4	AVDDL
PWRing5	OVDD2
R01	TCK
R03	XTAL_O
R27	IMP_RXD[1]
R29	IMP_RXD[0]
T02	XTAL_I
T05	XTAL_AVDD
T25	NC
T28	IMP_RXD[5]
U01	SS
U03	MISO/EN_EEE
U27	IMP_RXD[2]

Pin	Signal
U29	IMP_RXD[6]
V02	SCK
V05	LED[0]/MII_DUMB_FWDG_EN
V25	DVDD
V28	IMP_RXD[3]
W01	MOSI
W03	LED[1]
W27	OTP_VDD
W29	IMP_RXD[7]
Y02	LED[2]/LED_MODE[1]
Y05	LED[3]/SYS_FREQ[1]
Y25	NC
Y28	GMII_TXEN/NC

Pin List by Signal Name

Signal	Pin
AVDDH	AE08
AVDDH	AE10
AVDDH	AE14
AVDDH	AG15
AVDDH	E08
AVDDH	E10
AVDDH	E14
AVDDH	E18
AVDDL	PWRing0
AVDDL	PWRing4
DVDD	AA01
DVDD	AE18
DVDD	AG25
DVDD	E20
DVDD	M05
DVDD	M28
DVDD	V25
EGPHY_BVDD	C15
EGPHY_PLLVDD	A17
EGPHY_RDAC	E16
NC	C17
NC	F02
FCLK	J01
FCS_B	K02
FSI	K05
FSO	L03
GMII_GTXCLK/NC	AA29
GMII_LED_SEL	H02
GMII_RXCLK	AH24
GMII_RXD[0]/LED[10]	AJ23
GMII_RXD[1]/LED[11]	AH22
GMII_RXD[2]/LED[12]	AJ21
GMII_RXD[3]/LED[13]	AH20
GMII_RXD[4]/LED[14]	AG23
GMII_RXD[5]/LED[15]	AE20
GMII_RXD[6]/LED[16]	AG21
GMII_RXD[7]/LED[17]	AG19
GMII_RXDV/LED[18]	AJ25
GMII_RXER/LED[19]	AE22
GMII_TXCLK/NC	AA27
GMII_TXD[0]/NC	AC29
GMII_TXD[1]/NC	AB25
GMII_TXD[2]/NC	AE29
GMII_TXD[3]/NC	AF28
GMII_TXD[4]/NC	AB28
GMII_TXD[5]/NC	AC27
GMII_TXD[6]/NC	AD28
GMII_TXD[7]/NC	AE27
GMII_TXEN/NC	Y28
GMII_TXER/NC	AD25
GMII_VOL_REF	AE24
RGMII_VOL_SEL[1]	E03
IMP_GTXCLK	J29
IMP_RXCLK	P25
IMP_RXD[0]	R29
IMP_RXD[1]	R27
IMP_RXD[2]	U27
IMP_RXD[3]	V28
IMP_RXD[4]	P28
IMP_RXD[5]	T28
IMP_RXD[6]	U29
IMP_RXD[7]	W29
IMP_RXDV	N29
IMP_RXER	N27
IMP_TXCLK	L29
IMP_TXD[0]	E29
IMP_TXD[1]	G27
IMP_TXD[2]	H28
IMP_TXD[3]	K25
IMP_TXD[4]	E27
IMP_TXD[5]	F28
IMP_TXD[6]	G29
IMP_TXD[7]	J27
IMP_TXEN	K28
IMP_TXER	L27
IMP_VOL_REF	M25

Signal	Pin
IMP_VOL_SEL[1]	E01
$\overline{\text{INT}}$	L01
NC	M02
LED[0]/MII_DUMB_FWDG_EN	V05
LED[1]	W03
LED[2]/LED_MODE[1]	Y02
LED[3]/SYS_FREQ[1]	Y05
LED[4]/GMII_MODE[0]	AA03
LED[5]/GMII_MODE[1]	AB02
LED[6]/IMP_MODE[0]	AC01
LED[7]/IMP_MODE[1]	AC03
LED[8]/CPU_EEPROM_SEL	AB05
LED[9]/HW_FWDG_EN	AD02
LEDCLK/LED_MODE[0]	G01
LEDDATA/SYS_FREQ[0]	H05
MDC	AE01
MDIO	AE03
MISO/EN_EEE	U03
MOSI	W01
NC	A03
NC	A25
NC	A27
NC	AD05
NC	AE06
NC	AG01
NC	AG05
NC	AG17
NC	AG29
NC	AH26
NC	AJ03
NC	AJ27
NC	B26
NC	C01
NC	C21
NDRIVE	C25
NC	C29
NC	D02
NC	D28
NC	F05
NC	F25

Signal	Pin
NC	G06
NC	H25
NC	T25
NC	Y25
PDRIVE	C23
OTP_VDD	W27
OVDD	PWRing1
OVDD2	PWRing5
OVDD3	PWRing2
NC	E22
PLL_AVDD	AD17
NC	AJ19
PLL_VSS	ePAD
QGPHY1_BGND	ePAD
QGPHY1_BVDD	C09
QGPHY1_PLLGND	ePAD
QGPHY1_PLLVDD	A09
QGPHY1_RDAC	B10
NC	E12
QGPHY2_BGND	ePAD
QGPHY2_BVDD	AJ11
QGPHY2_PLLGND	ePAD
QGPHY2_PLLVDD	AG11
QGPHY2_RDAC	AE12
NC	AG09
$\overline{\text{RESET}}$	AF02
NC	J03
SCK	V02
SS	U01
SWREG_VDDO	F21
SWREG_AVSS	ePAD
SWREG_VSSO	ePAD
TCK	R01
TDI	P05
TDN_0_0	A19
TDN_0_1	A11
TDN_0_2	A07
TDN_0_3	AJ09
TDN_0_4	AJ13
TDN_1_0	C19

Signal	*Pin*
TDN_1_1	B12
TDN_1_2	C07
TDN_1_3	AH08
TDN_1_4	AG13
TDN_2_0	B22
TDN_2_1	B14
TDN_2_2	B04
TDN_2_3	AH06
TDN_2_4	AH16
TDN_3_0	A23
TDN_3_1	A15
TDN_3_2	C05
TDN_3_3	AJ05
TDN_3_4	AJ17
TDO/EN_8051	P02
TDP_0_0	B18
TDP_0_1	C11
TDP_0_2	B08
TDP_0_3	AH10
TDP_0_4	AH12
TDP_1_0	B20
TDP_1_1	C13
TDP_1_2	B06
TDP_1_3	AJ07
TDP_1_4	AH14
TDP_2_0	A21
TDP_2_1	A13
TDP_2_2	A05
TDP_2_3	AG07
TDP_2_4	AJ15
TDP_3_0	B24
TDP_3_1	B16
TDP_3_2	C03
TDP_3_3	AH04
TDP_3_4	AH18
TMS	N03
$\overline{\text{TRST}}$	N01
VSS	G03
VFB	F23
VSS	ePAD

Signal	*Pin*
VSS	ePAD
VSS	ePAD
VSS	ePAD
XTAL_AVDD	T05
XTAL_AVSS	ePAD
XTAL_I	T02
XTAL_O	R03

Section 7: Register Definitions

Register Definition

BCM53125S register sets can be accessed through the programming interfaces described on page 94. The register space is organized into pages, each containing a certain set of registers. Table 34 lists the pages defined in BCM53125S. To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their addresses. See “Programming Interfaces” on page 94 for more information.

Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or to write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Clear on read

Reserved bits must be written as the default value and ignored when read.

Global Page Register

Table 34: Global Page Register Map

Page	*Description*
00h	“Page 00h: Control Registers” on page 144
01h	“Page 01h: Status Registers” on page 163
02h	“Page 02h: Management/Mirroring Registers” on page 167
03h	“Page 03h: Interrupt Control Register” on page 176
04h	“Page 03h: Interrupt Control Register” on page 176
05h	“Page 05h: ARL/VTBL Access Registers” on page 182
06h, 07h	Reserved
08h	Reserved
09h	Reserved

Table 34: Global Page Register Map (Cont.)

Page	Description
0Ah	Reserved
0Bh–0Fh	Reserved
10h–14h	“Page 10h–14h: Internal GPHY MII Registers” on page 193
15h	“Block Address Number (Page 010h–017h: Address 03Eh)” on page 222
16h–1Fh	Reserved
20h–28h	“Page 20h–28h: Port MIB Registers” on page 223
29h–2Fh	Reserved
30h	“Page 30h: QoS Registers” on page 227
31h	“Page 31h: Port-Based VLAN Registers” on page 235
32h	“Page 32h: Trunking Registers” on page 236
33h	Reserved
34h	“Page 34h: IEEE 802.1Q VLAN Registers” on page 237
35h	Reserved
36h	“Page 36h: DoS Prevent Register” on page 246
37h–3Fh	Reserved
40h	“Page 40h: Jumbo Frame Control Register” on page 249
41h	“Page 41h: Broadcast Storm Suppression Register” on page 250
42h	“Page 42h: EAP Register” on page 258
43h	“Page 43h: MSPT Register” on page 261
44h–6Fh	Reserved
70h	“Page 70h: MIB Snapshot Control Register” on page 263
71h	“Page 71h: Port Snapshot MIB Control Register” on page 264
73h–7Fh	Reserved
80h–83h	Reserved
84h	Reserved
85h	“Page 85h: WAN Interface (Port 5) External PHY MII Registers” on page 264
86h–87h	Reserved
88h	“Page 88h: IMP Port External PHY MII Registers Page Summary” on page 265
90h	Reserved
91h	“Page 91h: Traffic Remarking Register” on page 272
92h–9Fh	“Page 92h: EEE Control Registers” on page 274
A0h	Reserved
A1h	Reserved
A2h–EFh	Reserved
Maps to all pages	“Global Registers” on page 279

Page 00h: Control Registers

Table 35: Control Registers (Page 00h)

Address	Bits	Register Name
00h–05h	8/port	"Port Traffic Control Register (Page 00h: Address 00h)" on page 145
06h–07h	8	Reserved
08h	8	"IMP Port Control Register (Page 00h: Address 08h)" on page 146
09h–0Ah	8	Reserved
0Bh	8	"Switch Mode Register (Page 00h: Address 0Bh)" on page 147
0Ch–0Dh	16	Reserved
0Eh	8	"IMP Port State Override Register (Page 00h: Address 0Eh)" on page 147
0Fh	8	"LED Refresh Register (Page 00h: Address 0Fh)" on page 148
10h–11h	16	"LED Function 0 Control Register (Page 00h: Address 10h)" on page 149
12h–13h	16	"LED Function 1 Control Register (Page 00h: Address 12h)" on page 150
14h–15h	16	"LED Function Map Register (Page 00h: Address 14h–15h)" on page 150
16h–17h	16	"LED Enable Map Register (Page 00h: Address 16h–17h)" on page 150
18h–19h	16	"LED Mode Map 0 Register (Page 00h: Address 18h–19h)" on page 151
1Ah–1Bh	16	"LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)" on page 151
1Ch–1Eh	–	Reserved
1Fh	8	Reserved
20h	–	Reserved
21h	8	"Port Forward Control Register (Page 00h: Address 21h)" on page 152
22h–23h	–	Reserved
24h–25h	16	"Protected Port Selection Register (Page 00h: Address 24h–25h)" on page 153
26h–27h	16	"WAN Port Select Register (Page 00h: Address 26h–27h)" on page 153
28h–2Bh	32	"Pause Capability Register (Page 00h: Address 28h–2Bh)" on page 153
2Ch–2Eh	–	Reserved
2Fh	8	"Reserved Multicast Control Register (Page 00h: Address 2Fh)" on page 154
30h	–	Reserved
31h	8	Reserved
32h–33h	16	"Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)" on page 155
34h–35h	16	"Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)" on page 156
36h–37h	16	"MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)" on page 156
38h–39h	16	"Pause Pass Through for RX Register (Page 00h: Address 38h–39h)" on page 157
3Ah–3Bh	16	"Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)" on page 157
3Ch–3Dh	16	"Disable Learning Register (Page 00h: Address 3Ch–3Dh)" on page 157
3Eh–3Fh	16	"Software Learning Register (Page 00h: Address 3Eh–3Fh)" on page 158
40h–49h	–	Reserved
4Ah–4Bh	–	Reserved

Table 35: Control Registers (Page 00h) (Cont.)

Address	Bits	Register Name
4Ch–57h	–	Reserved
58h–5Dh	8/port	"Port State Override Register (Page 00h: Address 58h)" on page 158
60h–65h	–	Reserved
66h–74h	–	Reserved
75h	–	"MDIO WAN Port Address Register (Page 00h: Address 75h)" on page 160
78h	–	"MDIO IMP PORT Address Register (Page 00h: Address 78h)" on page 160
79h	–	"Software Reset Control Register (Page 00h: Address 79h)" on page 160
7Ah–7Fh	–	Reserved
80h	8	"Pause Frame Detection Control Register (Page 00h: Address 80h)" on page 161
81h–87h	–	Reserved
88h	8	"Fast-Aging Control Register (Page 00h: Address 88h)" on page 161
89h	8	"Fast-Aging Port Control Register (Page 00h: Address 89h)" on page 161
8Ah–8Bh	16	"Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)" on page 161
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0-7
F8h–FDh	–	Reserved
8Ch–EFh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

Port Traffic Control Register (Page 00h: Address 00h)

Table 36: Port Traffic Control Register Address Summary

Address	Description
00h	Port 0
01h	Port 1
02h	Port 2
03h	Port 3
04h	Port 4
05h	Port 5

Table 37: Port Control Register (Page 00h: Address 00h–05h)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	CPU writes the current computed states of its spanning tree algorithm for a given port. 000 = No spanning tree (default for unmanaged mode). 001 = Disabled state (default for managed mode). 010 = Blocking state. 011 = Listening state. 100 = Learning state. 101 = Forwarding state. 110–111 = Reserved.	HW_FWDG_EN (controlled by strap option)
4:2	Reserved	–	–	000
1	TX_DISABLE	R/W	0 = Enable the transmit function of the port at the MAC level. 1 = Disable the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	0 = Enable the receive function of the port at the MAC level. 1 = Disable the receive function of the port at the MAC level.	0

IMP Port Control Register (Page 00h: Address 08h)

Table 38: IMP Port Control Register (Page 00h: Address 08h)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	–	–
4	RX_UCST_EN	R/W	Receive unicast enable. Allow unicast frames to be forwarded to the IMP, when the IMP is configured as the frame management port, and the frame was matching address table entry. When cleared, unicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the Frame Management Port.	0
3	RX_MCST_EN	R/W	Receive multicast enable. Allow multicast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port.	0

Table 38: IMP Port Control Register (Page 00h: Address 08h) (Cont.)

Bit	Name	R/W	Description	Default
2	RX_BCST_EN	R/W	Receive broadcast enable. Allow broadcast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port.	0
1:0	Reserved	R/W	–	0

Switch Mode Register (Page 00h: Address 0Bh)

Table 39: Switch Mode Register (Page 00h: Address 0Bh)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	–	000001
1	SW_FWDG_EN	R/W	Software forwarding enable. SW_FWDG_EN = 1: Frame forwarding is enabled. SW_FWDG_EN = 0: Frame forwarding is disabled. Managed switch implementations should be configured to disable forwarding on power-on to allow the processor to configure the internal address table and other parameters before frame forwarding is enabled.	HW_FWDG_EN
0	SW_FWDG_MODE	R/W	Software forwarding mode. 0 = Unmanaged mode. 1 = Managed mode. The ARL treats reserved multicast addresses differently depending on this selection.	$\overline{\text{HW\_FWDG\_EN}}$

IMP Port State Override Register (Page 00h: Address 0Eh)

Table 40: IMP Port State Override Register (Page 00h: Address 0Eh)

Bit	Name	R/W	Description	Default
7	MII_SW_OR	R/W	MII software override. 0 = Use MII hardware pin status. 1 = Use contents of this register.	0
6	Reserved	R/W	Reserved.	0
5	Tx Flow Control Capability	RO	Link partner flow control capability. 0 = Not PAUSE capable. 1 = PAUSE capable.	0

Table 40: IMP Port State Override Register (Page 00h: Address 0Eh) (Cont.)

Bit	Name	R/W	Description	Default
4	RX Flow Control Capability	R/W	Link partner flow control capability. 0 = Not PAUSE-capable. 1 = PAUSE-capable.	0
3:2	SPEED	R/W	Speed. 00 = 10 Mbps. 01 = 100 Mbps. 10 = 1000 Mbps. 11 = 200 Mbps.	10
1	FDX	R/W	Full duplex. 0 = Half duplex. 1 = Full duplex.	1
0	LINK	R/W	Link status. 0 = Link fail. 1 = Link pass.	0

LED Control Register (Page 00h: Address 0Fh–1Bh)

Table 41: LED Control Register Address Summary

Address	Description
0Fh	LED refresh control register
10h–11h	LED function 0 control register
12h–13h	LED function 1 control register
14h–15h	LED function map control register
16h–17h	LED enable map register
18h–19h	LED mode map 0 register
1Ah–1Bh	LED mode map 1 register

LED Refresh Register (Page 00h: Address 0Fh)

Table 42: LED Refresh Register (Page 00h: Address 0Fh)

Bit	Name	R/W	Description	Default
7	LED_EN	R/W	Enable LED.	1
6	POST_EXEC	R/W	Write 1 to restart POST.	0
5	POST_PSCAN_EN	R/W	When enabled, switch scans the port during the POST period.	0
4	POSt_Cable_diag_en	R/W	Enable cable diagnostics display during POST	0
3	Normal_Cable_diag_en	R/W	Enable cable diagnostics display in normal mode.	0

Table 42: LED Refresh Register (Page 00h: Address 0Fh) (Cont.)

Bit	Name	R/W	Description	Default
2:0	LED_Refresh_rate	R/W	LED refresh count register (that is, LED blinking rate). Refresh time = (N + 1) × 10 ms. • 000 = Reserved. • 001 = 20 ms/25 Hz. • 010 = 30 ms/16 Hz. • 011 = 40 ms/12 Hz. • 100 = 50 ms/10 Hz. • 101 = 60 ms/8 Hz. • 110 = 70 ms/7 Hz. • 111 = 80 ms/6 Hz.	3h

LED Function 0 Control Register (Page 00h: Address 10h)

Table 43: LED Function 0 Control Register (Page 00h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15:0	LED_Function	R/W	The following is the list of functions assigned to each bit: 15 = PHYLED3. 14 = Reserved. 13 = 1G/ACT. 12 = 10/100M/ACT. 11 = 100M/ACT. 10 = 10M/ACT. 9 = SPD1G. 8 = SPD100M. 7 = SPD10M. 6 = DPX/COL. 5 = LNK/ACT. 4 = COL. 3 = ACT. 2 = DPX. 1 = LNK. 0 = PHYLED4.	LED MODE[1:0] = 00: 16'h0121. LED MODE[1:0] = 01: 16'h0C41. LED MODE[1:0] = 10: 16'h0124. LED MODE[1:0] = 11: 16'h0C04.

LED Function 1 Control Register (Page 00h: Address 12h)

Table 44: LED Function 1 Control Register (Page 00h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:0	LED_Function	R/W	The following is the list of functions assigned to each bit: 15 = PHYLED3. 14 = Reserved. 13 = 1G/ACT. 12 = 10/100M/ACT. 11 = 100M/ACT. 10 = 10M/ACT. 9 = SPD1G. 8 = SPD100M. 7 = SPD10M. 6 = DPX/COL. 5 = LNK/ACT. 4 = COL. 3 = ACT. 2 = DPX. 1 = LNK. 0 = PHYLED4.	LED MODE[1:0] = 00: 16'h0321 LED MODE[1:0] = 01: 16'h3041 LED MODE[1:0] = 10: 16'h0324 LED MODE[1:0] = 11: 16'h2C04

LED Function Map Register (Page 00h: Address 14h–15h)

Table 45: LED Function Map Register (Page 00h: Address 14h–15h)

Blt	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	LED_FUNC_MAP	R/W	Per port select function bit. Each port LED follows the function table specified for each port. 1 = Select Function 1. 0 = Select Function 0. Bits [4:0] correspond to ports [4:0]. Bit 5 corresponds to port 5 in serial LED interface.	1FFh

LED Enable Map Register (Page 00h: Address 16h–17h)

Table 46: LED Enable Map Register (Page 00h: Address 16h–17h)

Blt	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0

Table 46: LED Enable Map Register (Page 00h: Address 16h–17h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	LED_EN_MAP	R/W	Per-port enable bit. 1 = Enable. 0 = Disable. Bits [4:0] correspond to ports [4:0]. Bit 5 corresponds to port 5 in serial LED interface.	9'h1F

LED Mode Map 0 Register (Page 00h: Address 18h–19h)

Table 47: LED Mode Map 0 Register (Page 00h: Address 18h–19h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	LED_MODE_MAP0	R/W	Combine with LED_MODE_MAP1 to decide per port LED output mode. Bits [4:0] correspond to ports [4:0]. Bit 5 corresponds to port 5 in serial LED interface.	1FFh

LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)

Table 48: LED Function Map 1 Control Register (Page 00h: Address 1Ah–1Bh)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	LED_MODE_MAP1	R/W	Per port select function bit. LED_FUNC_MAP[1:0]: 00 = LED off 01 = LED on 10 = LED blinking 11 = LED auto	1FFh

See “LED Interfaces” on page 117 for more information.

Port Forward Control Register (Page 00h: Address 21h)

Table 49: Port Forward Control Register (Page 00h: Address 21h)

Bit	Name	R/W	Description	Default
7	MCST_DLF_FWD_EN	R/W	Multicast Forward Enable when ARL Miss. 1 = Forward multicast lookup failed packets according to multicast lookup failed forward map register (page 00h: address 34h). 0 = Flood multicast lookup failed packets to all the ports.	0
6	UCST_DLF_FWD_EN	R/W	Unicast Forward Enable when ARL Miss. 1 = Forward unicast lookup failed packets according to multicast lookup failed forward map register (page 00h: address 32h). 0 = Flood unicast lookup failed packets to all the ports.	0
5:3	Reserved	R/W	–	–
2	INRANGE_ERR_DIS	R/W	In-Range Error Discard. When bit = 1, the ingress port will discard the frames with Length field mismatch the frame length. Following is the definition of InRangeErrors. In-Range Errors Frames: The frames received with good CRC and one of the following: • The value of µs is between 46 and 1500 inclusive, and does not match the number of (MAC Client Data + PAD) data octets received. • The value of µs is less than 46, and the number of data octets received is greater than 46(which does not require padding).	0
1	OUTRANGE_ERR_DIS	R/W	Out of Range Error Discard. When bit =1, the ingress port will discard the frames with length field between 1500 and 1536 (exclude 1500 and 1536) with good CRC. This option only controls the length field checking but not the frame length checking.	0
0	Reserved	R/W	–	1

See “Egress PCP Remarking” on page 57 for more information.

Protected Port Selection Register (Page 00h: Address 24h–25h)

Table 50: Protected Port Selection Register (Page 00h: Address 24h–25h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	Port_Select	R/W	Protected port selection. Bit 8 = IMP port. Bits [4:0] correspond to ports [4:0], respectively. 1 = Port protected. Cannot send/receive to other protected ports. 0 = Port is not protected.	0

See "Protected Ports" on page 48 for more information.

WAN Port Select Register (Page 00h: Address 26h–27h)

Table 51: WAN Port Select Register (Page 00h: Address 26h–27h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9	Reserved	R/W	–	–
8:6	Reserved	R/W	–	–
5:0	WAN_Port_MAP	R/W	Set assigned WAN port to 1. Bits [5:0] correspond to ports [5:0], respectively. Port 5 can be selected as a WAN port only in En_IMP_Port = 10 of Global Management Configuration Register (Page 02h: Address 00h).	0

Pause Capability Register (Page 00h: Address 28h–2Bh)

Table 52: Pause Capability Register (Page 00h: Address 28h–2Bh)

Bit	Name	R/W	Description	Default
31:24	Reserved	RO	–	0
23	EN_OVeRIDE	R/W	Forces the content of this register setting to be used over the auto negotiation result.	0
22:18	Reserved	–	–	–
17:9	EN_RX_PAUSE_CAP	–	Enabling the receive pause capability. Bit 17 = IMP port. Bits [14:9] correspond to ports [5:0], respectively.	0h
8:0	EN_TX_PAUSE_CAP	–	Enables the transmit pause capability. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0h

Reserved Multicast Control Register (Page 00h: Address 2Fh)

Table 53: Reserved Multicast Control Register (Page 00h: Address 2Fh)

Bit	Name	R/W	Description	Default
7	Multicast Learning	R/W	Multicast learning enable. 0 = Do not learn unicast source addresses of frames that have a reserved multicast destination address. 1 = Learn unicast source addresses even from frames that have a reserved multicast destination address. See “Address Management” on page 57 for more information.	0
6:5	Reserved	R/W	–	0
4	En_Mul_4	R/W	Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-20–01-80-C2-00-00-2F 0 = Forward. 1 = Drop.	0
3	En_Mul_3	R/W	Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-11–01-80-C2-00-00-1F 0 = Forward. 1 = Drop.	0
2	En_Mul_2	R/W	Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-10 0 = Forward. 1 = Drop.	0
1	En_mul_1	R/W	Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-02–01-80-C2-00-00-0F 0 = Forward. 1 = Drop.	1
0	En_Mul_0	R/W	Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-00 0 = Forward. 1 = Drop.	0

See “Multicast Addresses” on page 60 for more information.

Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)

Table 54: Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	Uni_DLF_MAP	R/W	Unicast lookup failed forward map. Bit 8 = IMP port. Bits [7:6] reserved. Bits [5:0] correspond to ports [5:0], respectively. When the UCST_DLF_FWD_EN bit in "Port Forward Control Register (Page 00h: Address 21h)" on page 152 is enabled and a unicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped. 0 = Do not forward a unicast lookup failure to this port. 1 = Forward a unicast lookup failure to this port.	0

See "Unicast Addresses" on page 59 for more information.

Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

Table 55: Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	MCST_DLF_MAP	R/W	Multicast lookup failed forward map. Bit 8 = IMP port. Bits [7:6] reserved. Bits [5:0] correspond to ports [5:0], respectively. When the MCST_DLF_FWD_EN bit in port forward control register (Page 00h:Address 21h) is enabled and a multicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped. 0 = Do not forward a multicast lookup failure to this port. 1 = Forward a multicast lookup failure to this port.	0

See “Multicast Addresses” on page 60 for more information.

MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)

Table 56: MLF IMPC Forward Map Register (Page 00h: Address 36h–37h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	MLF_IPMC_FWD_MAP	R/W	IPMC forward map. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. ***Note:*** The received pause frames are forwarded to all ports (flooded), which can cause a halt of all inputs to all ports.	0
Note: IP Multicast (IPMC) packets are multicast with the address range 01-00-5e-xx-xx-xx.				

Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

Table 57: Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	–	0
7:0	IGNORE_Pause frame _RX	R/W	RX pause pass through map. 1 = Ignore IEEE 802.3x. 0 = Comply with IEEE 802.3x pause frame receiving. Bits [5:0] correspond to ports [5:0], respectively.	0

Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

Table 58: Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	IGNORE_Pause frame _Tx	R/W	TX pause pass through map. 1 = Ignore IEEE 802.3x. 0 = Comply with IEEE 802.3x pause frame receiving. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0

Disable Learning Register (Page 00h: Address 3Ch–3Dh)

Table 59: Disable Learning Register (Page 00h: Address 3Ch–3Dh)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	DIS_LEARNING	R/W	1 = Disable learning. 0 = Enable learning. Bit 8 = IMP port. Bits [7:6] reserved. Bits [5:0] correspond to ports [5:0], respectively.	0

Software Learning Register (Page 00h: Address 3Eh–3Fh)

Table 60: Software Learning Control Register (Page 00h: Address 3Eh–3Fh)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Reserved	–
8:0	SW_LEARN_CNTL	R/W	1 = Software learning control enabled. The behaviors are as follows. Forwarding behavior: Incoming packet with unknown SA will be copied to CPU port. Learning behavior: Allow S/W to decide whether incoming packet learn or not. In S/W learning mode, the H/W learning mechanism will be disabled automatically. Refreshed behavior: Allow refreshed mechanism to operate properly even through the H/W learning had been disabled. 0 = Software learning control disabled. Forwarding/Learning/Refreshed behavior to keep hardware operation. Bit 8 = IMP port. Bits [7:6] reserved. Bits [5:0] correspond to ports [5:0].	0

Port State Override Register (Page 00h: Address 58h)

Table 61: Port State Override Register Address Summary

Address	Description
58h	Port 0
59h	Port 1
5Ah	Port 2
5Bh	Port 3
5Ch	Port 4
5Dh	Port 5

Table 62: Port State Override Register (Page 00h: Address 58h–5Fh)

Blt	Name	R/W	Description	Default
7	Reserved	R/W	–	–
6	Software Override	R/W	Writing 1 to this bit allows the values of the bits [5:0] to be written to the external PHY. Writing 0 to this bit prevents these values from overriding the present external PHY conditions.	0

Table 62: Port State Override Register (Page 00h: Address 58h–5Fh) (Cont.)

Bit	Name	R/W	Description	Default
5	Tx Flow Control Enable	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Flow control disabled for transmit traffic. 1 = Flow control enabled for transmit traffic.	0
4	RX Flow Control Enable	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Flow control disabled for receive traffic. 1 = Flow control enabled for receive traffic.	0
3:2	Speed	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 00 = 10 Mbps. 01 = 100 Mbps. 10 = 1000 Mbps. 11 = 200 Mbps (for Port5 only, Register Address 5Dh).	10
1	Duplex Mode	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Half duplex. 1 = Full duplex.	1
0	Link State	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written 1. 1 = Link-up. 0 = Link-down.	1

RGMII Timing Delay Register for IMP Port (Page 00h: Address 60h)

Table 63: RGMII Timing Delay Register for IMP Port (Page 00h: Address 60h)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0
1	EN_RGMII_RX_CLK	R/W	1 = RGMII RX_CLK delay. 0 = RGMII RX_CLK no delay.	0
0	EN_RGMII_TX_CLK	R/W	1 = RGMII TX_CLK delay. 0 = RGMII TX_CLK no delay.	0

RGMII Timing Delay Register for Port 5 (Page 00h, Address 65h)

Table 64: RGMII Timing Delay Register for Port 5 (Page 00h, Address 65h)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0
1	EN_RGMII_RX_CLK	R/W	1 = RGMII RX_CLK delay. 0 = RGMII RX_CLK no delay.	0
0	EN_RGMII_TX_CLK	R/W	1 = RGMII TX_CLK delay. 0 = RGMII TX_CLK no delay.	0

MDIO WAN Port Address Register (Page 00h: Address 75h)

Table 65: MDIO WAN Port Address Register (Page 00h: Address 75h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	–	0
4:0	WAN_MDIO_ADDRESS	R/W	WAN port MDIO SCAN address	15h

MDIO IMP PORT Address Register (Page 00h: Address 78h)

Table 66: MDIO IMP PORT Address Register (Page 00h: Address 78h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	–	0
4:0	IMP_MDIO_Address	R/W	IMP PORT MDIO address	18h

Software Reset Control Register (Page 00h: Address 79h)

Table 67: Software Reset Control Register (Page 00h: Address 79h)

Bit	Name	R/W	Description	Default
7	SW_RST	R/W	Software reset (bit 4 EN_SW_RST must be enabled as well). 1 = Activate reset. 0 = Clear reset.	–
6:5	Reserved	–	–	–
4	EN_SW_RST	R/W	Enable software reset.	0
3:0	Reserved	R/W	–	–
Note: A software reset samples the strap pin states in the same way as a hardware reset.				

Pause Frame Detection Control Register (Page 00h: Address 80h)

Table 68: Pause Frame Detection Control Register (Page 00h: Address 80h)

Bit	Name	R/W	Description	Default
7:1	Reserved	RO	–	0
0	Pause_ignore_Da	R/W	0 = Check DA field on pause frame detection. 1 = Ignore DA field on pause frame detection.	0

Fast-Aging Control Register (Page 00h: Address 88h)

Table 69: Fast-Aging Control Register (Page 00h: Address 88h)

Bit	Name	R/W	Description	Default
7	Fast_Age_Start/Done	R/W	Set bit to 1 triggers the fast aging process. When the fast aging process is done, this bit is cleared to 0.	0
6	Reserved	–	–	–
5	EN_AGE_MCAST	R/W	Enable Aging Multicast Entry. 1 = Aging multicast Entries in ARL Table. 0 = Disable Aging Multicast Entries in ARL Table. ***Note:*** The EN_AGE_MCAST and the EN_AGE_Port can not enable (set to 1) at the same time.	0
4	EN_AGE_SPT	R/W	When set, check spanning tree ID.	–
3	EN_AGE_VLAN	R/W	When set, check VLAN ID.	–
2	EN_AGE_Port	R/W	When set, check port ID.	–
1	EN_AGE_Dynamic	R/W	When set, age out dynamic entry.	–
0	EN_AGE_Static	R/W	When set, age out static entry.	–

Fast-Aging Port Control Register (Page 00h: Address 89h)

Table 70: Fast-Aging Port Control Register (Page 00h: Address 89h)

Bit	Name	R/W	Description	Default
7:4	Reserved	R/W	–	0
3:0	Fast Age Single Port	R/W	Fast age single port select. Writing bits [3:0] selects the port to be fast-aged.	0

Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

Table 71: Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	–	0

Table 71: Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh) (Cont.)

Bit	Name	R/W	Description	Default
11:0	Fast Age Single VID	R/W	Fast age single VID select. Writing bits [11:0] selects the VID to be fast-aged.	0

Page 01h: Status Registers

Table 72: Status Registers (Page 01h)

Address	Bits	Register Name
00h–01h	16	“Link Status Summary (Page 01h: Address 00h)” on page 163
02h–03h	16	“Link Status Change (Page 01h: Address 02h)” on page 164
04h–07h	32	“Port Speed Summary (Page 01h: Address 04h)” on page 164
08h–09h	16	“Duplex Status Summary (Page 01h: Address 08h)” on page 164
0Ah–0Dh	32	“Pause Status Summary (Page 01h: Address 0Ah)” on page 165
0Eh–0Fh	16	“Source Address Change Register (Page 01h: Address 0Eh)” on page 165
10h–45h	48/port	“Last Source Address Register (Page 01h: Address 10h)” on page 166
46h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

Link Status Summary (Page 01h: Address 00h)

Table 73: Link Status Summary Register (Page 01h: Address 00h–01h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	LINK_STATUS	RO	Link status. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Link fail. 1 = Link pass.	0

Link Status Change (Page 01h: Address 02h)

Table 74: Link Status Change Register (Page 01h: Address 02h–03h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	LINK_STATUS_CHANGE	RO	Link status change. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. Upon change of link status, a bit remains set until cleared by a read operation. 0 = Link status constant. 1 = Link status change.	0

Port Speed Summary (Page 01h: Address 04h)

Table 75: Port Speed Summary Register (Page 01h: Address 04h–07h)

Bit	Name	R/W	Description	Default
31:18	Reserved	PO	Reserved	0
17:0	PORT_SPEED	RO	Port speed. The speed of each port is reported based on the mapping below: • bits [17:16] = IMP port. • bits [15:12] = Reserved. • bits [11:10] = Port 5. • bits [9:8] = Port 4. • bits [7:6] = Port 3. • bits [5:4] = Port 2. • bits [3:2] = Port 1. • bits [1:0] = Port 0. The value of the bits are: • 00 = 10 Mbps. • 01 = 100 Mbps. • 10 = 1000 Mbps. • 11 = 200 Mbps (for IMP and Port5 only).	0

Duplex Status Summary (Page 01h: Address 08h)

Table 76: Duplex Status Summary Register (Page 01h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0

Table 76: Duplex Status Summary Register (Page 01h: Address 08h–09h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	DUPLEX_STATE	RO	Duplex state. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Half duplex. 1 = Full duplex.	1FFh

Pause Status Summary (Page 01h: Address 0Ah)

Table 77: PAUSE Status Summary Register (Page 01h: Address 0Ah–0Dh)

Bit	Name	R/W	Description	Default
31:18	Reserved	RO	Reserved	0
17:9	RECEIVE_PAUSE_STATE	RO	Pause state. Receive pause capability. Bit 17 = IMP port. Bits [14:9] correspond to ports [5:0], respectively. 0 = Disabled. 1 = Enabled.	120h
8:0	TRANSMIT_PAUSE_STATE	RO	Transmit pause capability. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Disabled. 1 = Enabled.	

Source Address Change Register (Page 01h: Address 0Eh)

Table 78: Source Address Change Register (Page 01h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	SRC_ADDR_CHANGE	RC	Source address change. Bit 8 = IMP port. Bits [4:0] correspond to ports [4:0], respectively. The value of this bit is 1 if a change in the source address is detected on the given port. The bit remains set until cleared by a read operation. 0 = No change in source address since last read. 1 = Source address has changed since last read.	0

Last Source Address Register (Page 01h: Address 10h)

Table 79: Last Source Address Register Address Summary

Address	Description
10h–15h	Port 0
16h–1Bh	Port 1
1Ch–21h	Port 2
22h–27h	Port 3
28h–2Dh	Port 4
2Eh–33h	Port 5
34h–39h	Reserved
3Ah–3Fh	Reserved
40h–45h	IMP port

Table 80: Last Source Address (Page 01h: Address 10h–45h)

Bit	Name	R/W	Description	Default
47:0	LAST_SOURCE_ADD	RO	The 48-bit source address detected on the last packet ingressed.	0

Page 02h: Management/Mirroring Registers

Table 81: Aging/Mirroring Registers (Page 02h)

Address	Bits	Register Name
00h	8	"Global Management Configuration Register (Page 02h: Address 00h)" on page 168
01h–02h	–	Reserved
03h	8	"Broadcom Header Control Register (Page 02h: Address 03h)" on page 168
04h–05h	16	"RMON MIB Steering Register (Page 02h: Address 04h)" on page 169
06h–09h	32	"Aging Time Control Register (Page 02h: Address 06h)" on page 169
0Ah–0Fh	–	Reserved
10h–11h	16	"Mirror Capture Control Register (Page 02h: Address 10h)" on page 169
12h–13h	16	"Ingress Mirror Control Register (Page 02h: Address 12h)" on page 170
14h–15h	16	"Ingress Mirror Divider Register (Page 02h: Address 14h)" on page 171
16h–1Bh	48	"Ingress Mirror MAC Address Register (Page 02h: Address 16h)" on page 171
1Ch–1Dh	16	"Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 172
1Eh–1Fh	16	"Egress Mirror Divider Register (Page 02h: Address 1Eh)" on page 173
20h–25h	48	"Egress Mirror MAC Address Register (Page 02h: Address 20h)" on page 173
26h–EFh	–	Reserved
30h–33h	8	Device ID number
34h–3Fh	–	Reserved
40h	8	Revision ID number
41h–4Fh	–	Reserved
50h–53h	32	"High-Level Protocol Control Register (Page 02h: Address 50h–53h)" on page 174
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

Global Management Configuration Register (Page 02h: Address 00h)

Table 82: Global Management Configuration Register (Page 02h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	En_IMP_Port	R/W	IMP port enable. 00 = No frame management port. 01 = Reserved. 10 = Enable IMP port only. All traffic to CPU from LAN and WAN ports will be forwarded to IMP port. 11 = Enable Dual-IMP ports (both IMP port and Port5). All traffic to CPU from LAN ports will be forwarded to IMP port and all traffic from WAN ports will be forwarded to Port 5. These bits are ignored when SW_FWD_MODE = Unmanaged in the "Switch Mode Register (Page 00h: Address 0Bh)" on page 147.	00
5.2	Reserved	–	–	–
1	En_RX_BPDU	R/W	Receive BPDU enable. Enables all ports to receive BPDUs and forwards to the IMP port. This bit must be set to globally allow BPDUs to be received.	0
0	Reset MIB	R/W	Reset MIB counters. Resets all MIB counters for all ports to 0 (pages 20h–28h). This bit must be set and then cleared in successive write cycles to activate the reset operation.	0

Broadcom Header Control Register (Page 02h: Address 03h)

Table 83: Broadcom Tag Control Register (Page 02h: Address 03h)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	–	0
1:0	BRCM_HDR_EN	R/W	Broadcom tag enable for GMII port. Bit 1 = Enable BRCM header for GMII port (port 5). • 1 = Additional header information is inserted into the original frame, between original SA field and type/length fields. The tag includes the BRCM tag field. • 0 = Without additional header information. Bit 0 = Enable BRCM header for IMP port. • 1 = Additional header information is inserted into the original frame, between original SA field and type/length fields. The tag includes the BRCM tag field. • 0 = Without additional header information.	11

RMON MIB Steering Register (Page 02h: Address 04h)

Table 84: RMON MIB Steering Register (Page 02h: Address 04h–05h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	Override RMON Receive	R/W	Override RMON receive. Forces the RMON packet size bucket counters from the normal default of snooping on the receive side of the MAC to the transmit side. This allows the RMON bucket counters to snoop either transmit or receive, allowing full-duplex MAC support. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0

Aging Time Control Register (Page 02h: Address 06h)

Table 85: Aging Time Control Register (Page 02h: Address 06h–09h)

Bit	Name	R/W	Description	Default
31:21	Reserved	RO	–	–
20	Age Change	R/W	Age change enable. 1 = Set age time using bits [19:0]. 0 = Age time default 300 seconds.	0
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned addresses. Maximum age time is 1,048,575s. Setting the AGE_TIME to 0 disables the aging process. For more information on ARL table aging, see “Address Aging” on page 63.	300d

Mirror Capture Control Register (Page 02h: Address 10h)

Table 86: Mirror Capture Control Register (Page 02h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15	Mirror Enable	R/W	Global mirror enable. 0 = Disable mirror capture feature. 1 = Enable mirror capture feature.	0
14	BLK_NOT_MIR	R/W	When enabled, all traffic to MIRROR_CAPTURE_PORT is blocked, except for mirror traffic. Nonmirror traffic is disabled. 0 = No traffic blocking on mirror capture port. 1 = Traffic to mirror capture port blocked unless mirror traffic.	0
13:4	Reserved	RO	–	0

Table 86: Mirror Capture Control Register (Page 02h: Address 10h–11h) (Cont.)

Bit	Name	R/W	Description	Default
3:0	Capture Port	R/W	Mirror capture port ID. Binary value identifies the single unique port that is designated as the port where all ingress and/or egress traffic is mirrored.	0

For additional information about port mirroring, see "Port Mirroring" on page 48.

Ingress Mirror Control Register (Page 02h: Address 12h)

Table 87: Ingress Mirror Control Register (Page 02h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:14	IN_MIRROR_FILTER	R/W	Ingress mirror filter. Filters frames to be forwarded to the mirror capture port, specified in "Mirror Capture Control Register (Page 02h: Address 10h)" on page 169. 00 = Mirror all ingress frames. 01 = Mirror all ingress frames with DA = IN_MIRROR_MAC. 10 = Mirror all ingress frames with SA = IN_MIRROR_MAC. 11 = Reserved. IN_MIRROR_MAC is specified in "Ingress Mirror MAC Address Register (Page 02h: Address 16h)" on page 171.	0
13	IN_DIV_EN	R/W	Ingress divider enable. The ingress divider mirrors every n^{th} ingress frame that has passed through the IN_MIRROR_FILTER (n represents the IN_MIRROR_DIV defined in "Ingress Mirror Divider Register (Page 02h: Address 14h)" on page 171). 0 = Disable ingress divider feature. 1 = Enable ingress divider feature.	0
12:9	Reserved	R/W	–	0
8:0	IN_MIRROR_MASK	R/W	Ingress mirror port mask. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. Ports with the corresponding bit set to 1 have ingress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an Ingress Mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the ingress mirrored port (s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter using bits [15:14] or divider using bit 13 may be helpful.	0

For additional information about port mirroring, see "Port Mirroring" on page 48.

Ingress Mirror Divider Register (Page 02h: Address 14h)

Table 88: Ingress Mirror Divider Register (Page 02h: Address 14h–15h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9:0	IN_MIRROR_DIV	R/W	Ingress mirror divider. Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the “Ingress Mirror Control Register (Page 02h: Address 12h)” on page 170 is set, frames that pass the IN_MIRROR_FILTER rule are further divided by n, where n = IN_MIRROR_DIV + 1.	0

For additional information about port mirroring, see “Port Mirroring” on page 48.

Ingress Mirror MAC Address Register (Page 02h: Address 16h)

Table 89: Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)

Bit	Name	R/W	Description	Default
47:0	IN_MIRROR_MAC	R/W	Ingress mirror MAC address. MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules in “Ingress Mirror Control Register (Page 02h: Address 12h)” on page 170.	0

For additional information about port mirroring, see “Port Mirroring” on page 48.

Egress Mirror Control Register (Page 02h: Address 1Ch)

Table 90: Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)

Bit	Name	R/W	Description	Default
15:14	OUT_MIRROR_FILTER	R/W	Egress mirror filter. Filters egress frames that are forwarded to the mirror capture port, specified in "Mirror Capture Control Register (Page 02h: Address 10h)" on page 169. 00 = Mirror all egress frames. 01 = Mirror all egress frames with DA = OUT_MIRROR_MAC. 10 = Mirror all egress frames with SA = OUT_MIRROR_MAC. 11 = Reserved. OUT_MIRROR_MAC is specified in "Egress Mirror MAC Address Register (Page 02h: Address 20h)" on page 173.	0
13	OUT_DIV_EN	R/W	Egress divider enable. The egress divider mirrors every n^{th} egress frame that has passed through the OUT_MIRROR_FILTER (n represents the OUT_MIRROR_DIV defined in "Egress Mirror Divider Register (Page 02h: Address 1Eh)" on page 173). 0 = Disable egress divider feature. 1 = Enable egress divider feature.	0
12:9	Reserved	R/W	–	0
8:0	OUT_MIRROR_MASK	R/W	Egress mirror port mask. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. Ports with the corresponding bit set to 1 have egress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an egress mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the egress mirrored port (s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter using bits [15:14] or a divider using bit 13 may be helpful.	0

For additional information about port mirroring, see "Port Mirroring" on page 48.

Egress Mirror Divider Register (Page 02h: Address 1Eh)

Table 91: Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9:0	OUT_MIRROR_DIV	R/W	Egress mirror divider. Egressed frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 172 is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by n, where n = OUT_MIRROR_DIV + 1.	0

For additional information about port mirroring, see "Port Mirroring" on page 48.

Egress Mirror MAC Address Register (Page 02h: Address 20h)

Table 92: Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)

Bit	Name	R/W	Description	Default
47:0	OUT_MIRROR_MAC	R/W	Egress mirror MAC address. MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules defined in "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 172.	0

For additional information about port mirroring, see "Port Mirroring" on page 48.

Device ID Register (Page 02h: Address 30h–33h)

Table 93: Device ID Register (Page 02h: Address 30h–33h)

Bit	Name	R/W	Description	Default
31:0	Device_ID	RO	Device ID	32'0005_3125

Revision Number Register (Page 02h: Address 40h)

Table 94: Egress Mirror MAC Address Register (Page 02h: Address 40h)

Bit	Name	R/W	Description	Default
7:0	Revision_ID	RO	Revision number	0

High-Level Protocol Control Register (Page 02h: Address 50h–53h)

Table 95: High-Level Protocol Control Register (Page 02h: Address 50h–53h)

Bit	Name	R/W	Description	Default
31:19	Reserved	R/W	Reserved	–
18	MLD_QRY_FWD_MODE	R/W	MLD Query Message Forwarding Mode. 1 = MLD Query message frames will be trapped to CPU port only. 0 = MLD Query message frames will be forwarded by L2 result and also copied to CPU.	0
17	MLD_QRY_EN	R/W	MLD Query Message Snooping/Redirect Enable. 1 = Enable MLD query message snooping/ redirect. 0 = Disable.	0
16	MLD_RPTDONE_FWD_MODE	R/W	MLD Report/Done Message Forwarding Mode. 1 = MLD report/done message frames will be trapped to CPU port only. 0 = MLD report/done message frames will be forwarded by L2 result and also copied to CPU.	0
15	MLD_RPTDONE_EN	R/W	MLD Report/Done Message Snooping/Redirect Enable. 1 = Enable MLD report/done message snooping/ redirect. 0 = Disable.	0
14	IGMP_UKN_FWD_MODE	R/W	IGMP Unknown Message Forwarding Mode. 1 = IGMP unknown message frames will be trapped to CPU port only. 0 = IGMP unknown message frames will be forwarded by L2 result and also copied to CPU.	0
13	IGMP_UKN_EN	R/W	IGMP Unknown Message Snooping/Redirect Enable. 1 = Enable IGMP unknown message snooping/ redirect. 0 = Disable.	0
12	IGMP_QRY_FWD_MODE	R/W	IGMP Query Message Forwarding Mode. 1 = IGMP query message frames will be trapped to CPU port only. 0 = IGMP query message frames will be forwarded by L2 result and also copied to CPU.	0
11	IGMP_QRY_EN	R/W	IGMP Query Message Snooping/Redirect Enable. 1 = Enable IGMP query message Snooping/ Redirect. 0 = Disable.	0

Table 95: High-Level Protocol Control Register (Page 02h: Address 50h–53h) (Cont.)

Bit	Name	R/W	Description	Default
10	IGMP_RPTLVE_FWD_MODE	R/W	IGMP Report/Leave Message Forwarding Mode. 1 = IGMP report/leave message frames will be trapped to CPU port only. 0 = IGMP report/leave message frames will be forwarded by L2 result and also copied to CPU.	0
9	IGMP_RPTLVE_EN	R/W	IGMP Report/Leave Message Snooping/ Redirect Enable. 1 = Enable IGMP report/leave message Snooping/Redirect. 0 = Disable.	0
8	IGMP_DIP_EN	R/W	IGMP L3 DIP checking Enable. In addition to the IP datagram with a protocol value of 2, IGMP will be classified by matching its DIP with the Class D IP address(224.0.0.0–239.255.255.255).	0
7:6	Reserved	R/W	Reserved	0
5	ICMPv6_FWD_MODE	R/W	ICMPv6 (exclude MLD) Forwarding Mode. 1 = ICMPv6 frames will be trapped to CPU port only. 0 = ICMPv6 frames will be forwarded by L2 result and also copied to CPU.	0
4	ICMPv6_EN	R/W	ICMPv6 (exclude MLD) Snooping/Redirect Enable. ICMPv6, with a next header value of 58, will be classified by IPv6 datagram.	0
3	ICMPv4_EN	R/W	ICMPv4 Snooping Enable. ICMPv6, with a next header value of 0 and extension header next header value of 58, will be classified by IPv6 datagram. 1 = ICMPv4 frames will be forwarded by L2 result and also copied to CPU. 0 = ICMPv4 frames will be forwarded by L2 result.	0
2	DHCP_EN	R/W	DHCP Snooping Enable. 1 = DHCP frames will be forwarded by L2 result and also copied to CPU. 0 = DHCP frames will be forwarded by L2 result.	0
1	RARP_EN	R/W	RARP Snooping Enable. 1 = RARP frames will be forwarded by L2 result and also copied to CPU. 0 = RARP frames will be forwarded by L2 result.	0
0	ARP_EN	R/W	ARP Snooping Enable. 1 = ARP frames will be forwarded by L2 result and also copied to CPU. 0 = ARP frames will be forwarded by L2 result.	0

Page 03h: Interrupt Control Register

Table 96: Interrupt Status Register (Page 03H: Address 00h-03h)

Bit	Name	R/W	Description	Default
31:25	Reserved	–	–	–
24:16	Link Status Change Interrupt	–	Each bit is set when corresponding port status is changed. 0 = No link status change. 1 = Link status change. Bit [24] = IMP port (port8). Bit [23:22] = Reserved. Bit [21:16] = Port[5:0].	–
15:2	Reserved	–	–	–
1:0	IMP_Sleep_Timer_Run	R/W	Each bit set indicates the corresponding port timer has been triggered. Bit [1] = WAN port (port5). Bit [0] = IMP port (port 8).	–

Table 97: Interrupt Enable Register (Page 03H: Address 08h-0Bh)

Bit	Name	R/W	Description	Default
31:25	Reserved	–	–	–
24:16	Link Status Change Interrupt_Enable	–	Each bit is set when corresponding port status is changed. 0 = Disable interrupt. 1 = Enable interrupt. Bit [24] = IMP port (port8). Bit [23:22] = Reserved. Bit [21:16] = Port[5:0].	–
15:2	Reserved	–	–	–
1:0	IMP_Sleep_Timer_Run_enable	R/W	Each bit set enables the corresponding port timer has been triggered. Bit [1] = WAN port (port5). Bit [0] = IMP port (port 8).	–

Table 98: IMP Sleep Timer Register (Page 03H: Address 10h-11h)

Bit	Name	R/W	Description	Default
15:13	Reserved	–	–	0x0

Table 98: IMP Sleep Timer Register (Page 03H: Address 10h-11h) (Cont.)

Bit	Name	R/W	Description	Default
12:0	IMP_Sleep_Timer	R/W	The configuration value of IMP port (port 8) sleep timer to indicate the desired sleep recovery time (i.e. wake-up time). When the timer is set by the CPU to a nonzero value, it puts the IMP port to sleep. The wake-up time is the set value decrease 1. The unit is in 1 µs.	0x0

Table 99: WAN Sleep Timer Register (Page 03H: Address 14h-15h)

Bit	Name	R/W	Description	Default
15:13	Reserved	–	–	0x0
12:0	WAN_Sleep_Timer	R/W	The configuration value of WAN port (port 5) sleep timer to indicate the desired sleep recovery time (i.e. wake-up time). When the timer is set by the CPU to a nonzero value, it puts the IMP port to sleep. The wake-up time is the set value decrease 1. The unit is in 1 µs.	0x0

Table 100: Sleep Status Register (Page 03H: Address 18h)

Bit	Name	R/W	Description	Default
7:2	Reserved	–	–	0x0
1	WAN_Port_Sleep_STS	RO	WAN Port(port5) Sleep Status. 0 = WAN port is not in IMP_Sleep mode whenever either reset or the counter of WAN SLEEP Timer is equal to zero. ***Note:*** The port is in IMP_SLEEP INIT state. 1 = WAN port is in IMP_Sleep mode when the counter of WAN Sleep Timer is not equal to zero. ***Note:*** The port is not in IMP_SLEEP INIT state.	0x0
0	IMP_Port_Sleep_STS	RO	IMP Port(port88) Sleep Status. 0 = IMP port is not in IMP_Sleep mode whenever either reset or the counter of IMP SLEEP Timer is equal to zero. ***Note:*** The port is in IMP_SLEEP INIT state. 1 = IMP port is in IMP_Sleep mode when the counter of IMP Sleep Timer is not equal to zero. ***Note:*** The port is not in IMP_SLEEP INIT state.	0x0

Page 04h: ARL Control Register

Table 101: ARL Control Registers (Page 04h)

Address	Bits	Register Name
00h	8	"Global ARL Configuration Register (Page 04h: Address 00h)" on page 179
01h–03h	–	Reserved
04h–09h	48	"BPDU Multicast Address Register (Page 04h: Address 04h)" on page 179
0Ah–0Dh	–	Reserved
0Eh–0Fh	16	"Multiport Control Register (Page 04h: Address 0Eh–0Fh)" on page 179
10h–17h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181
18h–1Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 182
1Ch–1Fh	–	Reserved
20h–27h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181
28h–2Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 182
2Ch–2Fh	–	Reserved
30h–37h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181
38h–3Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 182
3Ch–3Fh	–	Reserved
40h–47h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181
48h–4Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 182
4Ch–4Fh	–	Reserved
50h–57h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181
58h–5Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 182
5Ch–5Fh	–	Reserved
60h–67h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181
68h–6Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 182
6Ch–FEh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280

Table 101: ARL Control Registers (Page 04h) (Cont.)

Address	Bits	Register Name
FFh	8	"Page Register (Global, Address FFh)" on page 280

Global ARL Configuration Register (Page 04h: Address 00h)

Table 102: Global ARL Configuration Register (Page 04h: Address 00h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	–	0
4	Reserved	–	–	–
3	Reserved	RO	–	0
2	AGE_Accelerate	R/W	When enabled, the aging time is reduced by 1/128. 1 = Accelerate the aging 128 times. 0 = Keep the original age process.	–
1	Reserved	RO	–	1
0	Hash Disable	R/W	Hash function disable. Disables the hash function of the ARL table so that entries are directly mapped to the table instead of being hashed to an index. 1 = Disable hash function. 0 = Enable hash function. For more information see "Address Table Organization" on page 57.	0

BPDU Multicast Address Register (Page 04h: Address 04h)

Table 103: BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Bit	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/W	BPDU multicast address 1. Defaults to the IEEE 802.1 defined reserved multicast address for the bridge group address. Programming to an alternate value allows support of proprietary protocols in place of the normal spanning tree protocol. Frames with a matching DA to this address are forwarded to the designated management port.	01-80-c2-00-00-00

Multiport Control Register (Page 04h: Address 0Eh–0Fh)

Table 104: Multiport Control Register (Page 04h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Reserved	0

Table 104: Multiport Control Register (Page 04h: Address 0Eh–0Fh) (Cont.)

Bit	Name	R/W	Description	Default
14:12	Reserved	RO	Reserved	0
11:10	MPORT_CTRL5	R/W	Multiport 5 Control. 00 = Disable Multiport 5 Forward. 10 = Compare MPORT_ADD5 only; Forward based on MPORT_Vector 5 if matched. 01 = Compare MPORT_ETYPE5 only; Forward based on MPORT_Vector 5 if matched. 11 = Compare MPORT_ETYPE5 and MPORT_ADD5; Forward based on MPORT_Vector 5 if matched.	00
9:8	MPORT_CTRL4	R/W	Multiport 4 Control. 00 = Disable Multiport 4 Forward. 10 = Compare MPORT_ADD4 only; Forward based on MPORT_Vector 4 if matched. 01 = Compare MPORT_ETYPE4 only; Forward based on MPORT_Vector 4 if matched. 11 = Compare MPORT_ETYPE4 and MPORT_ADD4; Forward based on MPORT_Vector 4 if matched.	00
7:6	MPORT_CTRL3	R/W	Multiport 3 Control. 00 = Disable Multiport 3 Forward. 10 = Compare MPORT_ADD3 only; Forward based on MPORT_Vector 3 if matched. 01 = Compare MPORT_ETYPE3 only; Forward based on MPORT_Vector 3 if matched. 11 = Compare MPORT_ETYPE3 and MPORT_ADD3; Forward based on MPORT_Vector 3 if matched.	00
5:4	MPORT_CTRL2	R/W	Multiport 2 Control. 00 = Disable Multiport 2 Forward. 10 = Compare MPORT_ADD2 only; Forward based on MPORT_Vector 2 if matched. 01 = Compare MPORT_ETYPE2 only; Forward based on MPORT_Vector 2 if matched. 11 = Compare MPORT_ETYPE2 and MPORT_ADD2; Forward based on MPORT_Vector 2 if matched.	00
3:2	MPORT_CTRL1	R/W	Multiport 1 Control. 00 = Disable Multiport 1 Forward. 10 = Compare MPORT_ADD1 only; Forward based on MPORT_Vector 1 if matched. 01 = Compare MPORT_ETYPE1 only; Forward based on MPORT_Vector 1 if matched. 11 = Compare MPORT_ETYPE1 and MPORT_ADD1; Forward based on MPORT_Vector 1 if matched.	00

Table 104: Multiport Control Register (Page 04h: Address 0Eh–0Fh) (Cont.)

Bit	Name	R/W	Description	Default
1:0	MPORT_CTRL0	R/W	Multiport 0 Control. 00 = Disable Multiport 0 Forward. 10 = Compare MPORT_ADD0 only; Forward based on MPORT_Vector 0 if matched. 01 = Compare MPORT_ETYPE0 only; Forward based on MPORT_Vector 0 if matched. 11 = Compare MPORT_ETYPE0 and MPORT_ADD0; Forward based on MPORT_Vector 0 if matched.	00

Multiport Address N (N=0–5) Register (Page 04h: Address 10h)

Table 105: Multiport Address Register Address Summary

Address	Description
10h–17h	Multiport ETYPE Address 0
20h–27h	Multiport ETYPE Address 1
30h–37h	Multiport ETYPE Address 2
40h–47h	Multiport ETYPE Address 3
50h–57h	Multiport ETYPE Address 4
60h–67h	Multiport ETYPE Address 5

Table 106: Multiport Address Register (Page 04h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h, 50h–57h, 60h–67h)

Bit	Name	R/W	Description	Default
64:48	MPORT_ETYPE	R/W	Multiport Ethernet Type. Allows a frames with a matching MPORT_ETYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector Register. Must be enabled using the MPORT_CTRL bit in the Multiport Control Register.	0000
47:0	MPORT_ADDR	R/W	Multiport Address. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector Register. Must be enabled using the MPORT_CTRL bit in the Multiport Control Register.	0000000 00000

Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)

Table 107: Multiport Vector Register Address Summary

Address	Description
18h–1Bh	Multiport Vector 0
28h–2Bh	Multiport Vector 1
38h–3Bh	Multiport Vector 2
48h–4Bh	Multiport Vector 3
58h–5Bh	Multiport Vector 4
68h–6Bh	Multiport Vector 5

Table 108: Multiport Vector Register (Page 04h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh, 58h–5Bh, 68h–6Bh)

Bit	Name	R/W	Description	Default
31:9	Reserved	R/O	–	0
8:0	MPORT_VCTR_N	R/W	Multiport Vector. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address Register will be forwarded to each port with a bit set in the Multiport Vector bit map. Bits [5:0] correspond to ports[5:0]. Bit 8 = Management Port (MII Management).	0

Page 05h: ARL/VTBL Access Registers

Table 109: ARL/VTBL Access Registers (Page 05h)

Address	Bits	Register Name
00h	8	“ARL Table Read/Write Control Register (Page 05h: Address 00h)” on page 184
01h–0Fh	–	Reserved
02h–07h	48	“MAC Address Index Register (Page 05h: Address 02h)” on page 184
08h–09h	16	“VLAN ID Index Register (Page 05h: Address 08h)” on page 185
0Ah–0Fh	–	Reserved
10h–17h	64	“ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 185
18h–1Bh	16	“ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h)” on page 186
1Ch–1Fh	–	Reserved

Table 109: ARL/VTBL Access Registers (Page 05h) (Cont.)

Address	Bits	Register Name
20h-27h	64	“ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 185
28h-2Bh	32	“ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h)” on page 186
2Ch-2Fh	–	Reserved
30h-37h	64	“ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 185
38h-3Bh	32	“ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h)” on page 186
3Ch-3Fh	–	Reserved
40h-47h	64	“ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 185
48h-4Bh	32	“ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h)” on page 186
4Ch-4Fh	–	Reserved
50h	8	“ARL Table Search Control Register (Page 05h: Address 50h)” on page 187
51h–52h	16	ARL Search Address
60h–77h	64	“ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)” on page 188
68h–7Bh	32	“ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)” on page 189
7Ch–7Fh	–	Reserved
80h	8	“VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)” on page 190
81h–82h	16	“VLAN Table Address Index Register (Page 05h: Address 81h)” on page 191
83h–86h	32	“VLAN Table Entry Register (Page 05h: Address 83h–86h)” on page 191
67h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

ARL Table Read/Write Control Register (Page 05h: Address 00h)

Table 110: ARL Table Read/Write Control Register (Page 05h: Address 00h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done command. Write as 1 to initiate a read/write command to the ARL table. The bit returns to 0 to indicate that a read/write operation is complete.	0
6:1	Reserved	RO	–	–
0	ARL_R/W	R/W	ARL table read/write bit. Specifies whether the ARL command is a read or write operation. 1 = Read. 0 = Write.	0

For more information, see “Accessing the ARL Table Entries” on page 62.

MAC Address Index Register (Page 05h: Address 02h)

Table 111: MAC Address Index Register (Page 05h: Address 02h–07h)

Bit	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC address index. The ARL table read/write command uses this 48-bit address to index the ARL table. When IEEE 802.1Q is enabled, the ARL table is indexed by a combined hash of the MAC_ADDR_INDX and the VID_TBL_INDX, defined in the “VLAN ID Index Register (Page 05h: Address 08h)” on page 185. For more information, see “Accessing the ARL Table Entries” on page 62.	0

VLAN ID Index Register (Page 05h: Address 08h)

Table 112: VLAN ID Index Register (Page 05h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	–	0
11:0	VID_INDX	R/W	VLAN ID index. When IEEE 802.1Q is enabled, the VLAN ID Index is used with the MAC_ADDR_INDX, defined in the "MAC Address Index Register (Page 05h: Address 02h)" on page 184, to form the hash index for which status is to be read or written. For more information, see "Accessing the ARL Table Entries" on page 62.	0

ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)

Table 113: ARL Table MAC/VID Entry N (N=0-3) Register Address Summary

Address	Description
10h–17h	ARL Table MAC/VID Entry 0
20h–27h	ARL Table MAC/VID Entry 1
30h–37h	ARL Table MAC/VID Entry 2
40h–47h	ARL Table MAC/VID Entry 3

Table 114: ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h)

Bit	Name	R/W	Description	Default
63:60	Reserved	R/O	–	0
59:48	VID_N	R/W	VID entry N. The VID field is either read from or written to the ARL table entry N. The VID is a "don't-care" field when IEEE 802.1Q is disabled.	0
47:0	MACADDR_N	R/W	MAC address entry N. The 48-bit MAC Address field to be either read from or written to the ARL table entry N.	0

Note: Together, the "ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 185 and the "ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h)" on page 186 compose a complete entry in the ARL table. For more information, see "Accessing the ARL Table Entries" on page 62.

ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h)

Table 115: ARL Table Data Entry N (N=0-3) Register Address Summary

Address	Description
18h–1Bh	ARL Table Data Entry 0
28h–2Bh	ARL Table Data Entry 1
38h–3Bh	ARL Table Data Entry 2
48h–4Bh	ARL Table Data Entry 3

Table 116: ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	–	0
16	VALID_N	R/W	Valid bit entry N. Write this bit to 1 to indicate that a valid MAC address is stored in the MACADDR_N field defined in the "ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 185, and that the entry has not aged out. Reset when an entry is empty. This information is read from or written to the ARL table during a read/write command.	0
15	STATIC_N	R/W	Static bit entry N. Write this bit to 1 to indicate that the entry is controlled by the external register control. When cleared, the internal learning and aging process controls the validity of the entry. This information is read from or written to the ARL table during a read/write command.	0
14	AGE_N	R/W	Age bit entry N. Write this bit to 1 to indicate that an address entry has been learned or accessed. This bit is set to 0 by the internal aging algorithm. If the internal aging process detects that a valid entry has remained unused for the period set by the AGE_TIME (defined in the "Aging Time Control Register (Page 02h: Address 06h)" on page 169) and the entry has not been marked as static, the entry has the valid bit cleared. The age bit is ignored if the entry has been marked as Static. This information is read from or written to the ARL table during a read/write command.	0

Table 116: ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh) (Cont.)

Bit	Name	R/W	Description	Default
13:11	TC_N	R/W	TC bit for MAC-based QoS entry N. These bits define the TC field for MAC-based QoS packets. This information is read from or written to the ARL table during a read/write command.	0
10:9	Reserved	R/W	–	–
8:0	FWD_PRT_MAP_N	R/W	Multicast Group Forward portmap entry N. For multicast entries, these bits define the forward port map. Bit 8 = CPU port/MII port. Bits [5:0] correspond to ports [5:0], respectively.	0
	PORTID_N		Unicast Forward PortID entry N. For unicast entries, these bits define the port number associated with the entry of the ARL table. Bits [8:4] = Reserved. Bits [3:0] = Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0

ARL Table Search Control Register (Page 05h: Address 50h)

Table 117: ARL Table Search Control Register (Page 05h: Address 50h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done. Write as 1 to initiate a sequential search of the ARL table. Each entry found by the search is returned to the "ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)" on page 189 and the "ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)" on page 188. Reading the "ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)" on page 189 allows the ARL table search to continue. BCM53125S clears this bit when the ARL table search is complete.	0
6:1	Reserved	RO	–	0
0	ARL_SR_VALID	RC	ARL search result valid. Set by BCM53125S to indicate that an ARL entry is found by the ARL table search. The found entry is available in the "ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)" on page 189. This bit automatically returns to 0 after the ARL Search Result register is read.	0

For more information, see “Accessing the ARL Table Entries” on page 62.

ARL Search Address Register (Page 05h: Address 51h)

Table 118: ARL Search Address Register (Page 05h: Address 51h–52h)

Bit	Name	R/W	Description	Default
15	ARL_ADDR_VALID	R/W (SC)	ARL address valid. Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry that is currently being accessed. Intended for factory test/diagnostic use only.	0
14:0	ARL_ADDR	–	ARL address. 14-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location and is intended for factory test/diagnostic use only.	0

ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)

Table 119: ARL Table Search MAC/VID Result N (N=0-1) Register Address Summary

Address	Description
60h–67h	ARL Table Search MAC/VID Result 0
70h–77h	ARL Table Search MAC/VID Result 1

Table 120: ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h–67h, 70h–77h)

Bit	Name	R/W	Description	Default
63:60	Reserved	RO	–	0
59:48	ARL_SR_VID_N	RO	ARL search VID result. These bits store the VID of the ARL table entry found by the ARL table search function.	0
47:0	ARL_SR_MAC_N	RO	ARL search MAC address result. These bits store the MAC address of the ARL table entry found by the ARL table search function.	N/A

For more information, see “Accessing the ARL Table Entries” on page 62.

ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)

Table 121: ARL Table Search Data Result N (N=0-1) Register Address Summary

Address	Description
68h–6Bh	ARL Table Search Data Result 0
78h–7Bh	ARL Table Search Data Result 1

Table 122: ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	–	0
16	ARL_SR_VALID_N	RO	ARL search valid bit result. This bit stores the valid bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	0
15	ARL_SR_STATIC_N	RO	ARL search static bit result. This bit stores the static bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	N/A
14	ARL_SR_AGE_N	RO	ARL search age bit result. This bit stores the Age bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	–
13:11	ARL_SR_TC_N	RO	ARL search TC bits result. These bits store the TC bits of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	–
10:9	Reserved	RO	–	0

Table 122: ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)

Bit	Name	R/W	Description	Default
8:0	FWD_PRT_MAP_N	R/W	Multicast Group Forward portmap entry N. For multicast entries, these bits define the forward port map. Bit 8 = CPU port/MII port. Bits [5:0] correspond to ports [5:0].	0
	PORTID_N		Unicast Forward PortID entry N. For unicast entries, these bits define the port number associated with the entry of the ARL table. Bits [8:4] = Reserved. Bits [3:0] = Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0

For more information, see "Accessing the ARL Table Entries" on page 62.

VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

Table 123: VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done command. Write as 1 to initiate a read or write or clear-table command to the VLAN table. The bit returns to 0 to indicate that the read or write or clear-table operation is complete.	0
6:2	Reserved	R/W	–	–
1:0	VTBL_R/W/Clr	R/W	Read/Write/Clear-table. Specifies whether the current VLAN table read/write/clear-table command is a read or write or clear-table operation. 11 = Reserved. 10 = Clear-table. 01 = Read. 00 = Write.	0

See "Double Tagging" on page 41 for more information.

VLAN Table Address Index Register (Page 05h: Address 81h)

Table 124: VLAN Table Address Index Register (Page 05h: Address 81h–82h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	–	0
11:0	VTBL_ADDR_INDX	R/W	VLAN table address index. The current VLAN table read/write uses this 12-bit address to index the VLAN table.	–

See "Double Tagging" on page 41 for more information.

VLAN Table Entry Register (Page 05h: Address 83h–86h)

Table 125: VLAN Table Entry Register (Page 05h: Address 83h–86h)

Bit	Name	R/W	Description	Default
31:22	Reserved	RO	–	0
21	FWD_MODE	R/W	This indicates whether the packet forwarding should be based on VLAN membership or based on ARL flow. 1 = Based on VLAN membership (excluding Ingress port). 0 = Based on ARL flow. Note that the VLAN membership based forwarding mode is only used for certain ISP Tagged packets received from ISP port when BCM53125S is operating in Double-Tag mode.	0
20:18	MSPT_INDEX	R/W	Index for 8 spanning trees.	0
17:9	UNTAG_MAP	R/W	Untagged port map. Bit 17 = CPU Port/MII Port. Bits [14:9] correspond to ports [5:0], respectively. Ports written to 1 are designated as untagged VLAN ports. VLAN-tagged frames destined for these ports are untagged before they are forwarded. When the IEEE 802.1Q feature is enabled, frames sent using the CPU (MII port configured as a management port) are tagged. Note that the packet forwarded to IMP port should always be VLAN tagged.	–

Table 125: VLAN Table Entry Register (Page 05h: Address 83h–86h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	FWD_MAP	R/W	Forward PORT MAP. The VLAN-tagged Frame is allowed to be forwarded to the destination ports corresponding bits set in the Map Ports written to 1 are designated as capable of receiving VLAN-tagged frames. Bit 8 = CPU Port/MII Port. Bits [7:6] = Reserved. Bits [5:0] correspond to Ports [5:0], respectively.	–

See "Double Tagging" on page 41 for more information.

Internal Regulator Control Register (Page 0Fh: Address 12h)

Table 126: Internal Regulator Control Register (Page 0Fh: Address 12h)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	–	0x0
3:0	Voltage Setting	R/W	0000 – 1.2V 0001 – 0.975V 0010 – 1.000 0011 – 1.025 0100 – 1.050 0101 – 1.075 0110 – 1.100 0111 – 1.125 1000 – 1.150 1001 – 1.175 1010 – 1.225 1011 – 1.250 1100 – 1.275 1101 – 1.300 1110 – 1.325 1111 – 1.350	0000

Page 10h–14h: Internal GPHY MII Registers

Table 127: 10/100/1000 PHY Page Summary

Page	Description
10h	Port 0 Internal PHY MII Registers
11h	Port 1 Internal PHY MII Registers
12h	Port 2 Internal PHY MII Registers
13h	Port 3 Internal PHY MII Registers
14h	Port 4 Internal PHY MII Registers

Table 128: Register Map (Page 10h–14h)

SPI Offset Address	MII Address	Number of Bits	Register Table
10BASE-T/100BASE-TX/1000BASE-T Registers			
00h	00h	16	Table 129: "MII Control Register (Page 10h–14h: Address 00h–01h)," on page 195
02h	01h	16	Table 130: "MII Status Register (Page 10h–14h: Address 02h–03h)," on page 196
04h–06h	02h	32	Table 131: "PHY Identifier Register MSB (Page 10h–14h: Address 04–07h)," on page 196
08h	04h	16	Table 133: "Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)," on page 197
0Ah	05h	16	Table 134: "Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)," on page 198
0Ch	06h	16	Table 134: "Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)," on page 198
0Eh	07h	16	Table 136: "Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh)," on page 200
10h	08h	16	Table 137: "Link Partner Received Next Page Register (Page 10h–14h: Address 10h–11h)," on page 200
12h	09h	16	Table 138: "1000BASE-T Control Register (Page 10h–14h: Address 12h–13h)," on page 201
14h	0Ah	16	Table 139: "1000BASE-T Status Register (Page 10h–14h: Address 14h–15h)," on page 202
16h–1Dh	–	16	Reserved (Do not read from or write to a reserved register.)
1Eh	0Fh	16	Table 140: "IEEE Extended Status Register (Page 10h–14h: Address 1Eh–1Fh)," on page 203
20h	10h	16	Table 141: "PHY Extended Control Register (Page 10h–14h: Address 20h–21h)," on page 204
22h	11h	16	Table 142: "PHY Extended Status Register (Page 10h–14h: Address 22h–23h)," on page 205

Table 128: Register Map (Page 10h–14h) (Cont.)

SPI Offset Address	MII Address	Number of Bits	Register Table
24h	12h	16	Table 143: "Receive Error Counter Register (Page 10h–14h: Address 24h–25h)," on page 206
26h	13h	16	Table 144: "False Carrier Sense Counter Register (Page 10h–14h: Address 26h–27h)," on page 206
28h	14h	16	Table 146: "Receiver NOT_OK Counter Register (Page 10h–14h: Address 28h–29h)," on page 207
2Ah–2Ch	15h–16h		Reserved (Do not read from or write to a reserved register except for accessing the Expansion registers through register 15h.)
2Eh	17h	16	Reserved
30h	18h	16	Table 151: "Auxiliary Control Register (Page 10h–14h: Address 30h, Shadow Value 000)," on page 208 Table 152: "10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001)," on page 210 Table 153: "Power/MII Control Register (Page 10h–14h: Address 30h, Shadow Value 010)," on page 211 Table 154: "Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100)," on page 211 Table 155: "Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111)," on page 212
32h	19h	16	Table 156: "Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)," on page 213
34h	1Ah	16	Table 157: "Interrupt Status Register (Page 10h–14h: Address 34h–35h)," on page 214
36h	1Bh	16	–
38h	1Ch	16	Table 159: "Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100)," on page 216 Table 159: "Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100)," on page 216 Table 160: "Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010)," on page 216 Table 162: "Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111)," on page 219
3Ah	1Dh	16	Table 163: "Master/Slave Seed Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 0," on page 219 Table 164: "HCD Status Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 1," on page 220
3Ch	1Eh	16	Table 165: "Test Register 1 (Page 10h–14h: Address 3C–3Dh)," on page 222
3Eh	1Fh	16	Reserved (Do not read from or write to a reserved register.)
Expansion registers: Read/Write through register 2Ah (accessed by writing to register 2Eh, bits [11:0] = 1111 + expansion register number)			

MII Control Register (Page 10h–14h: Address 00h–01h)

Table 129: MII Control Register (Page 10h–14h: Address 00h–01h)

Bit	Name	R/W	Description	Default
15	Reset	R/W SC	1 = PHY reset. 0 = Normal operation.	0
14	Internal Loopback	R/W	1 = Loopback mode. 0 = Normal operation.	0
13	Speed Selection (LSB)	R/W	Bits [6,13]: 11 = Reserved. 10 = 1000 Mbps. 01 = 100 Mbps. 00 = 10 Mbps.	0
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation is enabled. 0 = Auto-negotiation is disabled.	1
11	Power Down	R/W	1 = Power-down. 0 = Normal operation.	0
10	Isolate	R/W	1 = Electrically isolate PHY from GMII. 0 = Normal operation.	0
9	Restart Auto-negotiation	R/W SC	1 = Restarting auto-negotiation. 0 = Auto-negotiation restart is complete.	0
8	Duplex Mode	R/W	1 = Full duplex. 0 = Half duplex.	1
7	Collision Test Enable	R/W	1 = Enable the collision test mode. 0 = Disable the collision test mode.	0
6	Speed Selection (MSB)	R/W	Works in conjunction with bit 13.	1
5	Reserved	R/W	Write as 0, ignore on read.	0
4	Reserved	R/W	Write as 0 ignore on read.	0
3	Reserved	R/W	Write as 0 ignore on read.	0
2	Reserved	R/W	Write as 0 ignore on read.	0
1	Reserved	R/W	Write as 0 ignore on read.	0
0	Reserved	R/W	Write as 0 ignore on read.	0

MII Status Register (Page 10h–14h: Address 02h)

Table 130: MII Status Register (Page 10h–14h: Address 02h–03h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capable	RO L	1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable	0
14	100BASE-X Full-Duplex Capable	RO H	1 = 100BASE-X full-duplex capable. 0 = Not 100BASE-X full-duplex capable.	1
13	100BASE-X Half-Duplex Capable	RO H	1 = 100BASE-X half-duplex capable. 0 = Not 100BASE-X half-duplex capable.	1
12	10BASE-T Full-Duplex Capable	RO H	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	1
11	10BASE-T Half-Duplex Capable	RO H	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	1
10	100BASE-T2 Full-Duplex Capable	RO L	1 = 100BASE-T2 full-duplex capable. 0 = Not 100BASE-T2 full-duplex capable.	0
9	100BASE-T2 Half-Duplex Capable	RO L	1 = 100BASE-T2 half-duplex capable. 0 = Not 100BASE-T2 half-duplex capable.	0
8	Extended Status	RO H	1 = Extended status information in reg 0Fh. 0 = No extended status information in reg 0Fh.	1
7	Reserved	RO	Ignore on read.	0
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed. 0 = Preamble always required.	1
5	Auto-negotiation Complete	RO	1 = Auto-negotiation is complete. 0 = Auto-negotiation is in progress.	0
4	Remote Fault	RO LH	1 = Remote fault detected. 0 = No remote fault detected.	0
3	Auto-negotiation Ability	RO H	1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	1
2	Link Status	RO LL	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0
1	Jabber Detect	RO LH	1 = Jabber condition detected. 0 = No jabber condition detected.	0
0	Extended Capability	RO H	1 = Extended register capabilities. 0 = No extended register capabilities.	1

PHY Identifier Register (Page 10h–14h: Address 04h)

Table 131: PHY Identifier Register MSB (Page 10h–14h: Address 04–07h)

Bit	Name	R/W	Description	Default
15:0	OUI	RO	Bits 3:18 of organizationally unique identifier	0x362 (hex)

Table 132: PHY Identifier Register LSB (Page 10h–14h: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:10	OUI	RO	Bits 19:24 of organizationally unique identifier	010111
9:4	MODEL	RO	Device model number	110010
3:0	REVISION	RO	Device revision number	n[a] (hex)

a. The revision number (*n*) changes with each silicon revision.

The IEEE has issued an Organizationally Unique Identifier (OUI) to Broadcom Corporation. This 24-bit number allows devices developed by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], six manufacturer's model number bits, and four revision number bits. The two
least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-0A-F7, expressed as hexadecimal values. The binary OUI is 0000-0000-0000-1010-1111-0111. The model number for BCM53125S is 38h. Revision numbers start with 0h and increment by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision [3:0]

Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h)

Table 133: Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next page ability is supported. 0 = Next page ability is not supported.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Remote Fault	R/W	1 = Advertise remote fault is detected. 0 = Advertise no remote fault is detected.	0
12	Reserved Technology	R/W	Write as 0, ignore on read.	0
11	Asymmetric Pause	R/W	1 = Advertise asymmetric pause. 0 = Advertise no asymmetric pause.	1
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation. 0 = Incapable of pause operation.	1
9	100BASE-T4 Capable	R/W	1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable.	0

Table 133: Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h) (Cont.)

Bit	Name	R/W	Description	Default
8	100BASE-TX Full-Duplex Capable	R/W	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	1
7	100BASE-TX Half-Duplex Capable	R/W	1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	1
6	10BASE-T Full-Duplex Capable	R/W	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	1
5	10BASE-T Half-Duplex Capable	R/W	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	1
4	Protocol Selector Field	R/W	Bits [4:0] = 00001 indicates IEEE 802.3 CSMA/CD.	0
3		R/W		0
2		R/W		0
1		R/W		0
0		R/W		1

Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah)

Table 134: Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)

Bit(s)	Name	R/W	Description	Default
15	Next Page	RO	1 = Link partner has next page ability. 0 = Link partner does not have next page ability.	0
14	Acknowledge	RO	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	0
13	Remote Fault	RO	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0
12	Reserved Technology	RO	Write as 0, ignore on read.	0
11	Link Partner Asymmetric Pause	RO	1 = Link partner wants asymmetric pause. 0 = Link partner does not want asymmetric pause.	0
10	Pause Capable	RO	1 = Link partner is capable of pause operation. 0 = Link partner is incapable of pause operation.	0
9	100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable. 0 = Link partner is not 100BASE-T4 capable.	0
8	100BASE-TX Full-Duplex Capable	RO	1 = Link partner is 100BASE-TX full-duplex capable. 0 = Link partner is not 100BASE-TX full-duplex capable.	0
7	100BASE-TX Half-Duplex Capable	RO	1 = Link partner is 100BASE-TX half-duplex capable. 0 = Link partner not 100BASE-TX half-duplex capable.	0

Table 134: Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh) (Cont.)

Bit(s)	Name	R/W	Description	Default
6	10BASE-T Full-Duplex Capable	RO	1 = Link partner is 10BASE-T full-duplex capable. 0 = Link partner is not 10BASE-T full-duplex capable.	0
5	10BASE-T Half-Duplex Capable	RO	1 = Link partner is 10BASE-T half-duplex capable. 0 = Link partner is not 10BASE-T half-duplex capable.	0
4:0	Protocol Selector Field	RO	Link partner protocol selector field.	0

Note: As indicated by bit 5 of the 10BASE-T/100BASE-TX/1000BASE-T MII Status register, the values contained in the 10BASE-T/100BASE-TX/1000BASE-T Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

Next Page

BCM53125S returns a 1 in bit 15 when the link partner wants to transmit Next Page information.

Acknowledge

BCM53125S returns a 1 in bit 14 when the link partner has acknowledged reception of the link code word; otherwise, BCM53125S returns a 0.

Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch)

Table 135: Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15	Reserved	R0	Ignore on read.	0
14	Reserved	R0	Ignore on read.	0
13	Reserved	R0	Ignore on read.	0
12	Reserved	R0	Ignore on read.	0
11	Reserved	R0	Ignore on read.	0
10	Reserved	R0	Ignore on read.	0
9	Reserved	R0	Ignore on read.	0
8	Reserved	R0	Ignore on read.	0
7	Reserved	R0	Ignore on read.	0
6	Next Page Receive Location Able	R/W	1 = Bit 5 in register 06h determines next page receive location. 0 = Bit 5 in register 06h does not determine next page receive location.	1
5	Next Page Receive Location	R/W	1 = Next pages stored in register 08h. 0 = Next pages stored in register 05h.	1

Table 135: Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh) (Cont.)

Bit	Name	R/W	Description	Default
4	Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
3	Link Partner Next Page Ability	RO	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	0
2	Next Page Capable	RO H	1 = BCM53125S is next page capable. 0 = BCM53125S is not next page capable.	1
1	Page Received	RO LH	1 = New page has been received from link partner. 0 = New page has not been received.	0
0	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not have auto-negotiation.	0

Next Page Transmit Register (Page 10h–14h: Address 0Eh)

Table 136: Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional next pages follow. 0 = Sending last next page.	0
14	Reserved	RO	Ignore on read.	0
13	Message Page	R/W	1 = Formatted page. 0 = Unformatted page.	1
12	Acknowledge2	R/W	1 = Complies with message. 0 = Cannot comply with message. ***Note:*** Not used with 1000BASE-T next pages.	0
11	Toggle	RO	Toggles between exchanges of different next pages.	0
10:1	Message/Unformatted Code Field	R/W	Next page message code or unformatted data.	0
0				1

Link Partner Received Next Page Register (Page 10h–14h: Address 10h)

Table 137: Link Partner Received Next Page Register (Page 10h–14h: Address 10h–11h)

Bit(s)	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional next pages follow. 0 = Sending last next page.	0
14	Acknowledge	RO	1 = Acknowledge. 0 = No acknowledge.	0

Table 137: Link Partner Received Next Page Register (Page 10h–14h: Address 10h–11h) (Cont.)

Bit(s)	Name	R/W	Description	Default
13	Message Page	RO	1 = Formatted page. 0 = Unformatted page.	0
12	Acknowledge2	RO	1 = Complies with message. 0 = Cannot comply with message. ***Note:*** Not used with 1000BASE-T next pages.	0
11	Toggle	RO	Toggles between exchanges of different next pages.	0
10:0	Message code field	RO	Next page message code or unformatted data.	0

1000BASE-T Control Register (Page 10h–14h: Address 12h)

Table 138: 1000BASE-T Control Register (Page 10h–14h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:13	Test Mode	R/W	1 X X = Test mode 4—Transmitter distortion test. 0 1 1 = Test mode 3—Slave transmit jitter test. 0 1 0 = Test mode 2—Master transmit jitter test. 0 0 1 = Test mode 1—Transmit waveform test. 0 0 0 = Normal operation.	0
12	Master/Slave Configuration Enable	R/W	1 = Enable master/slave manual configuration value. 0 = Automatic master/slave configuration.	0
11	Master/Slave Configuration Value	R/W	1 = Configure PHY as master. 0 = Configure PHY as slave.	1
10	Repeater/DTE	R/W	1 = Repeater/switch device port. 0 = DTE device.	1
9	Advertise 1000BASE-T Full-Duplex Capability	R/W	1 = Advertise 1000BASE-T full-duplex capability. 0 = Advertise no 1000BASE-T full-duplex capability.	1
8	Advertise 1000BASE-T Half-Duplex Capability	R/W	1 = Advertise 1000BASE-T half-duplex capability. 0 = Advertise no 1000BASE-T half-duplex capability.	1
7	Reserved	RO	Ignore on read.	0
6	Reserved	RO	Ignore on read.	0
5	Reserved	RO	Ignore on read.	0
4	Reserved	RO	Ignore on read.	0
3	Reserved	RO	Ignore on read.	0
2	Reserved	RO	Ignore on read.	0
1	Reserved	RO	Ignore on read.	0
0	Reserved	RO	Ignore on read.	0

Test Mode

The BCM53125S can be placed in 1 of 4 transmit test modes by writing bits [15:13] of the 1000BASE-T Control register. The transmit test modes are defined in IEEE 802.3ab. When read, these bits return the last value written. For test modes 1, 2, and 4, the PHY must have auto-negotiation disabled and forced to 1000BASE-T mode and Auto-MDIX disabled.

- Disable auto-negotiation and force to 1000BASE-T mode (write to register 00h = 0x0040)
- Disable Auto-MDIX (write to register 18h, shadow value 111, bit 9 = 0)
- Enter test modes (write to register 09h, bits [15:13] = the desired test mode)

Master/Slave Configuration Enable

When bit 12 is set = 1, the BCM53125S master/slave mode is configured using the manual master/slave configuration value. When the bit is cleared, the master/slave mode is configured using the automatic resolution function. This bit returns a 1 when manual master/slave configuration is enabled; otherwise, it returns a 0.

1000BASE-T Status Register (Page 10h–14h: Address 14h)

Table 139: 1000BASE-T Status Register (Page 10h–14h: Address 14h–15h)

Bit	Name	R/W	Description	Default
15	Master/Slave Configuration Fault	RO LH	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	0
14	Master/Slave Configuration Resolution	RO	1 = Local transmitter is master. 0 = Local transmitter is slave.	0
13	Local Receiver Status	RO	1 = Local receiver is OK. 0 = Local receiver is not OK.	0
12	Remote Receiver Status	RO	1 = Remote receiver is OK. 0 = Remote receiver is not OK.	0
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	1 = Link partner is 1000BASE-T full-duplex capable. 0 = Link partner is not 1000BASE-T full-duplex capable.	0
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	1 = Link partner is 1000BASE-T half-duplex capable. 0 = Link partner is not 1000BASE-T half-duplex capable.	0
9	Reserved	RO	Ignore on read.	0
8	Reserved	RO	Ignore on read.	0

Table 139: 1000BASE-T Status Register (Page 10h–14h: Address 14h–15h) (Cont.)

Bit	Name	R/W	Description	Default
7	Idle Error Count	RO CR	Number of idle errors since last read.	0
6		RO CR		0
5		RO CR		0
4		RO CR		0
3		RO CR		0
2		RO CR		0
1		RO CR		0
0		RO CR		0

Note: As indicated by bit 5 of the MII Status register (0h), the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

IEEE Extended Status Register (Page 10h–14h: Address 1Eh)

Table 140: IEEE Extended Status Register (Page 10h–14h: Address 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15	1000BASE-X Full-Duplex Capable	RO L	1 = 1000BASE-X full-duplex capable. 0 = Not 1000BASE-X full-duplex capable.	0
14	1000BASE-X Half-Duplex Capable	RO L	1 = 1000BASE-X half-duplex capable. 0 = Not 1000BASE-X half-duplex capable.	0
13	1000BASE-T Full-Duplex Capable	RO H	1 = 1000BASE-T full-duplex capable. 0 = Not 1000BASE-T full-duplex capable.	1
12	1000BASE-T Half-Duplex Capable	RO H	1 = 1000BASE-T half-duplex capable. 0 = Not 1000BASE-T half-duplex capable.	1
11	Reserved	RO	Ignore on read.	0
10	Reserved	RO	Ignore on read.	0
9	Reserved	RO	Ignore on read.	0
8	Reserved	RO	Ignore on read.	0
7	Reserved	RO	Ignore on read.	0
6	Reserved	RO	Ignore on read.	0

Table 140: IEEE Extended Status Register (Page 10h–14h: Address 1Eh–1Fh) (Cont.)

Bit	Name	R/W	Description	Default
5	Reserved	RO	Ignore on read.	0
4	Reserved	RO	Ignore on read.	0
3	Reserved	RO	Ignore on read.	0
2	Reserved	RO	Ignore on read.	0
1	Reserved	RO	Ignore on read.	0
0	Reserved	RO	Ignore on read.	0

PHY Extended Control Register (Page 10h–14h: Address 20h)

Table 141: PHY Extended Control Register (Page 10h–14h: Address 20h–21h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	Disable Automatic MDI Crossover	R/W	1 = Automatic MDI crossover is disabled. 0 = Automatic MDI crossover is enabled.	0
13	Transmit Disable	R/W	1 = Transmitter outputs are disabled. 0 = Normal operation.	0
12:11	Reserved	–	–	–
10	Bypass 4B/5B Encoder/ Decoder (100BASE-TX)	R/W	1 = Transmit and receive 5B codes over MII pins. 0 = Normal MII.	0
9	Bypass Scrambler/Descrambler (100BASE-TX)	R/W	1 = Scrambler and descrambler are disabled. 0 = Scrambler and descrambler are enabled.	0
8	Bypass NRZI/MLT3 Encoder/ Decoder (100BASE-TX)	R/W	1 = Bypass NRZI/MLT3 encoder and decoder. 0 = Normal operation.	0
7	Bypass Receive Symbol Alignment (100BASE-TX)	R/W	1 = The 5B receive symbols are not aligned. 0 = Receive symbols aligned to 5B boundaries.	0
6	Reset Scrambler (100BASE-TX)	R/W SC	1 = Reset scrambler to initial state. 0 = Normal scrambler operation.	0
5:3	Reserved	–	–	–
2	Reserved	R/W	Write as 0, ignore on read.	0
1	Reserved	R/W	Write as 0, ignore on read.	0
0	1000 Mbps PCS Transmit FIFO Elasticity	R/W	1 = High latency. 0 = Low latency.	0

PHY Extended Status Register (Page 10h–14h: Address 22h)

Table 142: PHY Extended Status Register (Page 10h–14h: Address 22h–23h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Base Page Selector Field Mismatch	RO LH	1 = Link partner base page selector field mismatched advertised selector field since last read. 0 = No mismatch detected since last read.	0
14	Ethernet@Wirespeed™ Downgrade	RO	1 = Auto-negotiation advertised speed downgraded. 0 = No advertised speed downgrade.	0
13	MDI Crossover State	RO	1 = Crossover MDI mode. 0 = Normal MDI mode.	0
12	Interrupt Status	RO	1 = Unmasked interrupt is currently active. 0 = Interrupt is cleared.	0
11	Remote Receiver Status	RO LL	1 = Remote receiver is OK. 0 = Remote receiver is not OK since last read.	0
10	Local Receiver Status	RO LL	1 = Local receiver is OK. 0 = Local receiver is not OK since last read.	0
9	Locked	RO	1 = Descrambler is locked. 0 = Descrambler is unlocked.	0
8	Link Status	RO	1 = Link pass 0 = Link fail	0
7	CRC Error Detected	RO LH	1 = CRC error detected. 0 = No CRC error since last read.	0
6	Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read. 0 = No carrier extension error since last read.	0
5	Bad SSD Detected (False Carrier)	RO LH	1 = Bad SSD error detected since last read. 0 = No bad SSD error since last read.	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read. 0 = No bad ESD error since last read.	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read. 0 = No receive error since last read.	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read. 0 = No transmit error code received since last read.	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read. 0 = No lock error since last read.	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read. 0 = No MLT3 code error since last read.	0

Receive Error Counter Register (Page 10h–14h: Address 24h)

Table 143: Receive Error Counter Register (Page 10h–14h: Address 24h–25h)[a]

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W CR	Number of noncollision packets with receive errors since last read.	0000h

a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, 1000BASE-T Receive Error Counter when register 38h, shadow value11011, bit 9 = 0.

Copper Receive Error Counter

When bit 9 = 0 in register 38h, shadow value 11011, this counter increments each time BCM53125S receives a 10BASE-T, 100BASE-TX, 1000BASE-T noncollision packet containing at least one receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

False Carrier Sense Counter Register (Page 10h–14h: Address 26h)

Table 144: False Carrier Sense Counter Register (Page 10h–14h: Address 26h–27h)[a]

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	00h
7:0	False Carrier Sense Counter	R/W CR	Number of false carrier sense events since last read.	00h

a. Bits 7:0 of this register become the 10BASE-T/100BASE-TX/1000BASE-T Carrier Sense Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch, bit 14 = 0.

Copper False Carrier Sense Counter

When bit 9 = 0 in register 1Ch, shadow value 11011 and bit 14 = 0 in register 3Ch, the False Carrier Sense Counter increments each time the BCM53125S detects a 10BASE-T, 100BASE-TX, 1000BASE-T false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

10BASE-T/100BASE-TX/1000BASE-T Packets Received with Transmit Error Codes Counter

Table 145: 10BASE-T/100BASE-TX/1000BASE-T Transmit Error Code Counter Register (Address 13h)[a]

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, ignore on read.	00h
7:0	Transmit Error Code Counter	R/W CR	Number of packets received with transmit error codes since last read.	00h

a. Bits 7:0 of this register become the 10BASE-T/100BASE-TX/1000BASE-T packets received with transmit error codes counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch, bit 14 = 1.

Packets Received with Transmit Error Codes Counter

BCM53125S detects a 10BASE-T/100BASE-TX/1000BASE-T packet with a transmit error code violation when bit 9 = 0 in register 38h, shadow value 11011, and when bit 14 = 1 in register 1Eh, Packets Received with Transmit Error Codes Counter increments each time. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Receiver NOT_OK Counter Register (Page 10h–14h: Address 28h)

Table 146: Receiver NOT_OK Counter Register (Page 10h–14h: Address 28h–29h)[a]

Bit	Name	R/W	Description	Default
15:8	Local Receiver NOT_OK Counter	R/W CR	Number of times local receiver was NOT_OK since last read.	00h
7:0	Remote Receiver NOT_OK Counter	R/W CR	Number of times BCM53125S detected that the remote receiver was NOT_OK since last read.	00h

a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, or 1000BASE-T Receiver NOT_OK Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch bit 15 = 0.

Copper Local Receiver NOT_OK Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 0 in register 3Ch, this counter increments each time the 10BASE-T, 100BASE-TX, or 1000BASE-T local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Copper Remote Receiver NOT_OK Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 0 in register 3Ch, this counter increments each time the 1000BASE-T, 100BASE-TX, or 10BASE-T remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Receive CRC Counter Register (Page 10h–14h: Address 28h)

Table 147: CRC Counter Register (Page 10h–14h: Address 28h–29h)[a]

Bit	Name	R/W	Description	Default
15:0	Receive CRC Counter	R/W CR	Number of times receive CRC errors were detected.	00h

a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, or 1000BASE-T Receive CRC Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch bit 15 = 1.

Copper CRC Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 1 in register 3Ch, this counter increments each time the 10BASE-T, 100BASE-TX, or 1000BASE-T detects a receive CRC error. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Auxiliary Control Shadow Value Access Register (Page 10h–14h: Address 30h)

Available 30h registers are listed in the Table 148.

Table 148: Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)

Shadow Value	*Register Name*
000	”Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)” on page 208
001	”10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001)” on page 210
010	”Power/MII Control Register (Page 10h–14h: Address 30h, Shadow Value 010)” on page 211
100	”Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100)” on page 211
111	”Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111)” on page 212

Read from register 30h, shadow value zzz.

Table 149: Reading Register 30h

Register Reads/Writes	*Description*
Write register 30h, bits [2:0] = 111	This selects the miscellaneous control register, shadow value 111. All reads must be done through the miscellaneous control register.
Bit 15 = 0	This allows only bits [14:12] and bits [2:0] to be written.
Bits [14:12] = zzz	This selects shadow value register zzz to be read.
Bits [11: 3] = <don't care>	When bit 15 = 0, these bits will be ignored.
Bits [2:0] = 111	This sets the shadow register select to 111 (miscellaneous control register).
Read register 30h	Data read back is the value from shadow register zzz.

Write to register 30h, shadow value yyy.

Table 150: Writing Register 30h

Register Writes	*Description*
Set Bits [15:3] = Preferred write values	Bits [15:3] contain the values to which the desired bits are written.
Set Bits [2:0] = yyy	This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written.

Table 151: Auxiliary Control Register (Page 10h–14h: Address 30h, Shadow Value 000)

Bit	*Name*	*R/W*	*Description*	*Default*
15	External Loopback	R/W	1 = External Loopback is enabled. 0 = Normal operation.	0

Table 151: Auxiliary Control Register (Page 10h–14h: Address 30h, Shadow Value 000) (Cont.)

Bit	Name	R/W	Description	Default
14	Receive Extended Packet Length	R/W	1 = Allow reception of extended length packets. 0 = Allow reception of normal length Ethernet packets only.	0
13	Edge Rate Control (1000BASE-T)	R/W	00 = 4.0 ns. 01 = 5.0 ns. 10 = 3.0 ns. 11 = 0.0 ns.	0
12		R/W		0
11	Reserved	R/W	Write as 0, ignore on read.	0
10	Reserved	R/W	Write as 1, ignore on read.	1
9	Reserved	R/W	Write as 0, ignore on read.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	Reserved	R/W	Write as 0, ignore on read.	0
5	Edge Rate Control (100BASE-TX)	R/W	00 = 4.0 ns. 01 = 5.0 ns. 10 = 3.0 ns. 11 = 0.0 ns.	0
4		R/W		0
3	Reserved	R/W	Write as 0, ignore on read.	0
2	Shadow Register Select	R/W	000 = Auxiliary control register. 001 = 10BASE-T register. 010 = Power/MII control register. 100 = Miscellaneous test register. 111 = Miscellaneous control register.	0
1		R/W		0
0		R/W		0

External Loopback

When bit 15 = 1, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

Receive Extended Packet Length

When bit 14 = 1, BCM53125S can receive packets up to 9720 bytes in length when in SGMII mode.

When the bit is cleared, the BCM53125S only receives packets up to standard maximum size in length.

Edge Rate Control (1000BASE-T)

Bits [13:12] control the edge rate of the 1000BASE-T transmit DAC output waveform.

Edge Rate Control (100BASE-TX)

Bits [5:4] control the edge rate of the 100BASE-TX transmit DAC output waveform.

Shadow Register Select

See the note on "Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)" on page 208 describing reading from and writing to register 18h.

The register set shown above is that for normal operation obtained when the lower 3 bits are 000.

10BASE-T Register

Table 152: 10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001)

Bit	Name	R/W	Description	Default
15	Manchester Code Error	RO LH	1 = Manchester code error (10BASE-T). 0 = No Manchester code error.	0
14	EOF Error	RO LH	1 = EOF error is detected (10BASE-T). 0 = No EOF error is detected.	0
13	Polarity Error	RO	1 = Channel polarity is inverted. 0 = Channel polarity is correct.	0
12	Block RX_DV Extension (IPG)	R/W	1 = Block RX_DV for four additional RXC cycles for IPG. 0 = Normal operation.	0
11	10BASE-T TXC Invert Mode	R/W	1 = Invert TXC output. 0 = Normal operation.	0
10	Reserved	R/W	Write as 0, ignore on read.	0
9	Jabber Disable	R/W	1 = Jabber function is disabled. 0 = Jabber function is enabled.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	10BASE-T Echo Mode	R/W	1 = Echo transmit data to receive data. 0 = Normal operation.	0
5	SQE Enable Mode	R/W	1 = Enable SQE. 0 = Disable SQE.	0
4	10BASE-T No Dribble	R/W	1 = Correct 10BASE-T dribble nibble. 0 = Normal operation.	0
3	Reserved	R/W	Write as 0, ignore on read.	0
2	Shadow Register Select	R/W	000 = Auxiliary control register.	0
1		R/W	001 = 10BASE-T register.	0
0		R/W	010 = Power/MII control register. 100 = Miscellaneous test register. 111 = Miscellaneous control register.	1

Power/MII Control Register (Page 10h–14h: Address 30h)

Table 153: Power/MII Control Register (Page 10h–14h: Address 30h, Shadow Value 010)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Reserved	R/W	Write as 0, ignore on read.	0
12	Reserved	R/W	Write as 0, ignore on read.	0
11	Reserved	R/W	Write as 0, ignore on read.	0
10:7	Reserved	–	–	–
6	Reserved	R/W	Write as 0, ignore on read.	1
5	Super Isolate (Copper Only)	R/W	1 = Isolate mode with no link pulses transmitted. 0 = Normal operation.	1
4	Reserved	R/W	Write as 0, ignore on read.	0
3	Reserved	R/W	Write as 0, ignore on read.	0
2	Shadow Register Select	R/W	000 = Auxiliary control register.	0
1		R/W	001 = 10BASE-T register.	1
0		R/W	010 = Power/MII control register. 100 = Miscellaneous test register. 111 = Miscellaneous control register.	0

Super Isolate (Copper Only)

Setting bit 5 = 1, places the BCM53125S into the super isolate mode.

Shadow Register Select

See the note on "Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)" on page 208 describing reading from and writing to register 30h.

Miscellaneous Test Register (Page 10h–14h: Address 30h)

Table 154: Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100)

Bit	Name	R/W	Description	Default
15	Lineside [Remote] Loopback Enable	R/W	1 = Enable lineside [remote] loopback. 0 = Disable loopback.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Reserved	R/W	Write as 0, ignore on read.	0
12	Reserved	R/W	Write as 0, ignore on read.	0
11	Reserved	R/W	Write as 0, ignore on read.	0
10	Reserved	R/W	Write as 0, ignore on read.	0

Table 154: Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100) (Cont.)

Bit	Name	R/W	Description	Default
9	Reserved	R/W	Write as 0, ignore on read.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	Reserved	R/W	Write as 0, ignore on read.	0
5	Reserved	R/W	Write as 0, ignore on read.	0
4	Swap RX MDIX	R/W	1 = RX and TX operate on same pair. 0 = Normal operation.	0
3	10BASE-T Halfout	R/W	1 = Transmit 10BASE-T at half amplitude. 0 = Normal operation.	0
2	Shadow Register Select	R/W	000 = Auxiliary control register. 001 = 10BASE-T register. 010 = Power/MII control register. 100 = Miscellaneous test register. 111 = Miscellaneous control register.	1
1		R/W		0
0		R/W		0

Miscellaneous Control Register (Page 10h–14h: Address 30h)

Table 155: Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W SC	1 = Write bits [14:3]. 0 = Only write bits [14:12].	0
14	Shadow Register Read Selector	R/W	These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read. 000 = Normal operation. 001 = 10BASE-T register. 010 = Power control register. 100 = Miscellaneous test register. 111 = Miscellaneous control register.	0
13		R/W		0
12		R/W		0
11	Packet Counter Mode	R/W	1 = Receive packet counter. 0 = Transmit packet counter.	0
10	Reserved	R/W	Write as 0, ignore on read.	0
9	Force Auto-MDIX Mode	R/W	1 = Auto-MDIX is enabled when auto-negotiation is disabled. 0 = Auto-MDIX is disabled when auto-negotiation is disabled.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	Reserved	R/W	Write as 0, ignore on read.	0
5	Reserved	R/W	Write as 0, ignore on read.	0

Table 155: Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111) (Cont.)

Bit	Name	R/W	Description	Default
4	Ethernet@WireSpeed Enable	R/W	1 = Enable Ethernet@WireSpeed. 0 = Disable Ethernet@WireSpeed.	1
3	MDIO All PHY Select	R/W	1 = The PHY ports accepts MDIO writes to PHY address = 00000. 0 = Normal operation.	0
2	Shadow Register Select	R/W	000 = Auxiliary control register.	1
1		R/W	001 = 10BASE-T register.	1
0		R/W	010 = Power/MII control register. 100 = Miscellaneous test register. 111 = Miscellaneous control register.	1

Auxiliary Status Summary Register (Page 10h–14h: Address 32h)

Table 156: Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Complete	RO	1 = Auto-negotiation is complete. 0 = Auto-negotiation is in progress.	0
14	Auto-negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link is good check state. 0 = State not entered since last read.	0
13	Auto-negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state. 0 = State not entered since last read.	0
12	Auto-negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state. 0 = State not entered since last read.	0
11	Auto-negotiation Next Page Wait	RO LH	1 = Entered auto-negotiation next page wait state. 0 = State not entered since last read.	0
10	Auto-negotiation HCD Current Operating Speed and Duplex Mode	RO	111 = 1000BASE-T full-duplex[a]	0
9		RO	110 = 1000BASE-T half-duplex[a]	0
8		RO	101 = 100BASE-TX full-duplex[a] 100 = 100BASE-T4. 011 = 100BASE-TX half-duplex[a] 010 = 10BASE-T full-duplex[a] 001 = 10BASE-T half-duplex[a] 000 = No highest common denominator or auto-negotiation is incomplete.	0
7	Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
6	Remote Fault	RO	1 = Link partner has detected a remote fault. 0 = Link partner has not detected a remote fault.	0

Table 156: Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h) (Cont.)

Bit	Name	R/W	Description	Default
5	Auto-negotiation Page Received	RO LH	1 = New page has been received from the link partner. 0 = New page has not been received.	0
4	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not perform auto-negotiation.	0
3	Link Partner Next Page Ability	RO	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	0
2	Link Status	RO	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0
1	Pause Resolution—Receive Direction	RO	1 = Enable pause receive. 0 = Disable pause receive.	0
0	Pause Resolution—Transmit Direction	RO	1 = Enable pause transmit. 0 = Disable pause transmit.	0

a. Indicates the negotiated HCD when Auto-negotiation Enable = 1, or indicates the manually selected speed and duplex mode when Auto-negotiation Enable = 0.

Interrupt Status Register (Page 10h–14h: Address 34h)

Table 157: Interrupt Status Register (Page 10h–14h: Address 34h–35h)

Bit	Name	R/W	Description	Default
15	Energy Detect Change	RO LH	1 = Energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1). 0 = Interrupt cleared.	0
14	Illegal Pair Swap	RO LH	1 = Illegal pair swap is detected. 0 = Interrupt cleared.	0
13	MDIX Status Change	RO LH	1 = MDIX status changed since last read. 0 = Interrupt cleared.	0
12	Exceeded High Counter Threshold	RO	1 = Value in one or more counters is above 32K. 0 = All counters below are 32K.	0
11	Exceeded Low Counter Threshold	RO	1 = Value in one or more counters is above 128K. 0 = All counters below are 128K.	0
10	Auto-negotiation Page Received	RO LH	1 = Page received since last read. 0 = Interrupt cleared.	0
9	No HCD Link	RO LH	1 = Negotiated HCD, did not establish link. 0 = Interrupt cleared.	0
8	No HCD	RO LH	1 = Auto-negotiation returned HCD = none. 0 = Interrupt cleared.	0
7	Negotiated Unsupported HCD	RO LH	1 = Auto-negotiation HCD is not supported by BCM53125S. 0 = Interrupt cleared.	0

Table 157: Interrupt Status Register (Page 10h–14h: Address 34h–35h) (Cont.)

Bit	Name	R/W	Description	Default
6	Scrambler Synchronization Error	RO LH	1 = Scrambler synchronization error occurred since last read. 0 = Interrupt cleared.	0
5	Remote Receiver Status Change	RO LH	1 = Remote receiver status changed since last read. 0 = Interrupt cleared.	0
4	Local Receiver Status Change	RO LH	1 = Local receiver status changed since last read. 0 = Interrupt cleared.	0
3	Duplex Mode Change	RO LH	1 = Duplex mode changed since last read. 0 = Interrupt cleared.	0
2	Link Speed Change	RO LH	1 = Link speed changed since last read. 0 = Interrupt cleared.	0
1	Link Status Change	RO LH	1 = Link status changed since last read. 0 = Interrupt cleared.	0
0	Receive CRC Error	RO LH	1 = Receive CRC error occurred since last read. 0 = Interrupt cleared.	0

The INTR LED output is asserted when any bit in 10BASE-T/100BASE-TX/1000BASE-T interrupt status register is set and the corresponding bit in the 10BASE-T/100BASE-TX/1000BASE-T interrupt mask register is cleared.

10BASE-T/100BASE-TX/1000BASE-T Register 38h Access

Reading from and writing to 10BASE-T/100BASE-TX/1000BASE-T register 38h is though register 38h bits [15:10]. The bits [14:10] set the shadow value of register 38h, and bit 15 enables the writing of the bits [9:0]. Setting bit 15 allows writing to bits [9:0] of register 38h. Before reading register 38h shadow zzzzz, writes to register 38h should be set with bit 15 = 0, and bits [14:10] to zzzzz. The subsequent register read from register 38h contains the shadow zzzzz register value. Table 158 lists all the register 38h shadow values.

Table 158: 10BASE-T/100BASE-TX/1000BASE-T Register 38h Shadow Values

Shadow Value	Register Name
00100	”Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100)” on page 216
00101	–
01000	–
01001	–
01010	”Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010)” on page 216
01101	–
01110	”LED Selector 2 Register (Page 10h–14h: Address 38h, Shadow Value 01110)” on page 217
11111	”Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111)” on page 219

Spare Control 2 Register (Page 10h–14h: Address 38h)

Table 159: Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0]. 0 = Read bits [9:0].	0
14	Shadow Register Selector	R/W	00100 = Spare control 2 register.	0
13		R/W		0
12		R/W		1
11		R/W		0
10		R/W		0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	–	–	–
7	Reserved	R/W	Write as 0, ignore when read.	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Reserved	R/W	Write as 0, ignore when read.	0
4	Ethernet@WireSpeed Retry Limit	RO	000 = Downgrade after 2 failed auto-negotiation attempts.	0
3			001 = Downgrade after 3 failed auto-negotiation attempts.	1
2			010 = Downgrade after 4 failed auto-negotiation attempts. 011 = Downgrade after 5 failed auto-negotiation attempts. 100 = Downgrade after 6 failed auto-negotiation attempts. 101 = Downgrade after 7 failed auto-negotiation attempts. 110 = Downgrade after 8 failed auto-negotiation attempts. 111 = Downgrade after 9 failed auto-negotiation attempts.	1
1	Energy Detect on $\overline{\text{INTR}}$ LED Pin	R/W	1 = Routes energy detect to interrupt signal. Use LED selectors (register 38h shadow 01101 and 01110) and program to $\overline{\text{INTR}}$ mode. 0 = $\overline{\text{INTR}}$ LED pin performs the Interrupt function.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Auto Power-Down Register (Page 10h–14h: Address 38h)

Table 160: Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0]. 0 = Read bits [9:0].	0
14	Shadow Register Selector	R/W	01010 = Auto power-down register.	0
13		R/W		1
12		R/W		0
11		R/W		1
10		R/W		0
9	Reserved	R/W	Write as 0, ignore when read.	0

Table 160: Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010) (Cont.)

Bit	Name	R/W	Description	Default
8	Reserved	R/W	Write as 0, ignore when read.	0
7	Reserved	R/W	Write as 0, ignore when read.	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Auto Power-Down Mode	R/W	1 = Auto power-down mode is enabled. 0 = Auto power-down mode is disabled.	0
4	Sleep Timer Select	R/W	1 = Sleep timer is 5.4 seconds. 0 = Sleep timer is 2.7 seconds.	0
3	Wake-up Timer Select	R/W	Counter for wake-up timer in units of 84 ms	0
2		R/W	0001 = 84 ms.	0
1		R/W	0010 = 168 ms.	0
0		R/W	... 1111 = 1.26 sec.	1

LED Selector 2 Register (Page 10h–14h: Address 38h)

Table 161: LED Selector 2 Register (Page 10h–14h: Address 38h, Shadow Value 01110)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0]. 0 = Read bits [9:0].	0
14	Shadow Register Selector	R/W	01110 = LED status register.	0
13		R/W		1
12		R/W		1
11		R/W		1
10		R/W		0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	R/W	Write as 0, ignore when read.	0

Table 161: LED Selector 2 Register (Page 10h–14h: Address 38h, Shadow Value 01110) (Cont.)

Bit	Name	R/W	Description	Default
7	LED4 Selector	R/W	0000 = $\overline{\text{LINKSPD[1]}}$.	0
6		R/W	0001 = $\overline{\text{LINKSPD[2]}}$.	1
5		R/W	0010 = $\overline{\text{XMITLED}}$.	1
4		R/W	0011 = $\overline{\text{ACTIVITY}}$. 0100 = $\overline{\text{FDXLED}}$. 0101 = $\overline{\text{SLAVE}}$. 0110 = $\overline{\text{INTR}}$. 0111 = $\overline{\text{QUALITY}}$. 1000 = $\overline{\text{RCVLED}}$. 1001 = $\overline{\text{WIRESPD\_DOWNGRADE}}$. 1010 = $\overline{\text{MULTICOLOR[2]}}$. 1011 = $\overline{\text{CABLE DIAGNOSTIC OPEN/SHORT}}$. 1100 = RESERVED. 1101 = CRS (SGMII mode). 1110 = Off (high). 1111 = On (low).	0
3	LED3 Selector	R/W	0000 = $\overline{\text{LINKSPD[1]}}$.	0
2		R/W	0001 = $\overline{\text{LINKSPD[2]}}$.	0
1		R/W	0010 = $\overline{\text{XMITLED}}$.	1
0		R/W	0011 = $\overline{\text{ACTIVITY}}$. 0100 = $\overline{\text{FDXLED}}$. 0101 = $\overline{\text{SLAVE}}$. 0110 = $\overline{\text{INTR}}$. 0111 = $\overline{\text{QUALITY}}$. 1000 = $\overline{\text{RCVLED}}$. 1001 = $\overline{\text{WIRESPD\_DOWNGRADE}}$. 1010 = $\overline{\text{MULTICOLOR[1]}}$. 1011 = $\overline{\text{CABLE DIAGNOSTIC OPEN/SHORT}}$. 1100 = RESERVED. 1101 = CRS (SGMII mode). 1110 = Off (high). 1111 = On (low).	1

Mode Control Register (Page 10h–14h: Address 38h)

Table 162: Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0]. 0 = Read bits [9:0].	0
14	Shadow Register Selector	R/W	11111 = LED status register.	1
13		R/W		1
12		R/W		1
11		R/W		1
10		R/W		1
9	Reserved	RO	Ignore on read.	0
8	Reserved	–	–	–
7	Copper Link	RO	1 = Link is good on the copper interface. 0 = Copper link is down.	0
6	Reserved	–	–	–
5	Copper Energy Detect	RO	1 = Energy detected on the copper interface. 0 = Energy not detected on the copper interface.	0
4	Reserved	RO	Ignore on read.	0
3	Reserved	RO	Ignore on read.	1
2	Mode Select	R/W	00 = GMII.	0
1			01 = Reserved. 10 = Reserved. 11 = Reserved.	0
0	Reserved	–	–	–

Master/Slave Seed Register (Page 10h–14h: Address 3Ah)

Table 163: Master/Slave Seed Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 0

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select shadow register. 0 = Normal operation. Writes to the selected register are done on a single cycle.	0
14	Master/Slave Seed Match	RO LH	1 = Seeds match. 0 = Seeds do not match.	0
13	Link Partner Repeater/DTE Bit	RO	1 = Link partner is a repeater/switch device. 0 = Link partner is a DTE device.	0
12	Link Partner Manual Master/ Slave Configuration Value	RO	1 = Link partner is configured as master. 0 = Link partner is configured as slave.	0

Table 163: Master/Slave Seed Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 0 (Cont.)

Bit	Name	R/W	Description	Default
11	Link Partner Manual Master/ Slave Configuration Enable	RO	1 = Link partner manual master/slave configuration is enabled. 0 = Link partner manual master/slave configuration is disabled.	0
10	Local Master/Slave Seed Value	R/W	Returns the automatically generated master/slave random seed.	0
9		R/W		0
8		R/W		0
7		R/W		0
6		R/W		0
5		R/W		0
4		R/W		0
3		R/W		0
2		R/W		0
1		R/W		0
0		R/W		0

HCD Status Register (Page 10h–14h: Address 3Ah)

Table 164: HCD Status Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 1

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select Shadow register. 0 = Normal operation.	0
14	Ethernet@WireSpeed Disable Gigabit Advertising	RO	1 = Disable advertising gigabit. 0 = Advertise gigabit based on register 09h.	0
13	Ethernet@WireSpeed Disable 100TX Advertising	RO	1 = Disable advertising 100TX. 0 = Advertise 100TX based on register 04h.	0
12	Ethernet@WireSpeed Downgrade	RO LH	1 = Ethernet@WireSpeed downgrade occurred since last read. 0 = Ethernet@WireSpeed downgrade cleared.	0
11	HCD 1000BASE-T Full-Duplex	RO LH	1 = Gigabit full-duplex occurred since last read. 0 = HCD cleared.	0
10	HCD 1000BASE-T Half-Duplex	RO LH	1 = Gigabit half-duplex occurred since last read. 0 = HCD cleared.	0
9	HCD 100BASE-TX Full-Duplex	RO LH	1 = 100BASE-TX full-duplex occurred since last read. 0 = HCD cleared.	0
8	HCD 100BASE-TX Half-Duplex	RO LH	1 = 100BASE-TX half-duplex occurred since last read. 0 = HCD cleared.	0
7	HCD 10BASE-T Full-Duplex	RO LH	1 = 10BASE-T full-duplex occurred since last read. 0 = HCD cleared.	0

Table 164: HCD Status Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 1 (Cont.)

Bit	Name	R/W	Description	Default
6	HCD 10BASE-T Half-Duplex	RO LH	1 = 10BASE-T half-duplex occurred since last read. 0 = HCD cleared.	0
5	HCD 1000BASE-T Full-Duplex (Link Never Came Up)	RO LH	1 = Gigabit full-duplex HCD and link never came up occurred since the last read. 0 = HCD cleared.	0
4	HCD 1000BASE-T Half-Duplex (Link Never Came Up)	RO LH	1 = Gigabit half-duplex HCD and link never came up occurred since the last read. 0 = HCD cleared.	0
3	HCD 100BASE-TX Full-Duplex (Link Never Came Up)	RO LH	1 = 100BASE-TX full-duplex HCD and link never came up occurred since the last read. 0 = HCD cleared.	0
2	HCD 100BASE-TX Half-Duplex (Link Never Came Up)	RO LH	1 = 100BASE-TX half-duplex HCD and link never came up occurred since the last read. 0 = HCD cleared.	0
1	HCD 10BASE-T Full-Duplex (Link Never Came Up)	RO LH	1 = 10BASE-T full-duplex HCD and link never came up occurred since the last read. 0 = HCD cleared.	0
0	HCD 10BASE-T Half-Duplex (Link Never Came Up)	RO LH	1 = 10BASE-T half-duplex HCD and link never came up occurred since the last read. 0 = HCD cleared.	0

Note: Bits [12:0] are also cleared when auto-negotiation is disabled using MII register 00h, bit 12 = 1, or restarted using MII register 00h, bit 9 = 1.

Test Register 1 (Page 10h–14h: Address 3Ch)

Table 165: Test Register 1 (Page 10h–14h: Address 3C–3Dh)

Bit	Name	R/W	Description	Default
15	CRC Error Counter Selector	R/W	1 = Receiver NOT_OK counters (register 14h) becomes 16-bit CRC error counter (CRC errors are counted only after this bit is set). 0 = Normal operation.	0
14	Transmit Error Code Visibility	R/W	1 = False carrier sense counters (register 13h) counts packets received with transmit error codes. 0 = Normal operation.	0
13	Reserved	R/W	Write as 0, ignore when read.	0
12	Force Link 10/100/1000BASE-T	R/W	1 = Force link state machine into link pass state. 0 = Normal operation.	0
11	Reserved	R/W	Write as 0, ignore when read.	0
10	Reserved	R/W	Write as 0, ignore when read.	0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	R/W	Write as 0, ignore when read.	0
7	Manual Swap MDI State	R/W	1 = Manually swap MDI state. 0 = Normal operation. ***Note:*** To change the MDI state when in forced 100BASE-TX mode, the PHY must first be put into a nonlink condition, then set bit 7 = 1 and finally set the PHY into force 100BASE-TX mode.	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Reserved	R/W	Write as 0, ignore when read.	0
4	Reserved	R/W	Write as 0, ignore when read.	0
3	Reserved	R/W	Write as 0, ignore when read.	0
2	Reserved	R/W	Write as 0, ignore when read.	0
1	Reserved	R/W	Write as 0, ignore when read.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Note: Preamble is still required on the first read or write. Preamble suppression cannot be disabled.

Block Address Number (Page 010h–017h: Address 03Eh)

Table 166: Block Address Number (Page 010h-017h: Address 03Eh-03Fh)

Bits	Name	R/W	Description	Default
15:4	RESERVED	R/W	Reserved. Write 0, ignore read.	0x000

Table 166: Block Address Number (Page 010h-017h: Address 03Eh-03Fh) (Cont.)

Bits	Name	R/W	Description	Default
3:0	BLK_NO	R/W	MII address registers 00-0Fh and 1Fh do not use the block addressing and are fixed. Block0, 2, or 3 selected using these bits: 0000 = Valid (block0). 0010 = Valid (block2). 0011 = Valid (block3). 0001, 1111 = reserved for future implementation.	0x0

Page 20h–28h: Port MIB Registers

Table 167: Port MIB Registers Page Summary

Page	Description
20h	Port 0
21h	Port 1
22h	Port 2
23h	Port 3
24h	Port 4
25h	Port 5
26h	Reserved
27h	Reserved
28h	IMP port

Table 168: Page 20h–28h Port MIB Registers

ADDR	Bits	Name	Description
00h–07h	64	TxOctets	Total number of good bytes of data transmitted by a port (excluding preamble, but including FCS).
08h–0Bh	32	TxDropPkts	This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.
0Ch–0Fh	32	TxQ0PKT	Total number of good packets transmitted on CoS0, which is specified in MIB queue select register when QoS is enabled.
10h–13h	32	TxBroadcastPkts	Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
14h–17h	32	TxMulticastPkts	Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.

Table 168: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
18h–1Bh	32	TxUnicastPkts	Number of good packets transmitted by a port that are addressed to a unicast address.
1Ch–1Fh	32	TxCollisions	Number of collisions experienced by a port during packet transmissions.
20h–23h	32	TxSingleCollision	Number of packets successfully transmitted by a port that experienced exactly one collision.
24h–27h	32	TxMultiple Collision	Number of packets successfully transmitted by a port that experienced more than one collision.
28h–2Bh	32	TxDeferredTransmit	Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.
2Ch–2Fh	32	TxLateCollision	Number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
30h–33h	32	TxExcessiveCollision	Number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.
34h–37h	32	TxFrameInDisc	Number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers [Page 0Ah].) This attribute only increments if a network device is not acting in compliance with a flow-control request, or the BCM53125S internal flow control/buffering scheme has been misconfigured.
38h–3Bh	32	TxPausePkts	Number of PAUSE events on a given port.
3Ch–3Fh	32	TxQ1PKT	Total number of good packets transmitted on CoS1, which is specified in MIB queue select register when QoS is enabled.
40h–43h	32	TxQ2PKT	Total number of good packets transmitted on CoS2, which is specified in MIB queue select register when QoS is enabled.
44h–47h	32	TxQ3PKT	Total number of good packets transmitted on CoS3, which is specified in MIB queue select register when QoS is enabled.
48h–4Bh	32	Reserved	Reserved
4Ch–4Fh	32	Reserved	Reserved
50h–57h	64	RxOctets	Number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets.
58h–5Bh	32	RxUndersizePkts	Number of good packets received by a port that are less than 64 bytes in length (excluding framing bits, but including the FCS).

Table 168: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
50h–5Fh	32	RxPausePkts	Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (88–08h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00–01), be a minimum of 64 bytes in length (excluding preamble, but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.
60h–63h	32	Pkts64Octets	Number of packets (including error packets) that are 64 bytes long.
64h–67h	32	Pkts65to127Octets	Number of packets (including error packets) that are between 65 and 127 bytes long.
68h–6Bh	32	Pkts128to255Octets	Number of packets (including error packets) that are between 128 and 255 bytes long.
6Ch–6Fh	32	Pkts256to511Octets	Number of packets (including error packets) that are between 256 and 511 bytes long.
70h–73h	32	Pkts512to1023Octets	Number of packets (including error packets) that are between 512 and 1023 bytes long.
74h–77h	32	Pkts1024toMaxPktOctets	Number of packets (including error packets) that are between 1024 and MaxPacket bytes long.
78h–7Bh	32	RxOversizePkts	Number of good packets received by a port that are greater than standard max frame size.
7Ch–7Fh	32	RxJabbers	Number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error.
80h–83h	32	RxAlignmentErrors	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.
84h–87h	32	RxFCSErrors	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.
88h–8Fh	64	RxGoodOctets	Total number of bytes in all good packets received by a port (excluding framing bits but including FCS).

Table 168: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
90h–93h	32	RxDropPkts	Number of good packets received by a port that were dropped due to lack of resources (e.g., lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters.
94h–97h	32	RxUnicastPkts	Number of good packets received by a port that are addressed to a unicast address.
98h–9Bh	32	RxMulticastPkts	Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
9Ch–9Fh	32	RxBroadcastPkts	Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
A0h–A3h	32	RxSAChanges	Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.
A4h–A7h	32	RxFragments	Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
A8h–ABh	32	JumboPkt	Number of frames received with frame size greater than the Standard Maximum Size and less than or equal to the Jumbo Frame Size, regardless of CRC or Alignment errors. ***Note:*** InFrame count should count “the JumboPkt count with good CRC.”
ACh–AFh	32	RXSymbolError	Total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increments once per carrier event and does not increment on detection of collision during the carrier event.
B0h–B3h	32	InRangeErrors	Number of frames received with good CRC and one of the following conditions: • The value of µs is between 46 and 1500 inclusive, and does not match the number or (MAC Client Data + PAD) data octets received. • The value of µs is less than 46, and the number of data octets received is greater than 46 (which does not require padding).
B4h–B7h	32	OutOfRangeErrors	Number of frames received with good CRC and the value of µs is greater than 1500 and less than 1536.
B8h–BBh	32	EEE Low-Power Idle	In asymmetric mode, this is simply a count of the number of times that the lowPowerAssert control signal has been asserted for each MAC. In symmetric mode, this is the count of the number of times both lowPowerAssert and the lowPowerIndicate (from the receive path) are asserted simultaneously.

Table 168: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
BCh–Bfh	32	EEE Low-Power Duration	This counter accumulates the number of microseconds that the associated MAC/PHY is in the low-power idle state. The unit is 1 µs.
C0h–C3h	32	RxDiscard	Number of good packets received by a port that were discarded by the Forwarding Process.
F0h–F7h	64	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7	–
F8h–FDh	–	Reserved	–
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280	–
FFh	8	"Page Register (Global, Address FFh)" on page 280	–

Page 30h: QoS Registers

Table 169: Page 30h QoS Registers

Address	Bits	Description
00h	8	"QoS Global Control Register (Page 30h: Address 00h)" on page 228
01h–02h	16	Reserved
03h	–	Reserved
04h–05h	16	"QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)" on page 229
06h–07h	16	"QoS DiffServ Enable Register (Page 30h: Address 06h)" on page 229
08h–0Fh	–	Reserved
10h–2Bh	32/port	"Port N (N=0-5, 8) PCP_To_TC Register (Page 30h: Address 10h)" on page 229
2Ch–2Fh	–	Reserved
30h–35h	48	"DiffServ Priority Map 0 Register (Page 30h: Address 30h)" on page 230
36h–3Bh	48	"DiffServ Priority Map 1 Register (Page 30h: Address 36h)" on page 231
3Ch–41h	48	"DiffServ Priority Map 2 Register (Page 30h: Address 3Ch)" on page 231
42h–47h	48	"DiffServ Priority Map 3 Register (Page 30h: Address 42h)" on page 232
48h–61h	–	Reserved
62h–63h	16	"TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 232
64h–67h	32	"CPU_To_CoS Map Register (Page 30h: Address 64h–67h)" on page 233
68h–7Fh	–	Reserved
80h	8	"TX Queue Control Register (Page 30h: Address 80h)" on page 234

Table 169: Page 30h QoS Registers (Cont.)

Address	Bits	Description
81h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 234, Queue 0
82h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 234, Queue 1
83h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 234, Queue 2
84h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 234, Queue 3
85h–86h	16	Reserved
87h–9Fh	–	Reserved
A0h	–	Reserved
A1h	–	Reserved
A2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

QoS Global Control Register (Page 30h: Address 00h)

Table 170: QoS Global Control Register (Page 30h: Address 00h)

Bit	Name	R/W	Description	Default
7	Aggregation Mode	R/W	When enable this bit, the IMP operated as the uplink port to the upstream network processor and the CoS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operated as the interface to the management CPU, and the CoS is decided based on the reasons for forwarding the packet to the CPU.	0
6	Port_QoS_En	R/W	Port-based QoS enable. When port-based QoS is enabled, ingress frames are assigned a priority ID value based on the PORT_QOS_PRI bits in the "Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)" on page 244. IEEE 802.1p and DiffServ priorities are disregarded. 0 = Disable port-based QoS. 1 = Enable port-based QoS. See "Quality of Service" on page 35 for more information.	0
5:4	Reserved	R/W	–	0
3:2	QoS_Layer_Sel	R/W	QoS priority selection. These bits determine which QoS priority scheme is associated with the frame. See Table 1 on page 38 for more information.	0
1:0	Reserved	R/W	Reserved	0

QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)

Table 171: QoS.1P Enable Register (Page 30h: Address 04h–05h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	802_1P_EN	R/W	QoS IEEE 802.1p port mask. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Disable IEEE 802.1p priority for individual ports. 1 = Enable IEEE 802.1p priority for individual ports. See “IEEE 802.1Q VLAN” on page 40 for more information.	0

QoS DiffServ Enable Register (Page 30h: Address 06h)

Table 172: QoS DiffServ Enable Register (Page 30h: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	DIFFSERV_EN	R/W	DiffServ port mask. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Disable DiffServ priority for individual ports. 1 = Enable DiffServ priority for individual ports.	0

See “Quality of Service” on page 35 for more information.

Port N (N=0-5, 8) PCP_To_TC Register (Page 30h: Address 10h)

Table 173: Port N (N=0-5,8) PCP_To_TC Register Address Summary

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	IMP Port

These bits map the IEEE 802.1p priority level to one of the eight priority ID levels in the “TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)” on page 232.

Table 174: Port N (N=0-5,8) PCP_To_TC Register (Page 30h: Address 10h–2Bh)

Bit	Name	R/W	Description	Default
31:24	Reserved	RO	–	0
23:21	1P_111_MAP	R/W	IEEE 802.1p priority tag field 111	111
20:18	1P_110_MAP	R/W	IEEE 802.1p priority tag field 110	110
17:15	1P_101_MAP	R/W	IEEE 802.1p priority tag field 101	101
14:12	1P_100_MAP	R/W	IEEE 802.1p priority tag field 100	100
11:9	1P_011_MAP	R/W	IEEE 802.1p priority tag field 011	011
8:6	1P_010_MAP	R/W	IEEE 802.1p priority tag field 010	010
5:3	1P_001_MAP	R/W	IEEE 802.1p priority tag field 001	001
2:0	1P_000_MAP	R/W	IEEE 802.1p priority tag field 000	000

See "Quality of Service" on page 35 for more information.

DiffServ Priority Map 0 Register (Page 30h: Address 30h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 232.

Table 175: DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)

Bit	Name	R/W	Description	Default
47:45	DiffServ_ 001111_Map	R/W	DiffServ DSCP priority tag field 001111	0
44:42	DiffServ_ 001110_Map	R/W	DiffServ DSCP priority tag field 001110	0
41:39	DiffServ_ 001101_Map	R/W	DiffServ DSCP priority tag field 001101	0
38:36	DiffServ_ 001100_Map	R/W	DiffServ DSCP priority tag field 001100	0
35:33	DiffServ_ 001011_Map	R/W	DiffServ DSCP priority tag field 001011	0
32:30	DiffServ_ 001010_Map	R/W	DiffServ DSCP priority tag field 001010	0
29:27	DiffServ_ 001001_Map	R/W	DiffServ DSCP priority tag field 001001	0
26:24	DiffServ_ 001000_Map	R/W	DiffServ DSCP priority tag field 001000	0
23:21	DiffServ_ 000111_Map	R/W	DiffServ DSCP priority tag field 000111	0
20:18	DiffServ_ 000110_Map	R/W	DiffServ DSCP priority tag field 000110	0
17:15	DiffServ_ 000101_Map	R/W	DiffServ DSCP priority tag field 000101	0
14:12	DiffServ_ 000100_Map	R/W	DiffServ DSCP priority tag field 000100	0
11:9	DiffServ_ 000011_Map	R/W	DiffServ DSCP priority tag field 000011	0
8:6	DiffServ_ 000010_Map	R/W	DiffServ DSCP priority tag field 000010	0
5:3	DiffServ_ 000001_Map	R/W	DiffServ DSCP priority tag field 000001	0
2:0	DiffServ_ 000000_Map	R/W	DiffServ DSCP priority tag field 000000	0

See "Quality of Service" on page 35 for more information.

DiffServ Priority Map 1 Register (Page 30h: Address 36h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 232.

Table 176: DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)

Bit	Name	R/W	Description	Default
47:45	DiffServ_ 011111_Map	R/W	DiffServ DSCP priority tag field 011111	0
44:42	DiffServ_ 011110_Map	R/W	DiffServ DSCP priority tag field 011110	0
41:39	DiffServ_ 011101_Map	R/W	DiffServ DSCP priority tag field 011101	0
38:36	DiffServ_ 011100_Map	R/W	DiffServ DSCP priority tag field 011100	0
35:33	DiffServ_ 011011_Map	R/W	DiffServ DSCP priority tag field 011011	0
32:30	DiffServ_ 011010_Map	R/W	DiffServ DSCP priority tag field 011010	0
29:27	DiffServ_ 011001_Map	R/W	DiffServ DSCP priority tag field 011001	0
26:24	DiffServ_ 011000_Map	R/W	DiffServ DSCP priority tag field 011000	0
23:21	DiffServ_ 010111_Map	R/W	DiffServ DSCP priority tag field 010111	0
20:18	DiffServ_ 010110_Map	R/W	DiffServ DSCP priority tag field 010110	0
17:15	DiffServ_ 010101_Map	R/W	DiffServ DSCP priority tag field 010101	0
14:12	DiffServ_ 010100_Map	R/W	DiffServ DSCP priority tag field 010100	0
11:9	DiffServ_ 010011_Map	R/W	DiffServ DSCP priority tag field 010011	0
8:6	DiffServ_ 010010_Map	R/W	DiffServ DSCP priority tag field 010010	0
5:3	DiffServ_ 010001_Map	R/W	DiffServ DSCP priority tag field 010001	0
2:0	DiffServ_ 010000_Map	R/W	DiffServ DSCP priority tag field 010000	0

See "Quality of Service" on page 35 for more information.

DiffServ Priority Map 2 Register (Page 30h: Address 3Ch)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 232.

Table 177: DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)

Bit	Name	R/W	Description	Default
47:45	DiffServ_ 101111_Map	R/W	DiffServ DSCP priority tag field 101111	0
44:42	DiffServ_ 101110_Map	R/W	DiffServ DSCP priority tag field 101110	0
41:39	DiffServ_ 101101_Map	R/W	DiffServ DSCP priority tag field 101101	0
38:36	DiffServ_ 101100_Map	R/W	DiffServ DSCP priority tag field 101100	0
35:33	DiffServ_ 101011_Map	R/W	DiffServ DSCP priority tag field 101011	0
32:30	DiffServ_ 101010_Map	R/W	DiffServ DSCP priority tag field 101010	0
29:27	DiffServ_ 101001_Map	R/W	DiffServ DSCP priority tag field 101001	0
26:24	DiffServ_ 101000_Map	R/W	DiffServ DSCP priority tag field 101000	0
23:21	DiffServ_ 100111_Map	R/W	DiffServ DSCP priority tag field 100111	0

Table 177: DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h) (Cont.)

Bit	Name	R/W	Description	Default
20:18	DiffServ_ 100110_Map	R/W	DiffServ DSCP priority tag field 100110	0
17:15	DiffServ_ 100101_Map	R/W	DiffServ DSCP priority tag field 100101	0
14:12	DiffServ_ 100100_Map	R/W	DiffServ DSCP priority tag field 100100	0
11:9	DiffServ_ 100011_Map	R/W	DiffServ DSCP priority tag field 100011	0
8:6	DiffServ_ 100010_Map	R/W	DiffServ DSCP priority tag field 100010	0
5:3	DiffServ_ 100001_Map	R/W	DiffServ DSCP priority tag field 100001	0
2:0	DiffServ_ 100000_Map	R/W	DiffServ DSCP priority tag field 100000	0

See "Quality of Service" on page 35 for more information.

DiffServ Priority Map 3 Register (Page 30h: Address 42h)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 232.

Table 178: DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)

Bit	Name	R/W	Description	Default
47:45	DiffServ_ 111111_Map	R/W	DiffServ DSCP priority tag field 111111	0
44:42	DiffServ_ 111110_Map	R/W	DiffServ DSCP priority tag field 111110	0
41:39	DiffServ_ 111101_Map	R/W	DiffServ DSCP priority tag field 111101	0
38:36	DiffServ_ 111100_Map	R/W	DiffServ DSCP priority tag field 111100	0
35:33	DiffServ_ 111011_Map	R/W	DiffServ DSCP priority tag field 111011	0
32:30	DiffServ_ 111010_Map	R/W	DiffServ DSCP priority tag field 111010	0
29:27	DiffServ_ 111001_Map	R/W	DiffServ DSCP priority tag field 111001	0
26:24	DiffServ_ 111000_Map	R/W	DiffServ DSCP priority tag field 111000	0
23:21	DiffServ_ 110111_Map	R/W	DiffServ DSCP priority tag field 110111	0
20:18	DiffServ_ 110110_Map	R/W	DiffServ DSCP priority tag field 110110	0
17:15	DiffServ_ 100101_Map	R/W	DiffServ DSCP priority tag field 100101	0
14:12	DiffServ_ 110100_Map	R/W	DiffServ DSCP priority tag field 110100	0
11:9	DiffServ_ 110011_Map	R/W	DiffServ DSCP priority tag field 110011	0
8:6	DiffServ_ 110010_Map	R/W	DiffServ DSCP priority tag field 110010	0
5:3	DiffServ_ 110001_Map	R/W	DiffServ DSCP priority tag field 110001	0
2:0	DiffServ_ 110000_Map	R/W	DiffServ DSCP priority tag field 110000	0

See "Quality of Service" on page 35 for more information.

TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)

All the bits in Table 179 map the priority ID to one of the TX queues.

Table 179: TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)

Bit	Name	R/W	Description	Default
15:14	Pri_111_QID	R/W	Priority ID 111 mapped to TX Queue ID	00
13:12	Pri_110_QID	R/W	Priority ID 110 mapped to TX Queue ID	00
11:10	Pri_101_QID	R/W	Priority ID 101 mapped to TX Queue ID	00
9:8	Pri_100_QID	R/W	Priority ID 100 mapped to TX Queue ID	00
7:6	Pri_011_QID	R/W	Priority ID 011 mapped to TX Queue ID	00
5:4	Pri_010_QID	R/W	Priority ID 010 mapped to TX Queue ID	00
3:2	Pri_001_QID	R/W	Priority ID 001 mapped to TX Queue ID	00
1:0	Pri_000_QID	R/W	Priority ID 000 mapped to TX Queue ID	00

See "Quality of Service" on page 35 for more information.

CPU_To_CoS Map Register (Page 30h: Address 64h–67h)

Table 180: CPU_To_CoS Map Register (Page 30h: Address 64h–67h)

Bit	Name	R/W	Description	Default
31:18	Reserved	RO	–	0
17:15	Exception/Flooding Processing to CPU CoS Map	R/W	The packet forwarded to the CPU for Exception Processing/Flooding reason. The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
14:12	Protocol Snooping to CPU CoS Map	R/W	The packet forwarded to the CPU for Protocol Snooping reason. The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
11:9	Protocol Termination to CPU CoS Map	R/W	The packet forwarded to the CPU for Protocol Termination reason. The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
8:6	Switching to CPU CoS Map	R/W	The packet forwarded to the CPU for Switching reason. The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
5:3	SA Learning to CPU CoS Map	R/W	The packet forwarded to the CPU for SA Learning reason. The CoS selection is based on the highest CoS among all the reasons for the packet.	0
2:0	Mirror to CPU CoS Map	R/W	The packet forwarded to the CPU for mirroring reason. The CoS selection is based on the highest CoS values among all the reasons for the packet.	0

TX Queue Control Register (Page 30h: Address 80h)

Table 181: TX Queue Control Register (Page 30h: Address 80h)

Bit	Name	R/W	Description	Default
7:4	Reserved	R/W	–	0
3:2	Reserved	R/W	–	–
1:0	QOS_PRIORITY_CTRL	R/W	Best Effort Queues Priority Control. This field controls the best effort queues' scheduling priority. 00 = All queues are weighted round robin 01 = CoS 3 is strict priority, CoS2-CoS0 are weighted round robin. 10 = CoS3 and CoS2 is strict priority, CoS1-CoS0 are weighted round robin. 11 = CoS3, CoS2, CoS1 and CoS0 are in strict priority. Strict priority: When it is in strict priority, the priority is CoS3 > CoS2 > CoS1 > CoS0. The G_TXPORT will serve the higher queue first if it is not empty. In this mode, the service weight are don't care. Weighted round robin: When it is in weighted round robin mode, the queues are scheduled in a round robin way according to the service weight of each queue.	00

See "Quality of Service" on page 35 for more information.

TX Queue Weight Register (Page 30h: Address 81h)

Table 182: TX Queue Weight Register Queue[0:3] (Page 30h: Address 81h–84h)

Bit	Name	R/W	Description	Default
7:0	QSerV_Weight	R/W	Queue weight register. The binary value of these bits sets the service weight of the given queue. The value of 1 allows the queue to send one packet for every round; the value of 4 allows the queue to send four packets for every round. It is suggested that the weight of each queue be Q3 > Q2 > Q1 > Q0 > 0. ***Note:*** The maximum allowable transmit queue weight is 31h. Programming a higher weight than 31h can yield unexpected results. This field must not be programmed as zero.	Queue: 0 = 0001 1 = 0010 2 = 0100 3 = 1000

See "Quality of Service" on page 35 for more information.

Page 31h: Port-Based VLAN Registers

Table 183: Page 31h VLAN Registers

Address	Bits	Description
00h–11h	16/port	"Port-Based VLAN Control Register (Page 31h: Address 00h)" on page 235
1Fh–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

Port-Based VLAN Control Register (Page 31h: Address 00h)

Table 184: Port-Based VLAN Control Register Address Summary

Address	Description
00h–01h	Port 0
02h–03h	Port 1
04h–05h	Port 2
06h–07h	Port 3
08h–09h	Port 4
0Ah–0Bh	Port 5
0Ch–0Dh	Reserved
0Eh–0Fh	Reserved
10h–11h	IMP port

Table 185: Port VLAN Control Register (Page 31h: Address 00h–11h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	–
8:0	Forward_Mask	R/W	VLAN forwarding mask. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Disable VLAN forwarding to egress port. 1 = Enable VLAN forwarding to egress port.	1FFh

For more information, see "Port-Based VLAN" on page 40.

Page 32h: Trunking Registers

Table 186: Page 32h Trunking Registers

Address	Bits	Description
00h	8	“MAC Trunking Control Register (Page 32h: Address 00h)” on page 236
01h–0Fh	–	Reserved
10h–11h	16	Trunk group 0 register
12h–13h	16	Trunk group 1 register
14h–15h	–	Reserved
16h–17h	–	Reserved
18h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

MAC Trunking Control Register (Page 32h: Address 00h)

Table 187: MAC Trunk Control Register (Page 32h: Address 00h)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	–	–
3	MAC_BASE_TRNK_EN	–	Enable MAC base trunking.	–
2	Reserved	–	–	–
1:0	Trk_hash_indx	R/W	Trunk hash index selector. 00 = Use hash [DA,SA] to generate index. 01 = Use hash [DA] to generate index. 10 = Use hash [SA] to generate index. 11 = Illegal state.	0

See “Port Trunking/Aggregation” on page 44 for more information.

Trunking Group 0 Register (Page 32h: Address 10h)

Table 188: Trunk Group 0 Register (Page 32h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0

Table 188: Trunk Group 0 Register (Page 32h: Address 10h–11h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	Trunk Group Enable	R/W	Trunk group enable. 1 = Enable trunk group. 0 = Disable trunk group. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0

See "Port Trunking/Aggregation" on page 44 for more information.

Trunking Group 1 Register (Page 32h: Address 12h)

Table 189: Trunk Group 1 Register (Page 32h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	Trunk Group Enable	R/W	Trunk group enable. 1 = Enable trunk group. 0 = Disable trunk group. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0

Page 34h: IEEE 802.1Q VLAN Registers

Table 190: Page 34h IEEE 802.1Q VLAN Registers

Address	Bits	Description
00h	8	"Global IEEE 802.1Q Register (Pages 34h: Address 00h)" on page 238
01h	8	"Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)" on page 239
02h	8	"Global VLAN Control 2 Register (Page 34h: Address 02h)" on page 240
03h–04h	16	"Global VLAN Control 3 Register (Page 34h: Address 03h)" on page 240
05h	8	"Global VLAN Control 4 Register (Page 34h: Address 05h)" on page 241
06h	8	"Global VLAN Control 5 Register (Page 34h: Address 06h)" on page 242
07h	8	Reserved
0Ah–0Bh	16	"" on page 242
Reserved	32	Reserved
10h–21h	16/port	"Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)" on page 244
20h–2Fh	–	Reserved
30h–31h	16	"Double Tagging TPID Register (Page 34h: Address 30h–31h)" on page 244
32h–33h	16	"ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)" on page 245

Table 190: Page 34h IEEE 802.1Q VLAN Registers (Cont.)

Address	Bits	Description
34h–3Fh	–	Reserved
40h–43h	32	Reserved
44h–48h	32	Reserved
49h–EFh	–	–
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

Global IEEE 802.1Q Register (Pages 34h: Address 00h)

Table 191: Global IEEE 802.1Q Register (Pages 34h: Address 00h)

Bit	Name	R/W	Description	Default
7	Enable IEEE 802.1Q	R/W	Enable IEEE 802.1Q VLAN. 0 = Disable IEEE 802.1Q VLAN. 1 = Enable IEEE 802.1Q VLAN. See “Double Tagging” on page 41 for more information. ***Note:*** This bit must be set if Double-Tagging mode enable (En_DT_Mode = 01 or 10) in “Global VLAN Control 4 Register (Page 34h: Address 05h)” on page 241.	0
6:5	VLAN Learning Mode	R/W	VLAN learning mode. 00 = SVL (Shared VLAN learning mode) (MAC hash ARL table). 11 = IVL (Individual VLAN learning mode) (MAC and VID hash ARL table). 10 = Illegal setting. 01 = Illegal setting. ***Note:*** Applied to 802.1Q enable, DT_Mode.	11
4	Reserved	R/W	Reserved	0
3	Change_1Q_VID	R/W	Change 1Q VID to PVID. 1 = • For a single-tag frame with VID not = 0, change the VID to PVID. • For a double-tag frame with outer VID not = 0, change outer VID to PVID. 0 = No change for 1Q/ISP tag if VID is not 0.	0
2	Reserved	R/W	Reserved	0
1	Reserved	R/W	Reserved	1
0	Reserved	R/W	Reserved	1

See "IEEE 802.1Q VLAN" on page 40 for more information.

Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)

Table 192: Global VLAN Control 1 Register (Page 34h: Address 01h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0
6	Multicast Untag Check	R/W	Multicast VLAN untagged map check bypass. 1 = Multicast frames are not checked against the VLAN untagged map. 0 = Multicast frames are checked against the VLAN untagged map. Does not apply to the frame management port.	0
5	Multicast Forward Check	R/W	Multicast VLAN forward map check bypass. 1 = Multicast frames are not checked against the VLAN forward map. 0 = Multicast frames are checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable, DT_Mode.	0
4	Reserved	R/W	It is illegal to set 1.	0
3	Reserved Multicast Untag Check	R/W	Reserved multicast (except GMRP and GVRP) VLAN untagged map check bit. 1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN untagged map. 0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN untagged map. Does not apply to the frame management port.	0
2	Reserved Multicast Forward Check	R/W	Reserved multicast (except GMRP and GVRP) VLAN forward map check bit. 1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN forward map. 0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable, DT_Mode.	0
1	Reserved	R/W	It is illegal to set 0.	1
0	Reserved	R/W	Reserved	0

For more information, see "IEEE 802.1Q VLAN" on page 40.

Global VLAN Control 2 Register (Page 34h: Address 02h)

Table 193: Global VLAN Control 2 Register (Page 34h: Address 02h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0
6	GMRP/GVRP Untag Check	R/W	GMRP or GVRP VLAN untag map check bit. 1 = GMRP or GVRP frames are checked against the VLAN untagged map. 0 = GMRP or GVRP frames are not checked against the VLAN untagged map. **Note:** Does not apply to the frame management port.	0
5	GMRP/GVRP Forward Check	R/W	GMRP or GVRP VLAN forward map check bit. 1 = GMRP or GVRP frames are checked against the VLAN forward map. 0 = GMRP or GVRP frames are not checked against the VLAN forward map. **Note:** Does not apply to the frame management port. Applied to 802.1Q enable, DT_Mode.	0
4	Reserved	R/W	Reserved	1
3	Reserved	R/W	Reserved	0
2	IMP Frame Forward Bypass	R/W	IMP Frame VLAN forward map check bit. 1 = IMP frames are not checked against the VLAN forward map. 0 = IMP frames are checked against the VLAN forward map. **Note:** Applied to 802.1Q enable, DT_Mode.	0
1:0	Reserved	R/W	Reserved	00

For more information, see “IEEE 802.1Q VLAN” on page 40.

Global VLAN Control 3 Register (Page 34h: Address 03h)

Table 194: Global VLAN Control 3 Register (Page 34h: Address 03h–04h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	–
7:0	Drop Non1Q Frames	R/W	Drop non1Q frames. When enabled, any frame without an IEEE 802.1Q tag is dropped by this port. This field does not apply to IMP port (includes Port 5 if Dual-IMP ports enabled, En_IMP_PORT = 11 in “Global Management Configuration Register (Page 02h: Address 00h)” on page 168. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0

Global VLAN Control 4 Register (Page 34h: Address 05h)

Table 195: Global VLAN Control 4 Register (Page 34h: Address 05h)

Bit	Name	R/W	Description	Default
7:6	Source Membership Check	R/W	Source membership check bit. Frames with a VID matching a corresponding entry in the VLAN table can be checked for source membership. The source is a member only when the source address of the frame is included as a member in the corresponding VLAN entry. 00 = Forward frame, but do not learn the SA into the ARL table. 01 = Drop frame. 10 = Forward frame, and learn the SA into the ARL table. 11 = Forward frame to IMP, but not learn. ***Note:*** Does not apply to IMP port (includes Port 5 if Dual-IMP ports enabled, En_IMP_PORT = 11 in "Global Management Configuration Register (Page 02h: Address 00h)" on page 168).	11
5	Forward GVRP to Management	R/W	Forward all GVRP frames to the frame management port bit. 1 = GVRP frames are forwarded to the management port. 0 = GVRP frames are not forwarded to the management port.	0
4	Forward GMRP to Management	R/W	Forward All GMRP Frames to the frame management port bit. 1 = GMRP frames are forwarded to the management port. 0 = GMRP frames are not forwarded to the management port.	0
3:2	En_DT_Mode	R/W	00 = Disable double-tagging mode. 01 = Enable DT_Mode (double-tagging mode). 10 = Reserved. 11 = Reserved.	2'b00
1	RSV_MCAST_FLOOD	R/W	This is used when the BCM53125S is configured to operate in double-tag feature (DT_Mode) and management mode. 1 = Flood (including all data port and CPU), reserved mcast is based on the VLAN rule. 0 = Trap reserved mcast to CPU. Reserved multicast includes 01-80-C2-00-00-(00,02–2F).	–
0	Reserved	R/W	–	0

For more information, see "IEEE 802.1Q VLAN" on page 40.

Global VLAN Control 5 Register (Page 34h: Address 06h)

Table 196: Global VLAN Control 5 Register (Page 34h: Address 06h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0
6	Tag Status Preserve	R/W	IEEE 802.1Q tag/untag status preserved at egress. 1 = Regardless of untag map in VLAN table, non-1Q frames (including 802.1p frames) will not be changed at TX (egress). This field has no effect in double-tagging mode (DT_Mode).	0
5	Reserved	R/W	Reserved	0
4	Trunk Check Bypass	R/W	Trunk check bypass. 1 = Egress directed frames issued from the IMP port bypass trunk checking. 0 = Egress directed frames issued from the IMP port are subject to trunk checking and redirection.	1
3	Drop Invalid VID	R/W	Drop frames with invalid VID. Frames with an invalid VID do not have a corresponding entry in the VLAN table. 1 = Ingress frames with invalid VID are dropped. 0 = Ingress frames with invalid VID are forwarded to the IMP port.	0
2	VID_FFF_Fwding	R/W	Enable VID FFF forward. 1 = Forward frame. 0 = Comply with standard, drop frame.	0
1	Reserved	R/W	Reserved	0
0	Management CRC Check Bypass	R/W	Bypass CRC check at the frame management port. 1 = Ignore CRC check. 0 = Check CRC.	0

For more information, see “IEEE 802.1Q VLAN” on page 40.

VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

Table 197: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	–	0
11	EN_MPORT5_untagmap	R/W	When set to 1, MPORT_ADD5 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0

Table 197: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh) (Cont.)

Bit	Name	R/W	Description	Default
10	EN_MPORT5 _fwdmap	R/W	When set to 1, MPORT_ADD5 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
9	EN_MPORT4_untagmap	R/W	When set to 1, MPORT_ADD4 will be checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
8	EN_MPORT4 _fwdmap	R/W	When set to 1, MPORT_ADD4 will be checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
7	EN_MPORT3_untagmap	R/W	When set to 1, MPORT_ADD3 will be checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
6	EN_MPORT3 _fwdmap	R/W	When set to 1, MPORT_ADD3 will be checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
5	EN_MPORT2_untagmap	R/W	When set to 1, MPORT_ADD2 will be checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
4	EN_MPORT2 _fwdmap	R/W	When set to 1, MPORT_ADD2 will be checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
3	EN_MPORT1_untagmap	R/W	When set to 1, MPORT_ADD1 will be checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
2	EN_MPORT1 _fwdmap	R/W	When set to 1, MPORT_ADD1 will be checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
1	EN_MPORT0_untagmap	R/W	When set to 1, MPORT_ADD0 will be checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
0	EN_MPORT0 _fwdmap	R/W	When set to 1, MPORT_ADD0 will be checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0

Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)

Table 198: Default IEEE 802.1Q Tag Register Address Summary

Address	Description
10h–11h	Port 0
12h–13h	Port 1
14h–15h	Port 2
16h–17h	Port 3
18h–19h	Port 4
1Ah–1Bh	Port 5
1Ch–1Dh	Reserved
1Eh–1Fh	Reserved
20h–21h	IMP port

Table 199: Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)

Bit	Name	R/W	Description	Default
15:13	DEFAULT_PRI/ PORT_QOS_PRI	R/W	Default IEEE 802.1Q priority. If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, these bits are the default priority value for the new tag. See “IEEE 802.1Q VLAN” on page 40 for more information. Port-based QoS priority map bits. When port-based QoS is enabled in the Table : “QoS Global Control Register (Page 30h: Address 00h),” on page 228, these bits represent the TC for the ingress port. The TC determines the TX queue for each frame based on the “TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)” on page 232.	000
12	CFI	R/W	Canonical form indicator.	0
11:0	deFAULT_VID	R/W	Default IEEE 802.1Q VLAN ID. If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, then these bits are the default VID for the new tag. See “IEEE 802.1Q VLAN” on page 40 for more information.	001

Double Tagging TPID Register (Page 34h: Address 30h–31h)

Table 200: Double Tagging TPID Register (Page 34h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:0	ISP_TPID	R/W	The TPID used to identify double-tagged frame.	9100

ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

Table 201: ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:8	Reserved	–	–	0
7:0	ISP_Portmap	R/W	Bitmap that defines which port is designated as the ISP port. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Indicates that it is not an ISP port. 1 = Indicates that it is an ISP port. ***Note:*** Multiple ISP port assignments are allowed.	–

Page 36h: DoS Prevent Register

Table 202: DoS Prevent Register

Address	Bits	Description
00h–03h	32	“DoS Control Register (Page 36h: Address 00h–03h)” on page 246
04h	8	“Minimum TCP Header Size Register (Page 36h: Address 04h)” on page 248
08h–0Bh	32	“Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)” on page 248
0Ch–0Fh	32	“Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)” on page 248
10h	8	“DoS Disable Learn Register (Page 36h: Address 10h)” on page 248
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

DoS Control Register (Page 36h: Address 00h–03h)

Table 203: DoS Control Register (Page 36h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:14	Reserved	RO	–	0
13	ICMPv6_LongPing_DROP_EN	R/W	The ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size. 1 = Drop. 0 = Do not drop.	0
12	ICMPv4_LongPing_DROP_EN	R/W	The ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header. 1 = Drop. 0 = Do not drop.	0
11	ICMPv6_Fragment_DROP_EN	R/W	The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram. 1 = Drop. 0 = Do not drop.	0
10	ICMPv4_Fragment_DROP_EN	R/W	The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram. 1 = Drop. 0 = Do not drop.	0

Table 203: DoS Control Register (Page 36h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
9	TCP_FragError_DROP_EN	R/W	The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data. 1 = Drop. 0 = Do not drop.	00
8	TCP_ShortHDR_DROP_EN	R/W	The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size. 1 = Drop. 0 = Do not drop.	00
7	TCP_SYNError_DROP_EN	R/W	SYN = 1, ACK = 0, and SRC_Port<1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop. 0 = Do not drop.	0
6	TCP_SYNFINScan_DROP_EN	R/W	SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop. 0 = Do not drop.	0
5	TCP_XMASScan_DROP_EN	R/W	Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop. 0 = Do not drop.	0
4	TCP_NULLScan_DROP_EN	R/W	Seq_Num = 0 and all TCP_FLAGs = 0 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop. 0 = Do not drop.	0
3	UDP_BLAT_DROP_EN	R/W	DPort = SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop. 0 = Do not drop.	0
2	TCP_BLAT_DROP_EN	R/W	DPort = SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop. 0 = Do not drop.	0

Table 203: DoS Control Register (Page 36h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
1	IP_LAN_DRIP_EN	R/W	IPDA = IPSA in an IPv4/v6 datagram. 1 = Drop. 0 = Do not drop.	0
0	RESERVED	R/W	Reserved	1

Minimum TCP Header Size Register (Page 36h: Address 04h)

Table 204: Minimum TCP Header Size Register (Page 36h: Address 04h)

Bit	Name	R/W	Description	Default
7:0	MIN_TCP_HDR_SZ	R/W	Minimum TCP header size allowed (0–256 bytes).	8'h14

Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)

Table 205: Maximum ICMPv4 Size Register (Page 36h: Address 08h-0Bh)

Bit	Name	R/W	Description	Default
31:0	MAX_ICMPv4_SIZE	R/W	Max ICMPv4 size allowed (0–9.6 KB).	32'd512

Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)

Table 206: Maximum ICMPv6 Size Register (Page 36h: Address 0Ch-0Fh)

Bit	Name	R/W	Description	Default
31:0	MAX_ICMPv6_SIZE	R/W	Max ICMPv6 size allowed (0–9.6 KB).	32'd512

DoS Disable Learn Register (Page 36h: Address 10h)

Table 207: DoS Disable Learn Register (Page 36h: Address 08h-0Bh)

Bit	Name	R/W	Description	Default
7:1	RESERVED	R/W	Reserved	–
0	DoS Disable Lrn	R/W	When this bit enabled, all frames dropped by DoS prevent will not be learned.	0

Page 40h: Jumbo Frame Control Register

Table 208: Page 40h Jumbo Frame Control Register

Address	Bits	Description
00h	–	Reserved
01h–04h	32	“Jumbo Frame Port Mask Register (Page 40h: Address 01h)” on page 249
05h–06h	16	“Standard Max Frame Size Register (Page 40h: Address 05h)” on page 250
07h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

Jumbo Frame Port Mask Register (Page 40h: Address 01h)

Table 209: Jumbo Frame Port Mask Registers (Page 40h: Address 01h–04h)

Bit	Name	R/W	Description	Default
31:25	Reserved	RO	–	0
24:9	Reserved	R/W	–	0
8:0	Jumbo_Port_Mask	R/W	Jumbo frame port mask. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively. 0 = Disable jumbo frame capability on the port. 1 = Enable jumbo frame capability on the port. Jumbo frames can be ingressed and egressed only to the ports enabled using this port mask. Jumbo frame port mask has no effect on the traffic of normal sized frames. See “Jumbo Frame Support” on page 44 for more information.	0

Note: When the Jumbo Frame feature is enabled, the assigned Weight value for the WRR scheduling cannot be applied fairly over the queues. This is due to the internal Packet Buffer Memory size limitation.

Note: The Jumbo Frame feature is only supported in 1000 Mbps mode.

Standard Max Frame Size Register (Page 40h: Address 05h)

Table 210: Standard Max Frame Size Registers (Page 40h: Address 05h–06h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	–	0
13:0	Standard Max Frame Size	R/W	Standard Max Frame Size. Defines the standard maximum frame size for MAC and MIB counter. This register only allowed to be configured as 14'd1518 or 14'd2000. When jumbo is disabled, the content of this register is used to define good frame length. • If it is configured as 1518, the tagged frames will be dropped if the frame length is larger than 1522 bytes; and the untagged frames will be dropped if the frame length is larger than 1518 bytes. • If it is configured as 2000, both tagged and untagged frames will be dropped if the frame length is larger than 2000 bytes. When jumbo is enabled, all frames will be dropped if the frame length is larger than 9720 bytes. The register setting affects the following MIB parameters: • RxSAChange • RxGoodOctets • RxUnicastPkts • RxMulticastPkts • RxBroadcastPkts • RxOverSizePkts	‘d2000

Page 41h: Broadcast Storm Suppression Register

Table 211: Broadcast Storm Suppression Register (Page 41h)

Address	Bits	Description
00h–03h	32	“Ingress Rate Control Configuration Register (Page 41h: Address 00h)” on page 251
04h–0Fh	–	Reserved
10h–33h	32/port	“Port Receive Rate Control Register (Page 41h: Address 10h)” on page 253
34h–4Fh	–	Reserved
50h–73h	–	Reserved
74h–7Fh	–	Reserved

Table 211: Broadcast Storm Suppression Register (Page 41h) (Cont.)

Address	Bits	Description
80h–91h	16/port	"Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)" on page 256
92h–BFh	–	Reserved
C0h–C1h	8	"IMP Port (IMP/Port 5) Egress Rate Control Configuration Register (Page 41h: Address C0h–C1h)" on page 256
C2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

Ingress Rate Control Configuration Register (Page 41h: Address 00h)

Table 212: Global Rate Control Register (Page 41h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:19	Reserved	RO	–	0
18	XLENEN	R/W	Packet Length Selection. 0 = Ingress/Egress Rate excludes IPG. 1 = Ingress/Egress rate includes IPG.	0
17	Buck1_ BRM_Sel	R/W	Bit rate mode selection 0 = Absolute bit rate mode—The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 represents the incoming bit rate as an absolute data rate. 1 = Bit rate normalized to link speed mode—The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 represents the incoming bit rate normalized with respect to the link speed mode. See "Rate Control" on page 46 for more details.	0
16	Reserved	R/W	Reserved	1

Table 212: Global Rate Control Register (Page 41h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
15:9	Buck1_Packet_Type	R/W	Suppressed packet type mask. This bit mask determines the type of packets to be monitored by bucket 1. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this bit field are defined as follows: Bit 9 = Unicast lookup hit. Bit 10 = Multicast lookup hit. Bit 11 = Reserved MAC Address Frame. Bit 12 = Broadcast. Bit 13 = Multicast lookup failure. Bit 14 = Unicast lookup failure. Bit 15 = Reserved. See "Rate Control" on page 46 for more details.	0
8	Buck0_ BRM_Sel	R/W	Bit rate mode selection. 0 = Absolute bit rate mode—The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 represents the incoming bit rate as an absolute data rate. 1 = Bit rate normalized to link speed mode—The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 represents the incoming bit rate normalized with respect to the link speed mode. See "Rate Control" on page 46 for more details.	0
7	Reserved	R/W	Reserved	1
6:0	Buck0_Packet_Type	R/W	Suppressed packet type mask. This bit mask determines the type of packets to be monitored by bucket 0. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this bit field are defined as follows: Bit 0 = Unicast lookup hit. Bit 1 = Multicast lookup hit. Bit 2 = Reserved MAC address frame. Bit 3 = Broadcast. Bit 4 = Multicast lookup failure. Bit 5 = Unicast lookup failure. Bit 6 = Reserved. See "Rate Control" on page 46 for more details.	0000000

Port Receive Rate Control Register (Page 41h: Address 10h)

Table 213: Port Rate Control Register Address Summary

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	Reserved
2Ch–2Fh	Reserved
30h–33h	IMP port for BCM53125S

Table 214: Port Rate Control Register (Page 41h: Address 10h–33h)

Bit	Name	R/W	Description	Default
31:29	Reserved	RO	–	0
28	STRM_SUPR_EN	R/W	Enable storm suppression (Supported by bucket1). 0 = Disable. 1 = Enable.	0
27	RsvMC_SUPR_EN	R/W	Enable reserved mulitcast storm suppression. 0 = Disable. 1 = Enable.	0
26	BC_SUPR_EN	R/W	Enable broadcast storm suppression. 0 = Disable. 1 = Enable.	0
25	MC_SUPR_EN	R/W	Enable multicast storm suppression. 0 = Disable. 1 = Enable.	0
24	DLF_SUPR_EN	R/W	Enable DLF storm suppression. 0 = Disable. 1 = Enable.	0
23	Enable Bucket1	R/W	Enable rate control of the ingress port, bucket 1. 0 = Disable. 1 = Enable.	0
22	Enable Bucket0	R/W	Enable rate control of the ingress port, bucket 0. 0 = Disable. 1 = Enable.	0

Table 214: Port Rate Control Register (Page 41h: Address 10h–33h) (Cont.)

Bit	Name	R/W	Description	Default
21:19	Buck1_Size	R/W	Bucket size. This bit determines the maximum size of bucket 1. This is specified on a per port basis. 000 = 4 KB. 001 = 8 KB. 010 = 16 KB. 011 = 32 KB. 100 = 64 KB. 101 = 500 KB. 110 = 500 KB. 111 = 500 KB. See "Rate Control" on page 46 for more details.	000
18:11	Buck1_Rate_Cnt	R/W	Rate count. The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the suppressed packet type mask in the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251. See "Rate Control" on page 46 for more details. Values written to these bits must be with the ranges specified by Table 3 on page 47. Values outside these ranges are not valid.	10h
10:8	Buck0_Size	R/W	Bucket size. This bit determines the maximum size of bucket 0. This is specified on a per port basis. 000 = 4 KB. 001 = 8 KB. 010 = 16 KB. 011 = 32 KB. 100 = 64 KB. 101 = 500 KB. 110 = 500 KB. 111 = 500 KB. See "Rate Control" on page 46 for more details.	000

Table 214: Port Rate Control Register (Page 41h: Address 10h–33h) (Cont.)

Bit	Name	R/W	Description	Default
7:0	Buck0_Rate_Cnt	R/W	Rate count. The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the Suppressed packet type mask in the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251. See "Rate Control" on page 46 for more details.	10h

Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)

Table 215: Port Egress Rate Control Configuration Register Address Summary

Address	Description
80h–81h	Port 0
82h–83h	Port 1
84h–85h	Port 2
86h–87h	Port 3
88h–89h	Port 4
8Ah–8Bh	Port 5
8Ch–8Dh	Reserved
8Eh–8Fh	Reserved
90h–91h	IMP port

Table 216: Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	–	0
11	ERC_EN	R/W	Egress rate control enable ((Absolute Bit Rate)	0
10:8	BKT_SZE	R/W	Bucket size. This bit determines the maximum size of bucket 0. This is specified on a per port basis. 000 = 4 KB. 001 = 8 KB. 010 = 16 KB. 011 = 32 KB. 100 = 64 KB. 101 = 500 KB. 110 = 500 KB. 111 = 500 KB. See “Rate Control” on page 46 for more details.	0
7:0	RFSH_CNT	R/W	Refresh count for bucket	0

IMP Port (IMP/Port 5) Egress Rate Control Configuration Register (Page 41h: Address C0h–C1h)

Table 217: IMP Port (IMP/Port5) Egress Rate Control Configuration Register Address Summary

Address	Description
C0h	IMP port

Table 217: IMP Port (IMP/Port5) Egress Rate Control Configuration Register Address Summary (Cont.)

Address	Description
C1h	Port 5 (enable dual-IMP ports, En_IMP_PORT=11 in "Global Management Configuration Register (Page 02h: Address 00h)" on page 168)

Table 218: IMP Port (IMP/Port5) Egress Rate Control Configuration Registers (Page 41h: Address C0h–C1h)

Blt	Name	R/W	Description	Default
7:6	RESERVED	RO	Reserved	0
5:0	Rate_Index	R/W	Rate_Index is used to configure different egress rates for IMP in packet per second (pps). See Table 219: "Using Rate_Index to Configure Different Egress Rates for IMP in pps," on page 257. When set to 0, the egress rate is limited to a maximum of 384 pps. When set to 63, the egress rate control function is disabled and all packets are transmitted at wire-speed. ***Note:*** If the Rate_Index is configured as a certain value, the egress rate is limited to the corresponding speed whether the switch is running at 10 Mbps, 100 Mbps, or 1 Gbps. ***Note:*** The Rate_Index should be a reasonable value under the corresponding network speed configuration. It does not make sense to set a value of 63 with the network configuration at 10 Mbps. In that case, the egress rate is limited up to 10 Mbps.	6'd63

Table 219: Using Rate_Index to Configure Different Egress Rates for IMP in pps

Rate_Index	pps	Rate_Index	pps	Rate_Index	pps	Rate_Index	pps
0	384	16	5376	32	25354	48	357143
1	512	17	5887	33	27382	49	423729
2	639	18	6400	34	29446	50	500000
3	768	19	6911	35	31486	51	568182
4	1024	20	7936	36	35561	52	641026
5	1280	21	8960	37	39682	53	714286
6	1536	22	9984	38	42589	54	781250
7	1791	23	11008	39	56818	55	862069
8	2048	24	12030	40	71023	56	925926
9	2303	25	13054	41	85324	57	1000000
10	2559	26	14076	42	99602	58	1086957
11	2815	27	15105	43	113636	59	1136364
12	3328	28	17146	44	127551	60	1190476

Table 219: Using Rate_Index to Configure Different Egress Rates for IMP in pps (Cont.)

Rate_Index	pps	Rate_Index	pps	Rate_Index	pps	Rate_Index	pps
13	3840	29	19201	45	142045	61	1250000
14	4352	30	21240	46	213675	62	1315789
15	4863	31	23299	47	284091	63	1388889

Page 42h: EAP Register

Table 220: Broadcast Storm Suppression Register (Page 42h)

Address	Bits	Description
00h	8	“EAP Global Control Register (Page 42h: Address 00h)” on page 258
01h	8	“EAP Multiport Address Control Register (Page 42h: Address 01h)” on page 259
02h–09h	64	“EAP Destination IP Register 0 (Page 42h: Address 02h)” on page 260
0Ah–12h	64	“EAP Destination IP Register 1 (Page 42h: Address 0Ah)” on page 260
20h–4Fh	64	“Port EAP Configuration Register (Page 42h: Address 20h)” on page 260
50h–57h	64	Reserved
58h–5Fh	64	Reserved
60h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

EAP Global Control Register (Page 42h: Address 00h)

Table 221: EAP Global Control Registers (Page 42h: Address 00h)

Bit	Name	R/W	Description	Default
7	Reserved	–	–	0
6	EN_RARP	–	When EAP_BLK_MODE is set: 1 = Allow RARP to pass. 0 = Drop RARP.	0
5	EN_BPDU	–	When EAP_BLK_MODE is set: 1 = BPDU Addresses are allowed to pass. 0 = Drop.	–
4	EN_RMC	–	When EAP_BLK_MODE is set: 1 = Allows DA = 01-80-C2-00-00-02, 04–0F to pass. 0 = Drop DA = 01-80-C2-00-00-02, 04–0F to pass.	–

Table 221: EAP Global Control Registers (Page 42h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
3	EN_DHCP	–	When EAP_BLK_MODE is set: 1 = Allows DHCP to pass. 0 = Drop DHCP.	–
2	EN_ARP	–	When EAP_BLK_MODE is set: 1 = Allows ARP to pass. 0 = Drop ARP.	–
1	EN_2DIP	R/W	When EAP_BLK_MODE bit is set: 1 = Two subnet IP addresses defined in EAP destination IP registers 0 and 1 are allowed to pass. 0 = Drop.	0
0	Reserved	–	–	0

EAP Multiport Address Control Register (Page 42h: Address 01h)

Table 222: EAP Multiport Address Control Register (Page 42h: Address 01h)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	–	–
5	EN_MPORT5	R/W	1 = Allow Multiport ETYPE Address 5 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 to pass. 0 = Drop.	–
4	EN_MPORT4	R/W	1 = Allow Multiport ETYPE Address 4 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 to pass. 0 = Drop.	–
3	EN_MPORT3	R/W	1 = Allow Multiport ETYPE Address 3 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 to pass. 0 = Drop.	–
2	EN_MPORT2	R/W	1 = Allow Multiport ETYPE Address 2 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 to pass. 0 = Drop.	–
1	EN_MPORT1	R/W	1 = Allow Multiport ETYPE Address 1 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 to pass. 0 = Drop.	–
0	EN_MPORT0	R/W	1 = Allow Multiport ETYPE Address 0 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 to pass. 0 = Drop.	–

EAP Destination IP Register 0 (Page 42h: Address 02h)

Table 223: EAP Destination IP Registers 0 (Page 42h: Address 02h–09h)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB 0	R/W	EAP destination IP subnet register 0.	0
31:0	DIP_MSK 0	R/W	EAP destination IP mask register 0.	0

EAP Destination IP Register 1 (Page 42h: Address 0Ah)

Table 224: EAP Destination IP Registers 1 (Page 42h: Address 0Ah–12h)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB 1	R/W	EAP destination IP subnet register 1.	0
31:0	DIP_MSK 1	R/W	EAP destination IP mask register 1.	0

Port EAP Configuration Register (Page 42h: Address 20h)

Table 225: Port EAP Configuration Register Address Summary

Address	Description
20h–27h	Port 0
28h–2Fh	Port 1
30h–37h	Port 2
38h–3Fh	Port 3
40h–47h	Port 4
48h–4Fh	Port 5

Table 226: Port EAP Configuration Registers (Page 42h: Address 20h–47h)

Bit	Name	R/W	Description	Default
63:55	Reserved	RO	–	0
52:51	EAP_MODE	R/W	00 = Basic mode, do not check SA. 01 = Reserved. 10 = Extend mode, check SA and port number, drop if SA is unknown. 11 = Simplified mode, check SA and port number trap to management port if SA is unknown.	0

Table 226: Port EAP Configuration Registers (Page 42h: Address 20h–47h) (Cont.)

Bit	Name	R/W	Description	Default
50:49	EAP_BLK_MODE	R/W	00 = Do not check EAP_BLK_MODE. 01 = To check EAP_BLK MODE on ingress port, only the frame defined in EAP_GCFG will be forwarded. Otherwise, the frame will be dropped. 10 = reserved. 11 = To check EAP_BLK MODE on both ingress and egress port, only the frame defined in EAP_GCFG will be forwarded. The forwarding process will verify that each egress port is at block mode.	0
48	EAP_EN_DA	R/W	Enable EAP frame with DA.	0
47:0	EAP_DA	R/W	EAP frame DA register.	00-00-00-00-00-00

Page 43h: MSPT Register

Table 227: Broadcast Storm Suppression Register (Page 43h)

Address	Bits	Description
00h	8	MSPT control register
01h	–	Reserved
02h–05h	32	“MSPT Aging Control Register (Page 43h: Address 02h)” on page 262
06h–0Fh	–	Reserved
10h–2Fh	32	“MSPT Table Register (Page 43h: Address 10h)” on page 262
30h–4Ah	–	Reserved
50h–51h	16	“SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)” on page 263
52h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

MSPT Control Register (Page 43h: Address 00h)

Table 228: MSPT Control Registers (Page 43h: Address 00h–01h)

Bit	Name	R/W	Description	Default
7:1	Reserved	–	–	0
0	EN_802.1S	R/W	0 = Disable. 1 = Enable.	0

MSPT Aging Control Register (Page 43h: Address 02h)

Table 229: MSPT Aging Control Registers (Page 43h: Address 02h–05h)

Bit	Name	R/W	Description	Default
31:8	Reserved	R/W	–	0
7:0	MSPT_AGE_MAP	R/W	Per spanning tree aging enable	0

MSPT Table Register (Page 43h: Address 10h)

Table 230: MSPT Table Register Address Summary

Address	Description
10h–13h	MSPT 0
14h–17h	MSPT 1
18h–1Bh	MSPT 2
1Ch–1Fh	MSPT 3
20h–23h	MSPT 4
24h–27h	MSPT 5
28h–2Bh	MSPT 6
2Ch–2Fh	MSPT 7

Table 231: MSPT Table Registers (Page 43h: Address 10h–2Fh)

Bit	Name	R/W	Description	Default
31:27	Reserved	RO	–	0
26:24	Reserved	R/W	–	0
23:21	Reserved	R/W	–	0
20:18	Reserved	R/W	–	0
17:15	SPT_STA5	R/W	Spanning tree state for port 5	0
14:12	SPT_STA4	R/W	Spanning tree state for port 4. 000 = No spanning tree. 001 = Disabled. 010 = Blocking. 011 = Listening. 100 = Learning. 101 = Forwarding.	0
11:9	SPT_STA3	R/W	Spanning tree state for Port 3.	0
8:6	SPT_STA2	R/W	Spanning tree state for Port 2.	0
5:3	SPT_STA1	R/W	Spanning tree state for Port 1.	0
2:0	SPT_STA0	R/W	Spanning tree state for Port 0.	0

SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

Table 232: SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

Bit	Name	R/W	Description	Default
15:6	Reserved	RO	–	–
5	EN_MPORT5_BYPASS_SPT	R/W	1 = The MPORT_ADD_5 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 is not checked by SPT status. 0 = The MPORT_ADD_5 is checked by SPT status.	–
4	EN_MPORT4_BYPASS_SPT	R/W	1 = The MPORT_ADD_4 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 is not checked by SPT status. 0 = The MPORT_ADD_4 will be checked by SPT status.	–
3	EN_MPORT3_BYPASS_SPT	R/W	1 = The MPORT_ADD_3 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 is not checked by SPT status. 0 = The MPORT_ADD_3 is checked by SPT status.	–
2	EN_MPORT2_BYPASS_SPT	R/W	1 = The MPORT_ADD_2 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 is not checked by SPT status. 0 = The MPORT_ADD_2 is checked by SPT status.	–
1	EN_MPORT1_BYPASS_SPT	R/W	1 = The MPORT_ADD_1 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 is not checked by SPT status. 0 = The MPORT_ADD_1 is checked by SPT status.	–
0	EN_MPORT0_BYPASS_SPT	R/W	1 = The MPORT_ADD_0 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 181 is not checked by SPT status. 0 = The MPORT_ADD_0 is checked by SPT status.	0

Page 70h: MIB Snapshot Control Register

Table 233: MIB Snapshot Control Register

Address	Bits	Description
00h	8	"MIB Snapshot Control Register (Page 70h: Address 00h)" on page 264
01h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280 bytes 0-7
F8h–FDh	–	Reserved

Table 233: MIB Snapshot Control Register (Cont.)

Address	Bits	Description
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

MIB Snapshot Control Register (Page 70h: Address 00h)

Table 234: MIB Snapshot Control Register (Page 70h: Address 00h)

Bit	Name	R/W	Description	Default
7	SNAPSHOT_START/DONE	R/W SC	Write 1'b1 to initiate MIB snapshot access, clear to 1'b0 when MIB snapshot access is done.	0
6	SNAPSHOT_MIRROR	R/W	1'b1 = enable read address to port MIB, but data from MIB snapshot memory. 1'b0 = enable to read from port MIB memory.	0
5:4	Reserved	R/W	–	–
3:0	SNAPSHOT_PORT	R/W	Port Number for MIB snapshot function.	0

Page 71h: Port Snapshot MIB Control Register

Table 235: Port Snapshot MIB Control Register

Address	Bits	Description
71h	–	The Port Snapshot MIB Registers.

Page 85h: WAN Interface (Port 5) External PHY MII Registers

Table 236: WAN Interface (Port 5) External PHY MII Registers

Address	Bits	Description
85h	–	MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are “Page 10h–14h: Internal GPHY MII Registers” on page 193.

Page 88h: IMP Port External PHY MII Registers Page Summary

Table 237: IMP Port External PHY MII Registers Page Summary

Address	Bits	Description
88h	–	MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are "Page 10h–14h: Internal GPHY MII Registers" on page 193.

Page 90h: BroadSync HD Register

Table 238: BroadSync HD Register

Address	Bits	Description
00h–01h	16	"BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)" on page 266
02h	8	"BroadSync HD Time Stamp Report Control Register (Page 90h: Address 02h)" on page 266
03h	–	Reserved
04h–05h	8	"BroadSync HD Max Packet Size Register (Page 90h: Address 04h)" on page 267
06h–09h	–	Reserved
10h–13h	32	"BroadSync HD Time Base Register (Page 90h: Address 10h–13h)" on page 267
14h–17h	32	"BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17)" on page 267
18h–1Bh	32	"BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)" on page 268
1Ch–1Fh	32	"BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)" on page 268
20h–2Fh	–	Reserved
30h–3Bh	16	"BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)" on page 269
3Ch–5Fh	–	Reserved
60h–6Bh	16	"BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h)" on page 270
6Ch–8Fh	–	Reserved
90h–A7h	32	"BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)" on page 270
AFh	8	"BroadSync HD Egress Time Stamp Status Register (Page 90h: Address AFh)" on page 271
A5h–AFh	–	Reserved

Table 238: BroadSync HD Register (Cont.)

Address	Bits	Description
B0h–B1h	16	"BroadSync HD Link Status Register (Page 90h: Address B0h–B1h)" on page 271
B2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280 bytes 0-7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)

Table 239: BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)

Bit	Name	R/W	Description	Default
15:6	Reserved	RO	Reserved	0
5:0	AV Enable	R/W	BroadSync HD enable. Bits [5:0] correspond to ports [5:0].	0

BroadSync HD Time Stamp Report Control Register (Page 90h: Address 02h)

Table 240: BroadSync HD Time Stamp Report Control Register (Page 90h: Address 02h)

Bit	Name	R/W	Description	Default
7:1	Reserved	RO	Reserved	0
0	TSRPT_PKT_EN	R/W	This field is to allow the Time Stamp Reporting Packet to IMP port when the time synchronization packet transmitted on egress port.	0

BroadSync HD PCP Value Control Register (page 90h: Address 03h)

Table 241: BroadSync HD PCP Value Control Register (page 90h: Address 03h)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0
5:3	ClassB_PCP	R/W	BroadSync HD Class B PCP value. This field is used to qualify the PCP value of the BroadSync HD packet. This BroadSync HD packet is sent to Queue4.	3'd4

Table 241: BroadSync HD PCP Value Control Register (page 90h: Address 03h) (Cont.)

Bit	Name	R/W	Description	Default
2:0	ClassA_PCP	R/W	BroadSync HD Class A PCP value. This field is used to qualify the PCP value of the BroadSync HD packet. This BroadSync HD packet is sent to Queue5.	3'd5

BroadSync HD Max Packet Size Register (Page 90h: Address 04h)

Table 242: BroadSync HD Max Packet Size Register (Page 90h: Address 04h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Reserved	0
11:0	MAX_AV_PACKET_SIZE	R/W	This field is to define the max packet size of BroadSync HD. The ingress port uses it to qualify if the packet is allowed to pass through an AV link. The egress port uses it to perform shaping gate.	12'd1518

BroadSync HD Time Base Register (Page 90h: Address 10h–13h)

Table 243: BroadSync HD Time Base Register (Page 90h: Address 10h–13h)

Bit	Name	R/W	Description	Default
31:0	TIME BASE	RO	Time Base. This is a 32-bit free running clock (running at 25 MHz) for BroadSync HD time base. Ingress port and Egress port use it for Time Synchronization Packet Time Stamp.	0

BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17)

Table 244: BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17h)

Bit	Name	R/W	Description	Default
31:12	Reserved	RO	Reserved	0
11:8	TIME ADJUST PERIOD	R/W	Time Adjust Period. This field defines the tick numbers to apply the adjusted Time Increment (when Time Increment does not equal to 40). For example, to increment the Time Base for 10 ticks with 41 ns per tick, Time Adjust Period is 10, and Time Increment is 41.	4'h0
7:6	Reserved	RO	Reserved	0

Table 244: BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17h) (Cont.)

Bit	Name	R/W	Description	Default
5:0	TIME INCREMENT	R/W	Time Increment. This field defines the value to add into Time Base in each 25 MHz tick. Default is 40.	6'd40

BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)

Table 245: BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)

Bit	Name	R/W	Description	Default
31:28	Reserved	RO	Reserved	0
27:16	TICK COUNTER	R/W	Tick Counter. This is the tick counter which defines when will Slot Number increment. It runs from 1 to 3125 (or 3124, or 3126, depends on "BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)" on page 268 setting) under 25 MHz.	12'h0
15:5	Reserved	RO	Reserved	0
4:0	SLOT NUMBER	R/W	This field specifies the Slot Number for BroadSync HD.	8'h0

BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)

Table 246: BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)

Bit	Name	R/W	Description	Default
31:18	Reserved	RO	Reserved	0
17:16	MACRO SLOT PERIOD	R/W	Macro Slot Period. This field defines the slot time of a macro slot for Class 4 traffic. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = Reserved. Class 5 traffic slot time is always 125s period.	2'h0
15:12	Reserved	RO	Reserved	0
11:8	SLOT ADJUST PERIOD	R/W	Slot Adjust Period. This field defines the number of slots to apply the alterable slot adjustment.	8'h0

Table 246: BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh) (Cont.)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0
1:0	SLOT ADJUSTMENT	R/W	Slot Adjustment. This field defines when the slot number counter increment by 1. Default is 40. 00 = Slot Number increased by 1 when tick counter rolls over 3125. 01 = 3126. 10 = 3124. 11 = Reserved.	2'h0

BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)

Table 247: BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)

Address	Description
30h–31h	Port 0
32h–33h	Port 1
34h–35h	Port 2
36h–37h	Port 3
38h–39h	Port 4
3Ah-3Bh	Port 5

Table 248: BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h–31h, 32h–33h, 34h–35h, 36h–37h, 38h–39h)

Bit	Name	R/W	Description	Default
15	C5_WINDOW	R/W	The purpose is to control the credit carry-over under different link speed. For a 100M link, the 125-µs slot is too small such that BroadSync HD packet could easily "slip slot", so the credit carry-over should be allowed. For a 1G link, 125-µs slot is reasonably big such that the BW reservation could be done in a conservative way to prevent "slot slipping", so credit carry-over is not needed.	1'b0
14	Reserved	R/W	Reserved	0
13:0	C5_BANDWIDTH	R/W	This field defines the byte count allowed for Class 5 traffic transmission within a slot time.	14'h0

BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h)

Table 249: BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h)

Address	Description
60h–61h	Port 0
62h–63h	Port 1
64h–65h	Port 2
66h–67h	Port 3
68h–69h	Port 4
6Ah-6Bh	Port 5

Table 250: BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h–61h, 62h–63h, 64h–65h, 66h–67h, 68h–69h)

Bit	Name	R/W	Description	Default
15:14	Reserved	R/W	Reserved	0
13:0	C4_BANDWIDTH	R/W	This field defines the byte count allowed for Class 4 traffic transmission within a slot time.	14'h0

BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)

Table 251: BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)

Address	Description
90h–93h	Port 0
94h–97h	Port 1
98h–9Bh	Port 2
9Ch–9Fh	Port 3
A0h–A3h	Port 4
A4h-A7h	Port 5

Table 252: BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h–93h, 94h–97h, 98h–9Bh, 9Ch–9Fh, A0h–A3h, A4h–A7h)

Bit	Name	R/W	Description	Default
31:0	EGRESS_TS	R	Egress Time Synchronous Packet Time Stamp. This field reports the time stamp of egress time synchronous packet. It uses 32-bit time base as time stamping. The time between the departure of first byte of MAC DA and the time stamping point should be constant.	32'h0

BroadSync HD Egress Time Stamp Status Register (Page 90h: Address AFh)

Table 253: BroadSync HD Egress Time Stamp Status Register (Page 90h: Address AFh)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0
5:0	VALID STATUS	RO	Valid Status. 5 bits field indicating the valid status for each "BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)" on page 270. When "BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)" on page 270 is read out by SPI, the valid status will be cleared, respectively.	6'h0

BroadSync HD Link Status Register (Page 90h: Address B0h–B1h)

Table 254: BroadSync HD Link Status Register (Page 90h: Address B0h–B1h)

Bit	Name	R/W	Description	Default
15:5	Reserved	R/W	Reserved	0
4:0	Port BroadSync HD Link Status	R/W	BroadSync HD Link Status. When software write the port BroadSync HD link status and select bit 14 in LED Function Control Register. The BroadSync HD link status is shown on the LED. Bits [4:0] correspond to ports [4:0].	5'h0

BroadSync HD Egress Time Stamp Status Registers (Page 90h: Address D0h)

Table 255: BroadSync HD Egress Time Stamp Status Registers (Page 90h: Address D0h)

Bit	Name	R/W	Description	Default
7:0	VALID STATUS	RO	Valid Status. 8-bit field indicating the valid status for each "BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)" on page 270. When the BroadSync HD Egress Time Stamp Register is read out by SPI, the valid status is cleared.	8'h0

BroadSync HD Link Status Register (Page 90h: Address E0h–E1h)

Table 256: BroadSync HD Link Status Register (Page 90h: Address E0h–E1h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Reserved	0
8:0	Port BroadSync HD Link Status	R/W	BroadSync HD Link Status. When software writes the port BroadSync HD link status and selects bit 14 in the LED Function Control Register, the BroadSync HD link status is shown on the LED. Bits [8:0] correspond to ports [8:0].	9'h0

Page 91h: Traffic Remarking Register

Table 257: Traffic Remarking Register

Address	Bits	Description
00h–03h	32	"Traffic Remarking Control Register (Page 91h: Address 00h)" on page 272
04h–0Fh	–	Reserved
10h-57h	32	"Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h)" on page 273
58h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 280, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 280
FFh	8	"Page Register (Global, Address FFh)" on page 280

Traffic Remarking Control Register (Page 91h: Address 00h)

Table 258: Traffic Remarking Control Register (Page 91h: Address 00h)

Bit	Name	R/W	Description	Default
31:25	Reserved	RO	Reserved	0
24:16	PCP_REMARKING_EN	R/W	PCP Remarking Enable. Bit 24 = IMP port. Bits [21:16] correspond to ports [5:0], respectively.	0
15:9	Reserved	R/W	Reserved	–
8:0	CFI_REMARKING_EN	R/W	CFI Remarking Enable. Bit 8 = IMP port. Bits [5:0] correspond to ports [5:0], respectively.	0

Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h)

Table 259: Egress Packet TC to PCP Mapping Register Address Summary

Address	Description
10h-17h	Port 0
18h-1Fh	Port 1
20h-27h	Port 2
28h-2Fh	Port 3
30h-37h	Port 4
38h-3Fh	Port 5
40h-47h	Reserved
48h-4Fh	Reserved
50h-57h	IMP

Table 260: Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h–17h, 18h–1Fh, 20h–27h, 28h–2Fh, 30h–37h, 38h–3Fh, 50h-57h)

Bit	Name	R/W	Description	Default
63:60	Reserved	R/W	Reserved	4'b1111
59:56	Reserved	R/W	Reserved	4'b1110
55:52	Reserved	R/W	Reserved	4'b1101
51:48	Reserved	R/W	Reserved	4'b1100
47:44	Reserved	R/W	Reserved	4'b1011
43:40	Reserved	R/W	Reserved	4'b1010
39:36	Reserved	R/W	Reserved	4'b1001
35:32	Reserved	R/W	Reserved	4'b1000
31:28	{CFI,PCP} for TC = 7	R/W	{CFI,PCP} field for TC = 7.	4'b0111
27:24	{CFI,PCP} for TC = 6	R/W	{CFI,PCP} field for TC = 6.	4'b0110
23:20	{CFI,PCP} for TC = 5	R/W	{CFI,PCP} field for TC = 5.	4'b0101
19:16	{CFI,PCP} for TC = 4	R/W	{CFI,PCP} field for TC = 4.	4'b0100
15:12	{CFI,PCP} for TC = 3	R/W	{CFI,PCP} field for TC = 3.	4'b0011
11:8	{CFI,PCP} for TC = 2	R/W	{CFI,PCP} field for TC = 2.	4'b0010
7:4	{CFI,PCP} for TC = 1	R/W	{CFI,PCP} field for TC = 1.	4'b0001
3:0	{CFI,PCP} for TC = 0	R/W	{CFI,PCP} field for TC = 0.	4'b0000

Page 92h: EEE Control Registers

Table 261: EEE Enable Control Register (Page 92h: Address 00h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	EN_EEE	R/W	Enable EEE function per port. 1 = Enable EEE (default). 0 = Disable EEE. Bit [8] = IMP port. Bits [7:6] = reserved. Bits [5:0] = port [5:0]. The port 0–port 4 (internal PHY) default values are read from EN_EEE strap pin during power-on. The value can be overwritten after power-on.	01Fh

Table 262: EEE LPI Assert Register (Page 92h: Address 02h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	–
8:0	LPI_Assert_status	RO	Low power assert input signal status 1 = Low Power asserted. 0 = Low Power deasserted. Bit [8] = IMP port. Bits [7:6] = reserved. Bits [5:0] = port [5:0]. Each bit indicates that lowPowerAssert input signal that commands the transmit MAC to generate low-power idle symbols to the PHY after the transmit MAC completes transmitting in-process packet data.	0x0

Table 263: EEE LPI Indicate Register (Page 92h: Address 04h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	–

Table 263: EEE LPI Indicate Register (Page 92h: Address 04h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	LPI_Indicate	RO	lowPowerIndicate output signal status. 1 = Low Power Indicate asserted. 0 = Low Power Indicate deasserted. Bit [8] = IMP port. Bits [7:6] = reserved. Bits [5:0] = port [5:0]. Each bit indicates that lowPowerIndicate output is asserted whenever the Receive PHY is sending low-power idle symbols to the receive MAC.	0x0

Table 264: EEE RX Idle Symbol Register (Page 92h: Address 06h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	–
8:0	RX_Idle_Symbol	RO	Receiving IdleSymbols output signal status. 1 = Idle Symbol output asserted. 0 = Idle Symbol output deasserted. Bit [8] = IMP port. Bits [7:6] = reserved. Bits [5:0] = port [5:0]. Each bit indicates that receiving Idle Symbols output that is asserted whenever the receive PHY is sending normal idle symbols to the receive MAC.	0x0

Table 265: EEE Pipeline Timer Register (Page 92h: Address 0Ch)

Bit	Name	R/W	Description	Default
31:0	Pipeline Timer	R/W	EEE pipeline delay timer load value. The unit is system clock rate (ex. If system clock = 100 MHz, unit = 10 nsec).	0x00000020

Table 266: EEE Sleep Timer Gig Register (Page 92h: Address 10h)

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2

Table 266: EEE Sleep Timer Gig Register (Page 92h: Address 10h) (Cont.)

Address	Description
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	Reserved
30h–33h	IMP

Table 267: EEE Sleep Timer G Register (Page 92h: Address 10h–33h)

Bit	Name	R/W	Description	Default
31:0	Sleep Timer G	–	EEE sleep delay timer load value for 1G operation. The unit is 1 µs.	0x00000004

Table 268: EEE Sleep Timer FE Register (Page 92h: Address 34h)

Address	Description
34h–37h	Port 0
38h–3Bh	Port 1
3Ch–3Fh	Port 2
40h–43h	Port 3
44h–47h	Port 4
48h–4Bh	Port 5
4Ch–53h	Reserved
54h–57h	IMP

Table 269: EEE Sleep Timer FE Register (Page 92h: Address 34h–57h)

Bit	Name	R/W	Description	Default
31:0	Sleep Timer FE	–	EEE sleep delay timer load value for 100M operation. The unit is 1 µs.	0x00000028

Table 270: EEE Min LP Timer Gig Register (Page 92h: Address 58h)

Address	Description
58h–5Bh	Port 0
5Ch–5Fh	Port 1
60h–63h	Port 2
64h–67h	Port 3

Table 270: EEE Min LP Timer Gig Register (Page 92h: Address 58h) (Cont.)

Address	Description
68h–6Bh	Port 4
6Ch–6Fh	Port 5
70h–77h	Reserved
78h–7Bh	IMP

Table 271: EEE Min LP timer G Register (Page 92h: Address 58h–7Bh)

Bit	Name	R/W	Description	Default
31:0	Min LP Timer G	–	EEE minimum low-power duration delay timer load value for 1G operation. The unit is 1 µs.	0x00000032

Table 272: EEE Min LP Timer FE Register (Page 92h: Address 7Ch)

Address	Description
7Ch–7Fh	Port 0
80h–83h	Port 1
84h–87h	Port 2
88h–8Bh	Port 3
8Ch–8Fh	Port 4
90h–93h	Port 5
94h–9Bh	Reserved
9Ch–9Fh	IMP

Table 273: EEE Min LP timer FE Register (Page 92h: Address 7Ch–9Fh)

Bit	Name	R/W	Description	Default
31:0	Min LP Timer FE	–	EEE minimum low-power duration delay timer load value for 100M operation. The unit is 1 µs.	0x000001F4

Table 274: EEE Wake Timer G Register (Page 92h: Address A0h)

Address	Description
A0h–A1h	Port 0
A2h–A3h	Port 1
A4h–A5h	Port 2
A6h–A7h	Port 3
A8h–A9h	Port 4

Table 274: EEE Wake Timer G Register (Page 92h: Address A0h) (Cont.)

Address	Description
AAh–ABh	Port 5
ACh–AFh	Reserved
B0h–B1h	IMP

Table 275: EEE Wake timer G Register (Page 92h: Address A0h–B1h)

Bit	Name	R/W	Description	Default
15:0	Wake Timer G	–	EEE wake transition delay timer load value for 1G operation. The unit is 1 µs.	0x0011

Table 276: EEE Wake Timer FE Register (Page 92h: Address B2h)

Address	Description
B2h–B3h	Port 0
B4h–B5h	Port 1
B6h–B7h	Port 2
B8h–B9h	Port 3
BAh–BBh	Port 4
BCh–BDh	Port 5
BEh–C1h	Reserved
C2h–C3h	IMP

Table 277: EEE Min LP timer FE Register (Page 92h: Address B2h–C3h)

Bit	Name	R/W	Description	Default
15:0	Wake Timer FE	R/W	EEE wake transition delay timer load value for 100M operation. The unit is 1 µs.	0x0024

Table 278: EEE Global Congestion Threshold Register (Page 92h: Address C4h)

Bit	Name	R/W	Description	Default
15:0	Reserved	RO	–	–

Table 278: EEE Global Congestion Threshold Register (Page 92h: Address C4h) (Cont.)

Bit	Name	R/W	Description	Default
9:0	GLB_CONG_TH	R/W	EEE global packet buffer congestion threshold. If this threshold is set to zero, then EEE is effectively disabled, if this threshold is set equal to or greater than 512(the number of cells implemented in the packet buffer), then protections against packet loss are disabled. The unit is buffer cell size: 256-byte cell.	0x100

Table 279: EEE TXQ Congestion Threshold Register (Page 92h: Address C6h)

Name	Description
C6h–C7h	TXQueue 0
C8h–C9h	TXQueue 1
CAh–CBh	TXQueue 2
CCh–CDh	TXQueue 3
CEh–CFh	TXQueue 4
D0h–D1h	TXQueue 5

Table 280: EEE TXQ Congestion Threshold Register (Page 92h: Address C6h–D1h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	–	–
9:0	TXQ_CONG_TH	R/W	EEE TXQ packet buffer congestion threshold. • If this threshold is set to zero, then EEE for queue N is effectively disabled. • If this threshold is set equal to or greater than 512(the number of cells implemented in the packet buffer), then protections against packet loss are disabled. The unit is buffer cell size: 256-byte cell.	Q0 = 0x03A Q1 = 0x03A Q2 = 0x03A Q3 = 0x001 Q4 = 0x001 Q5 = 0x001

Global Registers

Table 281: Global Registers (Maps to All Pages)

Address	Bits	Description
F0h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 0

Table 281: Global Registers (Cont.) (Maps to All Pages)

Address	Bits	Description
F1h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 1
F2h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 2
F3h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 3
F4h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 4
F5h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 5
F6h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 6
F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 280, 7
F8–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 280
FFh	8	“Page Register (Global, Address FFh)” on page 280

SPI Data I/O Register (Global, Address F0h)

Table 282: SPI Data I/O Register (Maps to All Registers, Address F0h–F7h)

Bit	Name	R/W	Description	Default
7:0	SPI Data I/O	R/W	SPI data bytes [7:0]	0

SPI Status Register (Global, Address FEh)

Table 283: SPI Status Register (Maps to All Registers, Address FEh)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI read/write complete flag	0
6	Reserved	RO	–	0
5	RACK	RO (SC)	SPI read data ready acknowledgement (self-clearing)	0
4:2	Reserved	RO	–	0
1	Reserved	RO	–	0
0	Reserved	RO	–	0

Page Register (Global, Address FFh)

Table 284: Page Register (Maps to All Registers, Address FFh)

Bit	Name	R/W	Description	Default
7:0	Page_Reg	R/W	The binary value determines the value of the accessed register page.	0

Section 8: Electrical Characteristics

Absolute Maximum Ratings

Table 285: Absolute Maximum Ratings

Symbol	Parameter and Pins	Minimum	Maximum	Units
AVDDL, DVDD, EGPHY_PLLVDD, QGPHY1_PLLVDD, QGPHY2_PLLVDD	Supply voltage	GND – 0.3	1.32	V
OVDD, OVDD3, OVDD2, OTP_VDD, EPHY_BVDD, QGPHY1_BVDD, QGPHY2_BVDD, SWREG_VDDO, XTAL_AVDD	Supply voltage	GND – 0.3	3.63	V
I_I	Input current	–	–	mA
T_{STG}	Storage temperature	–40	125	°C
V_{ESD}	Electrostatic discharge	–	1800V	V
–	Input voltage: Digital input pins	–	–	V

Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Recommended Operating Conditions

Table 286: Recommended Operating Conditions

Symbol	Parameter	Pins	Minimum	Maximum	Units
VDD	Supply voltage	–	1.14	1.26	V
		–	3.14	3.47	V
		–	–	–	V
		–	–	–	V
V_{IH}	High-level input voltage	All digital inputs	1.7	–	V
V_{IL}	Low-level input voltage for 2.5 V	All digital inputs	–	0.7	V
V_{IL}	Low-level input voltage for 3.3 V	All digital inputs	–	0.9	V
$-T_A$	Ambient operating temperature	–	0	70	°C

Note: The recommended minimum/maximum operating voltages are not final. The final numbers will be updated after the characterization.

Electrical Characteristics

Table 287: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Min.	Typical	Max.	Units
I_{DD}	Supply current (for GMII/ RvMII/MII operation)	1.2V power rail	estimated	–	870	–	mA
		3.3V power rail (excluding OVDD and OVDD3)	estimated	–	330	–	mA
		OVDD and OVDD 3 (3.3V for GMII/RvMII/MII)	estimated	–	90	–	mA
I_{DD}	Supply current (for RGMII operation)	1.2V power rail	estimated	–	870	–	mA
		3.3V power rail	estimated	–	330	–	mA
		2.5V power rail (OVDD and OVDD3)	–	–	60	–	mA
V_{OH}	High-level output voltage	Digital output pins at 3.3V	Ioh = –8 mA	2.4	–	–	V
		Digital output pins at 3.3V	I_{OH} = –8 mA	2.0	–	–	V
		Digital output pins at 1.5V	I_{OH} = –8 mA	1.0	–	–	V
V_{OL}	Low-level output voltage	Digital output pins at 3.3V	I_{OL} = 8 mA	–	–	0.4	V
		Digital output pins at 2.5V	I_{OL}= 8 mA	–	–	0.4	V
		Digital output pins at 1.5V	I_{OL} = 8 mA	–	–	0.4	V
V_{IH}	High-level input voltage	Digital input pins at 3.3V and 2.5V	–	1.7	–	–	V
		Digital input pins at 1.5V	–	0.9	–	–	V
		XTALI	–	1.7	–	–	V
V_{IL}	Low-level input voltage	Digital input pins for 3.3V	–	–	–	0.9	V
		Digital input pins for 2.5V	–	–	–	0.7	V
		Digital input pins at 1.5V	–	–	–	0.5	V
		XTALI	–	–	–	0.8	V
I_I	Input current	Digital Inputs w/pull-up resistors	–	–	–	–	µA
		Digital Inputs w/pull-up resistors	–	–	–	–	µA
		Digital Inputs w/pull-down resistors	–	–	–	–	µA
		Digital Inputs w/pull-down resistors	–	–	–	–	µA
		All other digital inputs	–	–	–	–	µA

Table 288: Internal Voltage Regulator Electrical Characteristics

Parameter	Min	Typ	Max
Switching Frequency	–	1 MHz	–
1.2V Regulator Output Range	0.975V	–	1.35V

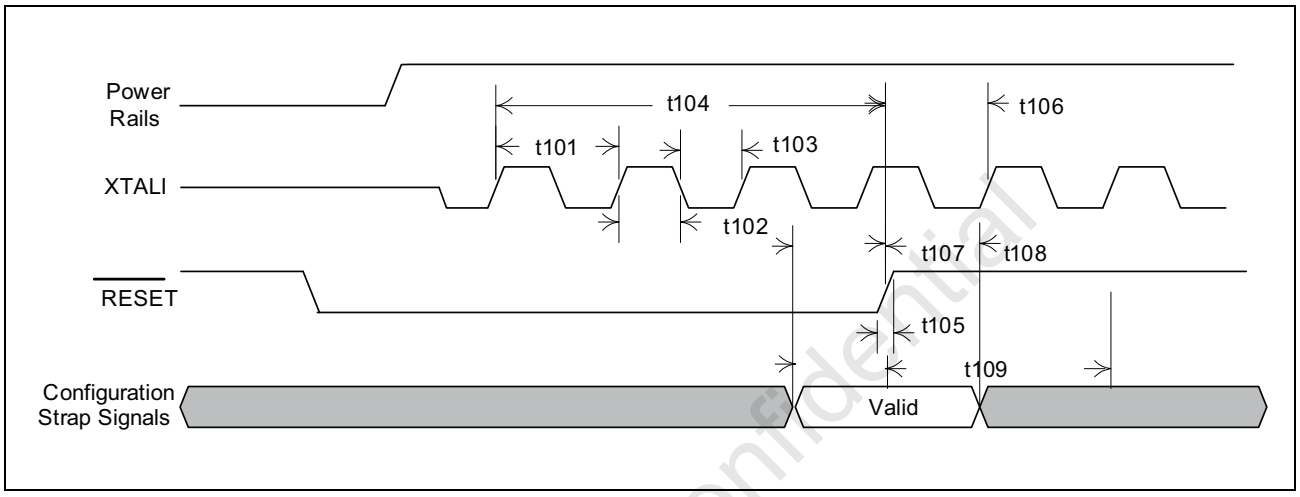
Table 288: Internal Voltage Regulator Electrical Characteristics (Cont.)

Parameter	*Min*	*Typ*	*Max*
1.2V Regulator Output Ripple	–	25 mV	–
1.2V Output Current	–	–	16 mA
1.2V Ramp Up Time	–	–	2 mS

Section 9: Timing Characteristics

Reset and Clock Timing

Figure 51: Reset and Clock Timing



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 289: Reset and Clock Timing

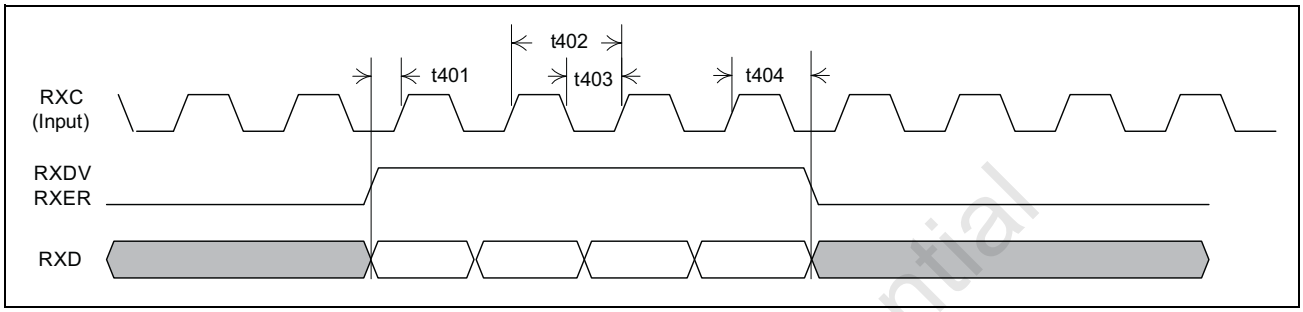
Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
XTALI period	t101	39.998 ns	40 ns	40.002 ns
XTALI high time	t102	18 ns	–	22 ns
XTALI low time	t103	18 ns	–	22 ns
$\overline{\text{RESET}}$ low pulse duration	t104	80 ms	100 ms	–
$\overline{\text{RESET}}$ rise time	t105	–	–	25 ns
Configuration valid setup to $\overline{\text{RESET}}$ rising	t107	100 ns	–	–
Configuration valid hold from $\overline{\text{RESET}}$ rising	t108	–	–	100 ns
Hardware initialization is complete. All the strap pin values are clocked in, and the internal registers can be accessed.	t109	5 ms before the registers can be accessed		

MII/TMII Interface Timing

The following specifies timing information for the MII/TMII Interface pins.

MII/TMII/TMII Input Timing

Figure 52: MII Input Timing



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 290: MII Input Timing

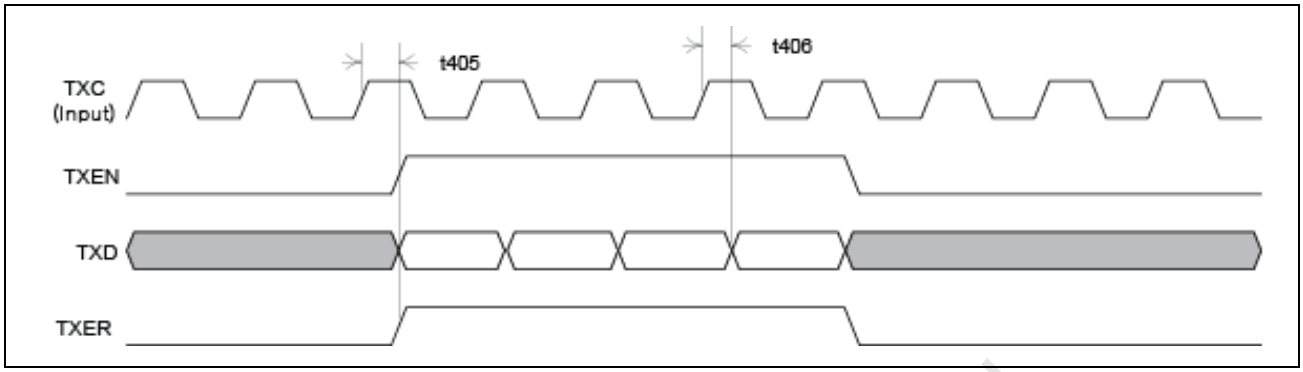
Parameter	Description	Min	Typ	Max
t401	RXDV, RXD to RXC rising setup time	10 ns	–	–
t402	RXC clock period (10BASE-T mode)	–	400 ns	–
	RXC clock period (100BASE-TX mode)	–	40 ns	–
t403	RXC high/low time (10BASE-T mode)	160 ns	–	240 ns
	RXC high/low time (100BASE-TX mode)	16 ns	–	24 ns
t404	RXDV, RXD to RXC rising hold time	10 ns	–	–
–	Duty cycle	–	–	–

Table 291: TMII Input Timing

Parameter	Description	Min	Typ	Max
t401	RXDV, RXD to RXC rising setup time	5 ns	–	–
t402	RXC clock period	–	20 ns	–
t403	RXC high/low time	8 ns	–	12 ns
t404	RXDV, RXD to RXC rising hold time	5 ns	–	–
–	Duty cycle	–	–	–

MII/TMII Output Timing

Figure 53: MII Output Timing



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 292: MII Output Timing

Parameter	Description	Min	Typ	Max
t405	TXC high to TXEN, TXD valid	0 ns	–	25 ns
t406	TXC high to TXEN, TXD invalid (hold)	0 ns	–	–

Table 293: TMII Output Timing

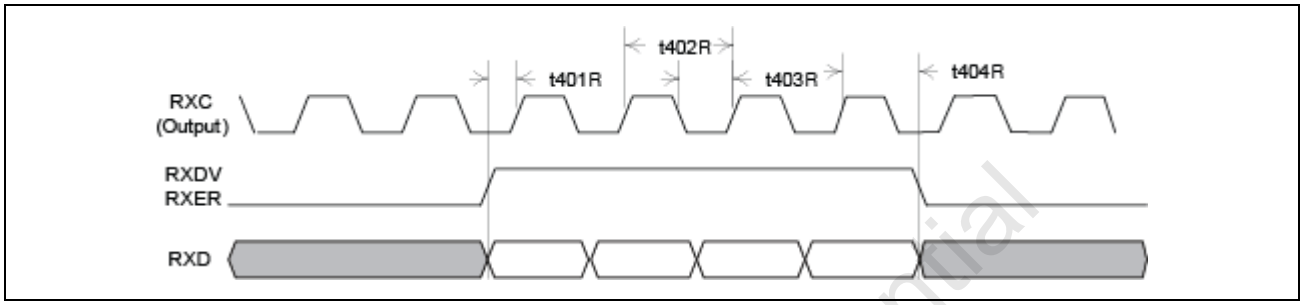
Parameter	Description	Min	Typ	Max
t405	TXC high to TXEN, TXD valid	0 ns	–	14 ns
t405	TXC high to TXEN, TXD invalid (hold)	0 ns	–	–

Reverse MII/TMII Interface Timing

The following specifies timing information regarding the Reverse MII/TMII interface pins.

Reverse MII/TMII Input Timing

Figure 54: Reverse MII Input Timing



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 294: Reverse MII Input Timing

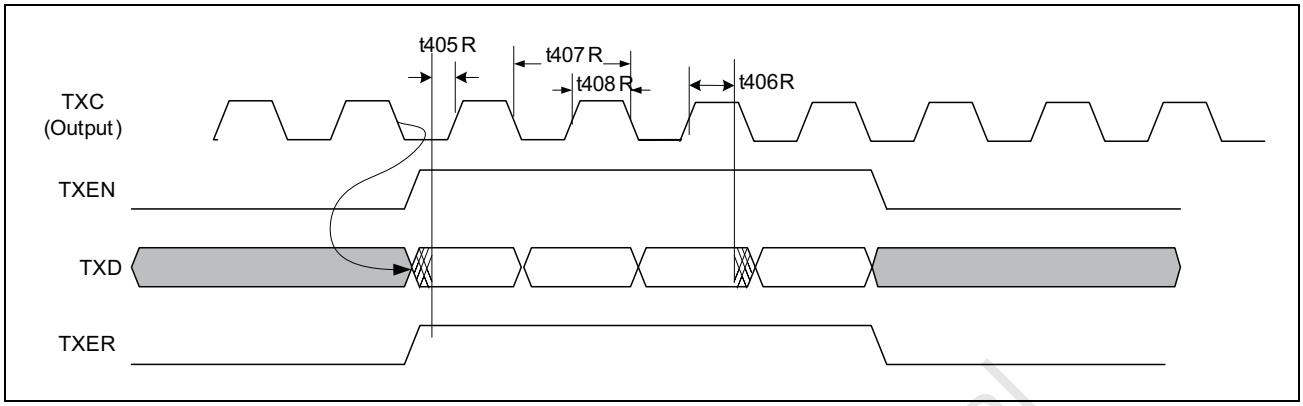
Description	Parameter	Min	Typ	Max	Units
RXDV, RXD to RXC rising setup time	t401R	10	–	–	ns
RXC (output) clock period (10BASE-T mode)	t402R	–	400	–	ns
RXC clock period (100BASE-TX mode)		–	40	–	ns
RXC high/low time (10BASE-T mode)	t403R	160	–	240	ns
RXC high/low time (100BASE-TX mode)		16	–	24	ns
RXDV, RXD to RXC rising hold time	t404R	0	–	–	ns

Table 295: Reverse TMII Input Timing

Description	Parameter	Min	Typ	Max	Units
RXDV, RXD to RXC rising setup time	t401R	12	–	–	ns
RXC (output) clock period	t402R	–	20	–	ns
RXC high/low time (10BASE-T mode)	t403R	8	–	12	ns
RXDV, RXD to RXC rising hold time	t404R	0	–	–	ns

Reverse MII/TMII Output Timing

Figure 55: Reverse MII Output Timing



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 296: Reverse MII Output Timing

Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Output (TXD, TX_EN) setup to TXC rising	t405R	15	–	25	ns
Output (TXD, TX_EN) hold from TXC rising	t406R	11	–	–	ns
TXC clock period	t407R	–	40	–	ns
TXC high/low time	t408R	15	–	22	ns

Table 297: Reverse TMII Output Timing

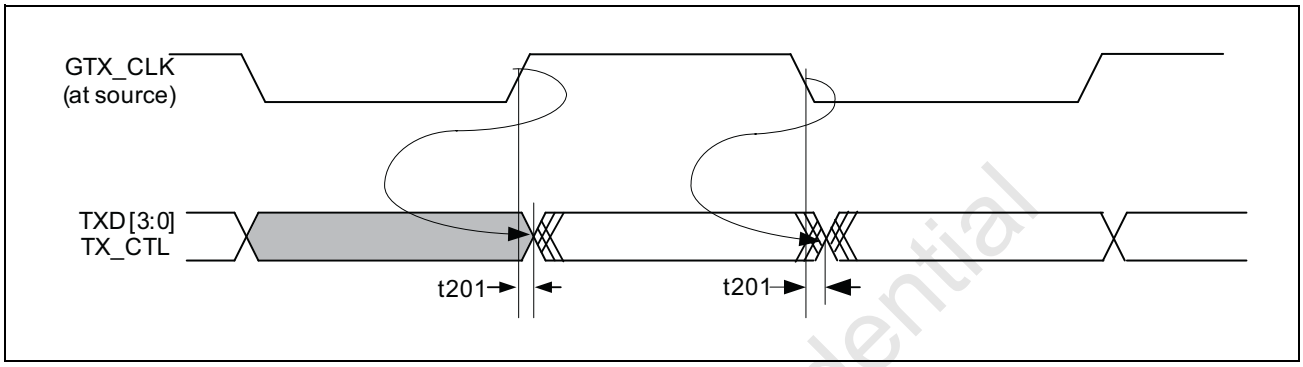
Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Output (TXD, TX_EN) setup to TXC rising	t405R	5	–	–	ns
Output (TXD, TX_EN) hold from TXC rising	t406R	5	–	–	ns
TXC clock period	t407R	–	20	–	ns
TXC high/low time	t408R	7.5	–	11	ns

RGMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in RGMII mode.

RGMII Output Timing (Normal Mode)

Figure 56: RGMII Output Timing (Normal Mode)



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

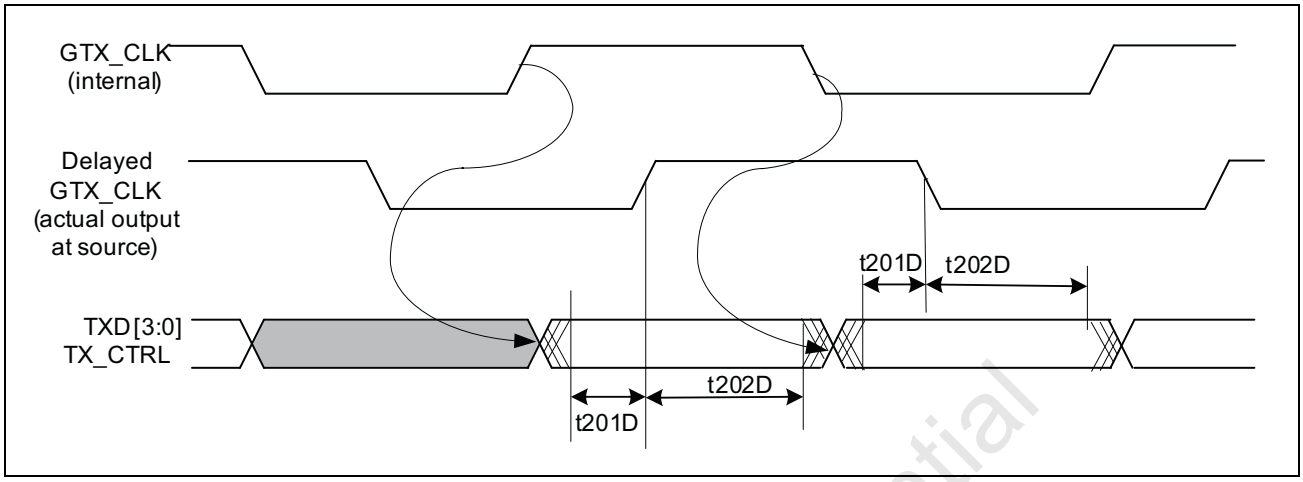
Table 298: RGMII Output Timing (Normal Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
MII1_TXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_TXC clock period (100M mode)	–	36	40	44	ns
MII1_TXC clock period (10M mode)	–	360	400	440	ns
TskewT: Data to clock output skew	t201	–500 (1000M)	0	+500 (1000M)	ps
TskewT: Data to Clock at 1.5V mode	t201	–750 (1000M)	0	+500 (1000M)	ps
Duty cycle for 1000M (GbE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

Note: The output timing in 10/100M operation is always as specified in the delayed mode.

RGMII Output Timing (Delayed Mode)

Figure 57: RGMII Output Timing (Delayed Mode)



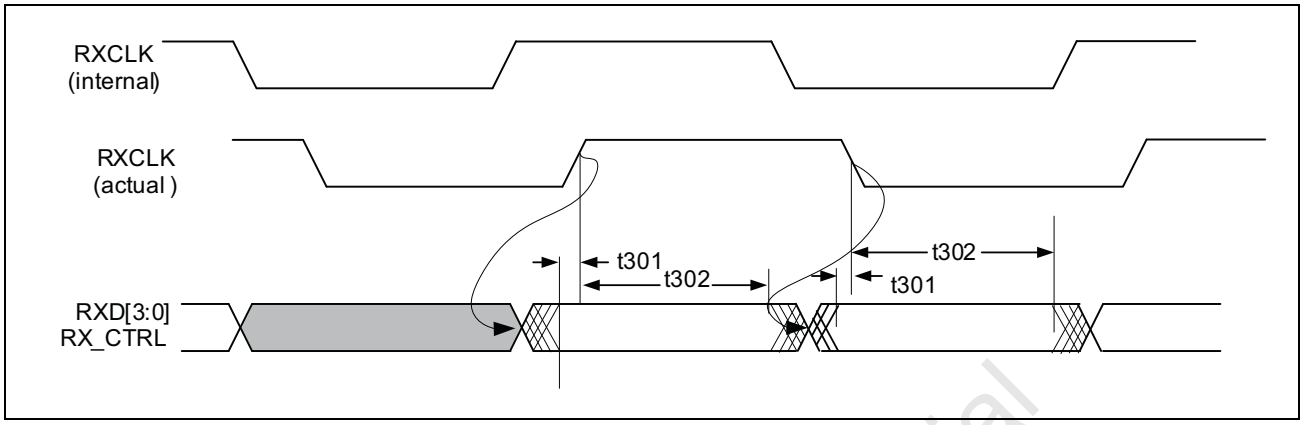
Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 299: RGMII Output Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
MII1_TXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_TXC clock period (100M mode)	–	36	40	44	ns
MII1_TXC clock period (10M mode)	–	360	400	440	ns
TsetupT Data valid to clock transition: Available setup time at the output source (delayed mode)	t201D	1.2 (all speeds)	2.0	–	ns
TholdT Clock transition to data valid: Available hold time at the output source (delayed mode)	t202D	1.2 (all speeds)	2.0	–	ns
TsetupT Data valid to clock transition: Available setup time at the output source (1.5V mode)	t201D	1.0 (all speeds)	2.0	–	ns
TholdT Clock transition to data valid: Available hold time at the output source (1.5V mode)	t202D	1.0 (all speeds)	2.0	–	ns
Duty cycle for 1000M (GbE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

RGMII Input Timing (Normal Mode)

Figure 58: RGMII Input Timing (Normal Mode)



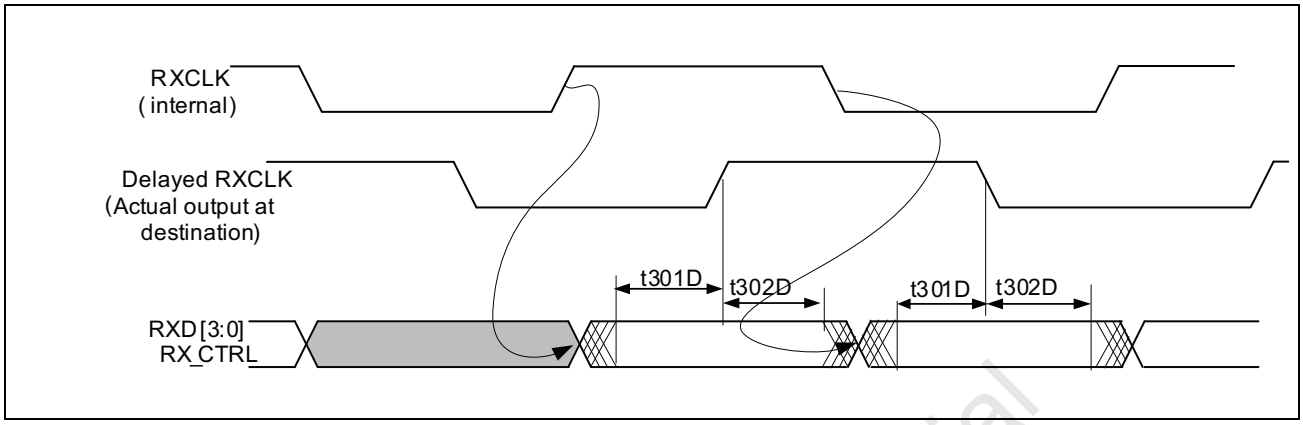
Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 300: RGMII Input Timing (Normal Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
MII1_RXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_RXC clock period (100M mode)	–	36	40	44	ns
MII1_RXC clock period (10M mode)	–	360	400	440	ns
TsetupR Input setup time: Valid data to clock	t301	1.0	2.0	–	ns
TholdR Input hold time: Clock to valid data	t302	1.0	2.0	–	ns
Duty cycle for 1000M (GbE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

RGMII Input Timing (Delayed Mode)

Figure 59: RGMII Input Timing (Delayed Mode)



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 301: RGMII Input Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
TsetupR	t301D	–1.0 (1000M)	–	–	ns
Input setup time (delayed mode)		–1.0 (10/100M)	–	–	ns
TholdR	t302D	3.0 (1000M)	–	–	ns
Input hold time (delayed mode)		9.0 (10/100M)	–	–	ns

GMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in GMII mode.

GMII Interface Output Timing

Figure 60: GMII Output Timing

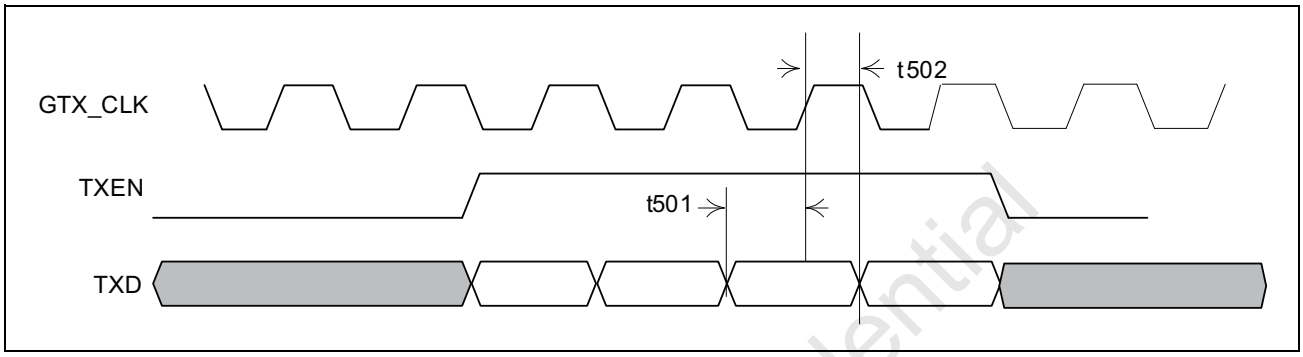


Table 302: GMII Output Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTX_CLK clock period (1000M mode)	–	7.5	8	8.5	ns
Output (TXD, TX_EN) setup to GTX_CLK rising	t501	2.5	–	–	ns
Output (TXD, TX_EN) hold from GTX_CLK rising	t502	0.5	–	5.5	ns
Duty cycle for 1000M (GbE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

GMII Interface Input Timing

Figure 61: GMII Input Timing

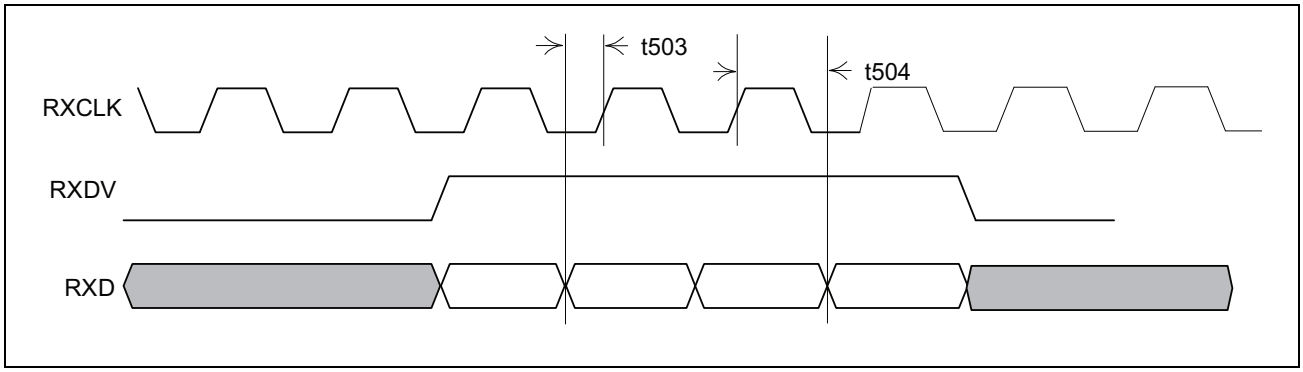


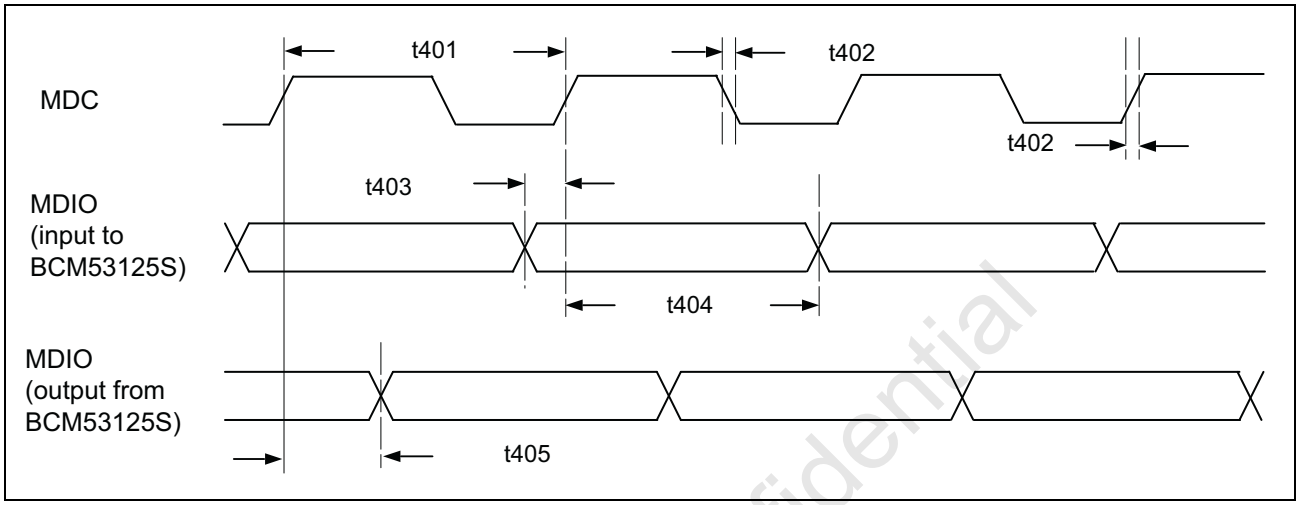
Table 303: GMII Input Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
RXCLK clock period (1000M mode)	–	–	8	–	ns
(RXD, RX_DV) setup to RX_CLK rising	t503	2.0	–	–	ns
(RXD, RX_DV) hold from RX_CLK rising	t504	0.1	–	–	ns

MDC/MDIO Timing

The following specifies timing information regarding the MDC/MDIO interface pins.

Figure 62: MDC/MDIO Timing (Slave Mode)



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 304: MDC/MDIO Timing (Slave Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
MDC cycle time	t401	80	–	–	ns
MDC high/low	–	30	–	–	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	7.5	–	–	ns
MDIO input hold time from MDC rising	t404	7.5	–	–	ns
MDIO output delay from MDC rising	t405	0	–	45	ns

Figure 63: MDC/MDIO Timing (Master Mode)

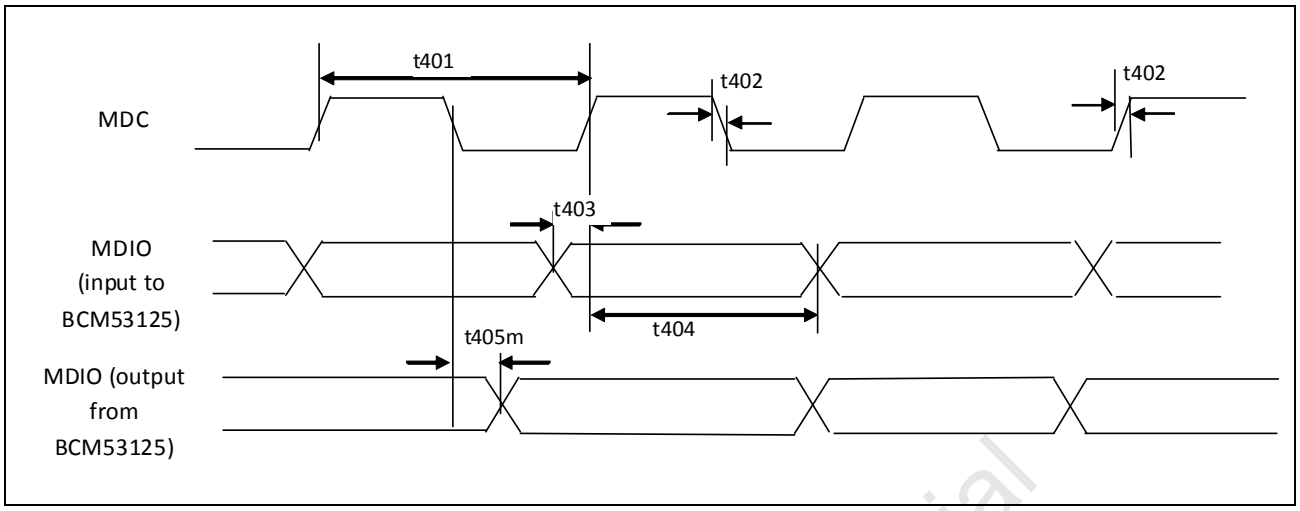


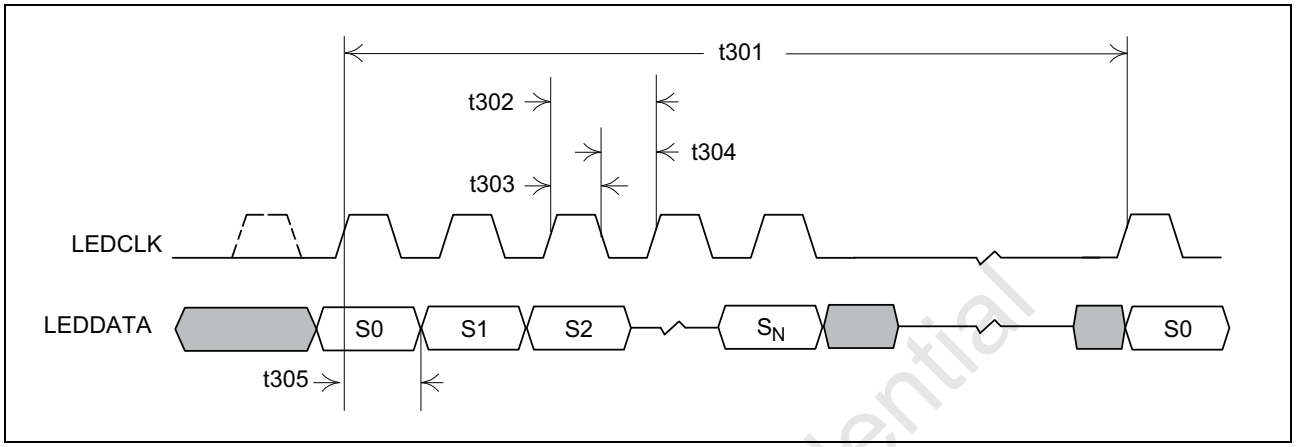
Table 305: MDC/MDIO Timing (Master Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
MDC cycle time	t401	400	–	–	ns
MDC high/low	–	160	–	240	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	20	–	–	ns
MDIO input hold time from MDC rising	t404	7.5	–	–	ns
MDIO output delay from MDC falling	t405m	–5	–	20	ns

Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

Figure 64: Serial LED Interface Timing



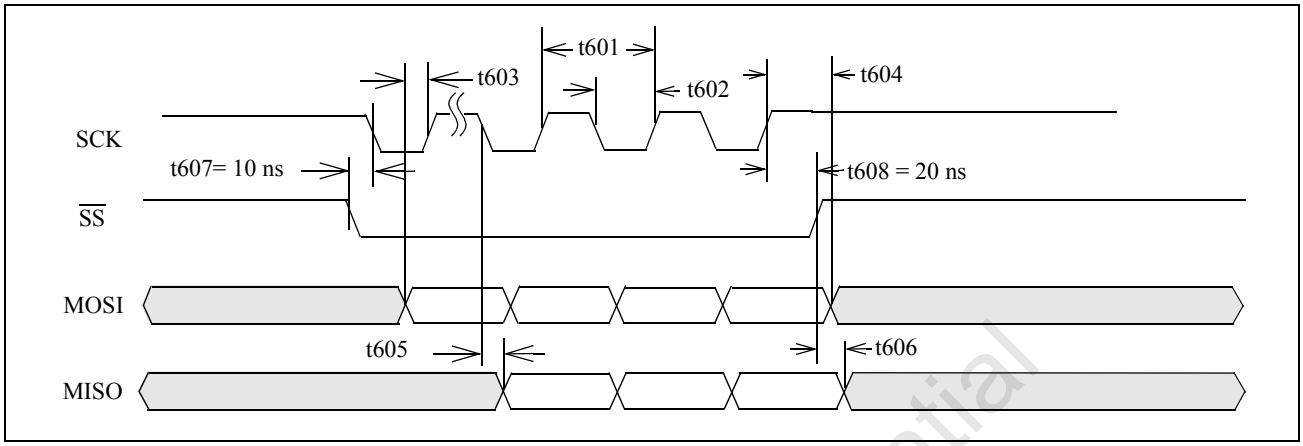
Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 306: Serial LED Interface Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
LED update cycle period	t301	–	42	–	ms
LEDCLK period	t302	–	320	–	ns
LEDCLK high-pulse width	t303	150	–	170	ns
LEDCLK low-pulse width	t304	150	–	170	ns
LEDCLK to LEDDATA output time	t305	140	–	180	ns

SPI Timings

Figure 65: SPI Timings, SS Asserted During SCK High



Note: $\overline{SS}$ should be asserted only while SCK is high.

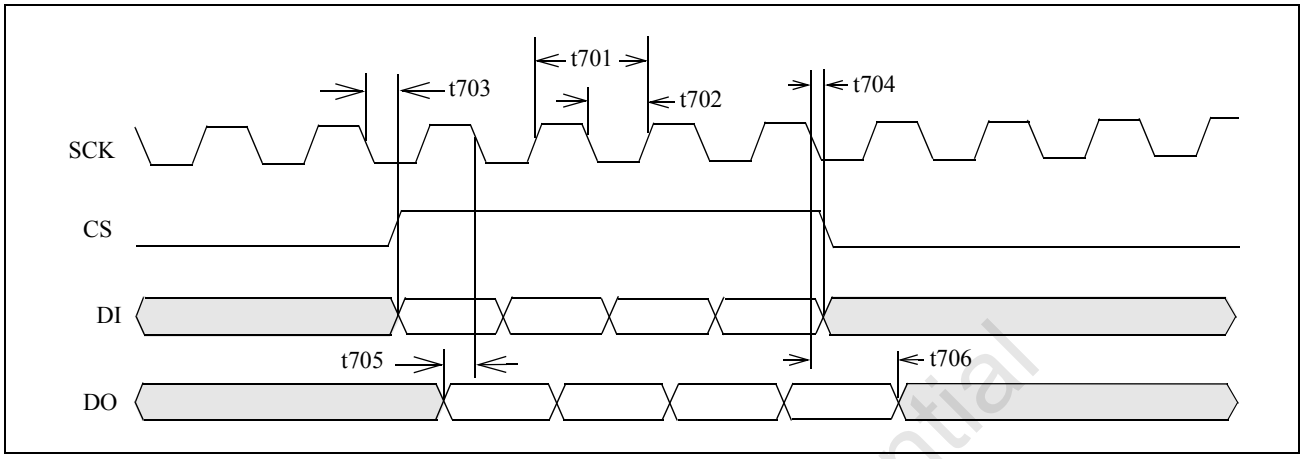
Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 307: SPI Timings

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
SCK clock period	t601	40 ns	500 ns	–
SCK high/low time	t602	20 ns	250 ns	–
MOSI to SCK setup time	t603	5 ns	–	–
MOSI to SCK hold time	t604	5 ns	–	–
SCK to MISO valid	t605	–	–	10 ns
SCK to MISO valid	t605	–	–	10 ns
Time interval from assert of $\overline{SS}$ to start of SCK	t607	10 ns	–	–
Time interval from end of SCK to deassert of $\overline{SS}$	t608	20 ns	–	–

EEPROM Timing

Figure 66: EEPROM Timing



Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 308: EEPROM Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
SCK clock frequency	t701	–	100 kHz	–
SCK high/low time	t702	–	5 µs	–
SCK low to CS, DI valid	t703	–	–	500 ns
SCK low to CS, DI invalid	t704	500 ns	–	–
DO to SCK falling setup time	t705	200 ns	–	–
DO to SCK falling hold time	t706	200 ns	–	–

JTAG Interface

Figure 67: JTAG Interface

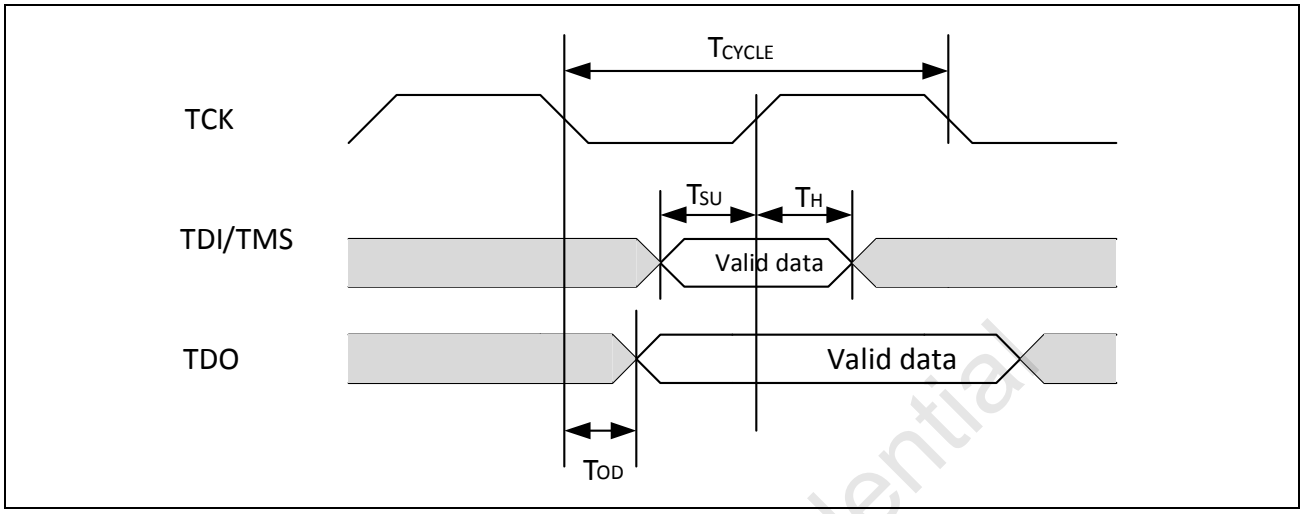


Table 309: JTAG Interface

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
JTAG TCK cycle time	TCYCLE	50	–	–	ns
Input setup time	TSU	10	–	–	ns
Input hold time	TH	10	–	–	ns
Output delay time measured from falling edge of JTAG TCK	TOD	–	–	14	ns

Section 10: Thermal Characteristics

BCM53125S 2-Layer PCB Package With a Heat Sink

Configuration:	5 GbE only, 2 layer PCB
Device power dissipation P (W):	2.1 W
Ambient air temperature T (°C):	70°C
Θ_{JA} (°C/W) in still air:	26.21
Θ_{Jb} (°C/W):	3.91
Θ_{Jc} (°C/W):	14.47

Table 310: BCM53125S 2-Layer PCB Package With a Heat Sink

AirFlow	*0 fpm, 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
T_{JMAX}	125.0	116.5	111.9	106.9	104.0
T_{CMAX}	116.0	107.2	102.40	97.0	94.5
Θ_{JA}	26.21	22.12	19.94	17.56	16.19
Ψ_{JT}	4.29	4.39	4.51	4.69	4.52
Ψ_{Jb}	7.01	6.94	6.81	4.52	6.43

Note:

- The heat sink used is 20x20x10 mm.
- With a heat sink, T_a = 70°C. This is an estimate based on a 2-layer PCB and P = 2.1W.
- 2.1W power consumption is based on 5 GbE port (no PHYless interface ports are active).
- Maximum junction temperature allowed is 125 °C.

BCM53125S 2-Layer PCB Package Without a Heat Sink

Configuration:	5 GbE only, 2 layer PCB (2s0p)
Device power dissipation P (W):	2.1 W
Ambient air temperature T (°C):	70°C
Θ_{JA} (°C/W) in still air:	31.31
Θ_{Jb} (°C/W):	3.91
Θ_{Jc} (°C/W):	14.47

Table 311: BCM53125S 2-Layer PCB Package Without Heat Sink

AirFlow	*0 fpm, 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
T_{JMAX}	135.8	126.3	121.5	116.8	114.1
T_{CMAX}	133.6	124.0	119.1	114.3	113.0
Θ_{JA}	31.31	26.80	24.53	22.31	21.01
Ψ_{JT}	1.04	1.09	1.15	1.23	1.32
Ψ_{Jb}	8.92	8.99	8.89	8.79	8.70

Note:

- Without a heat sink, T_a = 70°C. This is an estimate based on a 2-layer PCB and P = 2.1W.
- A configuration with no air flow and no heat sink will exceed the maximum junction temperature.
- Maximum junction temperature allowed is 125°C.

BCM53125S 4-Layer PCB Package Without a Heat Sink

Configuration:	5 GbE only, 4layer PCB
Device power dissipation P (W):	2.4w
Ambient air temperature T (°C):	70°C
Θ_{JA} (°C/W) in still air:	21.79
Θ_{Jb} (°C/W):	3.91
Θ_{Jc} (°C/W):	14.47

Table 312: BCM53125S 4-Layer PCB Package Without a Heat Sink

AirFlow	*0 fpm, 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
T_{JMAX}	122.3	116.6	114.3	111.6	110.1
T_{CMAX}	117.8	112.0	109.7	106.7	104.9
Θ_{JA}	21.79	19.41	18.46	17.35	16.72
Ψ_{JT}	1.87	1.91	1.93	2.08	2.19
Ψ_{Jb}	9.22	9.23	9.24	9.15	9.11

Section 11: Mechanical Information

Figure 68: 186-Pin Package (1 of 3) - Top View

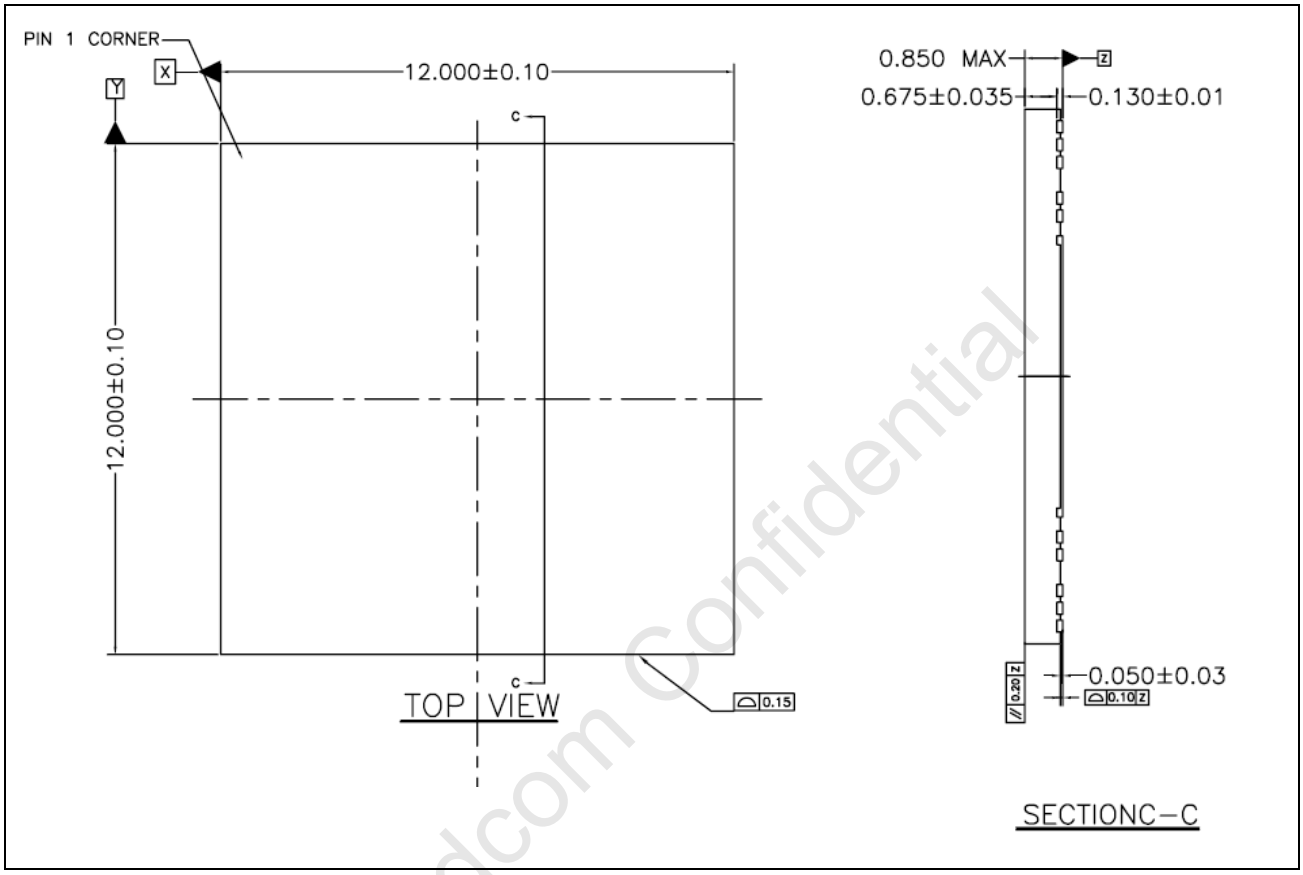


Figure 69: 186-Pin Package (2 of 3) - SectionC-C

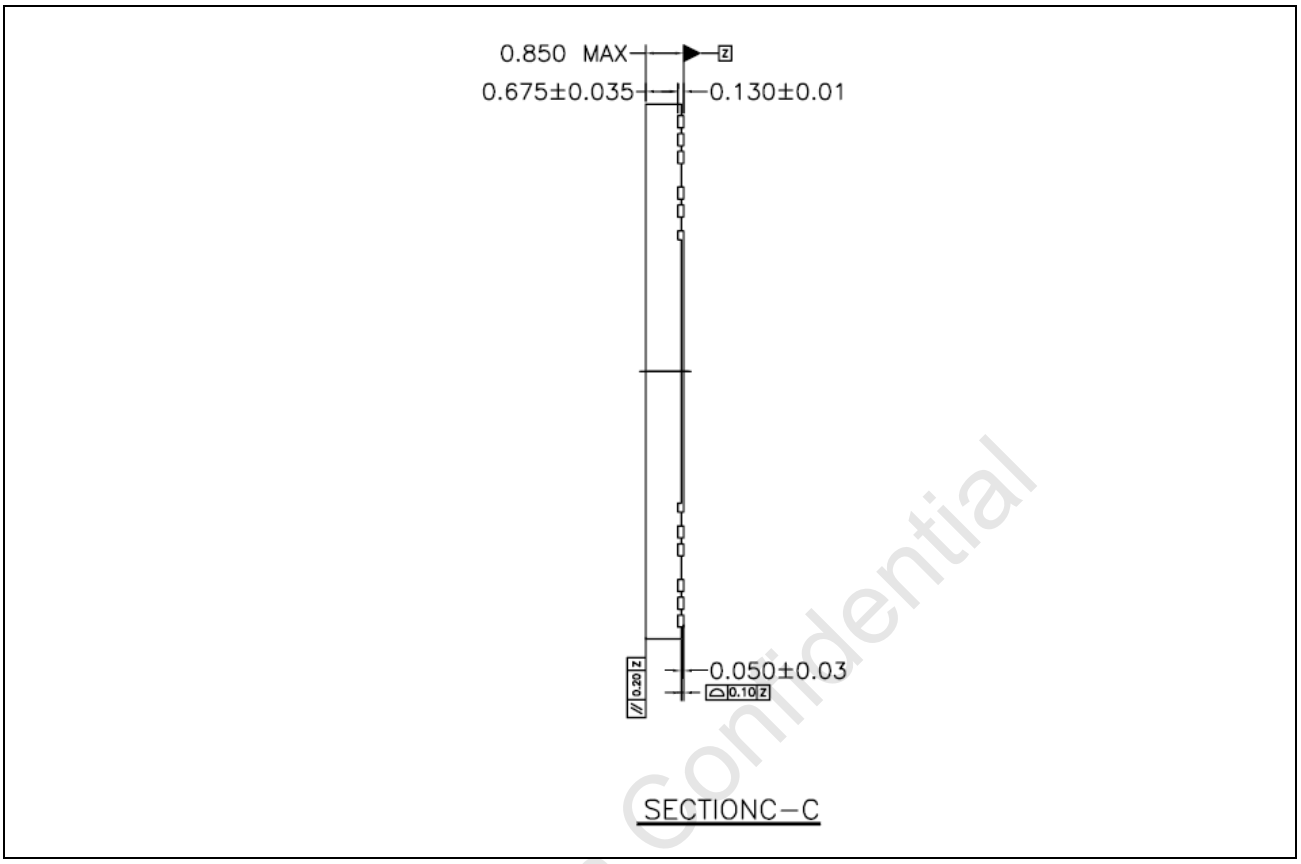
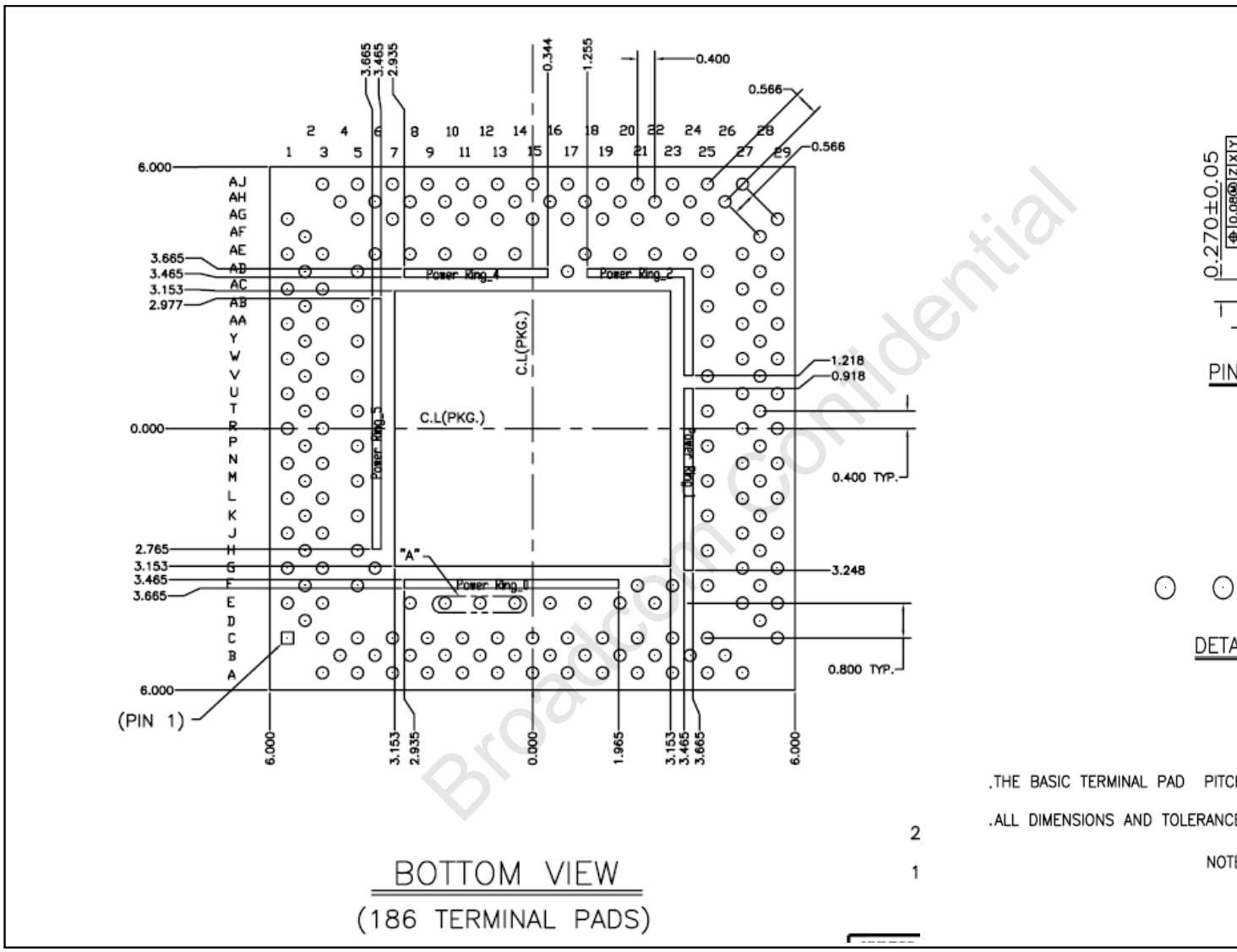


Figure 70: 186-Pin Package (3 of 3) - Bottom View



Section 12: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM53125SKMML(G)	186 MML	0°C–70°C
BCM53125SIMML(G)	186 MML	–45°C–85°C

Note: (G) represents the lead-free package option.

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